OPTOELECTRONICS
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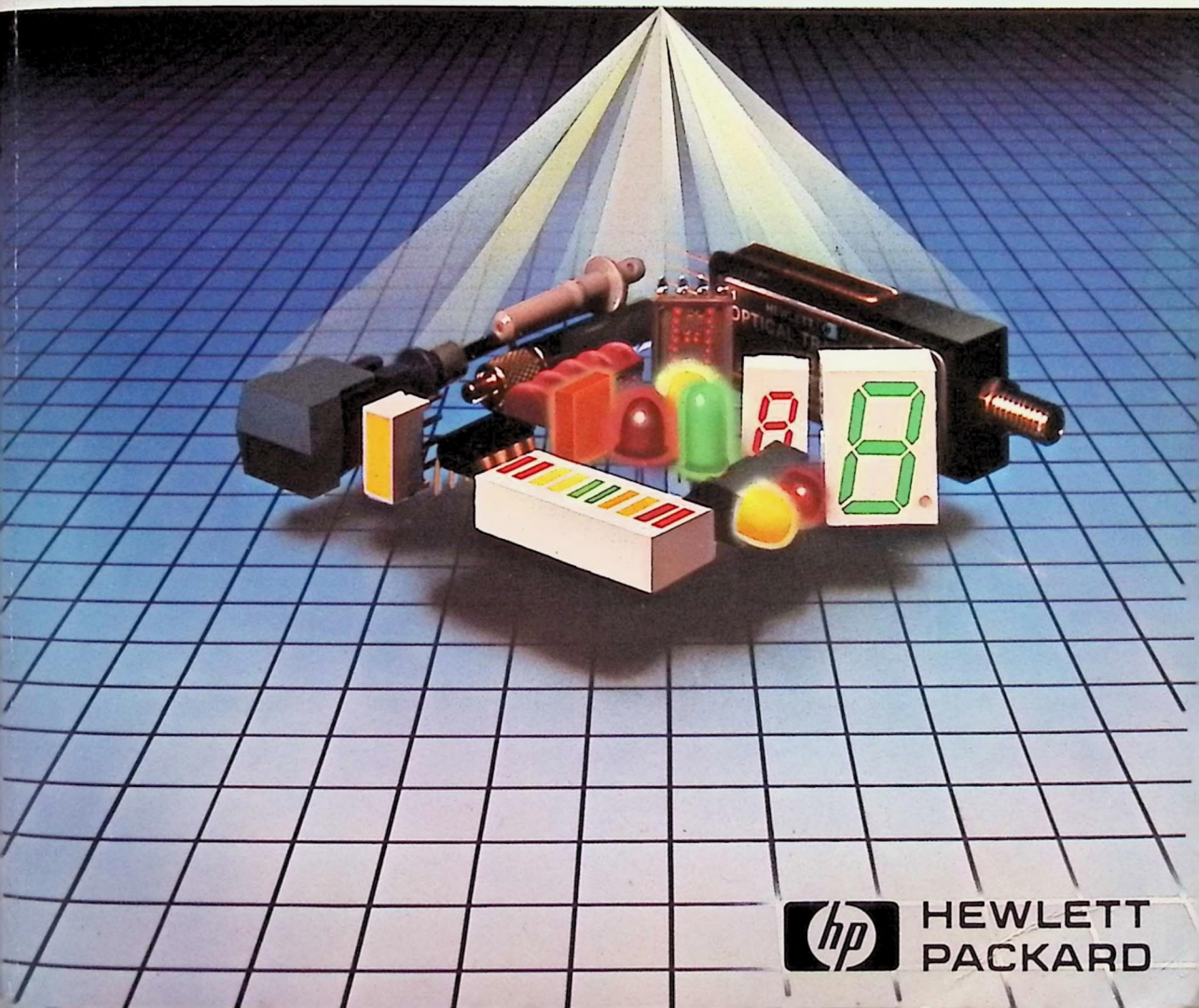


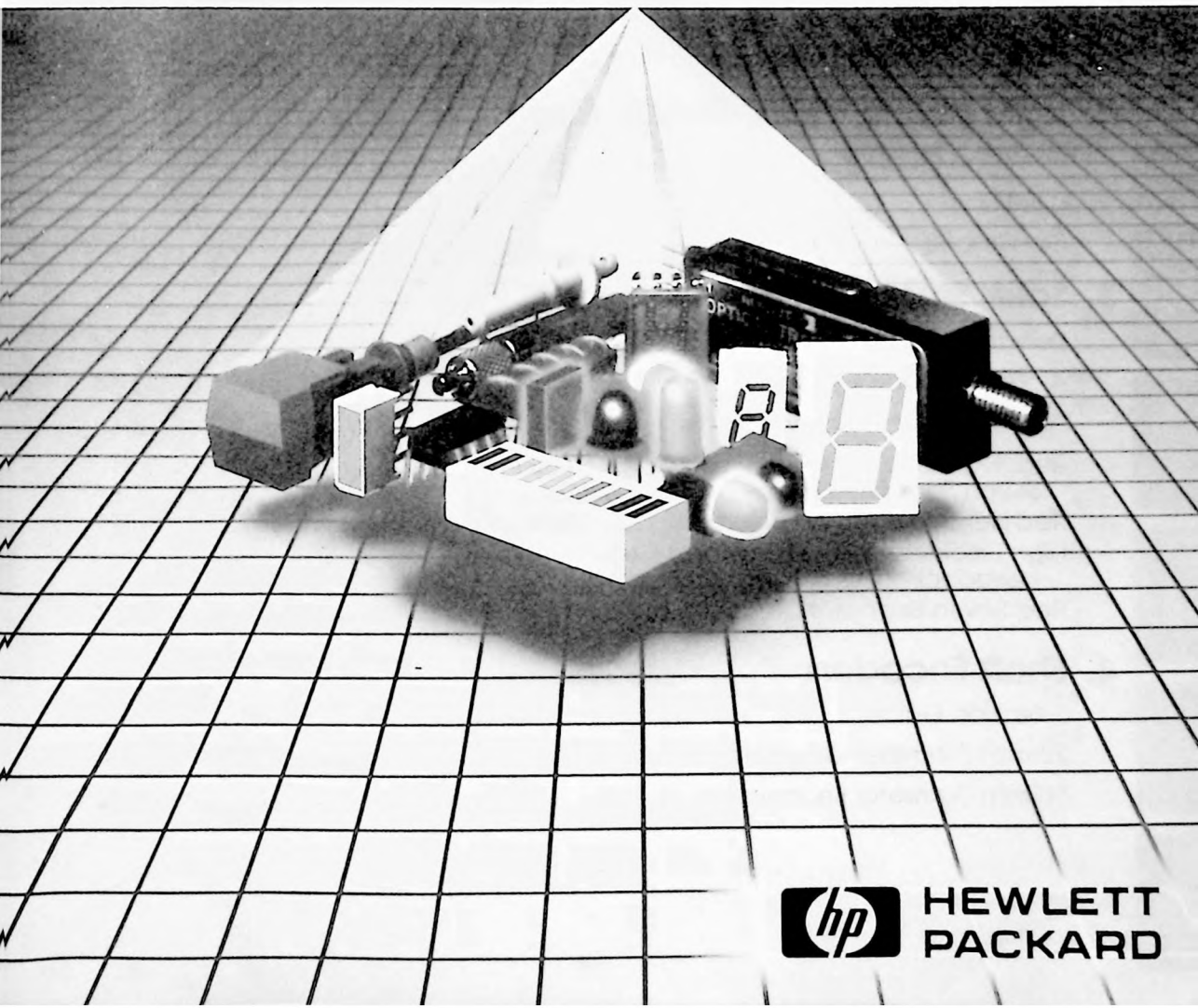
HEWLETT PACKARD

OPTOELECTRONICS
DESIGNER'S CATALOG 1984

Intensive solid state research, the development of advanced manufacturing techniques and continued expansion has enabled Hewlett-Packard to become a high volume supplier of quality, competitively priced LED displays, LED lamps, light bars, bar graph arrays, optocouplers, fiber optics, shaft encoders, and bar code products.

In addition to our broad product line, Hewlett-Packard also offers the following services: immediate delivery from any of our authorized stocking distributors, applications support, special QA testing, and a one year guarantee on most of our optoelectronic products.

This package of products and services has enabled Hewlett-Packard to become a recognized leader in the optoelectronic industry.



HEWLETT PACKARD

Table of Contents

1. Solid State Lamps

Selection Guide 1-3
Tape and Reel 1-3
New Low Current Lamp 1-11
High Efficiency Red, Yellow and Green Lamps 1-15
Right Angle Indicators 1-19
Integrated Resistor Lamps 1-21
T-1 3/4 and T-1 Lamps 1-32
Rectangular and Subminiature Lamps 1-51
Hermetic Lamps 1-64
Emitters 1-70

2. Light Bars and Bar Graph Arrays

Selection Guide 2-3
Light Bars 2-7
Bar Graphs 2-21

3. Solid State Displays

Selection Guide 3-3
Alphanumeric Displays 3-14
Alphanumeric Display Systems 3-63
Red, High Efficiency Red, Yellow and Green Seven Segment Displays 3-87
Red Hexadecimal and Numeric Dot Matrix Displays 3-127
High Efficiency Red, Yellow and Green Hexadecimal and Numeric Displays 3-144
Red Seven Segment Displays 3-164

4. Shaft Encoders

Selection Guide 4-3
28 mm Diameter Encoders 4-4
56 mm Diameter Encoders 4-12

5. Optocouplers

Selection Guide 5-3
High Speed Optocouplers 5-6
Low Current Optocoupler 5-26
High Gain Optocouplers 5-58
AC/DC to Logic Interface Optocouplers 5-70
20 mA Current Loop Optocouplers 5-76
Hermetic Optocouplers 5-92

6. Fiber Optics

Selection Guide 6-3
Snap-In Fiber Optic Link 6-5
Miniature Fiber Optic Link 6-13
High Performance Modules 6-41
Cable 6-53
Connectors 6-57
Multiplexer 6-61
Detectors 6-67

7. Bar Code Products

Selection Guide 7-3
Bar Code Scanner 7-4

8. High Reliability

Testing Programs 8-3
Selection Guide 8-10

9. Applications

Application Bulletins, Notes and Manual Listing 9-3
Abstracts 9-4
Application Bulletins and Notes 9-5

10. Appendix

HP Components Authorized Distributor and Representative Directory 10-2
HP Sales and Service Offices 10-5

Alphanumeric Index

HCPL-2200 5-26
HCPL-2300 5-30
HCPL-2502 5-6
HCPL-2503 5-10
HCPL-2530 5-17
HCPL-2531 5-17
HCPL-2533 5-21
HCPL-2601 5-40
HCPL-2602 5-44
HCPL-2630 5-50
HCPL-2631 5-54
HCPL-2730 5-62
HCPL-2731 5-62
HCPL-3700 5-70
HCPL-4100 5-76
HCPL-4200 5-84
HDSP-0760 3-144
HDSP-0761 3-144
HDSP-0762 3-144
HDSP-0763 3-144
HDSP-0770 3-144
HDSP-0771 3-144
HDSP-0772 3-144
HDSP-0781 3-150
HDSP-0781TXV 3-150
HDSP-0781TXVB 3-150
HDSP-0782 3-150
HDSP-0782TXV 3-150
HDSP-0782TXVB 3-150
HDSP-0783 3-150
HDSP-0783TXV 3-150
HDSP-0783TXVB 3-150
HDSP-0784 3-150
HDSP-0784TXV 3-150
HDSP-0784TXVB 3-150
HDSP-0791 3-150
HDSP-0791TXV 3-150
HDSP-0791TXVB 3-150
HDSP-0792 3-150
HDSP-0792TXV 3-150
HDSP-0792TXVB 3-150
HDSP-0793 3-150
HDSP-0793TXV 3-150
HDSP-0793TXVB 3-150
HDSP-0794 3-150
HDSP-0794TXV 3-150
HDSP-0794TXVB 3-150
HDSP-0881 3-150
HDSP-0881TXV 3-150
HDSP-0881TXVB 3-150
HDSP-0882 3-150
HDSP-0882TXV 3-150
HDSP-0882TXVB 3-150
HDSP-0883 3-150
HDSP-0883TXV 3-150
HDSP-0883TXVB 3-150
HDSP-0884 3-150
HDSP-0884TXV 3-150
HDSP-0884TXVB 3-150
HDSP-0860 3-144
HDSP-0861 3-144
HDSP-0862 3-144
HDSP-0863 3-144
HDSP-0960 3-144
HDSP-0961 3-144
HDSP-0962 3-144
HDSP-0963 3-144
HDSP-2000 3-14
HDSP-2001 3-14
HDSP-2002 3-14
HDSP-2003 3-14
HDSP-2010 3-18
HDSP-2010 TXV 3-18
HDSP-2010 TXVB 3-18
HDSP-2300 3-24
HDSP-2301 3-24
HDSP-2302 3-24
HDSP-2303 3-24
HDSP-2310 3-30
HDSP-2310TXV 3-30

New Products in **BOLD** Type.

HDSP-2310TXVB 3-30
HDSP-2311 3-30
HDSP-2311TXV 3-30
HDSP-2311TXVB 3-30
HDSP-2312 3-30
HDSP-2312TXV 3-30
HDSP-2312TXVB 3-30
HDSP-2416 3-63
HDSP-2424 3-63
HDSP-2432 3-63
HDSP-2440 3-63
HDSP-2450 3-41
HDSP-2450TXV 3-41
HDSP-2450TXVB 3-41
HDSP-2451 3-41
HDSP-2451TXV 3-41
HDSP-2451TXVB 3-41
HDSP-2452 3-41
HDSP-2452TXV 3-41
HDSP-2452TXVB 3-41
HDSP-2470 3-63
HDSP-2471 3-63
HDSP-2472 3-63
HDSP-2490 3-37
HDSP-2491 3-37
HDSP-2492 3-37
HDSP-2493 3-37
HDSP-3400 3-112
HDSP-3401 3-112
HDSP-3403 3-112
HDSP-3405 3-112
HDSP-3406 3-112
HDSP-3530 3-119
HDSP-3531 3-119
HDSP-3533 3-119
HDSP-3536 3-119
HDSP-3600 3-97
HDSP-3601 3-97
HDSP-3603 3-97
HDSP-3606 3-97
HDSP-3730 3-97
HDSP-3731 3-119
HDSP-3733 3-119
HDSP-3736 3-119
HDSP-3900 3-119
HDSP-3901 ..... 3-112, 3-119
HDSP-3903 ..... 3-112, 3-119
HDSP-3905 ..... 3-112, 3-119
HDSP-3906 ..... 3-112, 3-119
HDSP-4030 3-119
HDSP-4031 3-119
HDSP-4033 3-119
HDSP-4036 3-119
HDSP-4130 3-119
HDSP-4131 3-119
HDSP-4133 3-119
HDSP-4136 3-119
HDSP-4200 ..... 3-112, 3-119
HDSP-4201 ..... 3-112, 3-119
HDSP-4203 ..... 3-112, 3-119
HDSP-4205 ..... 3-112, 3-119
HDSP-4206 ..... 3-112, 3-119
HDSP-4600 3-97
HDSP-4601 3-97
HDSP-4603 3-97
HDSP-4606 3-97
HDSP-4820 2-21
HDSP-4830 2-21
HDSP-4832 2-21
HDSP-4836 2-21
HDSP-4840 2-21
HDSP-4850 2-21
HDSP-5301 3-104
HDSP-5303 3-104
HDSP-5307 3-104
HDSP-5308 3-104
HDSP-5321 3-104
HDSP-5323 3-104
HDSP-5501 3-104
HDSP-5503 3-104
HDSP-5507 3-104
HDSP-5508 3-104
HDSP-5521 3-104
HDSP-5523 3-104
HDSP-5531 3-119
HDSP-5533 3-119
HDSP-5537 3-119
HDSP-5538 3-119
HDSP-5601 3-104
HDSP-5603 3-104

New Products in **BOLD** Type.

HDSP-5607 3-104
HDSP-5608 3-104
HDSP-5621 3-104
HDSP-5623 3-104
HDSP-5701 3-104
HDSP-5703 3-104
HDSP-5707 3-104
HDSP-5708 3-104
HDSP-5721 3-104
HDSP-5723 3-104
HDSP-5731 3-119
HDSP-5733 3-119
HDSP-5737 3-119
HDSP-5738 3-119
HDSP-6300 3-58
HDSP-6504 3-52
HDSP-6505 3-52
HDSP-6508 3-52
HDSP-6509 3-52
HDSP-7301 3-87
HDSP-7302 3-87
HDSP-7303 3-87
HDSP-7304 3-87
HDSP-7307 3-87
HDSP-7308 3-87
HDSP-7311 3-87
HDSP-7313 3-87
HDSP-7317 3-87
HDSP-7318 3-87
HDSP-7401 3-87
HDSP-7402 3-87
HDSP-7403 3-87
HDSP-7404 3-87
HDSP-7407 3-87
HDSP-7408 3-87
HDSP-7501 3-87
HDSP-7502 3-87
HDSP-7503 3-87
HDSP-7504 3-87
HDSP-7507 3-87
HDSP-7508 3-87
HDSP-7801 3-87
HDSP-7802 3-87
HDSP-7803 3-87
HDSP-7804 3-87
HDSP-7807 3-87
HDSP-7808 3-87
HDSP-8600 3-112
HDSP-8601 3-112
HDSP-8603 3-112
HDSP-8605 3-112
HDSP-8606 3-112
HDSP-8716 3-75
HDSP-8724 3-75
HDSP-8732 3-75
HDSP-8740 3-75
HDSP-8820 2-27
HEDS-0100 7-3
HEDS-0150 7-3
HEDS-1000 7-4
HEDS-3000 7-3
HEDS-3001 7-3
HEDS-3050 7-3
HEDS-3200 7-3
HEDS-3201 7-3
HEDS-3250 7-3
HEDS-3251 7-3
HEDS-5000 4-4
HEDS-5010 4-4
HEDS-5100 4-4
HEDS-5110 4-4
HEDS-5200 4-4
HEDS-5210 4-4
HEDS-5300 4-4
HEDS-5310 4-4
HEDS-6000 4-12
HEDS-6010 4-12
HEDS-6100 4-12
HEDS-6110 4-12
HEDS-6200 4-12
HEDS-6210 4-12
HEDS-6300 4-12
HEDS-6310 4-12
HEDS-8923 4-4
HEDS-8924 4-4
HEDS-8925 4-4
HEDS-8926 4-4
HEDS-8927 4-4
HEDS-8928 4-4
HEDS-8931 4-4

New Products in **BOLD** Type.

HEMT-3300 1-70
HEMT-6000 1-72
HFBR-0010 6-3
HFBR-0100 6-59
HFBR-0101 6-59
HFBR-0102 6-59
HFBR-0200 6-13
HFBR-0221 6-33
HFBR-0222 6-33
HFBR-0223 6-33
HFBR-0224 6-33
HFBR-0500 6-5
HFBR-1001 6-41
HFBR-1002 6-45
HFBR-1201 6-13
HFBR-1202 6-13
HFBR-1203 6-21
HFBR-1204 6-21
HFBR-1500 6-5
HFBR-1501 6-5
HFBR-1502 6-5
HFBR-2001 6-49
HFBR-2201 6-13
HFBR-2202 6-13
HFBR-2203 6-13
HFBR-2204 6-13
HFBR-2500 6-5
HFBR-2501 6-5
HFBR-2502 6-5
HFBR-3000, OPT 001 6-53
HFBR-3000, OPT 002 6-53
HFBR-3001 6-53
HFBR-3021 6-53
HFBR-3099 6-57
HFBR-3100, OPT 001 6-53
HFBR-3100, OPT 002 6-53
HFBR-3200 6-55
HFBR-3300 6-53
HFBR-3500 6-5
HFBR-3501 6-5
HFBR-3502 6-5
HFBR-3503 6-5
HFBR-3504 6-5
HFBR-3505 6-5
HFBR-3506 6-5
HFBR-3507 6-5
HFBR-3508 6-5
HFBR-3589 6-5
HFBR-3590 6-5
HFBR-3591 6-5
HFBR-3600, OPT 001 6-5
HFBR-3602 6-5
HFBR-3603 6-5
HFBR-3604 6-5
HFBR-3605 6-5
HFBR-3606 6-5
HFBR-3607 6-5
HFBR-3608 6-5
HFBR-3689 6-5
HFBR-3690 6-5
HFBR-3691 6-5
HFBR-4000 6-57
HFBR-4201 6-13
HFBR-4202 6-13
HFBR-4501 6-5
HFBR-4511 6-5
HFBR-4595 6-5
HLMP-0103 1-62
HLMP-0300 1-51
HLMP-0301 1-51
HLMP-0354 1-64
HLMP-0380 1-64
HLMP-0381 1-64
HLMP-0400 1-51
HLMP-0401 1-51
HLMP-0454 1-64
HLMP-0480 1-64
HLMP-0481 1-64
HLMP-0500 1-51
HLMP-0501 1-51
HLMP-0503 1-51
HLMP-0504 1-51
HLMP-0554 1-64
HLMP-0580 1-64
HLMP-0581 1-64
HLMP-0904 1-64
HLMP-0930 1-64
HLMP-0931 1-64
HLMP-1000 1-49
HLMP-1002 1-49

New Products in **BOLD** Type.

HLMP-1071 1-49
HLMP-1080 1-49
HLMP-1100 1-21
HLMP-1120 1-21
HLMP-1142 1-27

HLMP-1200 1-49
HLMP-1201 1-49
HLMP-1300 1-44
HLMP-1301 1-44
HLMP-1302 1-44

HLMP-1320 1-44
HLMP-1321 1-44
HLMP-1340 1-15
HLMP-1350 1-48
HLMP-1400 1-44

HLMP-1401 1-44
HLMP-1402 1-44
HLMP-1420 1-44
HLMP-1421 1-44
HLMP-1440 1-15

HLMP-1450 1-48
HLMP-1500
(replaced by HLMP-1503) 1-44
HLMP-1501
(replaced by HLMP-1503 1-44
HLMP-1503 1-44
HLMP-1520 1-44

HLMP-1521 1-44
HLMP-1523 1-44
HLMP-1540 1-15
HLMP-1550 1-48
HLMP-1600 1-21

HLMP-1601 1-21
HLMP-1620 1-21
HLMP-1621 1-21
HLMP-1640 1-21
HLMP-1641 1-21

HLMP-1700 1-11
HLMP-1719 1-11
HLMP-2300 2-7
HLMP-2350 2-7
HLMP-2400 2-7

HLMP-2450 2-7
HLMP-2500 2-7
HLMP-2550 2-7

HLMP-2598 2-19
HLMP-2599 2-19

HLMP-2600 2-7
HLMP-2620 2-7
HLMP-2635 2-7
HLMP-2655 2-7
HLMP-2670 2-7

HLMP-2685 2-7
HLMP-2700 2-7
HLMP-2720 2-7
HLMP-2735 2-7
HLMP-2755 2-7

HLMP-2770 2-7
HLMP-2785 2-7
HLMP-2800 2-7
HLMP-2820 2-7
HLMP-2835 2-7

HLMP-2855 2-7
HLMP-2870 2-7
HLMP-2885 2-7
HLMP-2898 2-19
HLMP-2899 2-19

HLMP-2950 2-13
HLMP-2965 2-13
HLMP-3000 1-42
HLMP-3001 1-42
HLMP-3002 1-42

HLMP-3050 1-42
HLMP-3105 1-21
HLMP-3112 1-21
HLMP-3200 1-36
HLMP-3201 1-36

HLMP-3300 1-32
HLMP-3301 1-32
HLMP-3315 1-32
HLMP-3316 1-32
HLMP-3350 1-36

HLMP-3351 1-36
HLMP-3365 1-36
HLMP-3366 1-36
HLMP-3390 1-15
HLMP-3400 1-32

HLMP-3401 1-32
HLMP-3415 1-32

New Products in **BOLD** Type.

HLMP-3416 1-32
HLMP-3450 1-36
HLMP-3451 1-36
HLMP-3465 1-36
HLMP-3466 1-36
HLMP-3490 1-15
HLMP-3500
(replaced by HLMP-3502) 1-32
HLMP-3501
(replaced by HLMP-3507) 1-32
HLMP-3502 1-32
HLMP-3507 1-32
HLMP-3517 1-32
HLMP-3519 1-32
HLMP-3553 1-36
HLMP-3554 1-36
HLMP-3567 1-36
HLMP-3568 1-36
HLMP-3590 1-15
HLMP-3600 1-21
HLMP-3601 1-21
HLMP-3650 1-21
HLMP-3651 1-21
HLMP-3680 1-21
HLMP-3681 1-21
HLMP-3750 1-15
HLMP-3850 1-15
HLMP-3950 1-15
HLMP-4600 1-29
HLMP-4601 1-29
HLMP-4610 1-29
HLMP-4700 1-11
HLMP-4719 1-11
HLMP-5000 1-19
HLMP-5005 1-19
HLMP-5012 1-19
HLMP-5029 1-63
HLMP-5030 1-19
HLMP-5040 1-19
HLMP-5050 1-19
HLMP-5060 1-19
HLMP-5070 1-19
HLMP-5080 1-19
HLMP-6000 1-54
HLMP-6001 1-54
HLMP-6020 1-54
HLMP-6021 1-54
HLMP-6203 1-58
HLMP-6204 1-58
HLMP-6205 1-58
HLMP-6206 1-58
HLMP-6208 1-58
HLMP-6300 1-54
HLMP-6320 1-54
HLMP-6400 1-54
HLMP-6420 1-54
HLMP-6500 1-54
HLMP-6520 1-54
HLMP-6600 1-25
HLMP-6607 1-25
HLMP-6620 1-25
HLMP-6627 1-25
HLMP-6653 1-58
HLMP-6654 1-58
HLMP-6655 1-58
HLMP-6656 1-58
HLMP-6658 1-58
HLMP-6753 1-58
HLMP-6754 1-58
HLMP-6755 1-58
HLMP-6756 1-58
HLMP-6758 1-58
HLMP-6853 1-58
HLMP-6854 1-58
HLMP-6855 1-58
HLMP-6856 1-58
HLMP-6858 1-58
HLMP-7000 1-11
HLMP-7019 1-11
HPBK-2000 9-2
JANTX1N5765 1-64
JANTX1N6092 1-64
JANTX1N6093 1-64
JANTX1N6094 1-64
JAN1N5765 1-64
JAN1N6092 1-64
JAN1N6093 1-64
JAN1N6094 1-64
M19500/519-01 1-64
M19500/519-02 1-64

New Products in **BOLD** Type.

M19500/520-01 1-64
M19500/520-02 1-64
M19500/521-01 1-64
M19500/521-02 1-64
SL5505 5-15

1N5765 1-64
1N6092 1-64
1N6093 1-64
1N6094 1-64
16800A 7-3

16801A 7-3
16830A 7-3
16831A 7-3
39301A 6-61
4N45 5-66

4N46 5-66
4N51 3-136
4N51TXV 3-136
4N51TXVB 3-136
4N52 3-136

4N52TXV 3-136
4N52TXVB 3-136
4N53 3-136
4N53TXV 3-136
4N53TXVB 3-136

4N54 3-136
4N54TXV 3-136
4N54TXVB 3-136
4N55 5-103
4N55/883B 5-103

4N55TXV 5-103
4N55TXVB 5-103
5082-4100 (see HLMP-6000) 1-54
5082-4101 (see HLMP-6001) 1-54
5082-4150 (see HLMP-6400) 1-54

5082-4160 (see HLMP-6300) 1-54
5082-4190 (see HLMP-6500) 1-54
5082-4203 6-67
5082-4204 6-67
5082-4205 6-67

5082-4207 6-67
5082-4220 6-67
5082-4468 (see HLMP-1120) 1-21
5082-4480 (see HLMP-1000) 1-49
5082-4483 (see HLMP-1080) 1-49

5082-4484 (see HLMP-1000) 1-49
5082-4486 (see HLMP-1071) 1-49
5082-4487 (see HLMP-1200) 1-49
5082-4488 (see HLMP-1201) 1-49
5082-4494 (see HLMP-1002) 1-49

5082-4520 (see 1N6043) 1-64
5082-4550 (see HLMP-3400) 1-32
5082-4555 (see HLMP-3401) 1-32
5082-4557 (see HLMP-3415) 1-32
5082-4558 (see HLMP-3416) 1-32

5082-4570 (see HLMP-0401) 1-51
5082-4584 (see HLMP-0401) 1-51
5082-4587 1-64
5082-4590 (see HLMP-3450) 1-36
5082-4592 (see HLMP-3451) 1-36

5082-4595 (see HLMP-3465) 1-36
5082-4597 (see HLMP-3466) 1-36
5082-4620 (see 1N6092) 1-64
5082-4650 (see HLMP-3300) 1-32
5082-4655 (see HLMP-3301) 1-32

5082-4657 (see HLMP-3315) 1-32
5082-4658 (see HLMP-3316) 1-32
5082-4670 (see HLMP-0301) 1-51
5082-4684 (see HLMP-1301) 1-44
5082-4687 1-64

5082-4690 (see HLMP-3350) 1-36
5082-4693 (see HLMP-3351) 1-36
5082-4694 (see HLMP-3365) 1-36
5082-4695 (see HLMP-3366) 1-36
5082-4707 (see HLMP-0103) 1-62

5082-4732 (see HLMP-1142) 1-27
5082-4787 1-64
5082-4790 (see HLMP-3200) 1-36
5082-4791 (see HLMP-3201) 1-36
5082-4850 (see HLMP-3000) 1-32

5082-4855 (see HLMP-3001) 1-32
5082-4987 1-64
5082-7010 3-158
5082-7011 3-158
5082-7100 3-48

5082-7101 3-48
5082-7102 3-48
5082-7285 3-169
5082-7295 3-169
5082-7300 3-127

5082-7302 3-127
5082-7304 3-127
5082-7340 3-127
5082-7356 3-131
5082-7357 3-131
5082-7358 3-131
5082-7359 3-131
5082-7391 3-136
5082-7391TXV 3-136
5082-7391TXVB 3-136
5082-7392 3-136
5082-7392TXV 3-136
5082-7392TXVB 3-136
5082-7393 3-136
5082-7393TXV 3-136
5082-7393TXVB 3-136
5082-7395 3-136
5082-7395TXV 3-136
5082-7395TXVB 3-136
5082-7404 3-164
5082-7405 3-164
5082-7414 3-164
5082-7415 3-164
5082-7432 3-164
5082-7433 3-164
5082-7441 3-169
5082-7446 3-169
5082-7610 3-97
5082-7611 3-97
5082-7613 3-97
5082-7616 3-97
5082-7620 3-97
5082-7621 3-97
5082-7623 3-97
5082-7626 3-97
5082-7650 3-97
5082-7651 3-97
5082-7653 3-97
5082-7656 3-97
5082-7660 3-97
5082-7661 3-97
5082-7663 3-97
5082-7666 3-97
5082-7730 3-93
5082-7731 3-93
5082-7736 3-93
5082-7740 3-93
5082-7750 3-93
5082-7751 3-93
5082-7756 3-93
5082-7760 3-93
6N134 5-92
6N134TXV 5-92
6N134TXVB 5-92
6N135 5-6
6N136 5-6
6N137 5-36
6N138 5-58
6N139 5-58
6N140 5-99
6N140/883B 5-99
6N140TXV 5-99
6N140TXVB 5-99
810281OEC 5-95

Special Device Options

LED Lamp Tape and Reel 1-2
Plastic Optocoupler Burn-in 8-7

Hewlett-Packard Quality

When quality represents a competitive edge, or when the reputation and dependability of your products is on the line, you can depend on Hewlett-Packard Optoelectronic components. Reliability considerations and rigorous testing are an integral part of new product design and introduction at Hewlett-Packard. Once a product is in production, on-going product assurance monitors are aggressively applied to assure that you receive optimum value for your purchasing dollar.

In recent years, the term "parts per million " (PPM) has come to be considered an appropriate measure of on-going product quality with discriminating component users. Hewlett-Packard is pleased to acknowledge and encourage this trend. We are especially hopeful that we can make a contribution to your product by making visible the current product assurance level of Hewlett-Packard optoelectronic components in these same "parts per million" terms. Since the pursuit of improved quality is a continuous process, the standards are tightened periodically. Please consult your local Hewlett-Packard components field engineer for a listing of the current standards or write to Hewlett-Packard Optoelectronics Division at 640 Page Mill Road, Palo Alto, California 94304, Attention: Product Marketing and request such data. Hewlett-Packard believes this level of performance leads our industry, and we are committed to even further progress in the quality of our products.

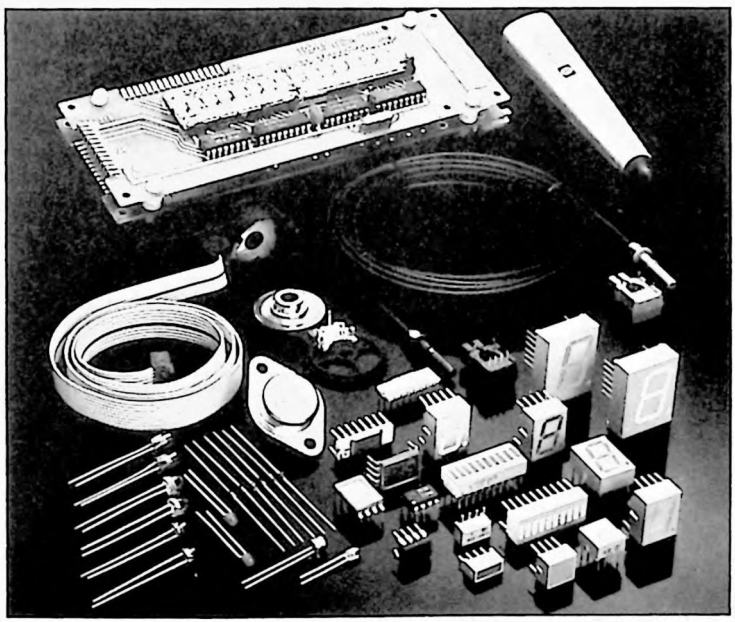
Look to Hewlett-Packard in the optoelectronics industry for quality, performance and innovation leadership.

A Brief Sketch

Hewlett-Packard is one of the world's leading designers and manufacturers of electronic, medical, analytical and computing instruments and systems, diodes, transistors, and optoelectronic products. Since its founding in Palo Alto, California, in 1939, HP has done its best to offer only products that represent significant technological advancements.

To maintain its leadership in instrument and component technology, Hewlett-Packard invests heavily in new product development. Research and development expenditures traditionally average about 10 percent of sales revenue, and over 1,500 engineers and scientists are assigned the responsibilities of carrying out the company's various R and D projects.

For the customer, Hewlett-Packard is no further away than the nearest telephone. Hewlett-Packard currently has sales and service offices located around the world.



These field offices are staffed by trained engineers, each of whom has the primary responsibility of providing technical assistance and data to customers. A vast communications network has been established to link each field office with the factories and with corporate offices. No matter what the product or the request, a customer can be accommodated by a single contact with the company.

Where Reputation and Quality Count

When quality represents a competitive edge, or when the reputation and dependability of your products is on the line, you can count on Hewlett-Packard Optoelectronic components for excellent product consistency.

The optoelectronic products available include a complete line of GaAsP and GaP discrete light emitting diodes (LED's), light bars, bar graph arrays, numeric, hexadecimal, and alphanumeric displays, optocouplers, fiber optics, optical shaft encoders and bar code products. There is complete technical data included in this designer's catalog for each of the Hewlett-Packard Optoelectronics products.

About this Catalog

This Optoelectronics Designer's Catalog contains detailed, up-to-date specifications on our complete optoelectronic product line. It is divided into eight major product sections: Solid State Lamps, Light Bars and Bar Graphs, Solid State Displays, Shaft Encoders, Optocouplers, Fiber Optics, Bar Code Products, and High Reliability. A special section which includes all of the application notes in either full or abstract form follows the High Reliability product section.

How to Use this Catalog

Three methods are incorporated for locating components:

- a Table of Contents with tabs that allow you to locate components by their general description
- a Numeric Index that lists all components by part number and,
- a Selection Guide for each product group giving a brief overview of the product line.

How to Order

All Hewlett-Packard components may be ordered through any of the Sales and Service Offices listed on pages 10-5 through 10-12. In addition, for immediate delivery of Hewlett-Packard optoelectronic components, contact any of the worldwide stocking distributors and representatives listed on pages 10-2 through 10-4.

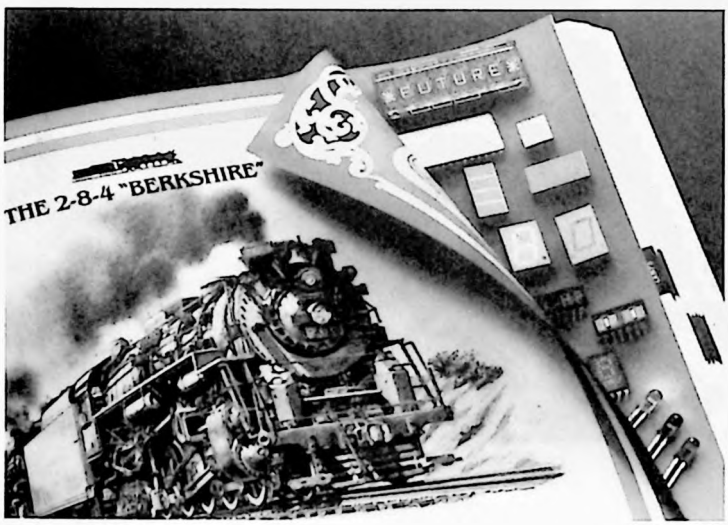
Warranty

HP's Components are warranted against defects in material and workmanship for a period of one year from the date of shipment (in the case of designated Fiber Optics and Bar Code products 90 days from the date of shipment). HP will repair or, at its option, replace components that prove to be defective in material or workmanship under proper use during the warranty period. This warranty extends only to HP customers.

NO OTHER WARRANTIES ARE EXPRESSED OR IMPLIED. HP SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE.

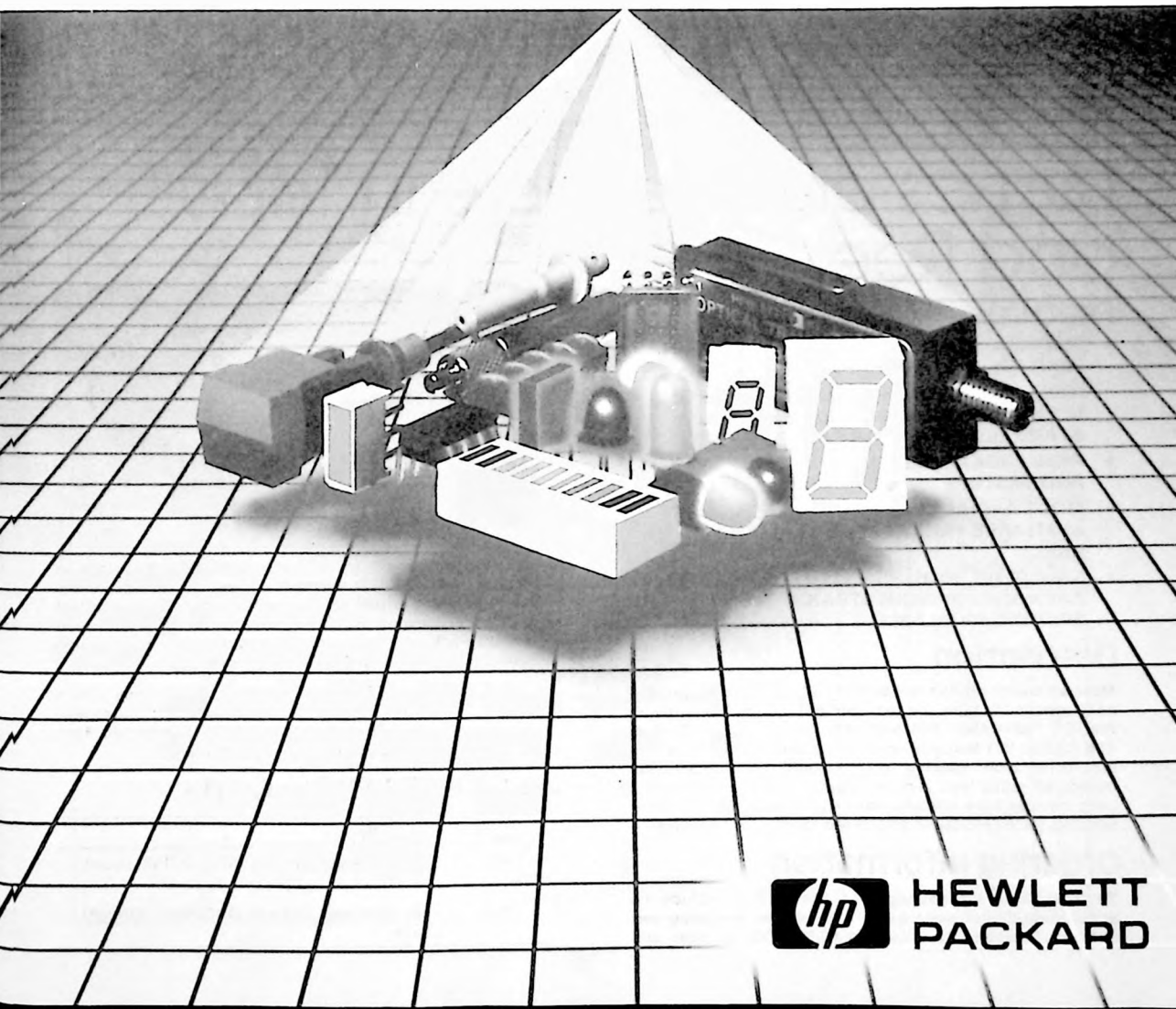
THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HP SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT OR ANY OTHER LEGAL THEORY.

The foregoing limitation of liability shall not apply in the event that any HP product sold hereunder is determined by a court of competent jurisdiction to be defective and to have directly caused bodily injury, death or property damage; provided, that in no event shall HP's liability for property damage exceed the greater of $50,000 or the purchase price of the specific product that caused such damage.



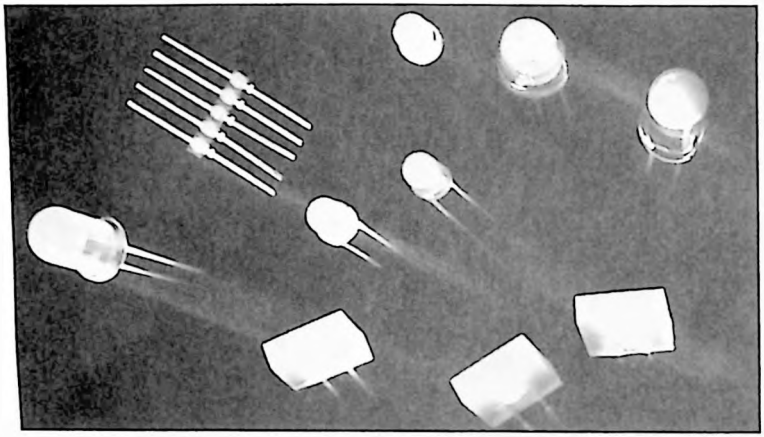
1. Solid State Lamps

- Low Current Lamp
- High Efficiency Red, Yellow, and Green Lamps
- Right Angle Indicators
- T-1 3/4 and T-1 Lamps
- Rectangular Subminiature Lamps
- Integrated Resistor Lamps
- Hermetically Sealed Lamps
- Panel Mounting Kit
- Emitters



HEWLETT PACKARD

Solid State Lamps



New product introductions characterize Hewlett-Packard's broad line of LED lamp products. New product developments have centered on contributing added-value to our customer applications. Examples include a family of low current, low power lamps specified at 2 mA DC for interface with CMOS circuits and portable equipment. Hewlett-Packard is also pioneering the use of automatic insertion equipment by introducing in this catalog the self-contained capability to put most LEDs in the catalog on tape and reel. See the description sheet below for more details.

Another example of easing the mechanical handling burden for our customers is HP's new family of right angle status indicators, providing LED lamps with pre-formed leads already inserted into a high contrast, flat seating plane molded plastic package. The popular family of HP integrated resistor lamps has also been expanded to include a full complement of package sizes in both 5 V and 12 V versions.

Lamps are Available in Tape and Reel

Features

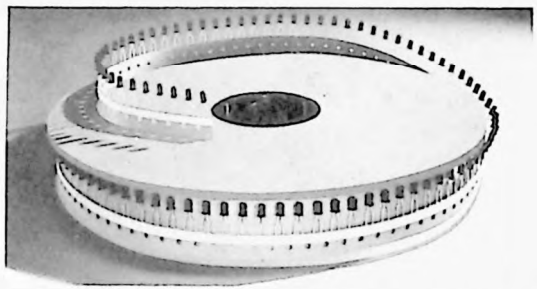
- **AUTOMATICALLY INSERTABLE WITH RADIAL LEAD INSERTION EQUIPMENT**
- **MEET DIMENSIONAL SPECIFICATIONS OF IEC PUBLICATION 286 AND ANSI/EIA STANDARD RS-468 FOR TAPE AND REEL**
- **REEL PACKAGING SIMPLIFIES HANDLING AND TESTING**
- **MOST RADIAL LEAD PLASTIC LED LAMPS AVAILABLE PACKAGED IN TAPE AND REEL**
- **5 mm (0.197 INCH) PREFORMED LEAD AND 2.54 mm (0.100 INCH) STRAIGHT LEAD SPACING AVAILABLE**

Description

Most standard catalog radial lead LED lamps are available packaged in the tape and reel configuration as specified by the IEC Publication 286 and ANSI/EIA Standard RS-468. The Option 001 lamp devices have preformed leads with 5 mm (0.197 inch) spacing for automatic insertion into PC boards by radial lead insertion equipment. The Option 002 lamp devices have straight leads with 2.54 mm (0.100 inch) spacing, packaged taped and reeled for ease of handling.

Ordering Information

To order LED lamps packaged on tape and reel, include the appropriate Option code along with the device catalog part number. Example: To order the HLMP-3300 on tape and reel with preformed leads (5 mm lead spacing) order as follows: HLMP-3300 Option 001. Minimum order quantities and quantities per reel vary by part number. Please contact your local Hewlett-Packard sales office or franchised Hewlett-Packard distributor for a complete list of lamps available taped and reeled and mechanical specifications.

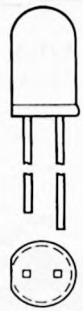
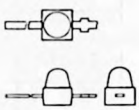


LED lamps with 0.46 mm (0.018 inch) square leads with 5 mm (0.197 inch) lead spacing are recommended for use with automatic insertion equipment. It is suggested that insertion machine compatibility be confirmed.

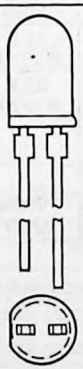
Device Selection Guide

Option	Description
001	Tape and Reel, 5 mm (0.197 inch) Preformed Leads
002	Tape and Reel, 2.54 mm (0.100 inch) Straight Leads

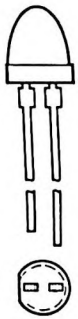
Low Current Lamps

Device		Description			Typical Luminous Intensity	2θ 1/2[1]	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color[2]	Package	Lens				
	HLMP-4700	High Efficiency Red	T-1 3/4	Tinted Diffused	2.0 mcd @ 2 mA	50°	1.8 V @ 20 mA	1-11
	HLMP-4719	Yellow			1.8 mcd @ 2 mA		1.9 V @ 2 mA	
	HLMP-1700	High Efficiency Red	T-1	Tinted Diffused	1.8 mcd @ 2 mA	50°	1.8 V @ 2 mA	
	HLMP-1719	Yellow			1.6 mcd @ 2 mA		1.9 V @ 2 mA	
	HLMP-7000	High Efficiency Red	Subminiature	Tinted Diffused	0.8 mcd @ 2 mA	70°	1.8 V @ 2 mA	
	HLMP-7019	Yellow			0.6 mcd @ 2 mA		1.9 V @ 2 mA	

Ultra Bright Lamps

Device		Description			Typical Luminous Intensity	2θ 1/2[1]	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color[2]	Package	Lens				
	HLMP-3750	High Efficiency Red	T-1 3/4	Untinted Non-Diffused	125 mcd @ 20 mA	24°	2.2 V @ 20 mA	1-15
	HLMP-3850	Yellow		Untinted Non-Diffused	140 mcd @ 20 mA			
	HLMP-3950	Green		Untinted Non-Diffused	120 mcd @ 20 mA		2.3 V @ 20 mA	

Ultra Bright Lamps (continued)

Device		Description			Typical Luminous Intensity	2θ 1/2[1]	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color[2]	Package	Lens				
	HLMP-3390	High Efficiency Red	T-1 3/4 Low Profile	Untinted Non-Diffused	55 mcd @ 20 mA	32°	2.2 V @ 20 mA	1-15
	HLMP-3490	Yellow		Untinted Non-Diffused				
	HLMP-3590	Green		Untinted Non-Diffused			2.3 V @ 20 mA	
	HLMP-1340	High Efficiency Red	T-1	Untinted Non-Diffused	35 mcd @ 20 mA	45°	2.2 V @ 20 mA	
	HLMP-1440	Yellow		Untinted Non-Diffused				
	HLMP-1540	Green		Untinted Non-Diffused			2.3 V @ 20 mA	

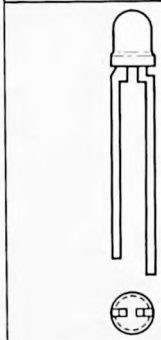
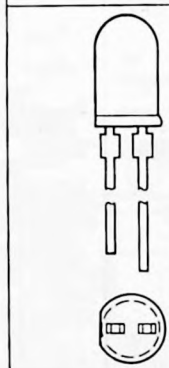
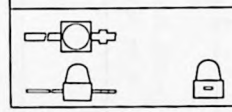
Right Angle Indicators without Integrated Current Limiting Resistor

Device		Description			Typical Luminous Intensity	2θ 1/2[1]	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-5000	Red (640 nm)	T-1 3/4 Right Angle Indicator	Red Diffused	4.0 mcd @ 20 mA	75°	1.6 V @ 20 mA	1-19
	HLMP-5030	High Efficiency Red (626 nm)			6.0 mcd @ 10 mA	65°	2.2 V @ 10 mA	
	HLMP-5040	Yellow (585 nm)		Yellow Diffused	6.0 mcd @ 10 mA	75°		
	HLMP-5050	Green (569 nm)		Green Diffused	6.0 mcd @ 20 mA		12 mA @ 5 V	

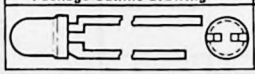
Right Angle Indicators with Integrated Current Limiting Resistors

Device		Description			Typical Luminous Intensity	2θ 1/2[1]	Typical Forward Current	Page No.
Package Outline Drawing	Part No.	Color[2]	Package	Lens				
	HLMP-5012	Red (640 nm)	T-1 3/4 Right Angle Indicator	Red Diffused	2 mcd @ 12 V	75°	13 mA @ 12 V	1-19
	HLMP-5005				2 mcd @ 5 V		13 mA @ 5 V	
	HLMP-5060	High Efficiency Red (626 nm)			4 mcd @ 5 V	65°	10 mA @ 5 V	
	HLMP-5070	Yellow (585 nm)		Yellow Diffused		75°		
	HLMP-5050	Green (569 nm)		Green Diffused			12 mA @ 5 V	

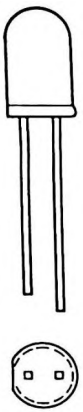
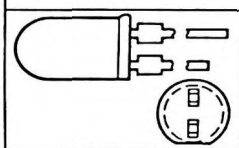
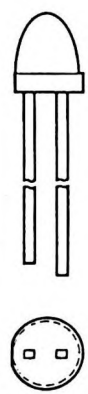
Integrated Resistor Lamps

Device		Description			Typical Luminous Intensity	2θ 1/2[1]	Typical Forward Current	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-1100	Red (640 nm)	T-1[4]	Tinted Diffused	1.5 mcd @ 5 V	60°	13 mA @ V	1-21
	HLMP-1120			Untinted Diffused		70°		
	HLMP-1600	High Efficiency Red (606 nm)		Tinted Diffused	4 mcd @ 5 V	60°	10 mA @ 5 V	1-21
	HLMP-1601				4 mcd @ 12 V		13 mA @ 12 V	
	HLMP-1620	Yellow (585 nm)			4 mcd @ 5 V		13 mA @ 5 mA	
	HLMP-1621				4 mcd @ 12 V		10 mA @ 12 V	
	HLMP-1640	Green (569 nm)			4 mcd @ 5 V		12 mA @ 5 V	
	HLMP-1641				4 mcd @ 12 V		13 mA @ 12 V	
	HLMP-3105	Red (640 nm)	T-1 3/4[3]		4 mcd @ 5 V	75°	10 mA @ 5 mA	
	HLMP-3112				4 mcd @ 12 V		13 mA @ 12 V	
	HLMP-3600	High Efficiency Red (640 nm)			4 mcd @ 5 V	65°	10 mA @ 5 V	
	HLMP-3601				4 mcd @ 12 V		13 mA @ 12 V	
	HLMP-3650	Yellow (585 nm)			4 mcd @ 5 V	75°	10 mA @ 5 mA	
	HLMP-3651				4 mcd @ 12 V		13 mA @ 12 V	
	HLMP-3680	Green (569 nm)			4 mcd @ 5 V		12 mA @ 5 V	
	HLMP-3681				4 mcd @ 12 V		13 mA @ 12 V	
	HLMP-6600	High Efficiency Red (626 nm)	Subminiature Radial Leads	Red Diffused	2.4 mcd @ 5 V	90°	9.6 mA @ 5 V	1-25
	HLMP-6620				0.6 mcd @ 5 V		3.5 mA @ 5 V	

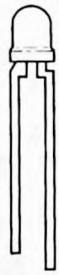
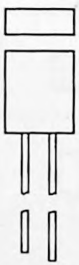
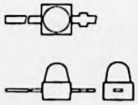
Voltage Sensing LED Lamps

Device		Description			Typical Luminous Intensity	2θ 1/2[1]	Typical Forward Current	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens				
	HLMP-1142	Red (640 nm)	T-1[4]	Red Diffused	0.7 mcd @ 2.75 V	60°	13 mA @ 2.75 V	1-27

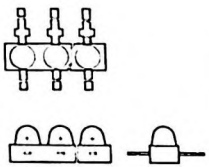
High Efficiency Red, Yellow, High Performance Green LED Lamps

Device		Description			Typical Luminous Intensity	2θ 1/2[1]	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color[2]	Package	Lens				
	HLMP-3300	High Efficiency Red (626 nm)	T-1 3/4[3]	Red Diffused	3.5 mcd @ 10 mA	65°	2.2 V @ 10 mA	1-32
	HLMP-3301				7.0 mcd @ 10 mA			
	HLMP-4600				10.0 mcd @ 20 mA	32°		1-29
	HLMP-4601				20.0 mcd @ 20 mA			
	HLMP-3315			Red Non-Diffused	18.0 mcd @ 10 mA	35°		1-32
	HLMP-3316				30.0 mcd @ 10 mA			
	HLMP-3400	Yellow (585 nm)		Yellow Diffused	4.0 mcd @ 10 mA	75°		
	HLMP-3401				8.0 mcd @ 10 mA			
	HLMP-3401				8.0 mcd @ 10 mA			
	HLMP-3415			Yellow Non-Diffused	18.0 mcd @ 10 mA	35°		
	HLMP-3416				30.0 mcd @ 10 mA			
	HLMP-3502	Green (569 nm)		Green Diffused	6.0 mcd @ 20 mA	75°	2.3 V @ 20 mA	
	HLMP-3507				12.0 mcd @ 20 mA			
	HLMP-3517			Green Non-Diffused	25.0 mcd @ 20 mA	24°		
	HLMP-3519				50.0 mcd @ 20 mA			
	HLMP-4610 [1]	High Efficiency Red (626 nm)	Heavy Leadframe	Red Diffused	10.0 mcd @ 20 mA	32°	2.2 V @ 10 mA	1-29
	HLMP-3350	High Efficiency Red (626 nm)	T-1 3/4 Low Profile	Red Diffused	3.5 mcd @ 10 mA	50°	2.2 V @ 10 mA	1-36
	HLMP-3351				7.0 mcd @ 10 mA			
	HLMP-3365			Red Non-Diffused	10.0 mcd @ 10 mA	45°		
	HLMP-3366				18.0 mcd @ 10 mA			
	HLMP-3450	Yellow (585 nm)		Yellow Diffused	4.0 mcd @ 10 mA	50°		
	HLMP-3451				10.0 mcd @ 10 mA			
	HLMP-3465			Yellow Non-Diffused	12.0 mcd @ 10 mA	45°		
	HLMP-3466				18.0 mcd @ 10 mA			
	HLMP-3553	Green (572 nm)		Green Diffused	8.0 mcd @ 20 mA	50°	2.4 V @ 20 mA	
	HLMP-3554				15.0 mcd @ 20 mA			
	HLMP-3567			Green Non-Diffused	15.0 mcd @ 20 mA	40°		
	HLMP-3568				35.0 mcd @ 20 mA			

High Efficiency Red, Yellow, High Performance Green LED Lamps (continued)

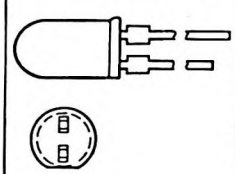
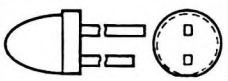
Device		Description			Typical Luminous Intensity	2θ 1/2[1]	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color[2]	Package	Lens				
	HLMP-1300	High Efficiency Red (626 nm)	T-1[4]	Red Diffused	2.0 mcd @ 10 mA	60°	2.2 V @ 10 mA	1-44
	HLMP-1301				2.5 mcd @ 10 mA			
	HLMP-1302				4.0 mcd @ 10 mA			
	HLMP-1320			Untinted Non-Diffused	12 mcd @ 10 mA	45°		
	HLMP-1321			Red Non-Diffused				
	HLMP-1400	Yellow (585 nm)		Yellow Diffused	2.0 mcd @ 10 mA	60°		
	HLMP-1401				3.0 mcd @ 10 mA			
	HLMP-1402				4.0 mcd @ 10 mA			
	HLMP-1420			Untinted Non-Diffused	12 mcd @ 10 mA	45°		
	HLMP-1421			Yellow Non-Diffused				
	HLMP-1503	Green (569 nm)		Green Diffused	5.0 mcd @ 20 mA	60°	2.3 V @ 20 mA	
	HLMP-1523				10.0 mcd @ 20 mA			
	HLMP-1520			Untinted Non-Diffused	12 mcd @ 20 mA	45°		
	HLMP-1521			Yellow Non-Diffused				
	HLMP-1350	High Efficiency Red (626 nm)	T-1 Low Profile[4]	Red Diffused	2.0 mcd @ 10 mA	54°	2.2 V @ 10 mA	1-48
	HLMP-1450	Yellow (585 nm)		Yellow Diffused				
	HLMP-1550	Green (569 nm)		Green Diffused	2.0 mcd @ 20 mA		2.3 V @ 20 mA	
	HLMP-0300	High Efficiency Red (626 nm)	Rectangular	Red Diffused	2.5 mcd @ 20 mA	100°	2.5 V @ 20 mA	1-51
	HLMP-0301				5.0 mcd @ 20 mA			
	HLMP-0400	Yellow (585 nm)		Yellow Diffused	2.5 mcd @ 20 mA			
	HLMP-0401				5.0 mcd @ 20 mA			
	HLMP-0503	Green (569 nm)		Green Diffused	2.5 mcd @ 20 mA		2.3 V @ 20 mA	
	HLMP-0504				5.0 mcd @ 20 mA			
	HLMP-6300	High Efficiency Red (626 nm)	Subminiature	Red Diffused	3.0 mcd @ 10 mA	80°	2.2 V @ 10 mA	1-54
	HLMP-6400	Yellow (585 nm)		Yellow Diffused		90°		
	HLMP-6500	Green (569 nm)		Green Diffused		70°	2.3 V @ 10 mA	

High Efficiency Red, Yellow, High Performance Green LED Lamps (continued)

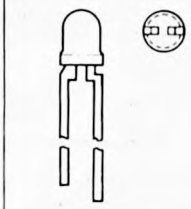
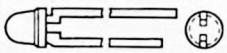
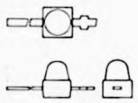
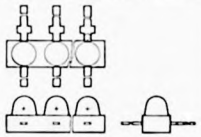
Device		Description				Typical Luminous Intensity	2θ 1/2[1]	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color[2]	Package	*	Lens				
	HLMP-6653 HLMP-6654 HLMP-6655 HLMP-6656 HLMP-6658	High Efficiency Red (626 nm)	Sub-miniature Array	3 4 5 6 8	Red Diffused	3.0 mcd @ 10 mA	80°	2.2 V @ 10 mA	1-58
	HLMP-6753 HLMP-6754 HLMP-6755 HLMP-6756 HLMP-6758	Yellow (585 nm)	Sub-miniature Array	3 4 5 6 8	Yellow Diffused		90°		
	HLMP-6853 HLMP-6854 HLMP-6855 HLMP-6856 HLMP-6858	Green (569 nm)	Sub-miniature Array	3 4 5 6 8	Green Diffused		70°	2.3 V @ 10 mA	

*Array Length

Red LED Lamps

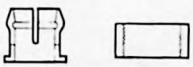
Device		Description			Typical Luminous Intensity	2θ 1/2[1]	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color[2]	Package	Lens				
	HLMP-3000	Red (640 nm)	T-1 3/4[3]	Red Diffused	2.0 mcd @ 20 mA	75°	1.6 V @ 20 mA	1-42
	HLMP-3001				4.0 mcd @ 20 mA			
	HLMP-3002		Thin Leadframe		3.0 mcd @ 20 mA			
	HLMP-3050		Thin Leadframe	Red Tinted Non-Diffused	2.5 mcd @ 20 mA	24°		
	HLMP-3200		T-1 3/4 Low Profile	Red Diffused	2.0 mcd @ 20 mA	60°		1-36
	HLMP-3201				4.0 mcd @ 20 mA			

Red LED Lamps (Continued)

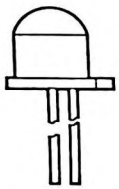
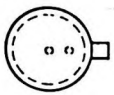
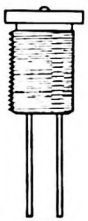
Device		Description			Typical Luminous Intensity	2θ 1/2[1]	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color[2]	Package	Lens				
	HLMP-1000	Red (640 nm)	T-1[4]	Red Diffused	1.0 mcd @ 10 mA	125°	1.6 V @ 20 mA	1-49
	HLMP-1002				2.5 mcd @ 20 mA			
	HLMP-1080			Untinted Diffused	1.5 mcd @ 20 mA			
	HLMP-1071			Untinted Non-Diffused	2.0 mcd @ 20 mA	80°		
	HLMP-1200		T-1 Low Profile[4]	Untinted Non-Diffused	1.0 mcd @ 20 mA	120°		
	HLMP-1201				2.5 mcd @ 20 mA			
	HLMP-6000		Subminiature	Red Diffused	1.0 mcd @ 10 mA	45°	1.6 V @ 10 mA	1-54
	HLMP-6001				1.5 mcd @ 10 mA			
	HLMP-6203 HLMP-6204 HLMP-6205 HLMP-6206 HLMP-6208		Sub-Miniature	• 3 4 5 6 8	Red Diffused	1.2 mcd @ 10 mA			1-58

*Array Length.

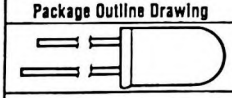
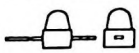
Mounting Hardware

Package Outline Drawing	Part No.	Description	Page No.
	HLMP-0103	Mounting Clip and Ring for T-1 3/4 Lamps	1-62
	HLMP-5029	Right Angle Housing for T-1 3/4 Lamps	1-63

Hermetically Sealed and High Reliability LED Lamps

Device		Description			Typical Luminous Intensity	2θ 1/2[1]	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color[2]	Package	Lens				
	1N5765 JAN1N5765[4] JANTX1N5765[4]	Red (640 nm)	Hermetic/ TO-46[3]	Red Diffused	0.5 mcd @ 20 mA	70°	1.6 V @ 20 mA	1-64
	1N6092 JAN1N6092[4] JANTX1N6092[4]	High Efficiency Red (626 nm)			1.0 mcd @ 20 mA		2.0 V @ 20 mA	
	1N6093 JAN1N6093[4] JANTX1N6093[4]	Yellow (585 nm)		Yellow Diffused				
	1N6094 JAN1N6094[4] JANTX1N6094[4]	Green (572 nm)		Green Diffused	0.8 mcd @ 25 mA		2.1 V @ 20 mA	
	HLMP-0930 HLMP-0931	Red (640 nm)	Panel Mount Version	Red Diffused	0.5 mcd @ 20 mA		1.6 V @ 20 mA	
	M19500/519-01[4] M19500/519-02[4]	High Efficiency Red (626 nm)			1.0 mcd @ 20 mA		2.0 V @ 20 mA	
	M19500/520-01[4] M19500/520-02[4]	Yellow (585 nm)		Yellow Diffused				
	M19500/521-01[4] M19500/521-02[4]	Green (572 nm)		Green Diffused	0.8 mcd @ 25 mA		2.1 V @ 20 mA	

Emitter Components

Package Outline Drawing	Part No.	Description	Features	Page No.
	HEMT-3300	670 nm High Radiant Intensity Emitter	• Visible (near IR) emission facilitates alignment • Compatible with most silicon phototransistors and photodiodes	1-70
	HEMT-6000	700 nm High Intensity Subminiature Emitter		1-72

NOTES:
1. θ1/2 is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. Peak Wavelength.
3. PC Board Mountable.
4. Military approval and qualified for High Reliability Applications. (-01 suffix is JAN level, -02 suffix is JANTX level).

HEWLETT PACKARD

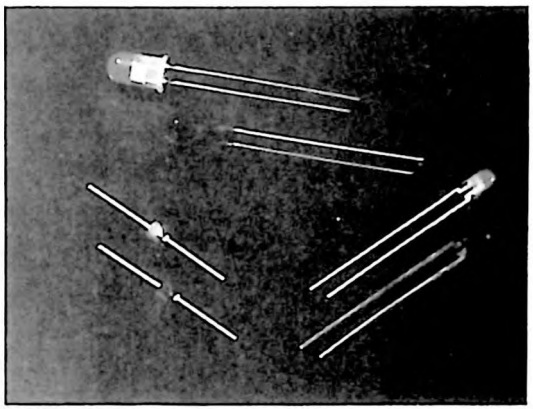
LOW CURRENT LED LAMP SERIES

T-1 3/4 (5mm)	HLMP-4700, -4719
T-1 (3mm)	HLMP-1700, -1719
SUBMINIATURE	HLMP-7000, -7019

TECHNICAL DATA JANUARY 1984

Features

- LOW POWER
- HIGH EFFICIENCY
- CMOS/MOS COMPATIBLE
- TTL COMPATIBLE
- WIDE VIEWING ANGLE
- CHOICE OF PACKAGE STYLES
- CHOICE OF COLORS



Applications

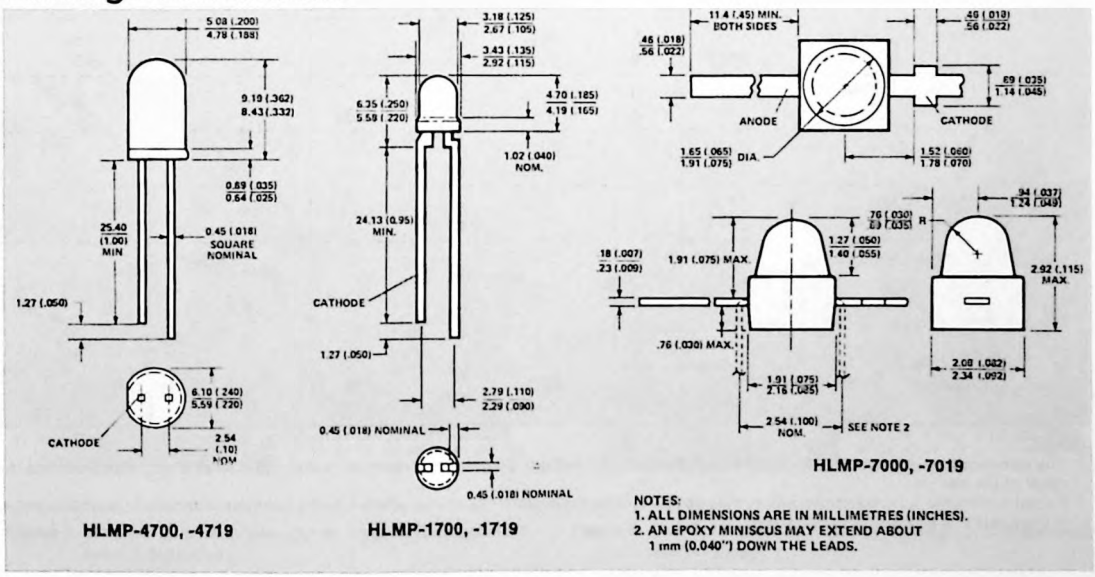
- LOW POWER DC CIRCUITS
- TELECOMMUNICATIONS INDICATORS
- PORTABLE EQUIPMENT
- KEYBOARD INDICATORS

Description

These tinted diffused LED lamps were designed and optimized specifically for low DC current operation. Luminous intensity and forward voltage are tested at 2 mA to assure consistent brightness at TTL output current levels.

The semiconductor material is Gallium Arsenide Phosphide on Gallium Phosphide. The HLMP-4700, -1700, -7000 are red LED's. The HLMP-4719, -1719, -7019 are yellow LED's.

Package Dimensions



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MINISCUS MAY EXTEND ABOUT 1 mm (0.040") DOWN THE LEADS.

AXIAL LUMINOUS INTENSITY AND VIEWING ANGLE @ 25° C

Part Number HLMP	Package Description	Color	I_V (mcd) @ 2 mA DC Min.	I_V (mcd) @ 2 mA DC Typ.	2θ 1/2[1]	Package Outline
-4700	T-1 3/4	Red	1.2	2.0	50°	A
-4719	Tinted Diffused	Yellow	1.2	1.8		
-1700	T-1 Tinted/	Red	1.0	1.8	50°	B
-1719	Diffused	Yellow	1.0	1.6		
-7000	Subminiature	Red	0.4	0.8	70°	C
-7019	Tinted Diffused	Yellow	0.4	0.6		

Notes:
1. Θ1/2 is the typical off-axis angle at which the luminous intensity is half the axial luminous intensity.

Absolute Maximum Ratings

Parameter	Maximum Rating		Units
Power Dissipation (Derate linearly from 92° C at 1.0 mA/° C	Red	27	mW
	Yellow	24	
DC and Peak Forward Current	7		mA
Transient Forward Current (10 msec pulse)	500		mA
Operating and Storage Temperature Range	-55° C to 100° C		
Lead Soldering Temperature (1.6 mm [0.063 in] from body)	260° C for 5 Seconds (T-1, T-1 3/4) 260° C for 3 Seconds (Subminiature)		

Electrical/Optical Characteristics at $T_A = 25°C$

Symbol	Description	T-1 3/4	T-1	Subminiature	Min.	Typ.	Max.	Units	Test Condition
V_F	Forward Voltage	4700 4719	1700 1719	7000 7019		1.8 1.9	2.2 2.7	V	2 mA
BV_R	Reverse Breakdown	4700 4719	1700 1719	7000 7019	5.0 5.0	30 40		V	$I_R = 50\ \mu A$
λ_P	Peak Wavelength	4700 4719	1700 1719	7000 7019		635 583		nm	Measurement at peak
λ_D	Dominant Wavelength	4700 4719	1700 1719	7000 7019		629 585		nm	Note 2
T_S	Speed of Response	4700 4719	1700 1719	7000 7019		100 200		ns	
C	Capacitance	4700 4719	1700 1719	7000 7019		4 4		pF	$V_F = 0$ f = 1 MHz
θ_{JC}	Thermal Resistance	4700 4719	1700 1719	7000 7019		190		°C/W	Junction to Cathode lead at 0.079 mm (0.031 in) from body
η_V	Luminous Efficacy	4700 4719	1700 1719	7000 7019		147 570		Lumens/ Watt	Note 3

Notes:
2. The dominant wavelength, λ_D, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

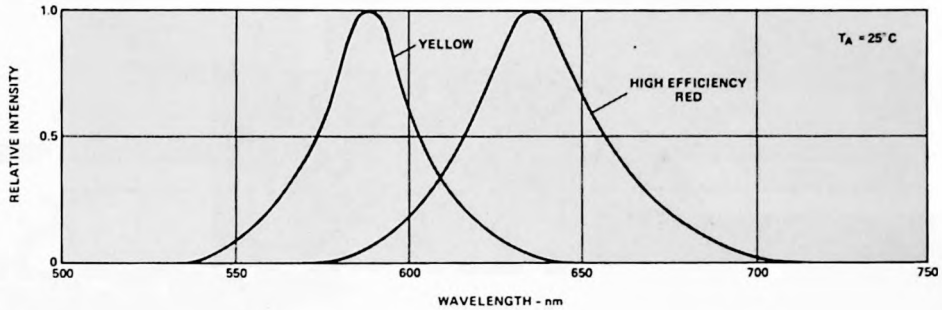


Figure 1. Relative Intensity vs. Wavelength

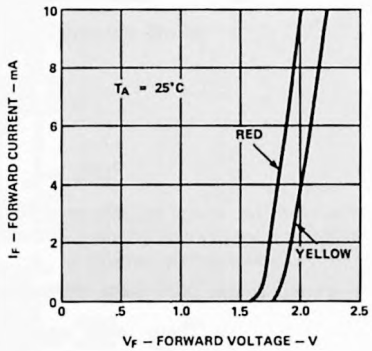


Figure 2. Forward Current vs. Forward Voltage

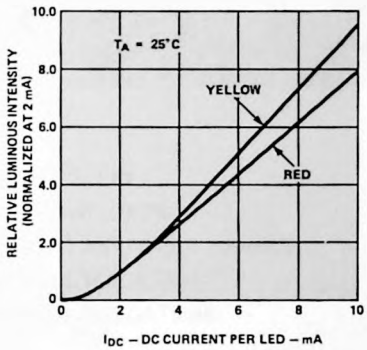


Figure 3. Relative Luminous Intensity vs. Forward Current

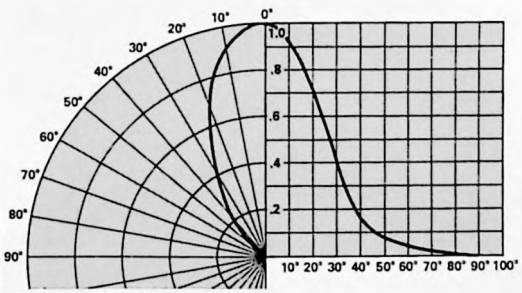


Figure 4. Relative Luminous Intensity vs. Angular Displacement for T-1 3/4 Lamp

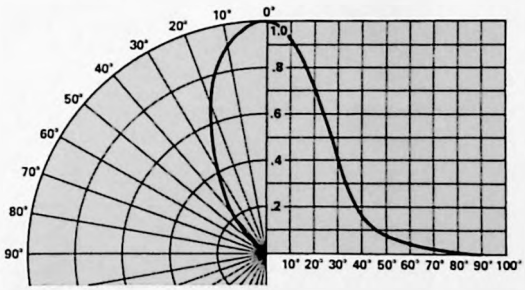


Figure 5. Relative Luminous Intensity vs. Angular Displacement for T-1 Lamp

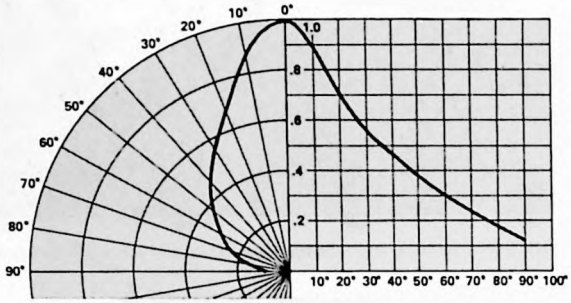


Figure 6. Relative Luminous Intensity vs. Angular Displacement for Subminiature Lamp

HEWLETT PACKARD

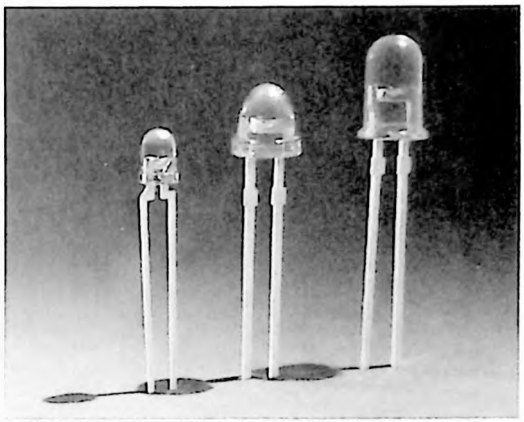
ULTRA-BRIGHT LED LAMP SERIES

T-1 3/4 HLMP-3750,-3850,-3950
T-1 3/4 LOW PROFILE HLMP-3390,-3490,-3590
T-1 HLMP-1340,-1440,-1540

TECHNICAL DATA JANUARY 1984

Features

- IMPROVED BRIGHTNESS
- IMPROVED COLOR PERFORMANCE
- AVAILABLE IN POPULAR T-1 and T-1 3/4 PACKAGES
- NEW STURDY LEADS
- IC COMPATIBLE/LOW CURRENT CAPABILITY
- RELIABLE AND RUGGED
- CHOICE OF 3 BRIGHT COLORS
  High Efficiency Red
  High Brightness Yellow
  High Performance Green



Description

These clear, non-diffused lamps out perform conventional LED lamps. By utilizing new higher intensity material, we achieve superior product performance.

The HLMP-3750/-3390/-1340 Series Lamps are Gallium Arsenide Phosphide on Gallium Phosphide red light emitting diodes. The HLMP-3850/-3490/-1440 Series are Gallium Arsenide Phosphide on Gallium Phosphide yellow light emitting diodes. The HLMP-3950/-3590/-1540 Series lamps are Gallium Phosphide green light emitting diodes.

Applications

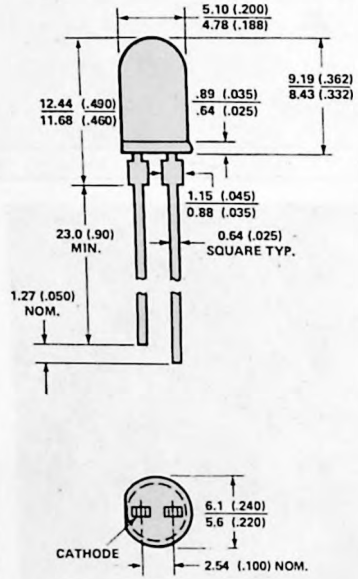
- LIGHTED SWITCHES
- BACKLIGHTING FRONT PANELS
- LIGHT PIPE SOURCES
- KEYBOARD INDICATORS

Axial Luminous Intensity and Viewing Angle @ 25°C

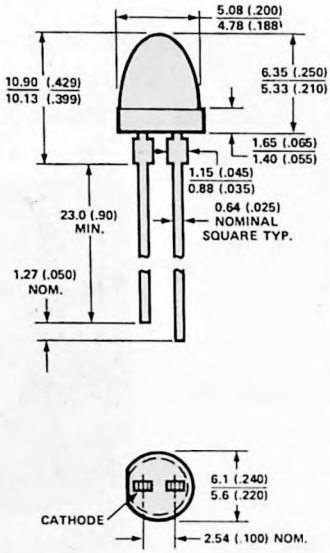
Part Number HLMP-	Package Description	Color	I_V (mcd) @ 20 mA DC		2θ 1/2 Note 1.	Package Outline
			Min.	Typ.		
3750	T-1 3/4	Red	80	125	24°	A
3850		Yellow	80	140	24°	A
3950		Green	80	120	24°	A
3390	T-1 3/4 Low Profile	Red	35	55	32°	B
3490		Yellow	35	55	32°	B
3590		Green	35	55	32°	B
1340	T-1	Red	24	35	45°	C
1440		Yellow	24	35	45°	C
1540		Green	24	35	45°	C

NOTE:
1. θ1/2 is the typical off-axis angle at which the luminous intensity is half the axial luminous intensity.

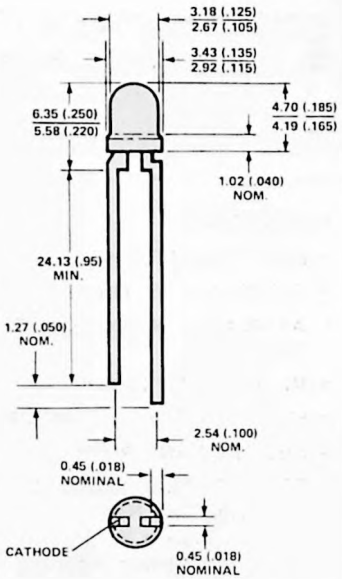
Package Dimensions



PACKAGE OUTLINE "A"
HLMP-3750, 3850, 3950



PACKAGE OUTLINE "B"
HLMP-3390, 3490, 3590



PACKAGE OUTLINE "C"
HLMP-1340, 1440, 1540

NOTES:
1. All dimensions are in millimeters (inches).
2. Silver plated leads. See Application Bulletin 3.
3. An epoxy meniscus may extend about 1mm (0.40") down the leads.

Absolute Maximum Ratings at $T_A = 25°C$

Parameter	Red	Yellow	Green	Units
Peak Forward Current	90	60	90	mA
Average Forward Current[1]	25	20	25	mA
DC Current[2]	30	20	30	mA
Power Dissipation[3]	135	85	135	mW
Operating Temperature Range	−55 to +100	−55 to +100	−40 to +100	C°
Storage Temperature Range			−55 to +100	
Lead Soldering Temperature [1.6 mm (0.063 in.) from body]	260° C for 5 seconds			

1. See Figure 2 to establish pulsed operating conditions.
2. For Red and Green series derate linearly from 50° C at 0.5 mA/° C. For Yellow series derate linearly from 50° C at 0.2 mA/° C.
3. For Red and Green series derate power linearly from 25° C at 1.8 mW/° C. For Yellow series derate power linearly from 50° C at 1.6 mW/° C.

Electrical/Optical Characteristics at $T_A = 25°C$

Symbol	Description	T-1 3/4	T-1 3/4 Low Dome	T-1	Min.	Typ.	Max.	Units	Test Conditions
λ_P	Peak Wavelength	3750 3850 3950	3390 3490 3590	1340 1440 1540		635 583 565		nm	Measurement at Peak
λ_d	Dominant Wavelength	3750 3850 3950	3390 3990 3590	1340 1440 1540		629 585 571		nm	Note 1
T_S	Speed of Response	3750 3850 3950	3390 3490 3590	1340 1440 1540		90 90 500		ns	
C	Capacitance	3750 3850 3950	3390 3490 3590	1340 1440 1540		16 18 18		pF	$V_F = 0$; f = 1 MHz
Θ_{JC}	Thermal Resistance	3750 3850 3950	3390 3490 3590	 1340 1440 1540		140 140 140 95 95 95		°C/W	Junction to Cathode Lead at 0.79 mm (0.031 in.) from Body
V_F	Forward Voltage	3750 3850 3950	3390 3490 3590	1340 1440 1540	1.6 1.6 1.6	2.2 2.2 2.3	3.0 3.0 3.0	V	I_F = 20 mA (Figure 3)
BV_R	Reverse Breakdown Voltage	3750 3850 3950	3390 3490 3590	1340 1440 1540	5.0			V	I_F = 100 μA
η_V	Luminous Efficacy	3750 3850 3950	3390 3490 3590	1340 1440 1540		147 570 630		lumens/watt	Note 2

NOTES:
1. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
2. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is the luminous efficacy in lumens/watt.

Red, Yellow and Green

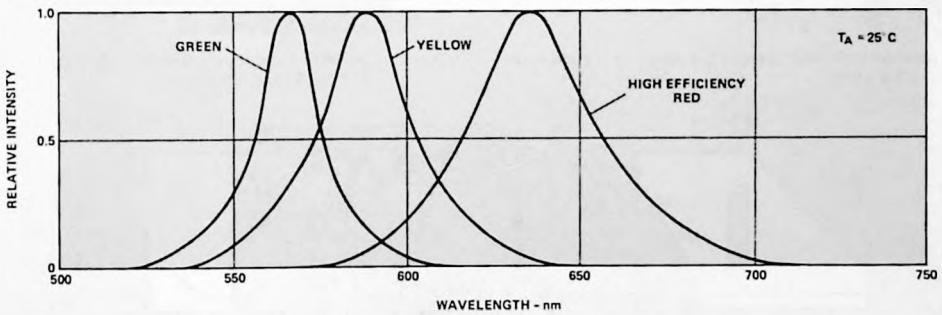


Figure 1. Relative Intensity vs. Wavelength.

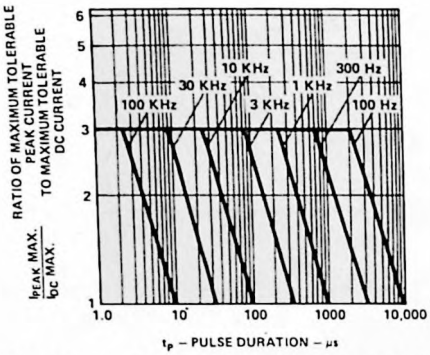


Figure 2. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings.)

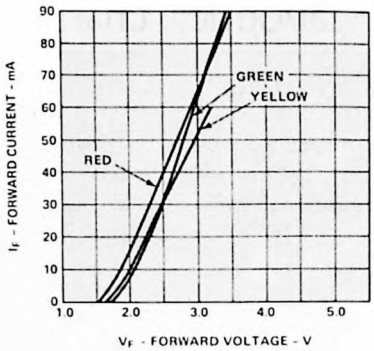


Figure 3. Forward Current vs. Forward Voltage.

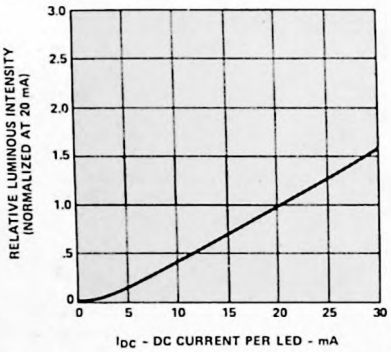


Figure 4. Relative Luminous Intensity vs. Forward Current.

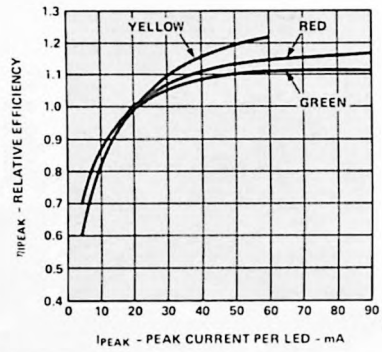


Figure 5. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

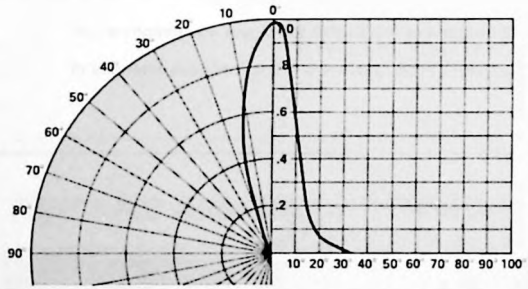


Figure 6. Relative Luminous Intensity vs. Angular Displacement. T-1 3/4 Lamp.

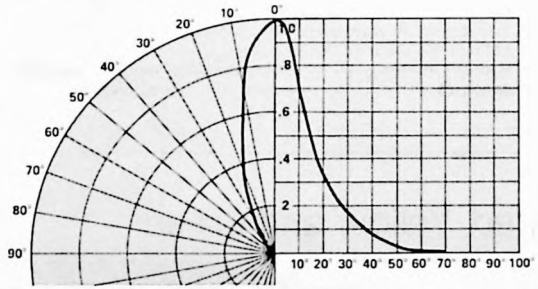


Figure 7. Relative Luminous Intensity vs. Angular Displacement. T-1 3/4 Low Profile Lamp.

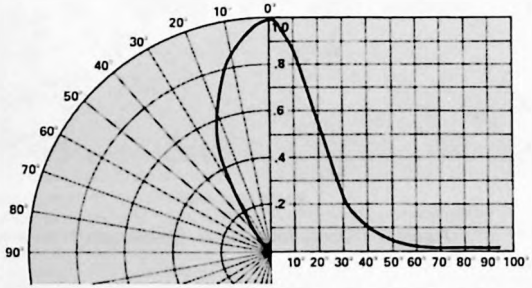


Figure 8. Relative Luminous Intensity vs. Angular Displacement. T-1 Lamp.

HEWLETT PACKARD

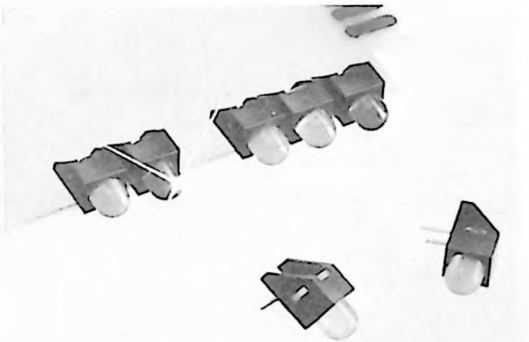
LED RIGHT ANGLE INDICATORS T-1 3/4 (5mm)

RED	HLMP-5000	HER	HLMP-5030	HER 5 V	HLMP-5060
RED 5 V	HLMP-5005	YELLOW	HLMP-5040	YELLOW 5 V	HLMP-5070
RED 12 V	HLMP-5012	GREEN	HLMP-5050	GREEN 5 V	HLMP-5080

TECHNICAL DATA JANUARY 1984

Features

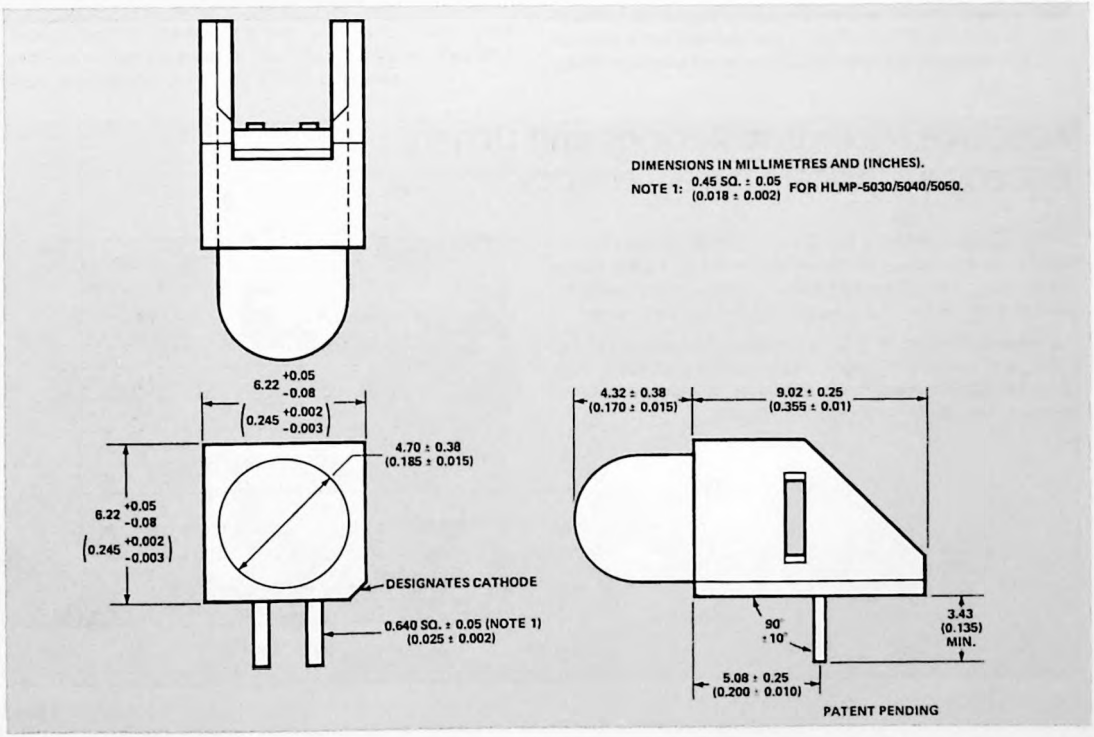
- IDEAL FOR CARD EDGE STATUS INDICATION
- PACKAGE DESIGN ALLOWS FLUSH SEATING ON A PC BOARD
- MAY BE SIDE STACKED ON 6.35 mm (0.25") CENTERS
- LEDs AVAILABLE IN FOUR COLORS, WITH OR WITHOUT INTEGRATED CURRENT LIMITING RESISTOR IN T-1 3/4 TINTED DIFFUSED PACKAGES



Description

The HLMP-5000 series of Right Angle Indicators are industry standard status indicators that incorporate a tinted diffused T-1 3/4 LED lamp in a black plastic housing. The indicators are available in standard Red, High Efficiency Red, Yellow, or High Performance Green with or without an integrated current limiting resistor. These products are designed to be used as back panel diagnostic indicators and card edge logic status indicators.

Package Dimensions



Electrical/Optical Characteristics at $T_A = 25°C$

RIGHT ANGLE INDICATORS WITHOUT INTEGRATED CURRENT LIMITING RESISTOR

Part Number	Color	Luminous Intensity (I_V) mcd		Forward Voltage (V_F)		Test Condition for I_V and V_F	Minimum Reverse Breakdown Voltage at (V_{BR}) $I_R = 100\ \mu A$
		Min.	Typ.	Typ.	Max.		
HLMP-5000	Red	2.0	4.0	1.6	2.0	$I_F = 20$ mA	3.0
HLMP-5030	High Efficiency Red	3.0	6.0	2.2	3.0	$I_F = 10$ mA	5.0
HLMP-5040	Yellow	3.0	6.0	2.2	3.0	$I_F = 10$ mA	5.0
HLMP-5050	Green	3.0	6.0	2.3	3.0	$I_F = 20$ mA	5.0

RIGHT ANGLE INDICATORS WITH CURRENT LIMITING RESISTOR

Part Number	Color	Luminous Intensity (I_V) mcd		Forward Current (I_F) mA		Test Condition for I_V and I_F	Minimum Reverse Breakdown Voltage at (V_{BR}) $I_R = 100\ \mu A$
		Min.	Typ.	Typ.	Max.		
HLMP-5012	Red	1.0	2.0	13	20	$V_F = 12$ V	3.0
HLMP-5005	Red	1.0	2.0	13	20	$V_F = 5$ V	3.0
HLMP-5060	High Efficiency Red	1.5	4.0	10	15	$V_F = 5$ V	5.0
HLMP-5070	Yellow	1.5	4.0	10	15	$V_F = 5$ V	5.0
HLMP-5080	Green	1.5	4.0	12	15	$V_F = 5$ V	5.0

Absolute Maximum Ratings and Other Electrical/Optical Characteristics

The absolute maximum ratings and typical device characteristics are identical to those of the T-1 3/4 LED lamps listed here. For information about these characteristics, see the data sheets of the equivalent T-1 3/4 LED lamp.

All Hewlett-Packard T-1 3/4 high-dome lamps, except ferrules, are available in right angle housing. Contact your local Hewlett-Packard Sales Office or authorized components distributor for ordering information.

Right Angle Indicator (Part Number)	Equivalent T-1 3/4 LED Lamp (Part Number)
HLMP-5000	HLMP-3001
HLMP-5005	HLMP-3105
HLMP-5012	HLMP-3112
HLMP-5030	HLMP-3300
HLMP-5040	HLMP-3400
HLMP-5050	HLMP-3502
HLMP-5060	HLMP-3600
HLMP-5070	HLMP-3650
HLMP-5080	HLMP-3680

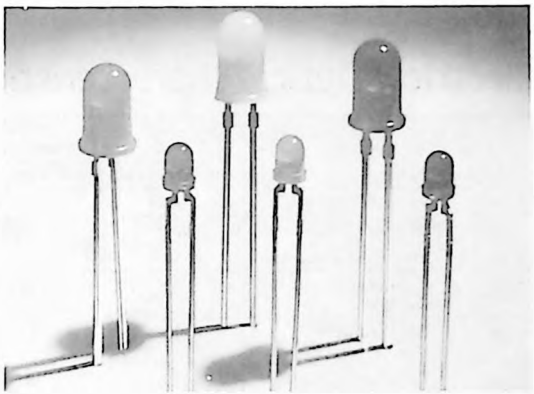
HEWLETT PACKARD

INTEGRATED RESISTOR LAMPS
5 Volt and 12 Volt Series in T-1 and T-1 3/4 Packages

TECHNICAL DATA JANUARY 1984

Features

- **INTEGRAL CURRENT LIMITING RESISTOR**
- **TTL COMPATIBLE**
  Requires no External Current Limiter with 5 Volt/12 Volt Supply
- **COST EFFECTIVE**
  Saves Space and Resistor Cost
- **WIDE VIEWING ANGLE**
- **AVAILABLE IN ALL COLORS**
  Red, High Efficiency Red, Yellow and High Performance Green in T-1 and T-1 3/4 Packages



Description

The 5 volt and 12 volt series lamps contain an integral current limiting resistor in series with the LED. This allows the lamp to be driven from a 5 volt/12 volt source without an external current limiter. The red LEDs are made from GaAsP on a GaAs substrate. The High Efficiency Red and Yellow devices use GaAsP on a GaP substrate.

The green devices use GaP on a GaP substrate. The diffused lamps provide a wide off-axis viewing angle.

The T-1 3/4 lamps are provided with sturdy leads suitable for wire wrap applications. The T-1 3/4 lamps may be front panel mounted by using the HLMP-0103 clip and ring.

Color	P/N HLMP-	Package	Operating Voltage	I_V mcd		2Θ 1/2[1]	Package Outline
				Min.	Typ.		
Red	1100	T-1 Tinted Diffused	5	0.8	1.5	60°	A
	1120	T-1 Untinted Diffused	5	0.8	1.5	60°	A
	3105	T-1 3/4 Tinted Diffused	5	1.0	2.0	75°	B
	3112		12	1.0	2.0	75°	B
High Efficiency Red	1600	T-1 Tinted Diffused	5	1.5	4.0	60°	A
	1601		12				
	3600	T-1 3/4 Tinted Diffused	5			65°	B
	3601		12				
Yellow	1620	T-1 Tinted Diffused	5	1.5	4.0	60°	A
	1621		12				
	3650	T-1 3/4 Tinted Diffused	5			75°	B
	3651		12				
High Performance Green	1640	T-1 Tinted Diffused	5	1.5	4.0	60°	A
	1641		12				
	3680	T-1 3/4 Tinted Diffused	5			75°	B
	3681		12				

Notes:
1. $\Theta 1/2$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.

Absolute Maximum Ratings at $T_A = 25°C$

	5 Volt Lamps	12 Volt Lamps
DC Forward Voltage ($T_A = 25°C$)	7.5 Volts[2]	15 Volts[3]
Operating Temperature Range	−40°C to 85°C	−40°C to 85°C
Storage Temperature Range	−55°C to 100°C	−55°C to 100°C
Lead Soldering Temperature	260°C for 5 seconds	

Notes:
2. Derate from $T_A = 50°C$ at 0.071V/°C, see Figure 3.
3. Derate from $T_A = 50°C$ at 0.086V/°C, see Figure 4.

Electrical/Optical Characteristics at $T_A = 25°C$

		Red			High Efficiency Red			Yellow			Green				
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units	Test Conditions
λ_{PEAK}	Peak Wavelength		655			635			583			565		nm	
λ_d	Dominant Wavelength		640			626			585			569		nm	Note 4
$R\theta_{J-PIN}$	Thermal Resistance		90			90			90			90		°C/W	Junction to lead at 3 mm from body
I_F	Forward Current 12 V Devices		13	20		13	20		13	20		13	20		
I_F	Forward Current 5 V Devices		13	20		10	15		10	15		12	15	mA	At rated voltage
η_V	Luminous Efficacy		55			147			570			630		lumen /watt	Note 5
V_{BR}	Reverse Breakdown Voltage	3.0			5.0			5.0			5.0			V	$I_R = 100\ \mu A$

Notes:
4. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
5. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_V/\eta_V$. Where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

Package Dimensions

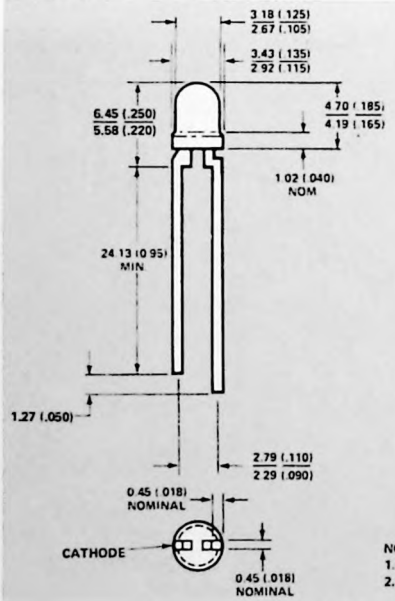


Figure A. T-1 Package

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MENISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

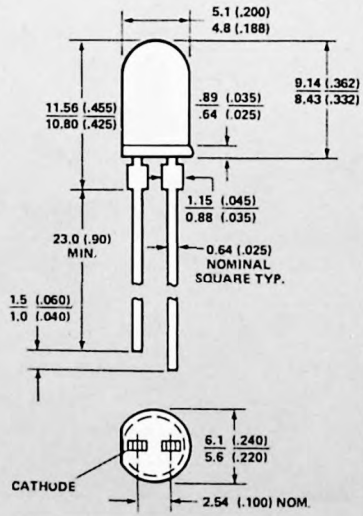


Figure B. T-1 3/4 Package

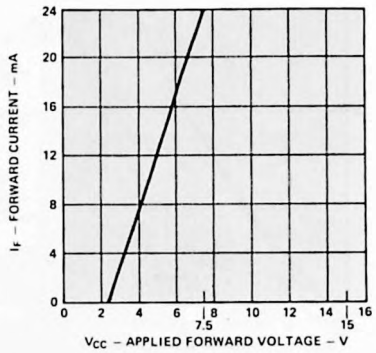


Figure 1. Forward Current vs. Applied Forward Voltage. 5 Volt Devices

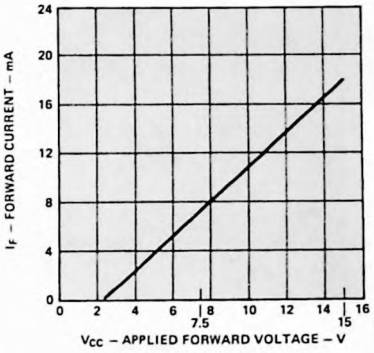


Figure 2. Forward Current vs. Applied Forward Voltage. 12 Volt Devices

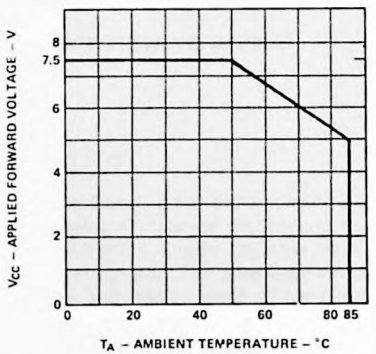


Figure 3. Maximum Allowed Applied Forward Voltage vs. Ambient Temperature $R\theta_{JA}$ = 175° C/W. 5 Volt Devices

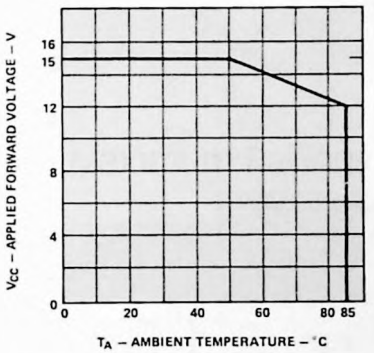


Figure 4. Maximum Allowed Applied Forward Voltage vs. Ambient Temperature $R\theta_{JA}$ = 175° C/W. 12 Volt Devices

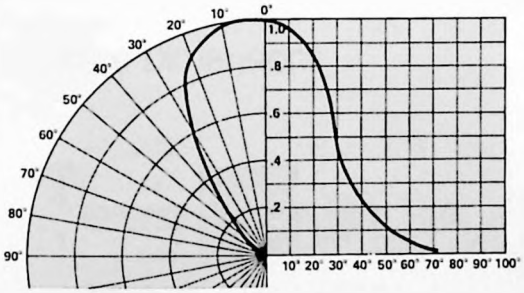


Figure 5. Relative Luminous Intensity vs. Angular Displacement for T-1 Package

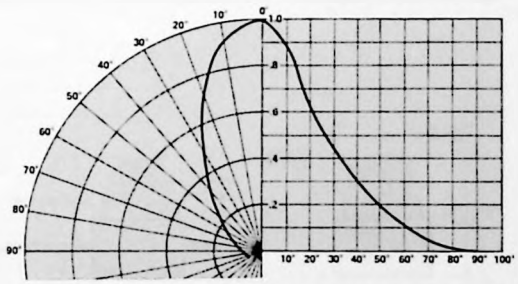


Figure 6. Relative Luminous Intensity vs. Angular Displacement for T-1 3/4 Package

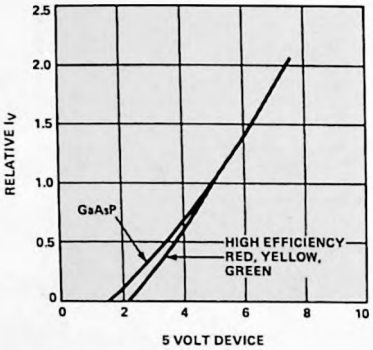


Figure 7. Relative Luminous Intensity vs. Applied Forward Voltage. 5 Volt Devices

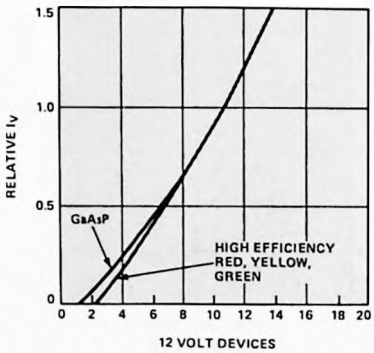


Figure 8. Relative Luminous Intensity vs. Applied Forward Voltage. 12 Volt Devices

HEWLETT PACKARD

SUBMINIATURE RESISTOR LAMPS

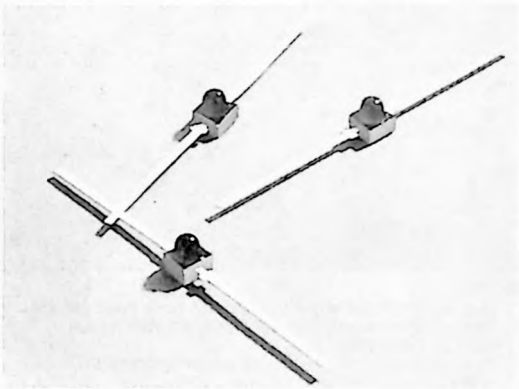
HIGH EFFICIENCY RED

5 VOLT, 4mA • HLMP-6620
5 VOLT, 10mA • HLMP-6600

TECHNICAL DATA JANUARY 1984

Features

- **IDEAL FOR TTL AND LSTTL GATE STATUS INDICATION**
- **REQUIRES NO EXTERNAL RESISTORS WITH 5 VOLT SUPPLY**
- **SPACE SAVING SUBMINIATURE PACKAGE**
- **TWO CHOICES OF CURRENT LEVEL**
- **EXCELLENT VIEWING ANGLE**



Description

The HLMP-6600 and HLMP-6620 provide a Red Gallium Arsenide Phosphide on Gallium Phosphide Light Emitting Diode together with an integral biasing resistor. The package has a red diffused lens and radial leads. Tape-and-reel mounting is available on request.

Special lead bending is available on 2.54mm (.100 in) and 5.08mm (.200 in) centers.

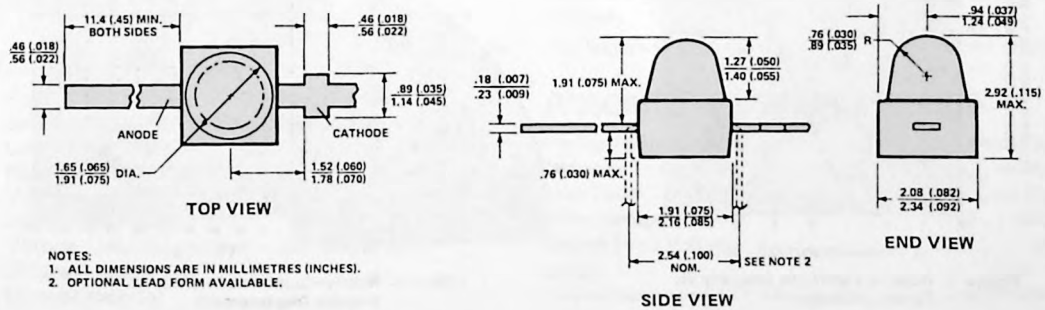
Absolute Maximum Ratings

	HLMP-6600/-6620
DC Forward Voltage	6 Volts
Operating Temperature Range	-55°C to 70°C
Storage Temperature Range	-55°C to 100°C
Lead Soldering Temperature [1.6mm (0.063 in.) from body]	260°C for 3 sec.

Tape and Reel Order Chart

Standard Product HLMP-	6600	6620
Tape & Reel P/N	HLMP-6607	HLMP-6627

Package Dimensions



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. OPTIONAL LEAD FORM AVAILABLE.

Electrical/Optical Characteristics at T_A=25°C

Symbol	Parameter	HLMP-6600			HLMP-6620			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.		
I_V	Axial Luminous Intensity	1.0	2.4	—	0.2	0.6	—	mcd	V_F = 5 Volts (See Figure 3)
$2\theta_{1/2}$	Included Angle Between Half Luminous Intensity Points		80°			80°			Note 1 (See Figure 4)
λ_{PEAK}	Peak Wavelength		635			635		nm	Measurement at Peak
λ_d	Dominant Wavelength		629			629		nm	Note 2
θ_j	Thermal Resistance		120			120		°C/W	Junction to Cathode Lead at 0.79mm (0.031 in.) From Body
I_F	Forward Current		9.6	13		3.5	5	mA	V_F=5 Volts (See Figure 2)
V_{BR}	Reverse Voltage	5.0	15.0		5.0	15.0		V	I_R = 100 μA
η_V	Luminous Efficacy		147			147		lm/W	Note 3

NOTES:
1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

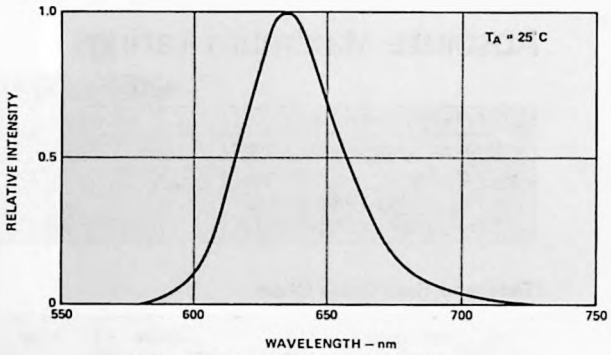


Figure 1. Relative Intensity vs. Wavelength.

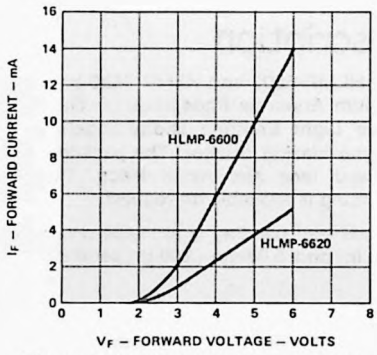


Figure 2. Forward Current vs. Forward Voltage.

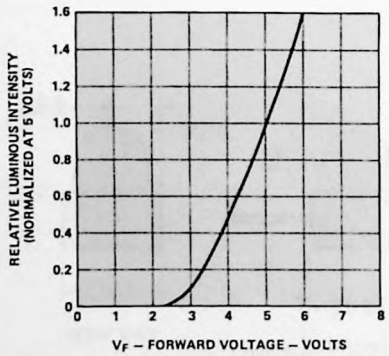


Figure 3. Relative Luminous Intensity vs. Forward Voltage.

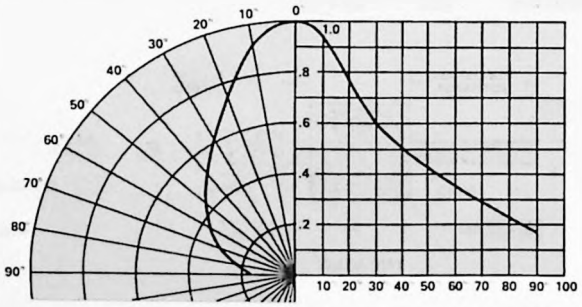


Figure 4. Relative Luminous Intensity vs. Angular Displacement.

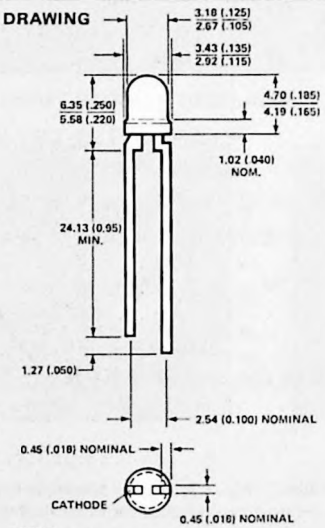
HEWLETT PACKARD

T-1 (3mm) VOLTAGE SENSING RED SOLID STATE LAMP

HLMP 1142

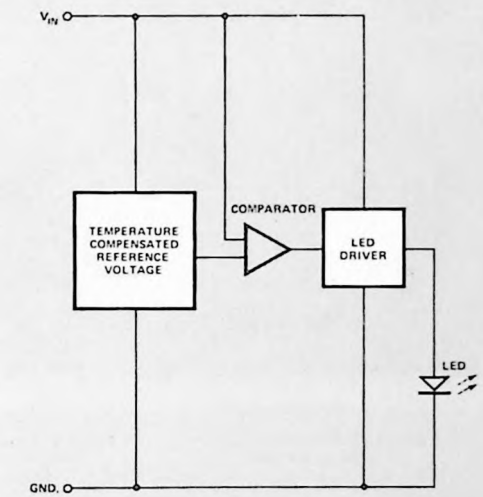
TECHNICAL DATA JANUARY 1984

OUTLINE DRAWING



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MENISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

BLOCK DIAGRAM



Features

- **HIGH SENSITIVITY: 10mV ON TO OFF**
- **BUILT IN LED CURRENT LIMITING**
- **TEMPERATURE COMPENSATED THRESHOLD VOLTAGE**
- **COMPACT: PACKAGE INCLUDES INTEGRATED CIRCUIT AND LED**
- **GUARANTEED MINIMUM LUMINOUS INTENSITY**
- **THRESHOLD VOLTAGE CAN BE INCREASED WITH EXTERNAL COMPONENT**

Applications

- Push-to-test battery voltage tester (pagers, cameras, appliances, radios, test equipment. . .)
- Logic level indicator
- Power supply voltage monitor
- V-U meter
- Analog level sense
- Voltage indicating arrays — use several with different thresholds
- Current monitor

Description

The HP voltage sensing LEDs use an integrated circuit and a red GaAsP LED to provide a complete voltage sensing function in a standard red diffused T-1 LED package. When the input voltage (V_{IN}) exceeds the threshold voltage (V_{TH}) the LED turns "on". The high gain of the comparator provides unambiguous indication by the LED of the input voltage with respect to the threshold voltage. The V-I characteristics are resistive above and below the threshold voltage. This allows battery testing under simulated load conditions. Use of a resistor, diode or zener in series allows the threshold voltage to be increased to any desired voltage. A resistor in parallel allows the sensing LED to be used as a current threshold indicator.

The HLMP-1142 has a nominal threshold voltage of 2.7V.

Absolute Maximum Ratings

Storage Temperature	-55°C to +100°C
Operating Temperature	-55°C to +85°C
Lead Solder Temperature	260°C for 5 Sec.
Input Voltage — V_{IN} [1]	+5V dc
Reverse Input Voltage — V_R	-0.5V

NOTES:
1. Derate linearly above 50°C free-air temperature at a rate of 37mV/°C.

Electro-Optical Characteristics at $T_A = 25°C$

Parameter	Sym.	HLMP-1142 Min.	HLMP-1142 Typ.	HLMP-1142 Max.	Units	Test Conditions	Fig.
Threshold Voltage	V_{TH}	2.5	2.7	2.9	V		1,2
Temperature Coefficient of Threshold	$\frac{\Delta V_{TH}}{\Delta T_A}$		−1		mV/°C		
Input Current	I_{IN}		13		mA	V_{IN} = 2.75V	2
			33	50	mA	V_{IN} = 5.0V	2
Luminous Intensity	I_v	0.3	0.7		mcd	V_{IN} = 2.75V	1
Wavelength	λ_{PEAK}		655		nm	Measurement at peak	
Dominant Wavelength	λ_d		640		nm	Note 1	

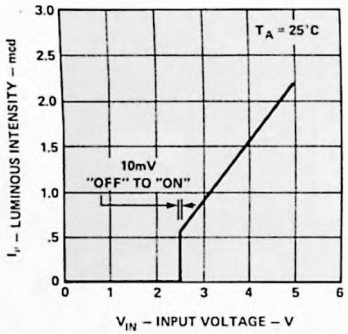


Figure 1. Luminous Intensity vs. Input Voltage.

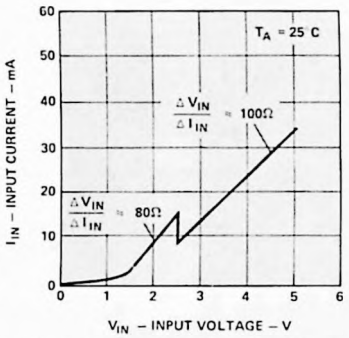


Figure 2. Input Current vs. Input Voltage.

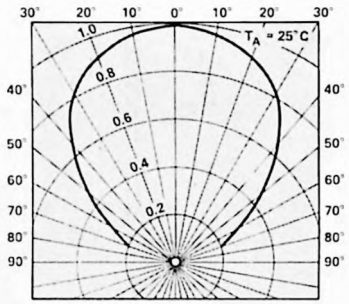
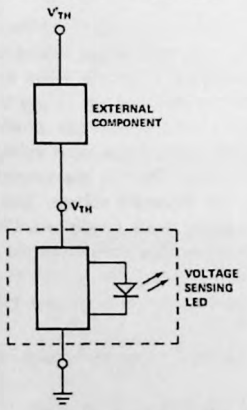


Figure 3. Relative Luminous Intensity vs. Angular Displacement.

Techniques For Increasing The Threshold Voltage



External Component	V'_{TH}	$TC = \frac{\Delta V'_{TH}}{\Delta T_A}$ (mV/°C)
Schottky Diode (HP 5082-2835)	V_{TH} + 0.45V	−2
P-N Diode (1N914)	V_{TH} + 0.75V	−2.5
LED (HLMP-1000)	V_{TH} + 1.6V	−2.9
Zener Diode	$V_{TH} + V_Z$	−1 + Zener TC

Notes:
1. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
2. I_{TH} is the maximum current just below the threshold, V_{TH}. Since both I_{TH} and V_{TH} are variable, a precise value of V'_{TH} is obtainable only by selecting R to fit the measured characteristics of the individual devices (e.g., with curve tracer).
3. The temperature coefficient (TC) will be a function of the resistor TC and the value of the resistor.

HEWLETT PACKARD

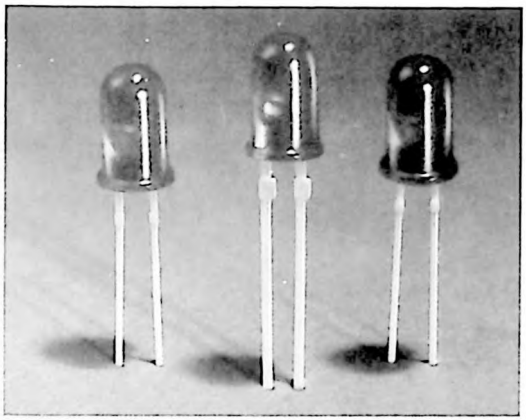
HIGH BRIGHTNESS DIFFUSED LED LAMPS

HIGH EFFICIENCY RED • HLMP-4600 SERIES

TECHNICAL DATA JANUARY 1984

Features

- HIGH INTENSITY
- HIGH PERFORMANCE RED LAMP
- POPULAR T-1¾ PACKAGE
- LIGHT OUTPUT CATEGORIES
- DIFFUSED LENS/NARROW VIEWING ANGLE
- GENERAL PURPOSE AND WIRE WRAPPABLE LEADS
- IC COMPATIBLE/LOW CURRENT REQUIREMENTS
- RELIABLE AND RUGGED
- COMPATIBLE WITH HLMP-0103 PANEL MOUNT



Description

The HLMP-4600 Series lamps are Gallium Arsenide Phosphide on Gallium Phosphide diodes emitting red light.

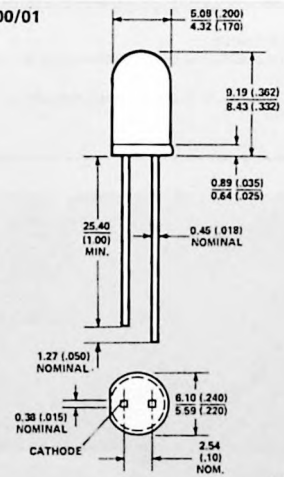
General purpose and selected brightness versions of the diffused lens type are available.

The HLMP-4600/-4601 are high performance red T-1 3/4 lamps made to be used in illuminator and general purpose applications. The HLMP-4610 is a 4600 lamp with .025" leads.

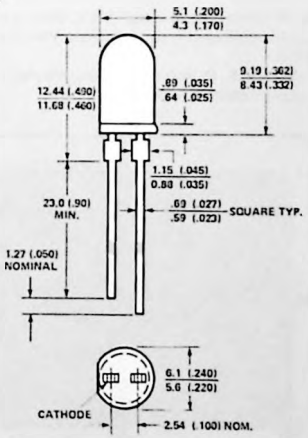
Part Number HLMP-	Application	Lens	Color
4600/ 4610	Indicator — General Purpose	Tinted Diffused	High Efficiency Red
4601	Indicator — High Brightness	Tinted Diffused	High Efficiency Red

Package Dimensions

HLMP-4600/01



HLMP-4610



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MENISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

Absolute Maximum Ratings at $T_A = 25°C$

Parame'er	4600 Series	Units
Power Dissipation[1]	135	mW
DC Forward Current[2]	30	mA
Average Forward Current[3]	25	mA
Peak Operating Forward Current	90	mA
Operating and Storage Temperature Range	-55° C to +100° C	
Lead Solder Temperature (1.6 mm [0.063 inch] below package base)	260° C for 5 seconds	

NOTES:
1. Derate from 25° C at 1.8 mW/° C.
2. Derate from 50° C at 0.5 mA/° C.
3. See Figure 5 to establish pulsed operating conditions.

Electrical Characteristics at $T_A = 25°C$

Symbol	Description	Device HLMP-	Min.	Typ.	Max.	Units	Test Conditions
I_V	Luminous Intensity	4600/10	2.0	4.0		mcd	I_F = 10mA (Fig. 3)
				10.0		mcd	I_F = 20mA
		4601	4.0	8.0		mcd	I_F = 10mA
				20.0		mcd	I_F = 20mA
$2\Theta_{1/2}$	Viewing Angle	4600/01/10		32		Deg	I_F = 10mA See Note 1 (Fig. 6)
λ_{PEAK}	Peak Wavelength	4600/01/10		635		nm	Measurement at Peak (Fig. 1)
λ_d	Dominant Wavelength	4600/01/10		626		nm	See Note 2
τ_S	Speed of Response	4600/01/10		90		ns	
C	Capacitance	4600/01/10		16		pF	V_F = 0, f = 1 MHz
Θ_{JC}	Thermal Resistance	4600/01/10		135		°C/W	Junction to Cathode Lead at Seating Plane
V_F	Forward Voltage	4600/01/10	1.5	2.2	3.0	V	I_F = 10mA (Fig. 2)
V_{BR}	Reverse Breakdown Voltage	4600/01/10	5.0			V	I_R = 100μA
η_V	Luminous Efficacy	4600/01/10		147		lumens/ watt	See Note 3

Notes:
1. $\Theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is the luminous efficacy in lumens/watt.

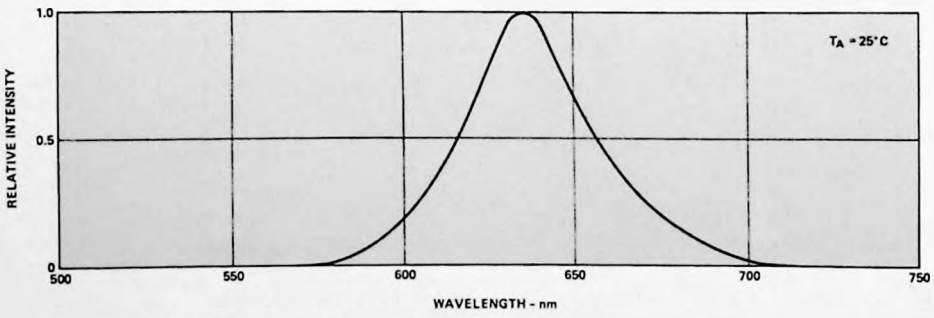


Figure 1. Relative Intensity vs. Wavelength

High Efficiency Red HLMP-4600 Series

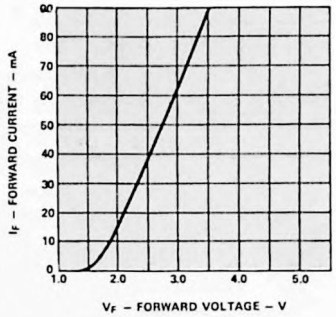


Figure 2. Forward Current vs Forward Voltage Characteristics.

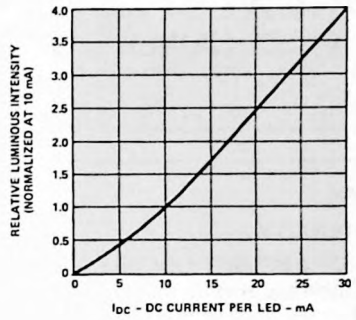


Figure 3. Relative Luminous Intensity vs. DC Forward Current.

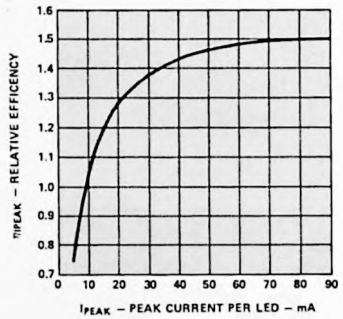


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. LED Peak Current.

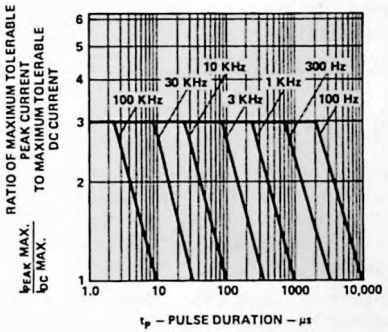
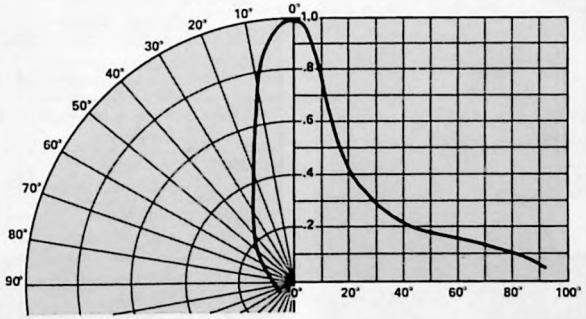


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings).



.Figure 6. Relative Luminous Intensity vs. Angular Displacement

HEWLETT PACKARD

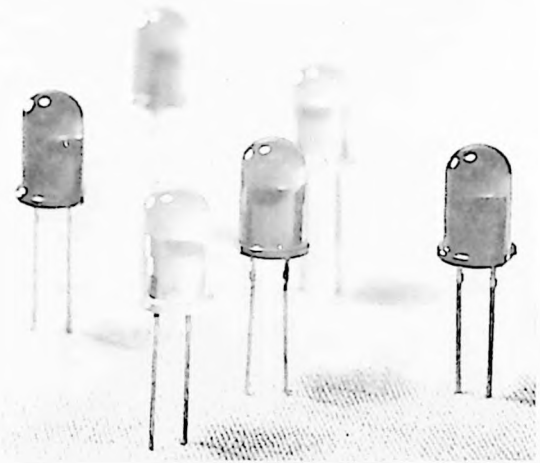
T-1 3/4 (5mm) SOLID STATE LAMPS

HIGH EFFICIENCY • HLMP-3300 SERIES
YELLOW • HLMP-3400 SERIES
HIGH PERFORMANCE GREEN • HLMP-3500 SERIES

TECHNICAL DATA JANUARY 1984

Features

- HIGH INTENSITY
- CHOICE OF 3 BRIGHT COLORS
  - High Efficiency Red
  - Yellow
  - High Performance Green
- POPULAR T-1¾ DIAMETER PACKAGE
- LIGHT OUTPUT CATEGORIES
- WIDE VIEWING ANGLE AND NARROW VIEWING ANGLE TYPES
- GENERAL PURPOSE LEADS
- IC COMPATIBLE/LOW CURRENT REQUIREMENTS
- RELIABLE AND RUGGED

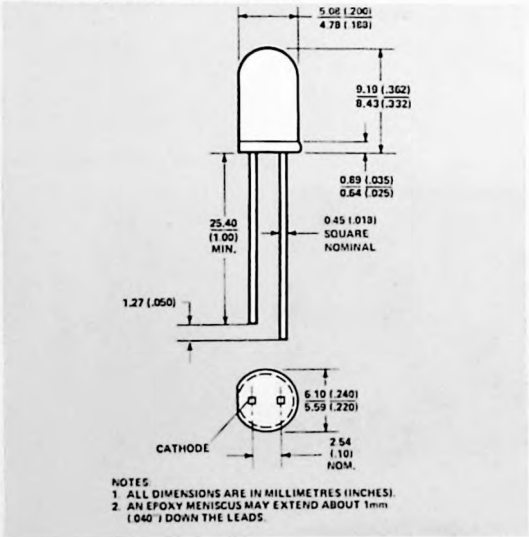


Description

The HLMP-3300 and the HLMP-3400 Series lamps are Gallium Arsenide Phosphide on Gallium Phosphide diodes emitting red and yellow light respectively. The HLMP-3500 Series lamps are green light emitting Gallium Phosphide diodes.

General purpose and selected brightness versions of both the diffused and non-diffused lens type are available in each family.

Package Dimensions



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MENISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

Part Number HLMP-	Application	Lens	Color
3300	Indicator - General Purpose	Diffused Wide Angle	High Efficiency Red
3301	Indicator - High Ambient		
3315	Illuminator/Point Source	Non Diffused Narrow Angle	
3316	Illuminator/High Brightness		
3400	Indicator General Purpose	Diffused Wide Angle	Yellow
3401	Indicator - High Ambient		
3415	Illuminator/Point Source	Non Diffused Narrow Angle	
3416	Illuminator/High Brightness		
3502	Indicator - General Purpose	Diffused Wide Angle	Green
3507	Indicator - High Ambient		
3517	Illuminator/Point Source	Non Diffused Narrow Angle	
3519	Illuminator/High Brightness		

Electrical Characteristics at $T_A = 25°C$

Symbol	Description	Device HLMP-	Min.	Typ.	Max.	Units	Test Conditions
I_V	Luminous Intensity	3300 3301 3315 3316	2.0 4.0 12.0 20.0	3.5 7.0 18.0 30.0		mcd	I_F = 10 mA (Figure 3)
		3400 3401 3415 3416	2.0 4.0 10.0 20.0	4.0 8.0 18.0 30.0		mcd	I_F = 10 mA (Figure 8)
		3502 3507 3517 3519	1.6 4.2 6.7 10.6	2.4 5.2 10.0 25.0		mcd	F_F = 10 mA (Figure 3)
2Θ 1/2	Including Angle Between Half Luminous Intensity Points	3300 3301 3315 3316		65 65 35 35		Deg.	I_F = 10 mA See Note 1 (Figure 6)
		3400 3401 3415 3416		75 75 35 35		Deg.	I_F = 10 mA See Note 1 (Figure 11)
		3502 3507 3517 3519		75° 75° 24° 24°		Deg.	I_F = 10 mA See Note 1 (Figure 16)
λ_{PEAK}	Peak Wavelength	3300 3400 3500		635 583 565		nm	Measurement at Peak (Figure 1)
λ_d	Dominant Wavelength	3300 3400 3500		626 585 569		nm	See Note 2 (Figure 1)
τ_s	Speed of Response	3300 3400 3500		90 90 500		ns	
C	Capacitance	3300 3400 3500		16 18 18		pF	V_F = 0; f = 1 MHz
θ_{JC}	Thermal Resistance	3300 3400 3500		140		°C/W	Junction to Cathode Lead at Seating Plane
V_F	Forward Voltage	3300 3400 3500	1.5 1.5 1.6	2.2 2.2 2.3	3.0 3.0 3.0	V	I_F = 10 mA (Figure 2) I_F = 10 mA (Figure 7) I_F = 20 mA (Figure 12)
V_{BR}	Reverse Breakdown Volt.	All	5.0			V	I_R = 100 μA
ηV	Luminous Efficacy	3300 3400 3500		147 570 630		lumens Watt	See Note 3

NOTES:
1. $\Theta\frac{1}{2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

Absolute Maximum Ratings at $T_A = 25°C$

Parameter	3300 Series	3400 Series	3500 Series	Units
Peak Forward Current	90	60	90	mA
Average Forward Current[1]	25	20	25	mA
DC Current[2]	30	20	30	mA
Power Dissipation[3]	135	85	135	mW
Operating Temperature Range	−55 to +100	−55 to +100	−40 to +100	C°
Storage Temperature Range			−55 to +100	
Lead Soldering Temperature [1.6 mm (0.063 in.) from body]	260° C for 5 seconds			

NOTES:
1. See Figure 5 (Red), 10 (Yellow) or 15 (Green) to establish pulsed operating conditions.
2. For Red and Green series derate linearly from 50° C at 0.5 mA/° C. For Yellow series derate linearly from 50° C at 0.2 mA/° C.
3. For Red and Green series derate power linearly from 25° C at 1.8 mW/° C. For Yellow series derate power linearly from 50° C at 1.6 mW/° C.

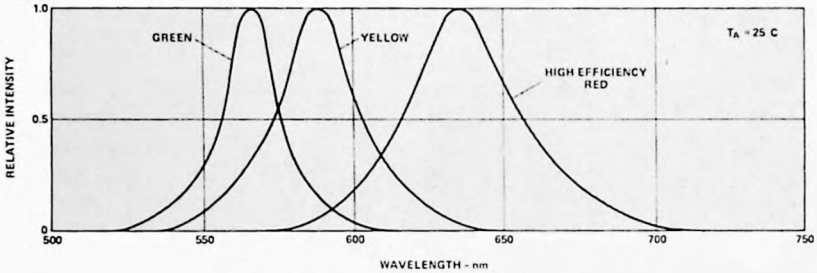


Figure 1. Relative Intensity vs. Wavelength

High Efficiency Red HLMP-3300 Series

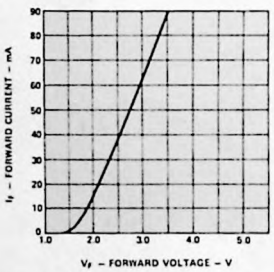


Figure 2. Forward Current vs. Forward Voltage Characteristics.

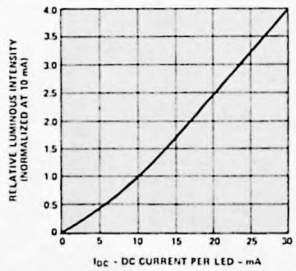


Figure 3. Relative Luminous Intensity vs. DC Forward Current.

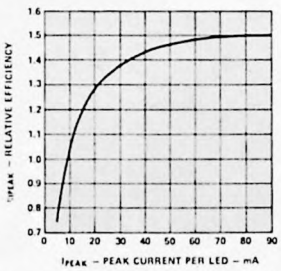


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. LED Peak Current.

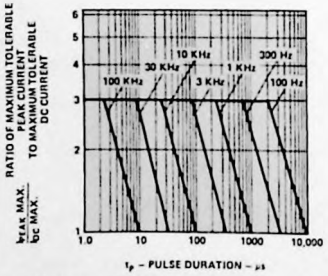


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings

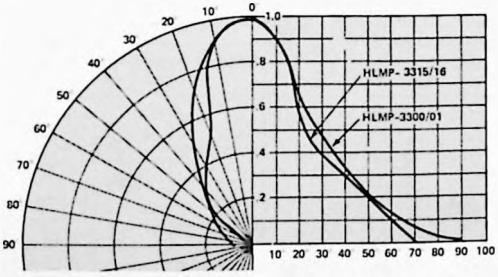


Figure 6. Relative Luminous Intensity vs. Angular Displacement.

Yellow HLMP-3400 Series

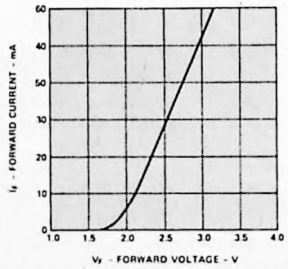


Figure 7. Forward Current vs. Forward Voltage Characteristics.

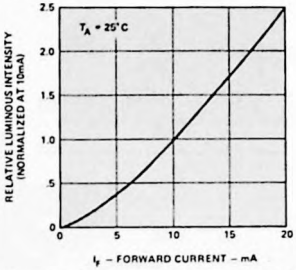


Figure 8. Relative Luminous Intensity vs. Forward Current.

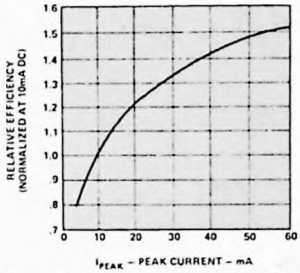


Figure 9. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

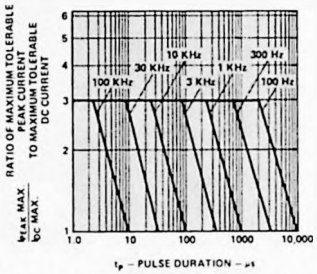


Figure 10. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

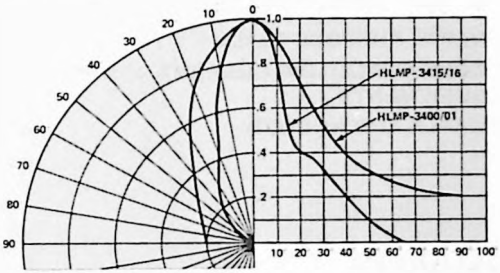


Figure 11. Relative Luminous Intensity vs. Angular Displacement.

Green HLMP-3500 Series

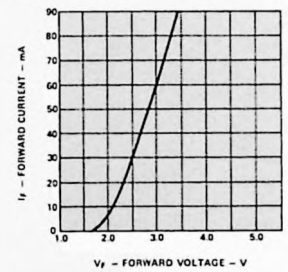


Figure 12. Forward Current vs. Forward Voltage Characteristics.

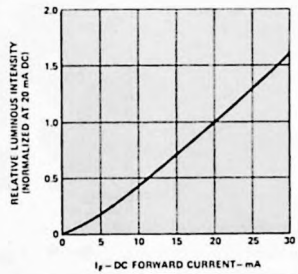


Figure 13. Relative Luminous Intensity vs. DC Forward Current.

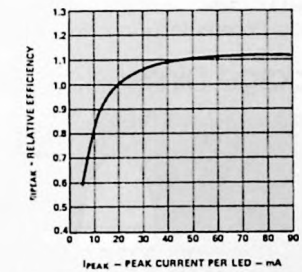


Figure 14. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak LED Current.

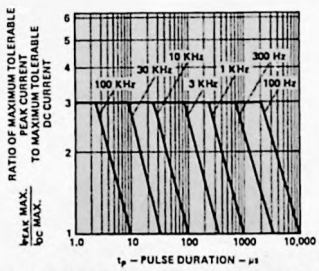


Figure 15. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

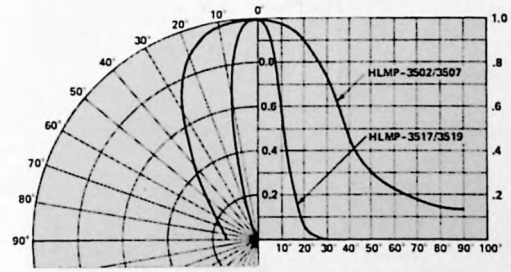


Figure 16. Relative Luminous Intensity vs. Angular Displacement. T-1 3/4 Lamp.

HEWLETT PACKARD

T-1 3/4 (5mm) LOW PROFILE SOLID STATE LAMPS

RED ● HLMP-3200 SERIES
HIGH EFFICIENCY RED ● HLMP-3350 SERIES
YELLOW ● HLMP-3450 SERIES
HIGH PERFORMANCE GREEN ● HLMP-3550 SERIES

TECHNICAL DATA JANUARY 1984

Features

- **HIGH INTENSITY**
- **LOW PROFILE: 5.8mm (0.23 in) NOMINAL**
- **T-1¾ DIAMETER PACKAGE**
- **LIGHT OUTPUT CATEGORIES**
- **DIFFUSED AND NON-DIFFUSED TYPES**
- **GENERAL PURPOSE LEADS**
- **IC COMPATIBLE/LOW CURRENT REQUIREMENTS**
- **RELIABLE AND RUGGED**

Description

The HLMP-3200 Series are Gallium Arsenide Phosphide Red Light Emitting Diodes with a red diffused lens.

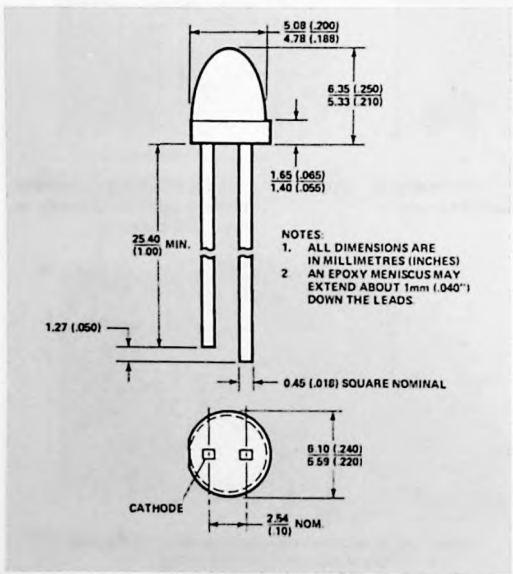
The HLMP-3350 Series are Gallium Arsenide Phosphide on Gallium Phosphide High Efficiency Red Light Emitting Diodes.

The HLMP-3450 Series are Gallium Arsenide Phosphide on Gallium Phosphide Yellow Light Emitting Diodes.

The HLMP-3550 Series are Gallium Phosphide Green Light Emitting Diodes.

The Low Profile T-1¾ package provides space savings and is excellent for backlighting applications.

Package Dimensions



Part Number HLMP-	Application	Lens	Color
3200	Indicator — General Purpose	Tinted Diffused Wide Angle	Red
3201	Indicator — High Brightness		
3350	Indicator — General Purpose	Tinted Diffused Wide Angle	High Efficiency Red
3351	Indicator — High Brightness		
3365	General Purpose Point Source	Tinted Non-diffused Narrow Angle	
3366	High Brightness Annunciator		
3450	Indicator — General Purpose	Tinted Diffused Wide Angle	Yellow
3451	Indicator — High Brightness		
3465	General Purpose Point Source	Tinted Non-diffused Narrow Angle	
3466	High Brightness Annunciator		
3553	Indicator — General Purpose	Tinted Diffused Wide Angle	Green
3554	Indicator — High Brightness		
3567	General Purpose Point Source	Tinted Non-diffused Narrow Angle	
3568	High Brightness Annunciator		

Absolute Maximum Ratings at $T_A = 25°C$

Parameter	3200 Series	3350 Series	3450 Series	3550 Series	Units
Peak Forward Current	1000	90	60	90	mA
Average Forward Current[1]	50	25	20	25	mA
DC Current[2]	50	30	20	30	mA
Power Dissipation[3]	100	135	85	135	mW
Operating Temperature Range	−55 to +100	−55 to +100	−55 to +100	−40 to +100	C°
Storage Temperature Range				−55 to +100	
Lead Soldering Temperature [1.6 mm (0.063 in.) from body]	260° C for 5 seconds				

NOTES:
1. See Figure 5 (Red), 10 (High Efficiency Red), 15 (Yellow) or 20 (Green) to establish pulsed operating conditions.
2. For High Efficiency Red and Green Series derate linearly from 50°C at 0.5 mA/°C. For Red and Yellow Series derate linearly from 50°C at 0.2 mA/°C.
3. For High Efficiency Red and Green Series derate power linearly from 25°C at 1.8 mW/°C. For Red and Yellow Series derate power linearly from 50°C at 1.6 mW/°C.

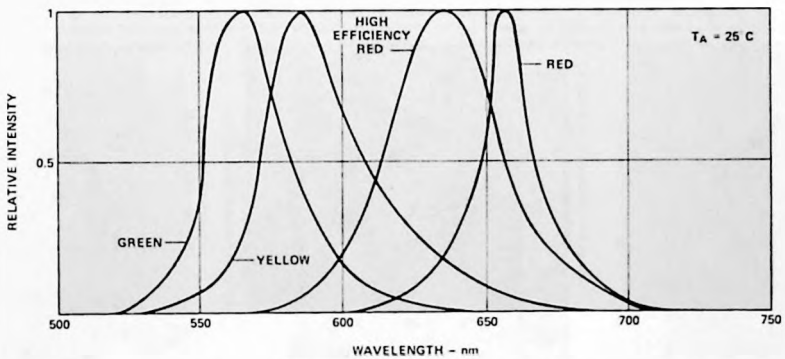


Figure 1. Relative Intensity versus Wavelength.

RED HLMP-3200 SERIES

Electrical Specifications at T_A=25°C

Symbol	Description	Device HLMP-	Min.	Typ.	Max.	Units	Test Conditions
I_V	Axial Luminous Intensity	3200	1.0	2.0		mcd	I_F = 20mA (Fig. 3)
		3201	2.0	4.0			
$2\theta_{1/2}$	Included Angle Between Half Luminous Intensity Points			60		deg.	Note 1 (Fig. 6)
λ_{PEAK}	Peak Wavelength			655		nm	Measurement @ Peak (Fig. 1)
λ_d	Dominant Wavelength			648		nm	Note 2
τ_s	Speed of Response			15		ns	
C	Capacitance			100		pF	V_F = 0; f = 1 MHz
θ_{JC}	Thermal Resistance			125		°C/W	Junction to Cathode Lead 1.6 mm (0.063 in.) from Body
V_F	Forward Voltage		1.4	1.6	2.0	V	I_F = 20mA (Fig. 2)
V_{BR}	Reverse Breakdown Voltage		3	10		V	I_R = 100μA
η_V	Luminous Efficacy			55		lm/W	Note 3

Notes: 1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity. 2. Dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device. 3. Radiant Intensity I_e, in watts/steradian may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

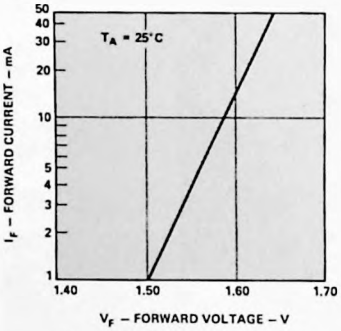


Figure 2. Forward Current versus Forward Voltage.

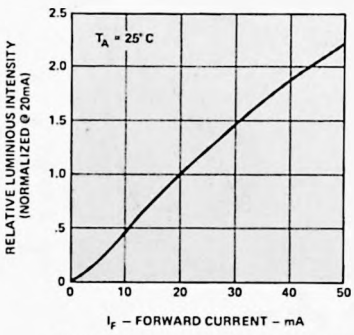


Figure 3. Relative Luminous Intensity versus Forward Current.

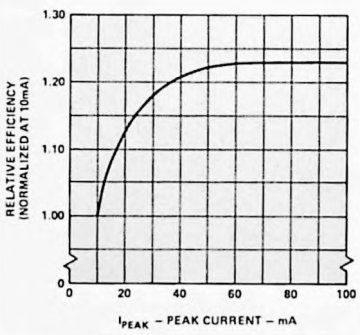


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) versus Peak Current.

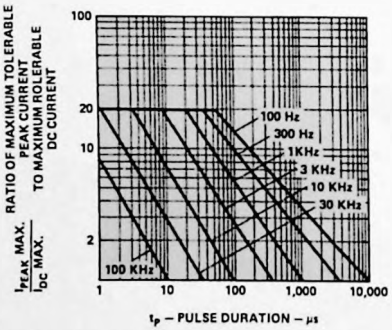


Figure 5. Maximum Tolerable Peak Current versus Pulse Duration. (I_{DC} MAX as per MAX Ratings)

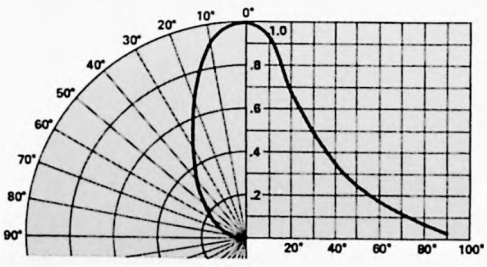


Figure 6. Relative Luminous Intensity versus Angular Displacement.

HIGH EFFICIENCY RED HLMP-3350 SERIES

Electrical Specifications at T_A=25°C

Symbol	Description	Device HLMP	Min.	Typ.	Max.	Units	Test Conditions
I_V	Axial Luminous Intensity	3350 3351 3365 3366	2.0 5.0 7.0 12.0	3.5 7.0 10.0 18.0		mcd	I_F = 10mA (Fig.8)
$2\theta_{1/2}$	Included Angle Between Half Luminous Intensity Points	3350 3351 3365 3366		50 50 45 45		deg.	Note 1 (Fig. 11)
λ_{PEAK}	Peak Wavelength			635		nm	Measurement @ Peak (Fig. 1)
λ_d	Dominant Wavelength			626		nm	Note 2
τ_s	Speed of Response			90		ns	
C	Capacitance			16		pF	V_F = 0; f = 1 MHz
θ_{JC}	Thermal Resistance			130		°C/W	Junction to Cathode Lead 1.6mm (0.063 in.) from Body
V_F	Forward Voltage		1.5	2.2	3.0	V	I_F = 10mA (Fig. 7)
V_{BR}	Reverse Breakdown Voltage		5.0			V	I_R = 100μA
η_V	Luminous Efficacy			147		lm/W	Note 3

Notes: 1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity. 2. Dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device. 3. Radiant Intensity I_e, in watts/steradian may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

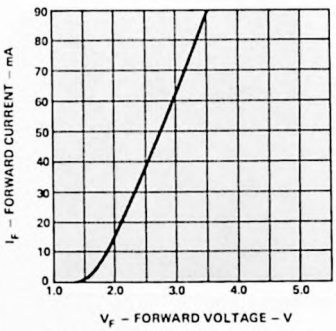


Figure 7. Forward Current versus Forward Voltage.

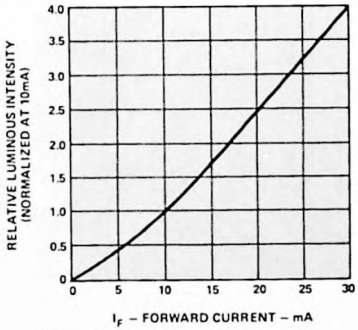


Figure 8. Relative Luminous Intensity versus Forward Current.

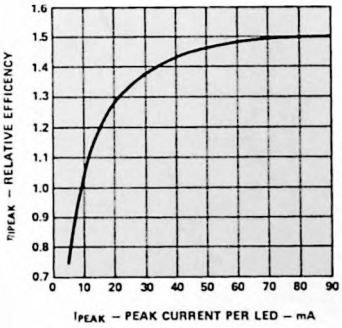


Figure 9. Relative Efficiency (Luminous Intensity per Unit Current) versus Peak Current.

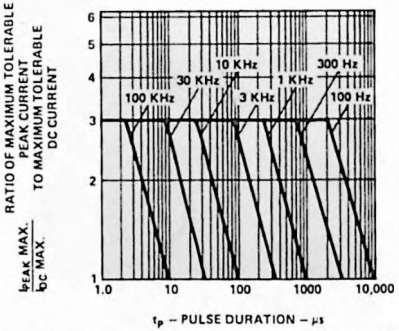


Figure 10. Maximum Tolerable Peak Current versus Pulse Duration. (I_{DC} MAX as per MAX Ratings)

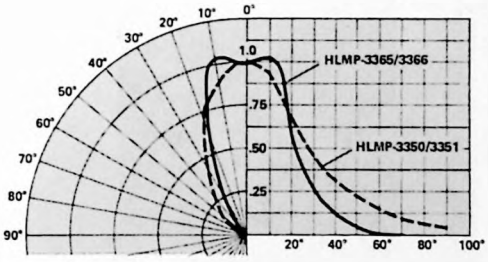


Figure 11. Relative Luminous Intensity versus Angular Displacement.

YELLOW HLMP-3450 SERIES

Electrical Specifications at T_A=25°C

Symbol	Description	Device HLMP	Min.	Typ.	Max.	Units	Test Conditions
I_V	Axial Luminous Intensity	3450 3451 3465 3466	2.5 6.0 6.0 12.0	4.0 10.0 12.0 18.0		mcd	I_F = 10mA (Fig. 13)
$2\theta_{1/2}$	Included Angle Between Half Luminous Intensity Points	3450 3451 3465 3466		50 50 45 45		deg.	Note 1 (Fig. 16)
λ_{PEAK}	Peak Wavelength			583		nm	Measurement @ Peak (Fig. 1)
λ_d	Dominant Wavelength			585		nm	Note 2
τ_s	Speed of Response			90		ns	
C	Capacitance			18		pF	V_F = 0; f = 1 MHz
θ_{JC}	Thermal Resistance			100		°C/W	Junction to Cathode Lead 1.6mm (0.063 in.) from Body
V_F	Forward Voltage		1.5	2.2	3.0	V	I_F = 10mA (Fig. 12)
V_{BR}	Reverse Breakdown Voltage		5.0			V	I_R = 100μA
η_v	Luminous Efficacy			570		lm/W	Note 3

Notes: 1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity. 2. Dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device. 3. Radiant Intensity I_e, in watts/steradian may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

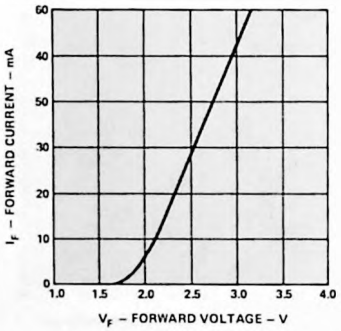


Figure 12. Forward Current versus Forward Voltage.

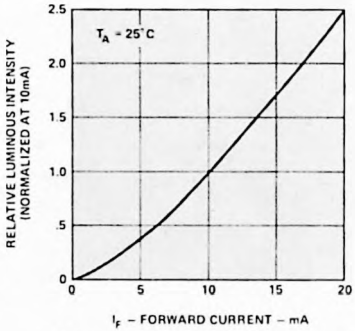


Figure 13. Relative Luminous Intensity versus Forward Current.

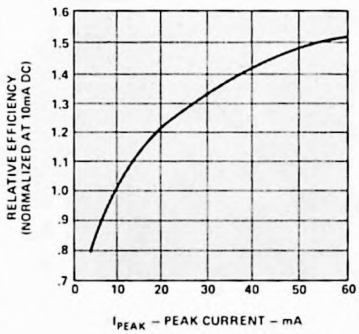


Figure 14. Relative Efficiency (Luminous Intensity per Unit Current) versus Peak Current.

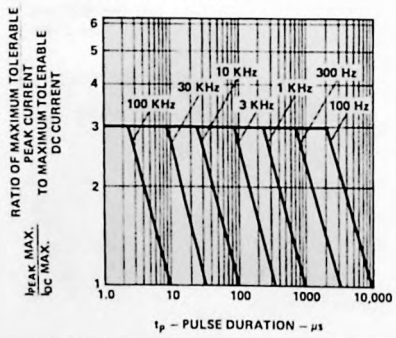


Figure 15. Maximum Tolerable Peak Current versus Pulse Duration. (I_{DC} MAX as per MAX Ratings).

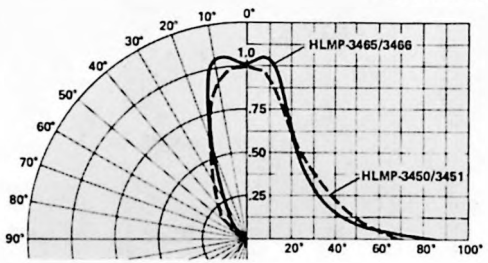


Figure 16. Relative Luminous Intensity versus Angular Displacement

GREEN HLMP-3550 SERIES
Electrical Specifications at T_A=25°C

Symbol	Description	Device HLMP-	Min.	Typ.	Max.	Units	Test Conditions
I_V	Axial Luminous Intensity	3553 3554 3567 3568	1.6 6.7 4.2 10.6	3.2 10.0 7.0 15.0		mcd	I_F = 10 mA (Figure 18)
2Θ 1/2	Included Angle Between Half Luminous Intensity Points	3553 3554 3567 3568		50 50 40 40		deg.	Note 1 (Figure 21)
λ_{PEAK}	Peak Wavelength			565		nm	Measurement @ Peak (Figure 1)
λ_d	Dominant Wavelength			569		nm	Note 2
τ_s	Speed of Response			500		ns	
C	Capacitance			18		pF	V_F = 0; f = 1 MHz
Θ_{JC}	Thermal Resistance			90		°C/W	Junction to Cathode Lead 1.6 mm (0.063 in.) from Body
V_F	Forward Voltage		1.6	2.3	3.0	V	I_F = 20 mA (Figure 17)
V_{BR}	Reverse Breakdown Voltage		5.0			V	I_R = 100 μA
η_V	Luminous Efficacy			630		lm/W	Note 3

Notes: 1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity. 2. Dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device. 3. Radiant Intensity I_e, in watts/steradian may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

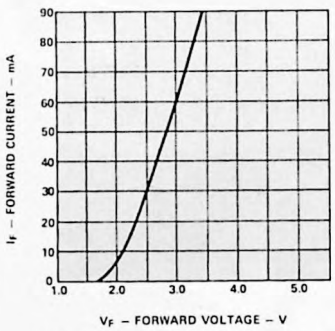


Figure 17. Forward Current versus Forward Voltage.

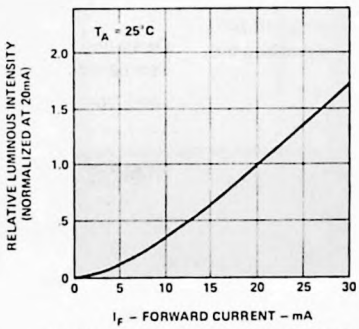


Figure 18. Relative Luminous Intensity versus Forward Current.

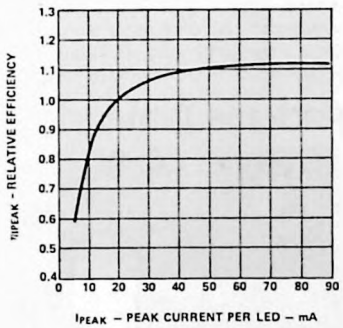


Figure 19. Relative Efficiency (Luminous Intensity per Unit Current) versus Peak Current.

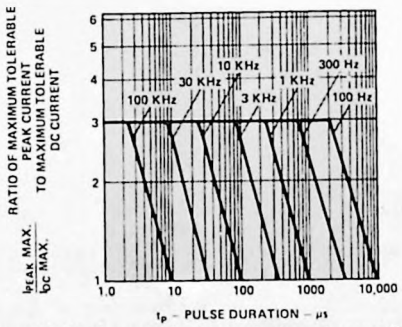


Figure 20. Maximum Tolerable Peak Current versus Pulse Duration. (I_{DC} MAX as per MAX ratings).

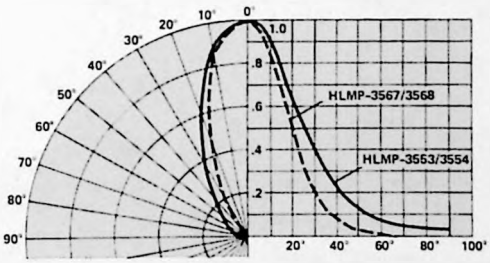


Figure 21. Relative Luminous Intensity versus Angular Displacement.

HEWLETT PACKARD

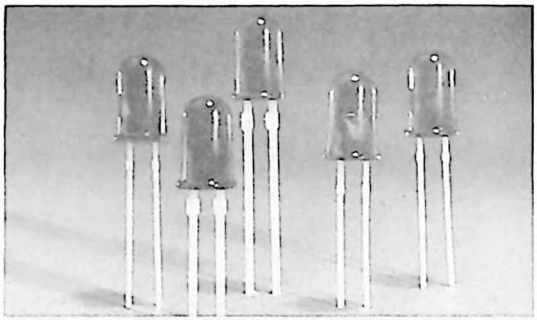
T-1 3/4 (5mm) RED SOLID STATE LAMPS

HLMP-3000
HLMP-3001
HLMP-3002
HLMP-3050

TECHNICAL DATA JANUARY 1984

Features

- LOW COST, BROAD APPLICATIONS
- LONG LIFE, SOLID STATE RELIABILITY
- LOW POWER REQUIREMENTS: 20 mA @ 1.6V
- HIGH LIGHT OUTPUT:
  2.0 mcd Typical for HLMP-3000
  4.0 mcd Typical for HLMP-3001
- WIDE AND NARROW VIEWING ANGLE TYPES
- RED DIFFUSED AND NON-DIFFUSED VERSIONS



Description

The HLMP-3000 series lamps are Gallium Arsenide Phosphide light emitting diodes intended for High Volume/ Low Cost applications such as indicators for appliances, smoke detectors, automobile instrument panels and many other commercial uses.

The HLMP-3000/-3001/-3002 have red diffused lenses where as the HLMP-3050 has a red non-diffused lens. These lamps can be panel mounted using mounting clip HLMP-0103. The HLMP-3000/-3001 lamps have .025" leads and the HLMP-3002/-3050 have .018" leads.

Absolute Maximum Ratings at T_A=25°C

Power Dissipation 100mW

DC Forward Current (Derate linearly from 50° C at 0.2 mA/° C) ..... 50 mA

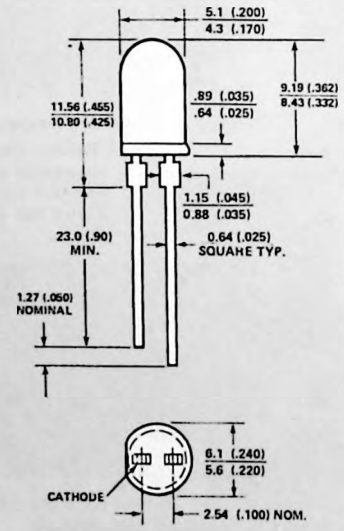
Peak Transient Forward Current ..... 1 Amp (1μsec pulse width, 300pps)

Operating and Storage Temperature Range ..... -55° C to +100° C

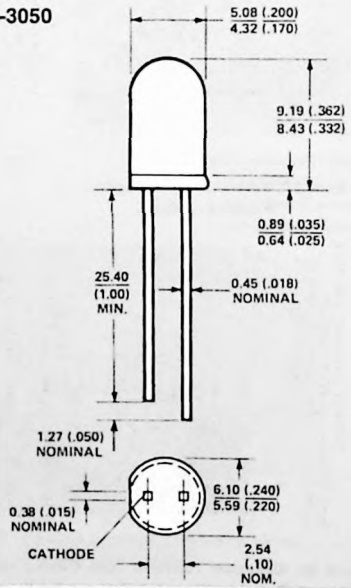
Lead Soldering Temperature ..... 260° C for 5 sec.

Package Dimensions

HLMP-3000/-3001



HLMP-3002/-3050



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MENISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

Electrical Characteristics at T_A=25°C

Symbol	Parameters	HLMP-3000			HLMP-3001			HLMP-3002			HLMP-3050			Units	Test Condtions
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_V	Luminous Intensity	1.0	2.0		2.0	4.0		1.0	2.0		1.0	2.5		mcd	I_F = 20 mA
λ_{PEAK}	Peak Wavelength		655			655			655			655		nm	Measurement at Peak
λ_O	Dominant Wavelength		648			648			648			648			
τ_S	Speed of Response		10			10			10			10		ns	
C	Capacitance		100			100			100			100		pF	V_F = 0, f = 1 MHz
V_F	Forward Voltage	1.4	1.6	2.0	1.4	1.6	2.0	1.4	1.6	2.0	1.4	1.6	2.0	V	I_F = 20 mA
V_{BR}	Reverse Breakdown Voltage	3	10		3	10		3	10		3	10		V	I_R = 100 μA
θ_{JC}	Thermal Resistance		100			100			100			100		°C/W	Junction to Cathode Lead
$2\theta 1/2$	Included Angle Between Half Luminous Intensity Points, Both Axes		75			75			75			24		Deg.	I_F = 20 mA

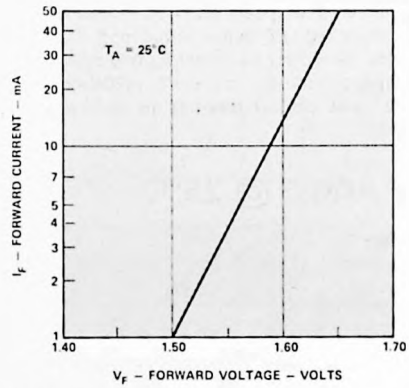


Figure 1. Forward Current Versus Forward Voltage Characteristic For HLMP-3000/-3001/-3050/-3002.

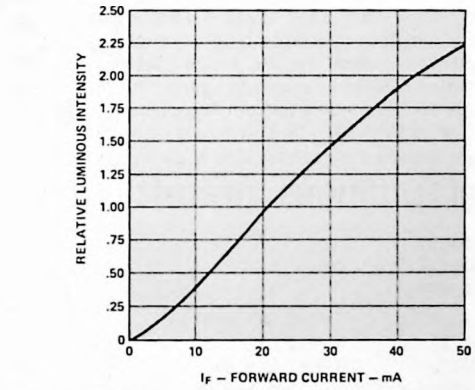


Figure 2. Relative Luminous Intensity Versus Forward Current For HLMP-3000/-3001/-3050/-3002.

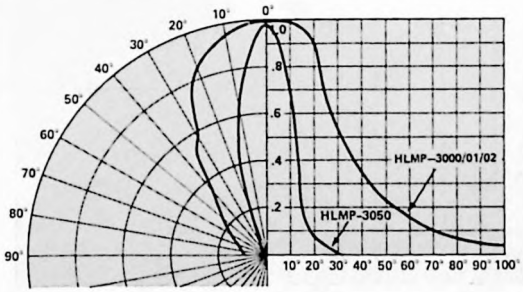


Figure 3. Relative Luminous Intensity Versus Angular Displacement. T-1 3/4 Lamp. HLMP-3050 and HLMP-3000/-3001/-3002.

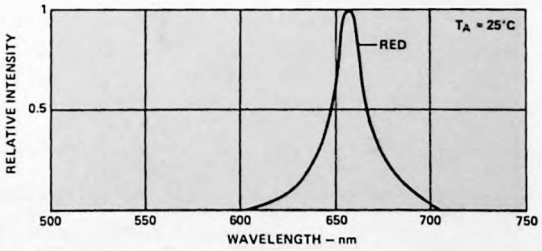


Figure 4. Relative Luminous Intensity Versus Wavelength.

HEWLETT PACKARD

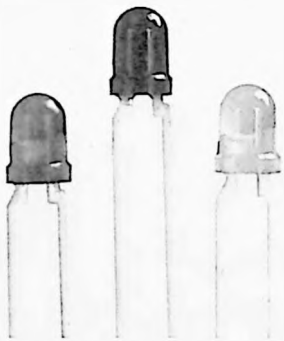
T-1 (3mm) LED LAMPS

High Efficiency Red HLMP-1300 Series
Yellow HLMP-1400 Series
High Performance Green HLMP-1500 Series

TECHNICAL DATA JANUARY 1984

Features

- IMPROVED INTENSITY
- CHOICE OF VIEWING ANGLE
- SMALL SIZE T-1 DIAMETER
  3.18 mm (0.125 inch)
- IC COMPATIBLE
- RELIABLE AND RUGGED
- CHOICE OF 3 BRIGHT COLORS
  High Efficiency Red
  Yellow
  High Performance Green



Description

These solid state lamps are available in a broad matrix of colors and finished package appearance to suit your particular application. Each device is designed to generate high axial luminous intensity and good on-off contrast.

The red and yellow devices utilize Gallium Arsenide Phosphide on Gallium Phosphide light emitting diode and the green devices utilize a Gallium Phosphide light emitting diode. The HLMP-1300, -1301, -1302 are high efficiency red lamps particularly designed for wide angle viewabilty under a variety of ambient conditions. The HLMP-1400, -1401, -1402 serve a similar function in yellow, The HLMP-1503 and -1523 do likewise for green. The HLMP-1320 and -1321 are high efficiency red LED lamps with a more narrow viewing angle better suited for backlighting or particularly severe high ambient conditions. The HLMP-1420/1421 and HLMP-1520/1521 are similar devices in yellow and green respectively.

Axial Luminous Intensity and Viewing Angle @ 25°C

Part Number HLMP-	Description	I_V (mcd) Min.	I_V (mcd) Typ.	Test Condition (mA)	2θ1/2 (Typ.) [1]	λD (nm-Typ.) [2]	Color
1300	Tinted, Diffused	1.0	2.0	10	60°	626	High Efficiency Red
1301	Tinted, Diffused	2.0	2.5		60°		
1302	Tinted, Diffused	3.0	4.0		60°		
1320	Untinted, Non-Diffused	6.0	12.0		45°		
1321	Tinted, Non-Diffused	6.0	12.0		45°		
1400	Tinted, Diffused	1.0	2.0	10	60°	585	Yellow
1401	Tinted, Diffused	2.0	3.0		60°		
1402	Tinted, Diffused	3.0	4.0		60°		
1420	Untinted, Non-Diffused	6.0	12.0		45°		
1421	Tinted, Non-Diffused	6.0	12.0		45°		
1503	Tinted, Diffused	1.0	2.0	10	60°	569	Green
			5.0	20			
1523	Tinted, Diffused	2.6	4.0	10	60°		
			10.0	20			
1520	Untinted, Non-Diffused	4.2	5.0	10	45°	571	
			12.0	20			
1521	Tinted, Non-Diffused	4.2	5.0	10	45°	569	
			12.0	20			

NOTES:
1. θ1/2 is the off-axis angle at which the luminous intensity is half the axial intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.

Absolute Maximum Ratings at T_A = 25°C

Parameter	Red	Yellow	Green	Units
Peak Forward Current	90	60	90	mA
Average Forward Current[1]	25	20	25	mA
DC Current[2]	30	20	30	mA
Power Dissipation[3]	135	85	135	mW
Operating Temperature Range	−55 to +100	−55 to +100	−40 to +100	C°
Storage Temperature Range			−55 to +100	
Lead Soldering Temperature [1.6 mm (0.063 in.) from body]	260° C for 5 seconds			

NOTES:
1. See Figure 5 to establish pulsed operating conditions.
2. For Red and Green Series derate linearly from 50° C at 0.5 mA/° C. For Yellow Series derate linearly from 50° C at 0.2 mA/° C.
3. For Red and Green series derate power linearly from 25° C at 1.8 mW/° C. For Yellow series derate power linearly from 50° C at 1.6 mW/° C.

Electrical/Optical Characteristics at T_A = 25°C

Symbol	Description	HLMP-1300, -1301 -1302, -1320, -1321			HLMP-1400, -1401 -1402, -1420, -1421			HLMP-1503, -1523 -1520, -1521			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
λ_{peak}	Peak Wavelength		635			583			565		nm	Measurement at Peak, Fig. 1
τ_s	Speed of Response		90			90			500		ns	
C	Capacitance		20			15			18		pF	V_F=0; f=1 MHz
θ_{JC}	Thermal Resistance		95			95			95		°C/W	Junction to Cathode Lead at 0.79mm (0.031 in.) From Body
V_F	Forward Voltage	1.5	2.2	3.0	1.5	2.2	3.0	1.6 at I_F = 20mA	2.3	3.0	V	I_F=10mA (Figs. 2,7,12)
BV_R	Reverse Breakdown Voltage	5.0			5.0			5.0			V	I_R=100μA
η_v	Luminous Efficacy		147			570			630		1m/W	Note 1

NOTES:
1. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is the luminous efficacy in lumens/watt.

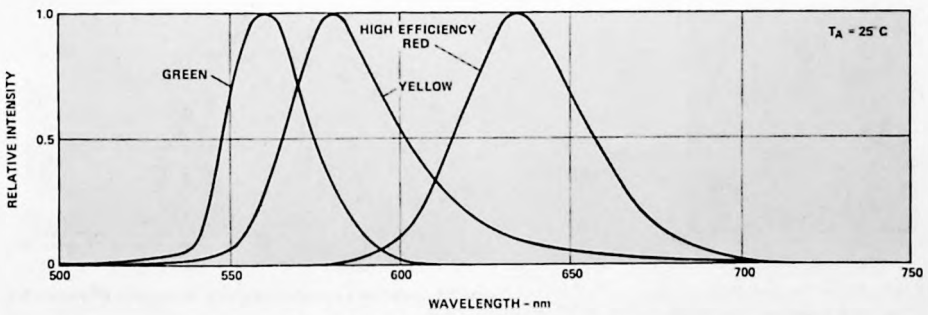


Figure 1. Relative Intensity vs. Wavelength.

High Efficiency Red HLMP-1300, -1301, -1302, -1320, -1321

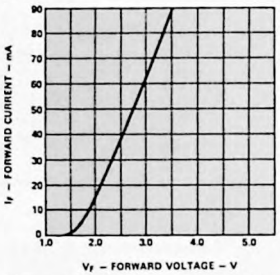


Figure 2. Forward Current vs. Forward Voltage Characteristics.

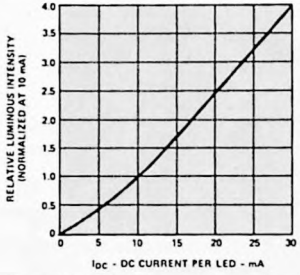


Figure 3. Relative Luminous Intensity vs. DC Forward Current.

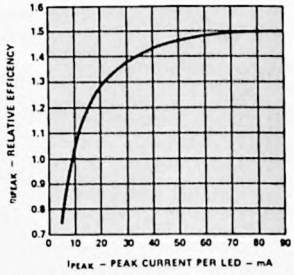


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak LED Current.

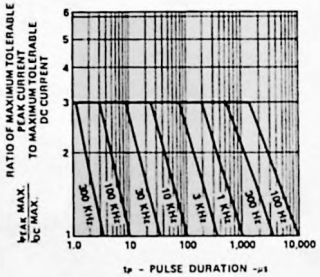


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC}MAX as per MAX Ratings).

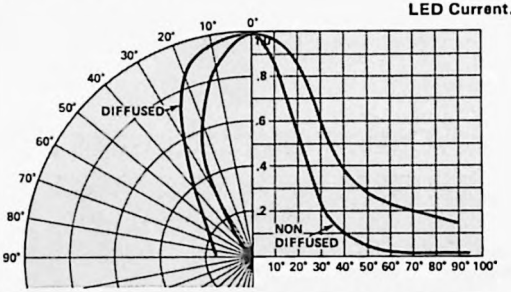


Figure 6. Relative Luminous Intensity vs. Angular Displacement.

Yellow HLMP-1400, -1401, -1402, -1420, -1421

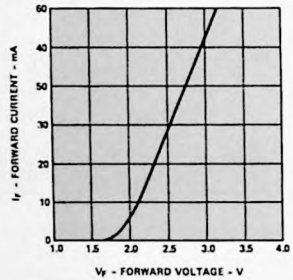


Figure 7. Forward Current vs. Forward Voltage Characteristics.

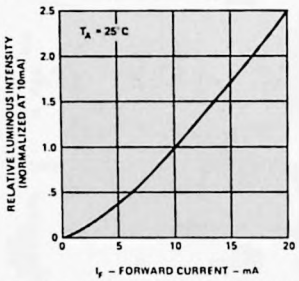


Figure 8. Relative Luminous Intensity vs. Forward Current.

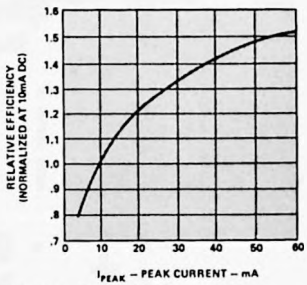


Figure 9. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

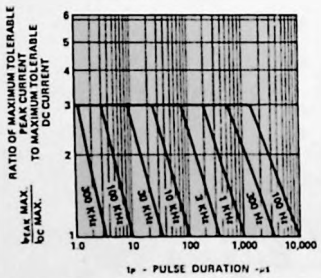


Figure 10. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings.)

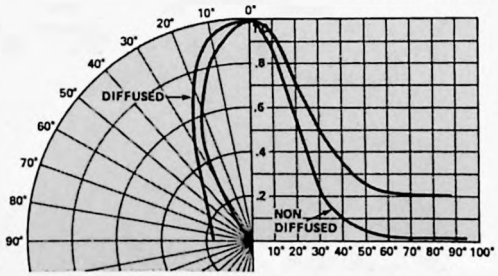


Figure 11. Relative Luminous Intensity vs. Angular Displacement.

Green HLMP-1503, -1523, -1520, -1521

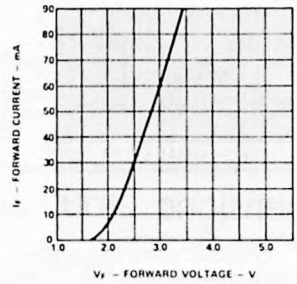


Figure 12. Forward Current vs. Forward Voltage Characteristics.

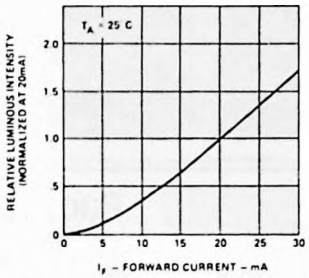


Figure 13. Relative Luminous Intensity vs. Forward Current.

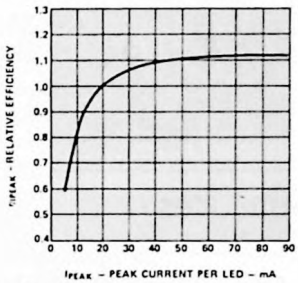


Figure 14. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak LED Current.

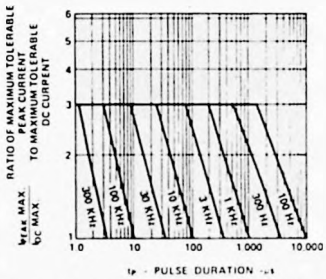


Figure 15. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings.)

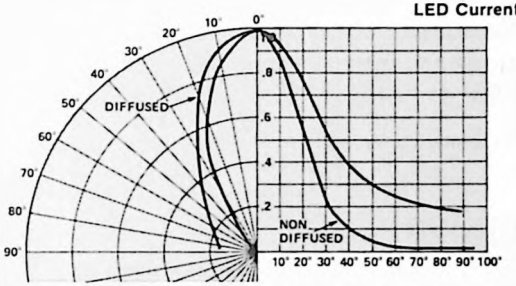
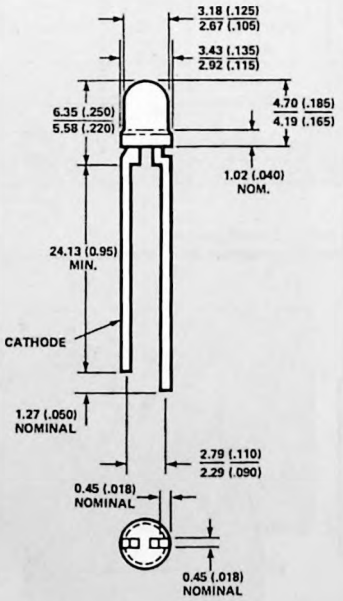


Figure 16. Relative Luminous Intensity vs. Angular Displacement.

Package Dimensions



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MENISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

HEWLETT PACKARD

LOW PROFILE T-1 (3mm) LED LAMPS

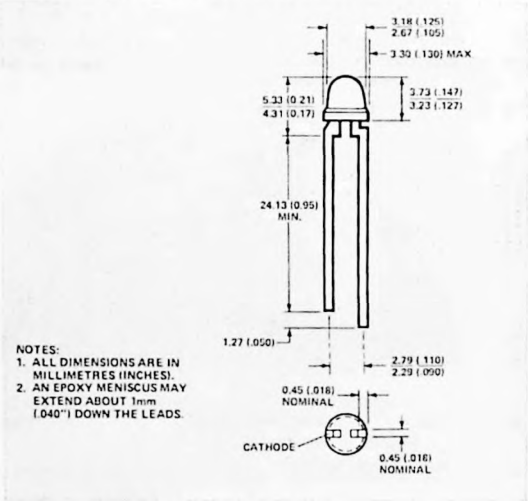
High Efficiency Red HLMP-1350
Yellow HLMP-1450
High Performance Green HLMP-1550

TECHNICAL DATA JANUARY 1984

Features

- LOW PROFILE HEIGHT
- SMALL T-1 SIZE DIAMETER 3.18 mm (.125 inch)
- HIGH INTENSITY
- IC COMPATIBLE
- CHOICE OF 3 BRIGHT COLORS
  High Efficiency Red
  Yellow
  High Performance Green

Package Dimensions



Description

This family of solid state lamps is especially suited for applications where small package size is required without sacrificing luminous intensity. The HLMP-1350 is a red tinted, diffused lamp providing a wide viewing angle. The HLMP-1450 and HLMP-1550 are similar products in yellow and green respectively.

Axial Luminous Intensity and Viewing Angle @ 25°C

Part Number HLMP-	Description	I_V (mcd)		Test Condition mA	$2\Theta 1/2$ (Typ.) [1]	λd (nm-Typ.) [2]	Color
		Min.	Typ.				
1350	Tinted, Wide Angle	1.0	2.0	10	55°	626	High Efficiency Red
1450	Tinted, Wide Angle	1.0	2.0	10	55°	585	Yellow
1550	Tinted, Wide Angle	1.0	2.0	10	55°	569	Green
			5.0	20			

NOTES:
1. $\Theta 1/2$ is the off-axis angle at which the luminous intensity is half the axial intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.

For Maximum Ratings and Electrical/Optical Characteristics (including figures) see HLMP-1300/-1400/-1500 data sheet, publication number 5953-7735, except for Figure A shown here.

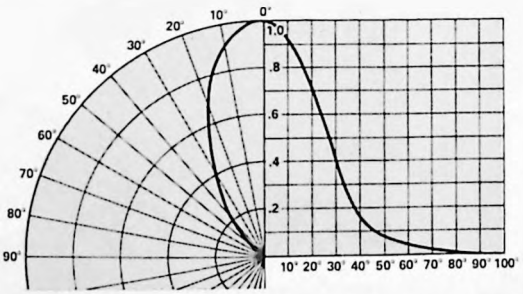


Figure A. Relative Luminous Intensity vs. Angular Displacement.

HEWLETT PACKARD

T-1 (3mm) RED SOLID STATE LAMPS

HLMP-1000 Series
HLMP-1200 Series

TECHNICAL DATA JANUARY 1984

Features

- **WIDE VIEWING ANGLE**
- **SMALL SIZE T-1 DIAMETER 3.18mm (0.125")**
- **IC COMPATIBLE**
- **RELIABLE AND RUGGED**

Description

The HLMP-1000 is a series of Gallium Arsenide Phosphide Light Emitting Diodes designed for applications where space is at a premium, such as in high density arrays.

The HLMP-1000 series is available in three lens configurations.

HLMP-1000 — Red Diffused lens provides excellent on-off contrast ratio, high axial luminous intensity, and wide viewing angle.

HLMP-1080 — Same as HLMP-1000, but untinted diffused to mask red color in the "off" condition.

HLMP-1071/-1201 — Untinted non-diffused plastic lens provides a point source. Useful when illuminating external lens, annunciators, or photo-detectors.

Part Number HLMP-	Package & Lens Type	Iv (mcd) @ 20 mA		Viewing Angle 2Θ 1/2
		Min.	Typ.	
-1000	A-Tinted Diffused	.5	1.0	125°
-1002	A-Tinted Diffused	1.5	2.5	125°
-1080	A-Untinted Diffused	.5	1.5	125°
-1071	A-Untinted Non-Diffused	1.0	2.0	80°
-1200	B-Untinted Non-Diffused	.5	1.0	120°
-1201	B-Untinted Non-Diffused	1.5	2.5	120°

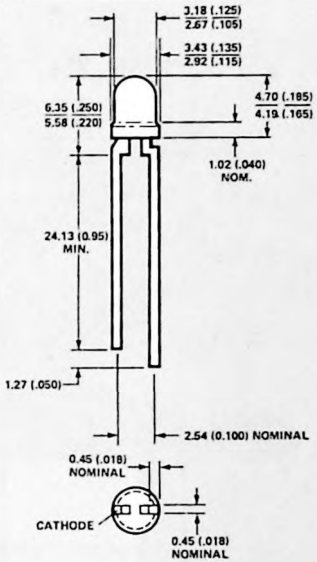


Figure A.

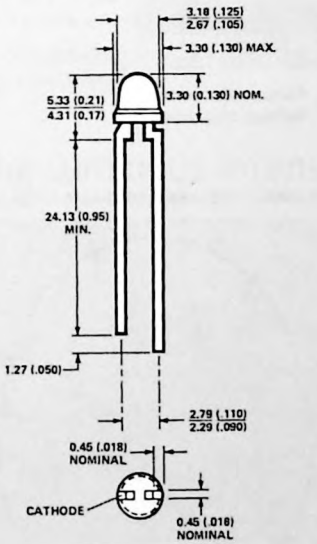


Figure B.

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MENISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

Maximum Ratings at T_A=25°C

DC Power Dissipation 100mW

DC Forward Current 50mA
(Derate linearly from 50°C at 0.2mA/°C)

Peak Forward Current . . . . . 1 Amp
(1 μsec pulse width, 300 pps)

Operating and Storage
Temperature Range . . . . . −55°C to +100°C

Lead Soldering Temperature . . . . . 260°C for 5 sec.

Electrical Characteristics at T_A=25°C

Symbol	Parameters	Min.	Typ.	Max.	Units	Test Conditions
λ_{PEAK}	Wavelength		655		nm	
τ_s	Speed of Response		15		ns	
C	Capacitance		100		pF	V_F = 0, f = 1MHz
θ_{JC}	Thermal Resistance		270		°C/W	Junction to Cathode Lead
V_F	Forward Voltage	1.4	1.6	2.0	V	I_F = 20mA
V_{BR}	Reverse Breakdown Voltage	3	10		V	I_R = 100 μA

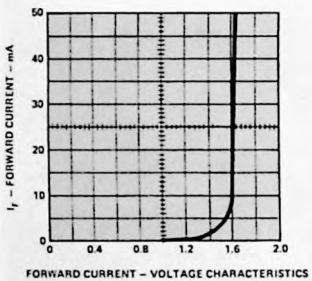


Figure 1. Forward Current vs. Voltage Characteristic.

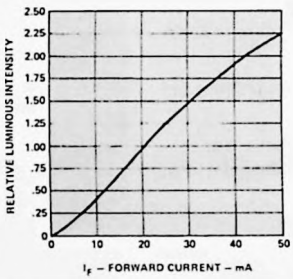


Figure 2. Luminous Intensity vs. Forward Current (IF).

HLMP-1200/-1201 (5082-4487/-4488)

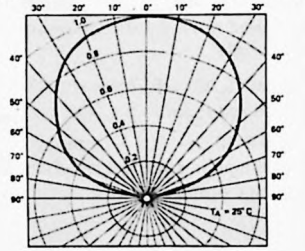


Figure 3. Typical Relative Luminous Intensity vs. Angular Displacement.

HLMP-1000/-1002/-1080 (5082-4480/-4494/-4483)

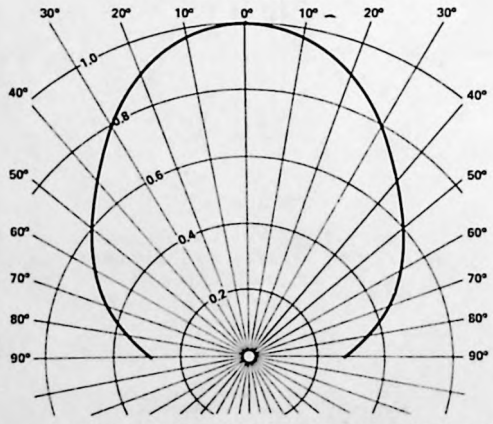


Figure 4. Relative Luminous Intensity vs. Angular Displacement.

HLMP-1071 (5082-4486)

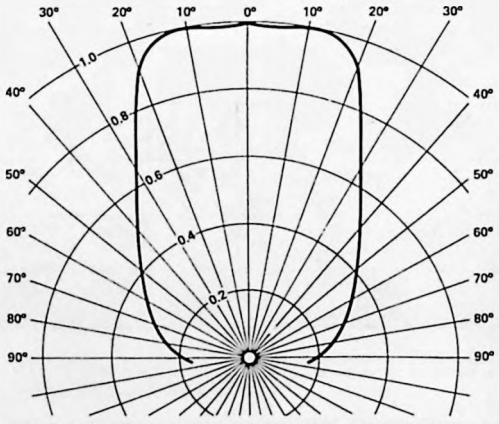


Figure 5. Relative Luminous Intensity vs. Angular Displacement.

HEWLETT PACKARD

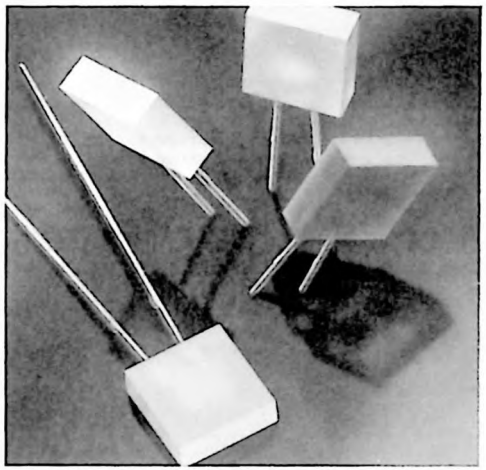
RECTANGULAR SOLID STATE LAMPS

HIGH EFFICIENCY RED	HLMP-0300/0301
YELLOW	HLMP-0400/0401
HIGH PERFORMANCE GREEN	HLMP-0503/0504

TECHNICAL DATA JANUARY 1984

Features

- RECTANGULAR LIGHT EMITTING SURFACE
- FLAT HIGH STERANCE EMITTING SURFACE
- STACKABLE ON 2.54 MM (0.100 INCH) CENTERS
- IDEAL AS FLUSH MOUNTED PANEL INDICATORS
- IDEAL FOR BACKLIGHTING LEGENDS
- LONG LIFE: SOLID STATE RELIABILITY
- CHOICE OF 3 BRIGHT COLORS
  - HIGH EFFICIENCY RED
  - YELLOW
  - HIGH PERFORMANCE GREEN
- IC COMPATIBLE/LOW CURRENT REQUIREMENTS



Description

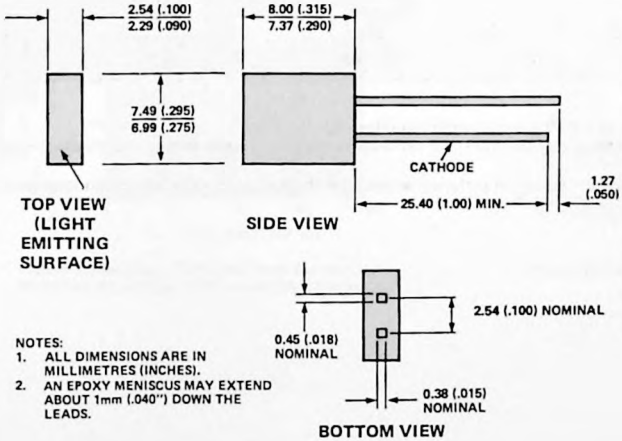
The HLMP-030X, -040X, -050X are solid state lamps encapsulated in an axial lead rectangular epoxy package. They utilize a tinted, diffused epoxy to provide high on-off contrast and a flat high intensity emitting surface. Borderless package design allows creation of uninterrupted light emitting areas.

The HLMP-0300 and -0301 have a high efficiency red GaAsP on GaP LED chip in a light red epoxy package. This lamp's efficiency is comparable to that of the GaP red, but extends to higher current levels.

The HLMP-0400 and -0401 provide a yellow GaAsP on GaP LED chip in a yellow epoxy package.

The HLMP-0503 and -0504 provide a green GaP LED chip in a green epoxy package.

Package Dimensions



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. AN EPOXY MENISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

Axial Luminous Intensity

Color	Part Number	I_V (mcd) @ 20 mA DC	
		Min.	Typ.
High Efficiency Red	HLMP-0300	1.0	2.5
	HLMP-0301	2.5	5.0
Yellow	HLMP-0400	1.5	2.5
	HLMP-0401	3.0	5.0
High Performance Green	HLMP-0503	1.5	2.5
	HLMP-0504	3.0	5.0

Absolute Maximum Ratings at $T_A = 25°C$

Parameter	HLMP-0300/-0301	HLMP-0400/-0401	HLMP-0503/-0504	Units
Peak Forward Current	90	60	90	mA
Average Forward Current[1]	25	20	25	mA
DC Current[2]	30	20	30	mA
Power Dissipation[3]	135	85	135	mW
Operating Temperature Range	−55 to +100	−55 to +100	−40 to +100	C°
Storage Temperature Range			−55 to +100	
Lead Soldering Temperature [1.6 mm (0.063 in.) from body]	260° C for 5 seconds			

NOTES:
1. See Figure 5 to establish pulsed operating conditions.
2. For Red and Green Series derate linearly from 50° C at 0.5 mA/° C. For Yellow Series derate linearly from 50° C at 0.2 mA/° C.
3. For Red and Green series derate power linearly from 25° C at 1.8 mW/° C. For Yellow series derate power linearly from 50° C at 1.6 mW/° C.

Electrical/Optical Characteristics at $T_A = 25°C$

Symbol	Description	HLMP-0300/0301			HLMP-0400/0401			HLMP-0503/0504			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
$2\theta_{1/2}$	Included Angle Between Half Luminous Intensity Points, Both Axes		100			100			100		deg.	Note 1. Figure 6.
λ_{PEAK}	Peak Wavelength		635			583			565		nm	Measurement at Peak
λ_d	Dominant Wavelength		626			585			569		nm	Note 2
τ_S	Speed of Response		90			90			500		ns	
C	Capacitance		17			17			18		pF	V_F=0; f=1 MHz
θ_{JC}	Thermal Resistance		140			140			140		°C/W	Junction to Cathode Lead at 1.6 mm (0.063 in.) from Body
V_F	Forward Voltage	1.6	2.1	3.0	1.6	2.2	3.0	1.6	2.3	3.0	V	I_F= 20mA Figure 2.
V_{BR}	Reverse Breakdown Voltage	5.0			5.0			5.0			V	I_R = 100 μA
η_V	Luminous Efficacy		147			570			630		lm/W	Note 3

NOTES:
1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

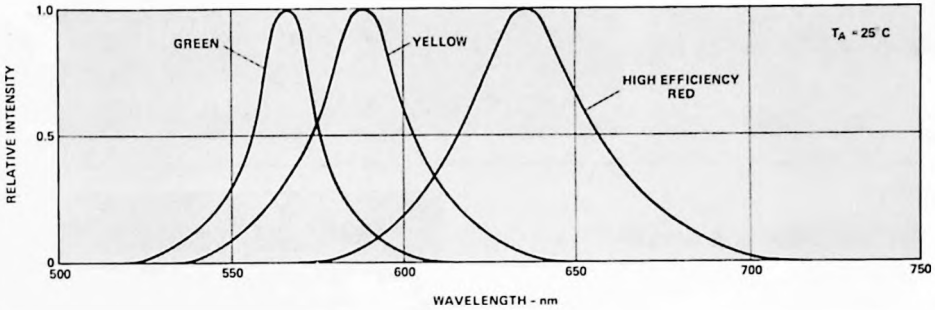


Figure 1. Relative Intensity vs. Wavelength.

High Efficiency Red, Yellow and Green Rectangular Lamps

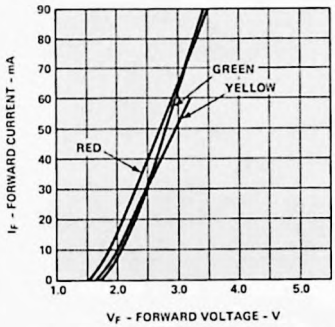


Figure 2. Forward Current vs. Forward Voltage.

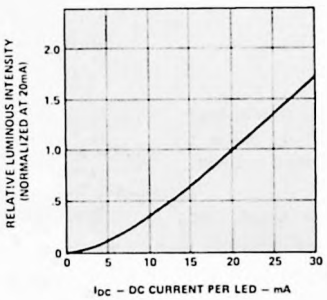


Figure 3. Relative Luminous Intensity vs. Forward Current.

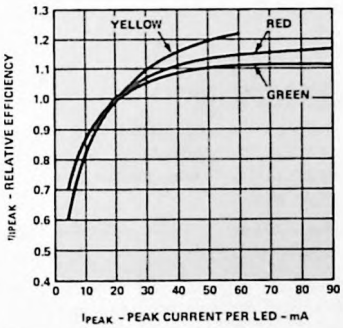


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

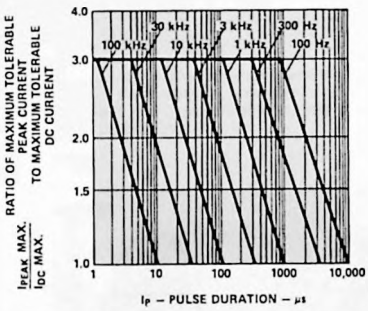


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings.)

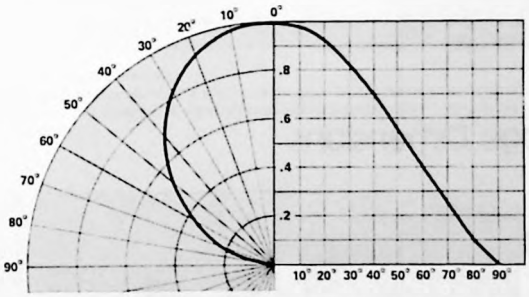


Figure 6. Relative Luminous Intensity vs. Angular Displacement.

HEWLETT PACKARD

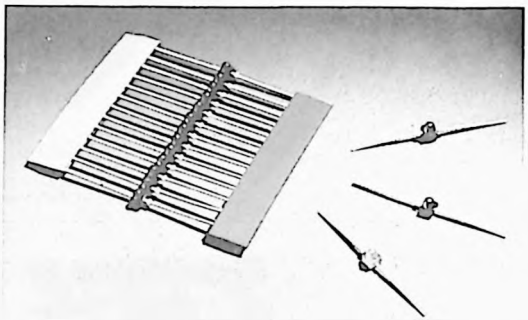
SUBMINIATURE SOLID STATE LAMPS

RED • HLMP-6000/6001
HIGH EFFICIENCY RED • HLMP-6300
YELLOW • HLMP-6400
HIGH PERFORMANCE GREEN • HLMP-6500

TECHNICAL DATA JANUARY 1984

Features

- **SUBMINIATURE PACKAGE STYLE**
- **END STACKABLE**
- **LOW PACKAGE PROFILE**
- **RADIAL LEADS**
- **WIDE VIEWING ANGLE**
- **LONG LIFE — SOLID STATE RELIABILITY**



Description

The 6xxx are solid state lamps encapsulated in a radial lead subminiature package of molded epoxy. They utilize a tinted, diffused lens providing high on-off contrast and wide angle viewing.

The 6000/6001 utilizes a GaAsP LED chip in a deep red molded package.

The 6300 has a high-efficiency red GaAsP on GaP LED chip in a light red molded package.

The 6400 provides a yellow GaAsP on GaP LED chip in a yellow molded package.

The 6500 provides a green GaP LED chip in a green molded package.

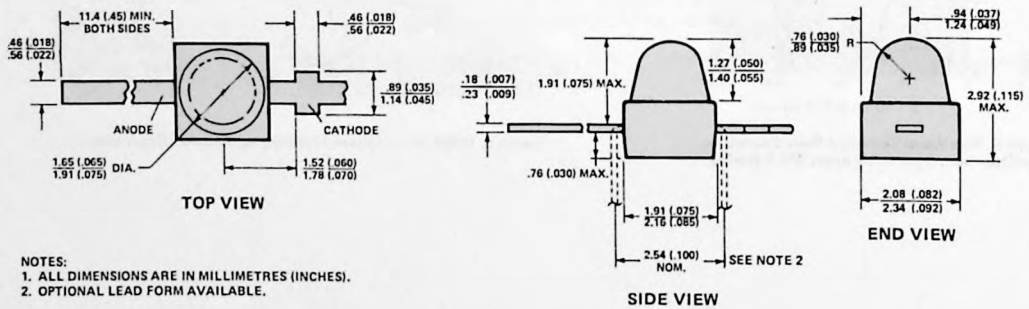
Special lead bending is available on 2.54mm (.100 in) and 5.08mm (.200 in) centers.

Tape-and-reel mounting is available on request.

Tape and Reel Order Chart

Std. Product HLMP-	6000	6001	6300	6400	6500
Tape & Reel P/N	HLMP-6020	HLMP-6021	HLMP-6320	HLMP-6420	HLMP-6520

Package Dimensions



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. OPTIONAL LEAD FORM AVAILABLE.

Absolute Maximum Ratings at T_A=25°C

Parameter	Red HLMP-6000/1	High Eff. Red HLMP-6300	Yellow HLMP-6400	Green HLMP-6500	Units
Power Dissipation	100	120	120	120	mW
DC Forward Current	50[1]	30[2]	20[1]	30[2]	mA
Peak Forward Current	1000 See Fig. 5	60 See Fig. 10	60 See Fig. 15	60 See Fig. 20	mA
Operating Temperature Range	−55 to +100	−55 to +100	−55 to +100	−40 to +100	C°
Storage Temperature Range				−55 to +100	
Lead Soldering Temperature [1.6 mm (0.063 in.) from body]	260° C for 3 seconds				

NOTES: 1. Derate from 50° C at 0.2mA/° C
2. Derate from 50° C at 0.5 mA/° C

Electrical/Optical Characteristics at T_A=25°C

Symbol	Description	HLMP-6000/1			HLMP-6300			HLMP-6400			HLMP-6500			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_V	Axial Luminous Intensity	−/0.5	1.2		1.0	3.0		1.0	3.0		1.0	3.0		mcd	I_F=10mA, Figs. 3,8,13,18
$2\theta_{1/2}$	Included Angle Between Half Luminous Intensity Points		45			80			90			70		deg.	Note 1. Figures 6, 11, 16, 21
λ_{PEAK}	Peak Wavelength		655			635			583			565		nm	Measurement at Peak
λ_d	Dominant Wavelength		640			629			585			569		nm	Note 2
τ_S	Speed of Response		15			90			90			500		ns	
C	Capacitance		100			11			15			18		pF	V_f=0; f=1 MHz
θ_{JC}	Thermal Resistance		125			120			100			100		°C/W	Junction to Cathode Lead at 0.79mm (.031 in) from Body
V_F	Forward Voltage	1.4	1.6	2.0	1.5	2.2	3.0	1.5	2.2	3.0	1.5	2.3	3.0	V	I_F=10mA, Figures 2, 7, 12, 17
V_{BR}	Reverse Breakdown Voltage	3.0	10		5.0	15		5.0	15		5.0	20		V	I_R = 100μA
η_v	Luminous Efficacy		55			147			570			630		lm/W	Note 3

NOTES:
1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is the luminous efficacy in lumens/watt.

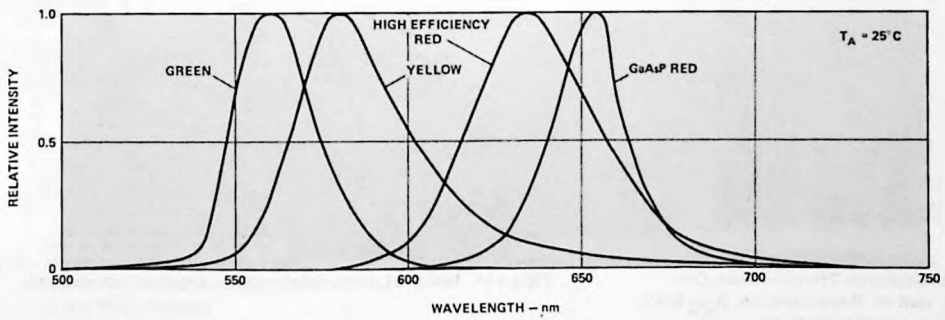


Figure 1. Relative Intensity vs. Wavelength.

HLMP-6000/6001

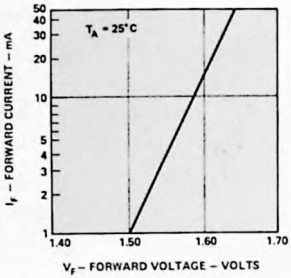


Figure 2. Forward Current vs. Forward Voltage.

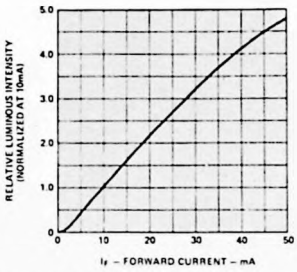


Figure 3. Relative Luminous Intensity vs. Forward Current.

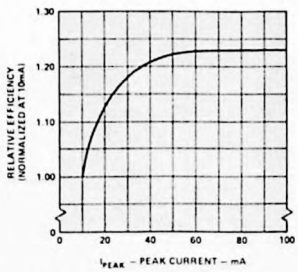


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

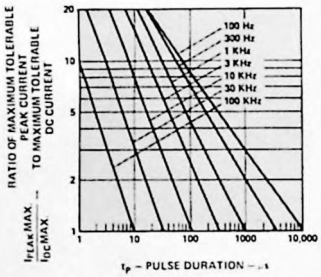


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

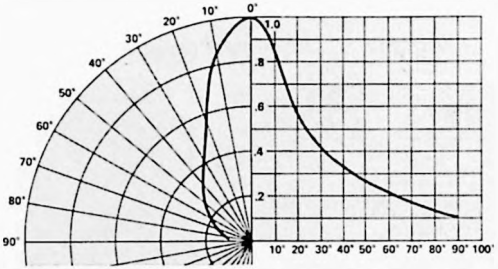


Figure 6. Relative Luminous Intensity vs. Angular Displacement.

High Efficiency Red HLMP-6300

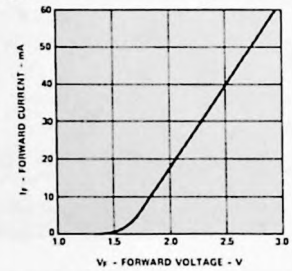


Figure 7. Forward Current vs. Forward Voltage Characteristics

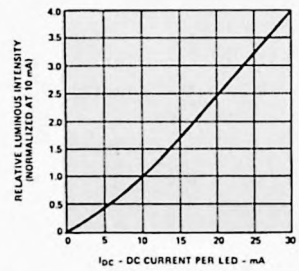


Figure 8. Relative Luminous Intensity vs. Forward Current.

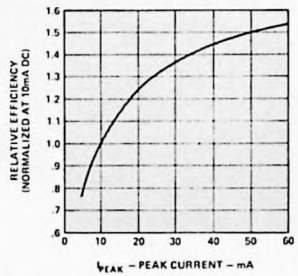


Figure 9. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

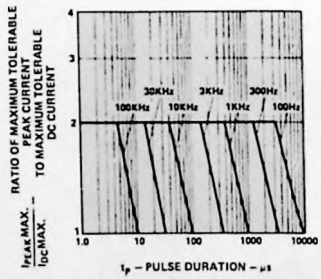


Figure 10. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

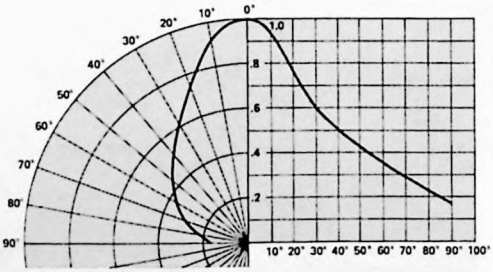


Figure 11. Relative Luminous Intensity vs. Angular Displacement.

Yellow HLMP-6400

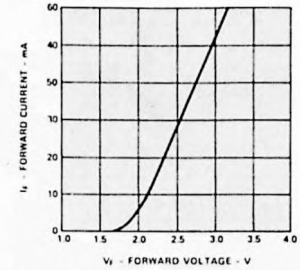


Figure 12. Forward Current vs. Forward Voltage Characteristics

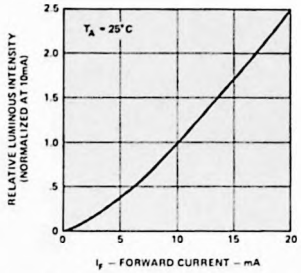


Figure 13. Relative Luminous Intensity vs. Forward Current.

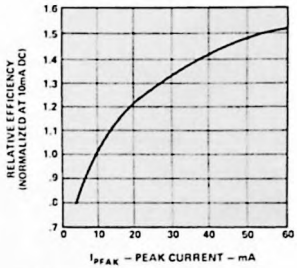


Figure 14. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

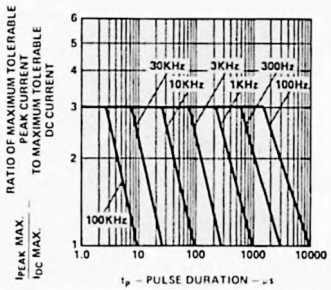


Figure 15. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

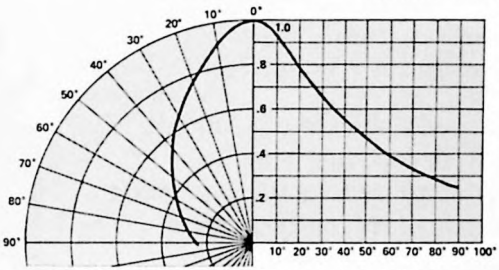


Figure 16. Relative Luminous Intensity vs. Angular Displacement.

Green HLMP-6500

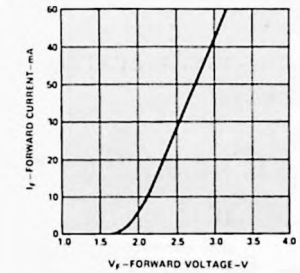


Figure 17. Forward Current vs. Forward Voltage.

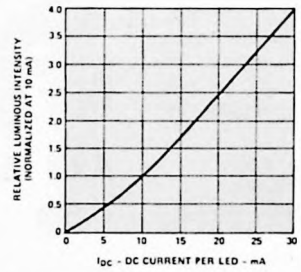


Figure 18. Relative Luminous Intensity vs. DC Forward Current

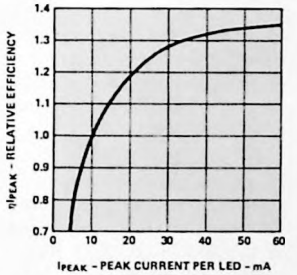


Figure 19. Relatiave Efficiency (Luminous Intensity per Unit Current) vs. Peak LED Current

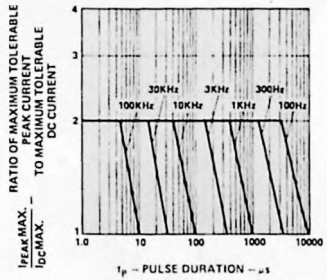


Figure 20. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

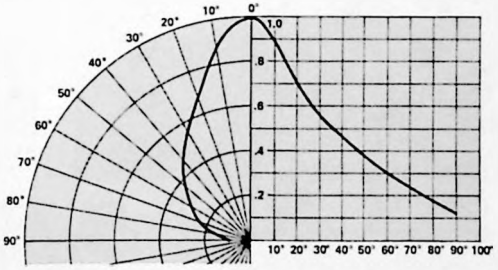


Figure 21. Relative Luminous Intensity vs. Angular Displacement.

HEWLETT PACKARD

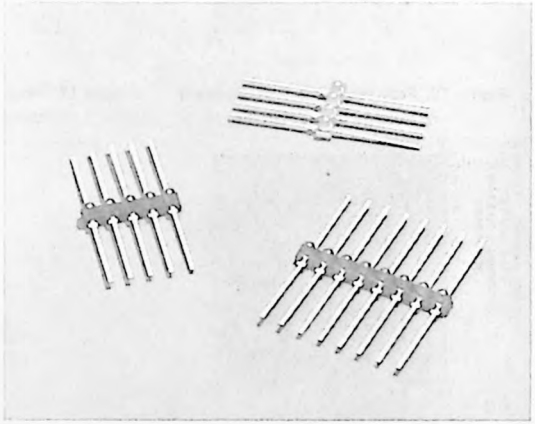
MATCHED ARRAYS OF SUBMINIATURE LAMPS

RED HLMP-6200 SERIES
HIGH EFFICIENCY RED HLMP-6650 SERIES
YELLOW HLMP-6750 SERIES
GREEN HLMP-6850 SERIES

TECHNICAL DATA JANUARY 1984

Features

- IMPROVED BRIGHTNESS
- AVAILABLE IN 4 BRIGHT COLORS
  Red
  High Efficiency Red
  Yellow
  High Performance Green
- EXCELLENT UNIFORMITY BETWEEN ELEMENTS
- END STACKABLE FOR LONGER ARRAYS
- SELECTION OF VARIOUS LENGTHS
- COMPACT SUBMINIATURE PACKAGE STYLE
- NO CROSSTALK BETWEEN ELEMENTS



Description

The HLMP-6XXX Series Arrays are comprised of several subminiature lamps molded as a single bar. Arrays are tested to assure 2.1 to 1 matching between elements and intensity binned for matching between arrays.

The HLMP-620X Series Arrays are Gallium Arsenide Phosphide red light emitting diodes. The HLMP-665X, HLMP-675X series arrays are Gallium Arsenide Phosphide on Gallium Phosphide red and yellow light emitting diodes. The HLMP-685X series arrays are Gallium Phosphide green light emitting diodes.

Each element has separately accessible leads and a diffused lens which provides a wide viewing angle and a high on/off contrast ratio. The center-to-center spacing is 2.54 mm (.100 in.) between elements. Special lead bending is available on 2.54 mm (.100 in.) and 5.08 mm (.200 in.) centers.

Array Length	Red	High Efficiency Red	Yellow	High Performance Green
3-Element HLMP-	6203	6653	6753	6853
4-Element HLMP-	6204	6654	6754	6854
5-Element HLMP-	6205	6655	6755	6855
6-Element HLMP-	6206	6656	6756	6856
8-Element HLMP-	6208	6658	6758	6858

Applications

- INDUSTRIAL CONTROLS
- POSITION INDICATORS
- OFFICE EQUIPMENT
- INSTRUMENTATION LOGIC INDICATORS
- CONSUMER PRODUCTS

Axial Luminous Intensity and Viewing Angle at 25°C

Part Number	Number of Elements	Color	I_V per Element (mcd) @ 10 mA DC		$2\Theta 1/2$ Note 1.
			Min.	Typ.	
HLMP-620X	X = 3,4, 5,6,8	Red	.5	1.2	45°
HLMP-665X	X = 3,4 5,6,8	High Efficiency Red	1.0	3.0	80°
HLMP-675X	X = 3,4 5,6,8	Yellow	1.0	3.0	90°
HLMP-685X	X = 3,4 5,6,8	Green	1.0	3.0	70°

NOTE:

1. $\Theta 1/2$ is the off-axis angle at which the Luminous Intensity is half the axial luminous intensity.

Absolute Maximum Ratings at T_A = 25°C

Parameter	Red	High Efficiency Red	Yellow	Green	Units
Peak Forward Current	1000	60	60	60	mA
DC Current	50[1]	30[2]	20[1]	30[2]	mA
Power Dissipation	100	120	120	120	mW
Operating Temperature Range	−55 to +100	−55 to +100	−55 to +100	−40 to +100	C°
Storage Temperature Range				−55 to +100	
Lead Soldering Temperature 1.6 mm [(0.063 in.) from body]	260° C for 3 seconds				

NOTES: 1. Derate from 50° C at 0.2 mA/° C. 2. Derate from 50° C at 0.5 mA/° C.

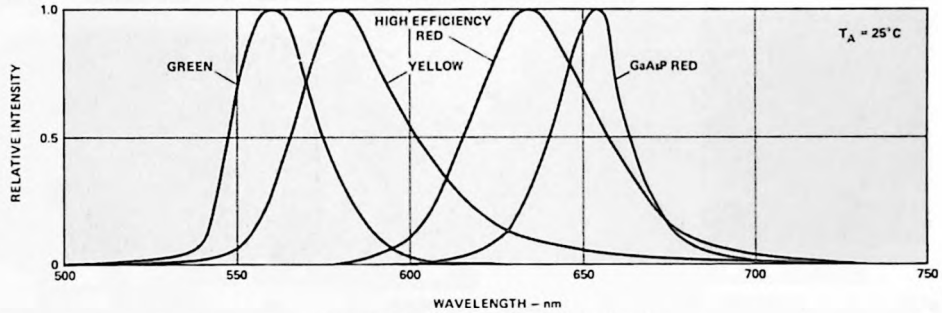


Figure 1. Relative Intensity vs. Wavelength.

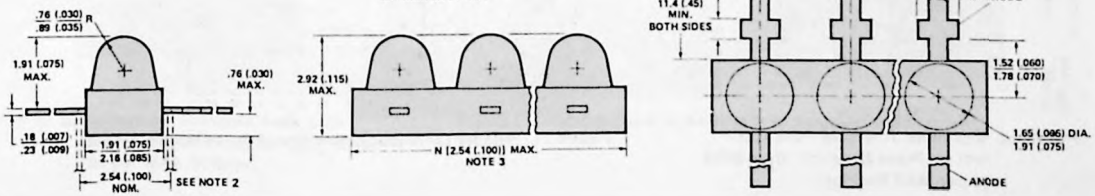
Electrical/Optical Characteristics at T_A=25°C

Symbol	Description	HLMP-62XX			HLMP-665X			HLMP-675X			HLMP-685X			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
λ_{PEAK}	Peak Wavelength		655			635			583			565		nm	Measurement at Peak
λ_d	Dominant Wavelength		640			629			585			569		nm	Note 1.
τ_S	Speed of Response		15			90			90			500		ns	
C	Capacitance		100			11			15			18		pF	V_f=0; f=1 MHz
θ_{JC}	Thermal Resistance		125			120			100			100		°C/W	Junction to Cathode Lead at 0.79mm (.031 in) from Body
V_F	Forward Voltage	1.4	1.6	2.0	1.5	2.2	3.0	1.5	2.2	3.0	1.5	2.3	3.0	V	I_f=10mA, Figures 2, 7, 12, 17
BV_R	Reverse Breakdown Voltage	3.0	10		5.0	15		5.0	15		5.0	20		V	I_R = 100μA
η_v	Luminous Efficacy		55			147			570			630		lm/W	Note 2.

NOTES:
1. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
2. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is the luminous efficacy in lumens/watt.

Package Dimensions

Notes:
1. All dimensions are in millimetres (inches).
2. Optional lead form available.
3. Overall length is the number of elements times 2.54mm (.100 in.).



Red HLMP-62XX Series

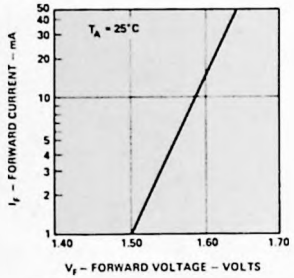


Figure 2. Forward Current vs. Forward Voltage.

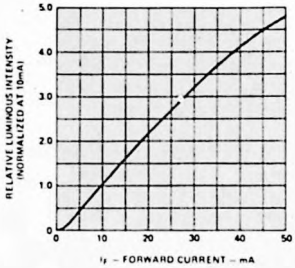


Figure 3. Relative Luminous Intensity vs. Forward Current.

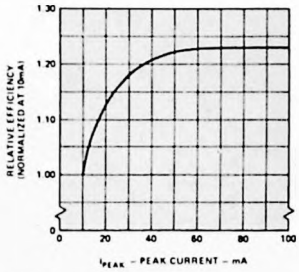


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

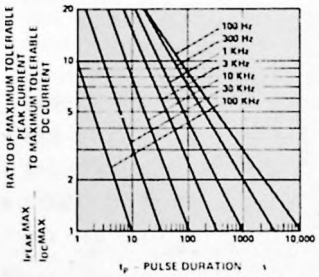


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

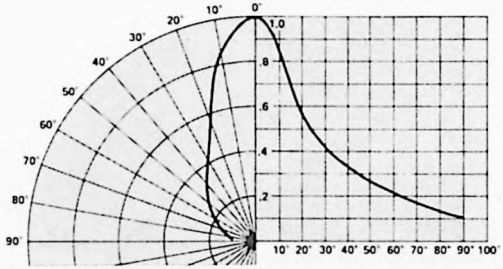


Figure 6. Relative Luminous Intensity vs. Angular Displacement.

High Efficiency Red HLMP-665X Series

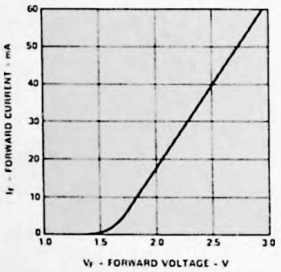


Figure 7. Forward Current vs. Forward Voltage.

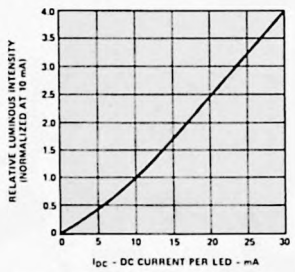


Figure 8. Relative Luminous Intensity vs. DC Forward Current.

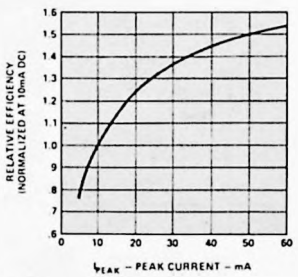


Figure 9. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

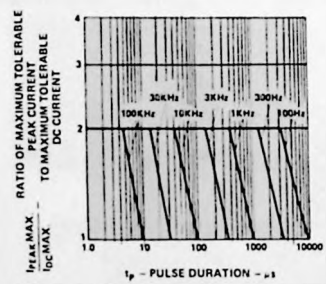


Figure 10. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

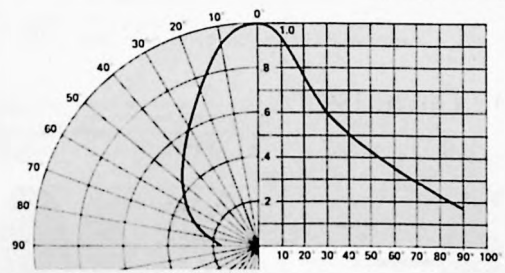


Figure 11. Relative Luminous Intensity vs. Angular Displacement.

Yellow HLMP-675X Series

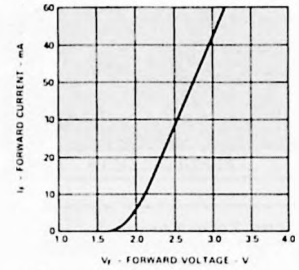


Figure 12. Forward Current vs. Forward Voltage.

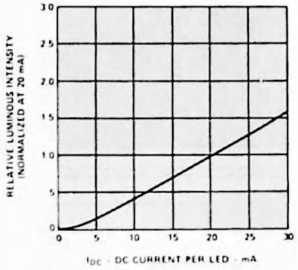


Figure 13. Relative Luminous Intensity vs. DC Forward Current.

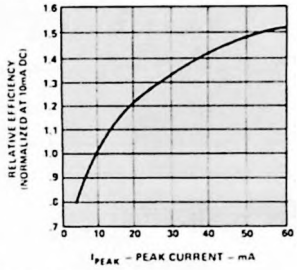


Figure 14. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

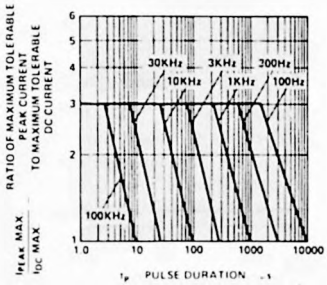


Figure 15. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

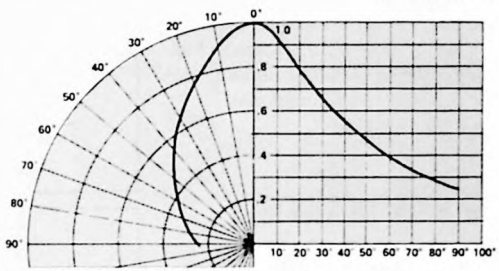


Figure 16. Relative Luminous Intensity vs. Angular Displacement.

Green HLMP-685X Series

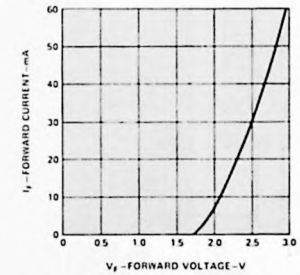


Figure 17. Forward Current vs. Forward Voltage.

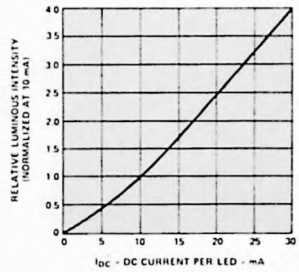


Figure 18. Relative Luminous Intensity vs. DC Forward Current.

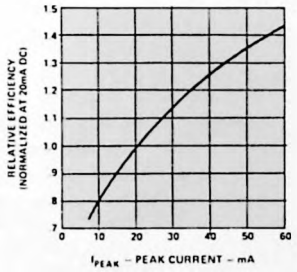


Figure 19. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

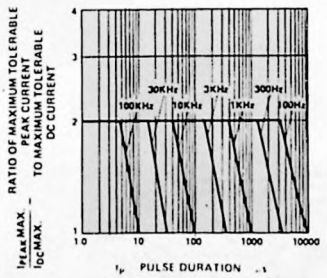


Figure 20. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

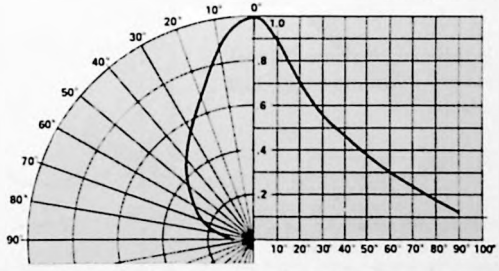


Figure 21. Relative Luminous Intensity vs. Angular Displacement.

HEWLETT PACKARD

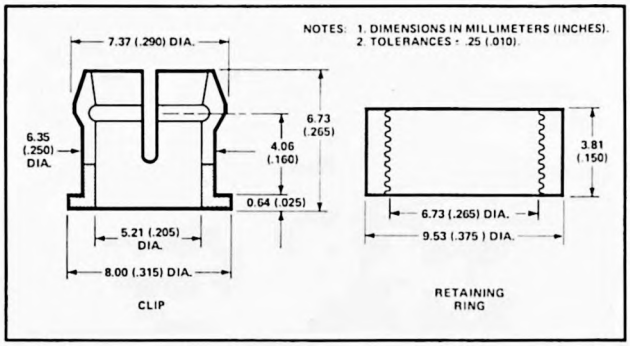
CLIP AND RETAINING RING FOR PANEL MOUNTED T1 3/4 LEDs

HLMP-0103

TECHNICAL DATA JANUARY 1984

Description

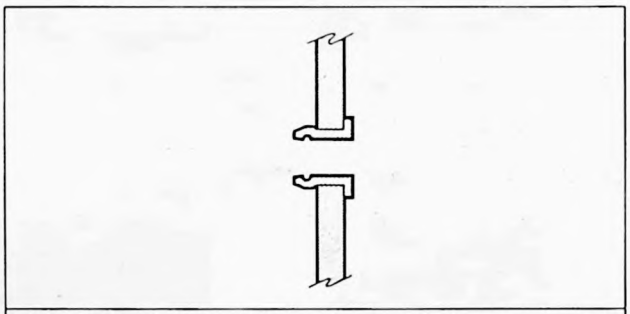
The HLMP-0103 is a black plastic mounting clip and retaining ring. It is designed to panel mount Hewlett Packard Solid State high profile T - 1¾ size lamps. This clip and ring combination is intended for installation in instrument panels from 1.52mm (.060") to 3.18mm (.125") thick. For panels greater than 3.18mm (.125"), counterboring is required to the 3.18mm (.125") thickness.



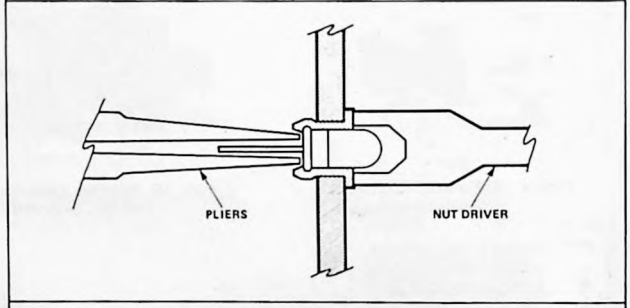
Mounting Instructions

1. Drill an ASA C size 6.15mm (.242") dia. hole in the panel. Deburr but do not chamfer the edges of the hole.

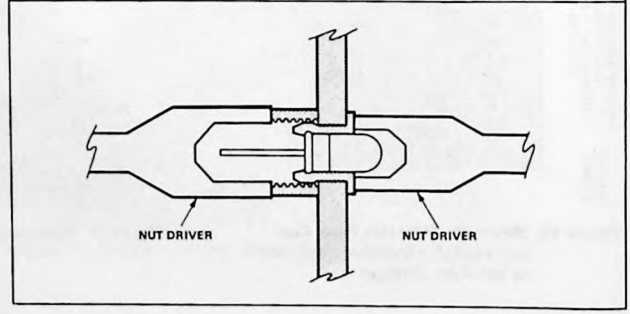
2. Press the panel clip into the hole from the front of the panel.



3. Press the LED into the clip from the back. Use blunt long nose pliers to push on the LED. Do not use force on the LED leads. A tool such as a nut driver may be used to press on the clip.



4. Slip a plastic retaining ring onto the back of the clip and press tight using tools such as two nut drivers.



Note: Clip and retaining ring are also available for T-1 package, from a non-HP source. Please contact your Hewlett-Packard sales representative for information.

HEWLETT PACKARD

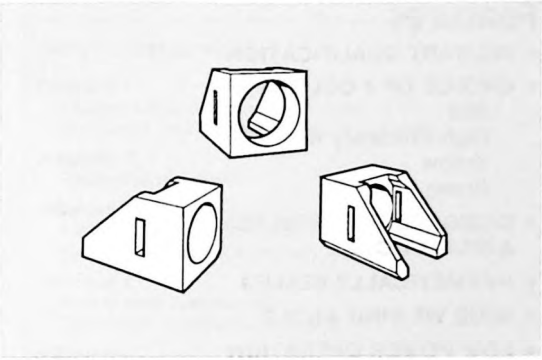
T-1 3/4 LED LAMP RIGHT ANGLE HOUSING

HLMP-5029

TECHNICAL DATA JANUARY 1984

Features

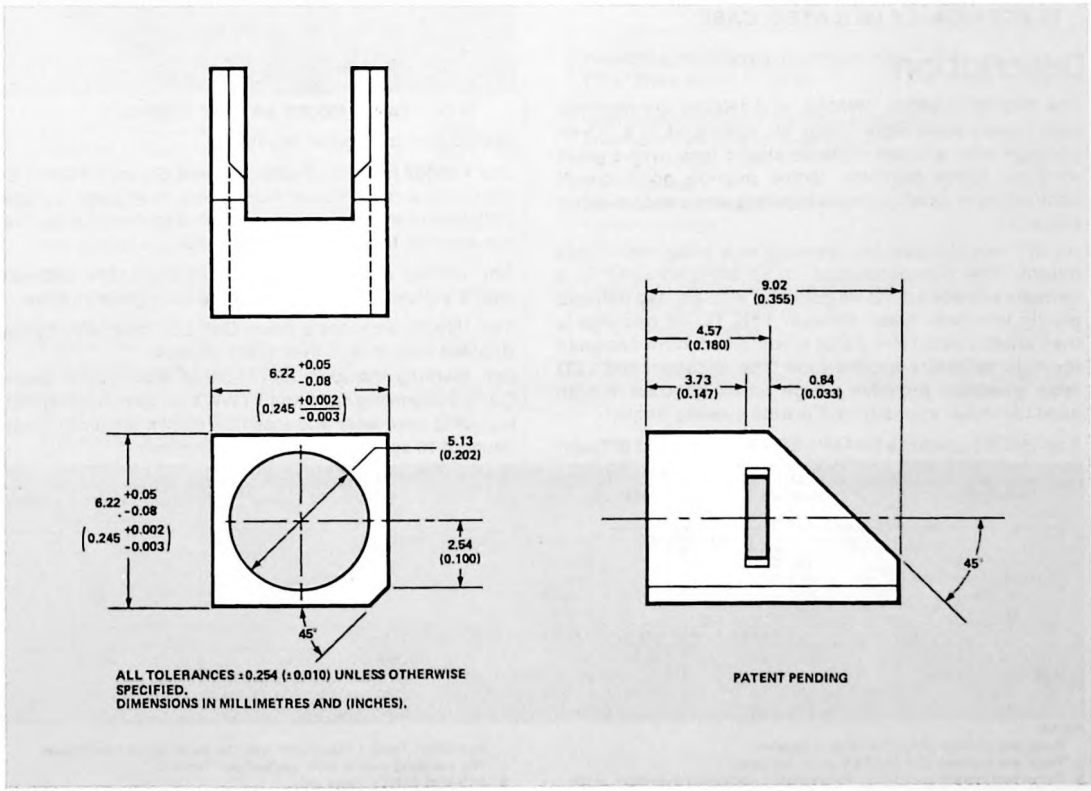
- FITS ANY HP HIGH DOME T-1 3/4 LED LAMP
- SNAP-IN FIT MAKES MOUNTING SIMPLE
- HIGH CONTRAST BLACK PLASTIC



Description

The HLMP-5029 is a black plastic right angle housing which mates with any Hewlett-Packard High Dome T-1 3/4 lamp. The lamp snaps into place. The material is fully compatible with environmental specifications of all Hewlett-Packard T-1 3/4 lamps.

Physical Dimensions



ALL TOLERANCES ±0.254 (±0.010) UNLESS OTHERWISE SPECIFIED.
DIMENSIONS IN MILLIMETRES AND (INCHES).

PATENT PENDING

HEWLETT PACKARD

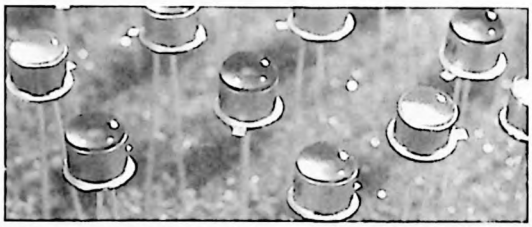
JAN QUALIFIED HERMETIC SOLID STATE LAMPS*

1N5765 JAN1N5765 JANTX1N5765	1N6093 JAN1N6093 JANTX1N6093
1N6092 JAN1N6092 JANTX1N6092	1N6094 JAN1N6094 JANTX1N6094

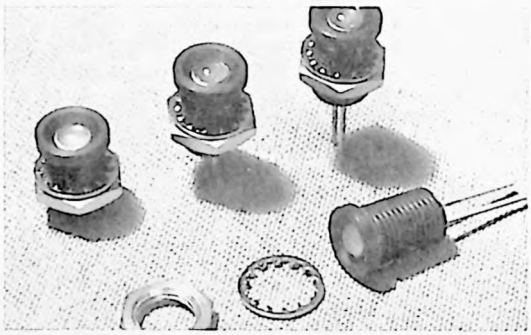
TECHNICAL DATA JANUARY 1984

Features

- MILITARY QUALIFICATION
- CHOICE OF 4 COLORS
  - Red
  - High Efficiency Red
  - Yellow
  - Green
- DESIGNED FOR HIGH-RELIABILITY APPLICATIONS
- HERMETICALLY SEALED
- WIDE VIEWING ANGLE
- LOW POWER OPERATION
- IC COMPATIBLE
- LONG LIFE
- PANEL MOUNT OPTION HAS WIRE WRAPPABLE LEADS AND AN ELECTRICALLY ISOLATED CASE



HERMETIC TO-46 LAMP



PANEL MOUNT AS LAMP ASSEMBLY

Description

The 1N5765, 1N6092, 1N6093, and 1N6094 are hermetically sealed solid state lamps encapsulated in a TO-46 package with a tinted diffused plastic lens over a glass window. These hermetic lamps provide good on-off contrast, high axial luminous intensity and a wide viewing angle.

All of these devices are available in a panel mountable fixture. The semiconductor chips are packaged in a hermetically sealed TO-46 package with a tinted diffused plastic lens over glass window. This TO-46 package is then encapsulated in a panel mountable fixture designed for high reliability applications. The encapsulated LED lamp assembly provides a high on-off contrast, a high axial luminous intensity and a wide viewing angle.

The 1N5765 utilizes a GaAsP LED chip with a red diffused plastic lens over glass window.

The 1N6092 has a high efficiency red GaAsP on GaP LED chip with a red diffused plastic lens over glass window. This lamp's efficiency is comparable to that of a GaP red but extends to higher current levels.

The 1N6093 provides a yellow GaAsP on GaP LED chip with a yellow diffused plastic lens over glass window.

The 1N6094 provides a green GaP LED chip with a green diffused plastic lens over glass window.

Part marking includes: part number from matrix below. CAQI designating code and YYWWX lot identification code including year, week and assembly plant if required. A maximum of 18 spaces can be accommodated.

COLOR — PART NUMBER — LAMP AND PANEL MOUNT MATRIX

Description	Standard Product	With JAN Qualification[1]	JAN Plus TX Testing[2]	Controlling MIL-S-19500 Document[4]
TABLE I HERMETIC TO-46 PART NUMBER SYSTEM				
Standard Red	1N5765	JAN1N5765	JANTX1N5765	/467
High Efficiency Red	1N6092	JAN1N6092	JANTX1N6092	/519
Yellow	1N6093	JAN1N6093	JANTX1N6093	/520
Green	1N6094	JAN1N6094	JANTX1N6094	/521
TABLE II PANEL MOUNTABLE PART NUMBER SYSTEM[3]				
Standard Red	HLMP-0904	HLMP-0930 ——	HLMP-0931 ——	NONE
High Efficiency Red	HLMP-0354	HLMP-0380 MI9500/519-01	HLMP-0381 MI9500/519-02	/519
Yellow	HLMP-0454	HLMP-0480 MI9500/520-01	HLMP-0481 MI9500/520-02	/520
Green	HLMP-0554	HLMP-0580 MI9500/521-01	HLMP-0581 MI9500/521-02	/521

Notes:

1. Parts are marked J1NXXXX or as indicated.
2. Parts are marked JTX INXXXX or as indicated.
3. Panel mountable packaging incorporates additional assembly of the equivalent Table I TO-46 part into the panel mount enclosure. The resulting part is then marked per Table II.
4. JAN and JANTX parts only.

*Panel mount versions of all of the above are available per the selection matrix on this page.

JAN PART: Samples of each lot are subjected to Group A, B and C tests listed below. All tests are to the conditions and limits specified by the appropriate MIL-S-19500 slash sheet for the device under test. A summary of the data gathered in Groups A, B and C lot acceptance testing is supplied with each shipment.

JANTX PART: Devices undergo 100% screening tests as listed below to the conditions and limits specified by MIL-S-19500 slash sheet. The JANTX lot has also been subjected to Group A, B and C tests as for the JAN PART above. A summary of the data gathered in Groups A, B and C acceptance testing is supplied with each shipment.

Examination or Test	MIL-STD-750 Method
GROUP A INSPECTION	
Subgroup 1	
Visual and mechanical examination	2071
Subgroup 2	
Luminous intensity ($\theta = 0°$)	—
Luminous intensity ($\theta = 30°$)	—
Reverse current	4016
Forward voltage	4011
Subgroup 3	
Capacitance	4001
GROUP B INSPECTION	
Subgroup 1	
Physical dimensions	2066
Subgroup 2	
Solderability	2026
Thermal shock (temperature cycling)	1051
Thermal shock (glass strain)	1056
Hermetic seal	1071
Moisture resistance	1021
End points: Luminous intensity ($\theta = 0°$)	—
Subgroup 3	
Shock	2016
Vibration, variable frequency	2056
Constant acceleration	2006
End points: (same as subgroup 2)	
Subgroup 4	
Terminal strength	2036
End points: Hermetic seal	1071
Subgroup 5	
Salt atmosphere (corrosion)	1041
Subgroup 6	
High-temperature life (nonoperating)	1032
End points: Luminous intensity ($\theta = 0°$)	—
Subgroup 7	
Steady-state operation life	1027
End points: (same as subgroup 6)	

Examination or Test	MIL-STD-750 Method
GROUP C INSPECTION	
Subgroup 1	
Thermal shock (temperature cycling)	1051
End points: (same as subgroup 2 of group B)	
Subgroup 2	
Resistance to solvents	—
Subgroup 3	
High-temperature life (nonoperating)	1031
End points: Luminous intensity ($\theta = 0°$)	—
Subgroup 4	
Steady-state operation life	1026
End points: (same as subgroup 3)	
Subgroup 5	
Peak forward pulse current (transient)	—
End points: (same as subgroup 6 of group B)	
Subgroup 6	
Peak forward pulse current (operating)	—
End points: (same as subgroup 6 of group B)	
PROCESS AND POWER CONDITION ("TX" types only)	
High temperature storage (nonoperating)	—
Thermal shock (temperature cycling)	1051
Constant acceleration	2006
Hermetic seal	1071
Luminous intensity ($\theta = 0°$)	—
Forward voltage	4011
Reverse current	4016
Burn-in (Forward bias)	—
End points (within 72 hours of burn-in):	
Δ Luminous intensity ($\theta = 0°$)	—
Δ Forward voltage	4011

Absolute Maximum Ratings at T_A=25°C

Parameter	Red HLMP-0904	High Eff. Red HLMP-0354	Yellow HLMP-0454	Green HLMP-0554	Units
Power Dissipation (derate linearly from 50°C at 1.6mW/°C)	100	120	120	120	mW
DC Forward Current	50[1]	35[2]	35[2]	35[2]	mA
Peak Forward Current	1000 See Fig. 5	60 See Fig. 10	60 See Fig. 15	60 See Fig. 20	mA
Operating and Storage Temperature Range	-65°C to 100°C				
Lead Soldering Temperature [1.6mm (0.063 in.) from body]	260°C for 7 seconds.				

Notes: 1. Derate from 50°C at 0.2mA/°C 2. Derate from 50°C at 0.5mA/°C

Electrical/Optical Characteristics at T_A=25°C

Symbol	Description	HLMP-0904			HLMP-0354			HLMP-0454			HLMP-0554			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{V1}	Axial Luminous Intensity	0.5	1.0		1.0	5		1.0	5		0.8	3		mcd	I_F = 20mA Figs. 3,8,13,18 θ = 0°
											At I_F = 25mA				
I_{V2}	Luminous Intensity at θ = 30°[5]	0.3			0.5			0.5			0.4			mcd	I_F = 20 mA θ = 30°
$2\theta_{1/2}$	Included Angle Between Half Luminous Intensity Points		60			70			70			70		deg.	[1] Figures 6, 11, 16, 21
λ_{PEAK}	Peak Wavelength[5]	630	655	700	590	635	695	550	583	660	525	565	600	nm	Measurement at Peak
λ_d	Dominant Wavelength		640			626			585			570		nm	[2]
τ_s	Speed of Response		10			200			200			200		ns	
C	Capacitance[5]		200	300		35	100		35	100		35	100	pF	V_t=0; f=1 MHz
θ_{JC}	Thermal Resistance*		425			425			425			425		°C/W	[3]
θ_{JC}	Thermal Resistance**		550			550			550			550		°C/W	[3]
V_F	Forward Voltage		1.6	2.0		2.0	3.0		2.0	3.0		2.1	3.0	V	I_F = 20mA Figures 2, 7, 12, 17
												At I_F = 25mA			
I_R	Reverse Current[5]			1.0			1.0			1.0			1.0	μA	V_R = 3V
BV_R	Reverse Breakdown Voltage	4	5		5.0			5.0			5.0			V	I_R = 100μA
η_v	Luminous Efficacy		58			140			455			600		lm/W	[4]

NOTES:
1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Junction to Cathode Lead with 3.18mm (0.125 inch) of leads exposed between base of flange and heat sink.
4. Radiant Intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is the luminous efficacy in lumens/watt.
5. Limits do not apply to non JAN parts.

*Panel mount.
**T0-46

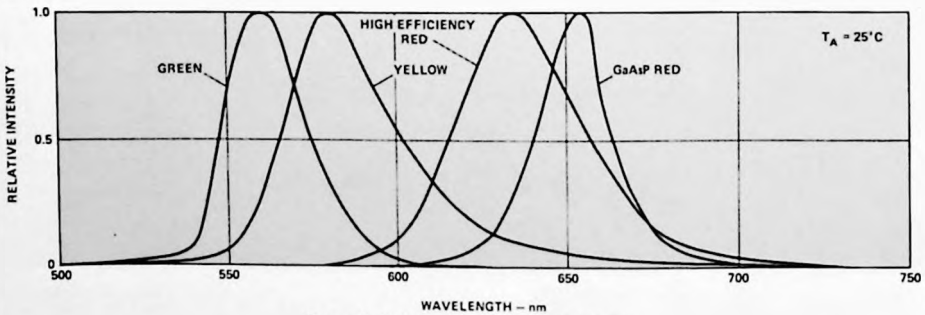
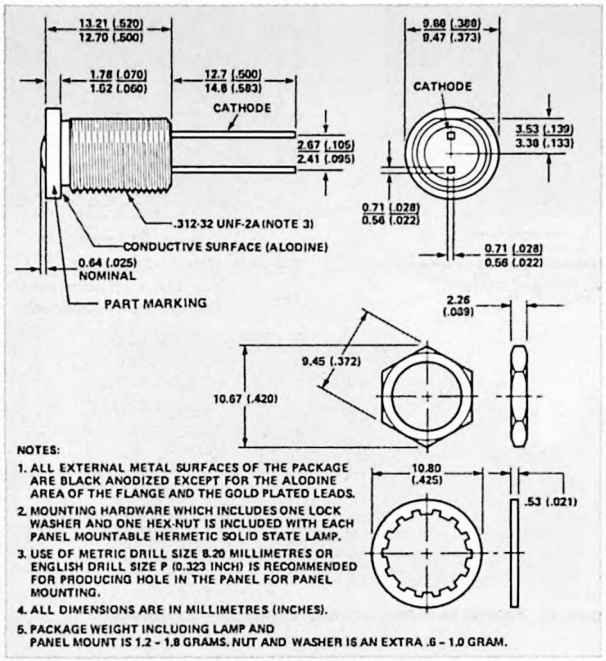


Figure 1. Relative Intensity vs. Wavelength.

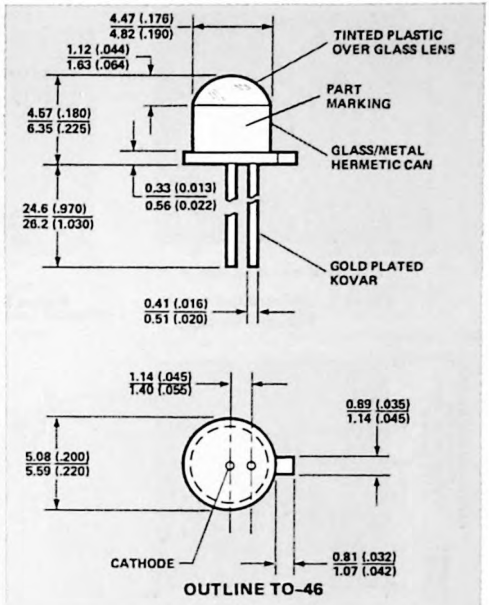
Package Dimensions

HLMP-0904, 0354, 0454, 0554



NOTES:
1. ALL EXTERNAL METAL SURFACES OF THE PACKAGE ARE BLACK ANODIZED EXCEPT FOR THE ALODINE AREA OF THE FLANGE AND THE GOLD PLATED LEADS.
2. MOUNTING HARDWARE WHICH INCLUDES ONE LOCK WASHER AND ONE HEX-NUT IS INCLUDED WITH EACH PANEL MOUNTABLE HERMETIC SOLID STATE LAMP.
3. USE OF METRIC DRILL SIZE 8.20 MILLIMETRES OR ENGLISH DRILL SIZE P (0.323 INCH) IS RECOMMENDED FOR PRODUCING HOLE IN THE PANEL FOR PANEL MOUNTING.
4. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
5. PACKAGE WEIGHT INCLUDING LAMP AND PANEL MOUNT IS 1.2 – 1.8 GRAMS. NUT AND WASHER IS AN EXTRA .6 – 1.0 GRAM.

1N5765, 1N6092, 1N6093, 1N6094



OUTLINE TO-46

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. GOLD PLATED LEADS.
3. PACKAGE WEIGHT OF LAMP ALONE IS .25 – .35 GRAMS.

Family of Red 1N5765/HLMP-0904

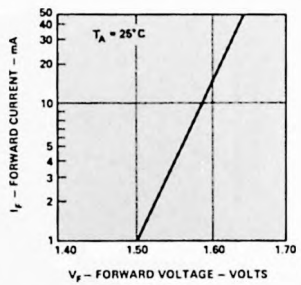


Figure 2. Forward Current vs. Forward Voltage.

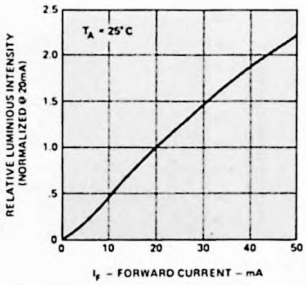


Figure 3. Relative Luminous Intensity vs. Forward Current.

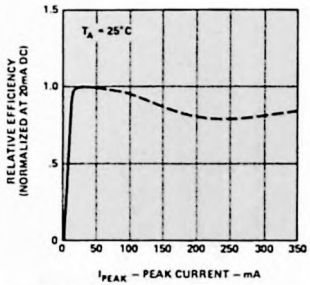


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

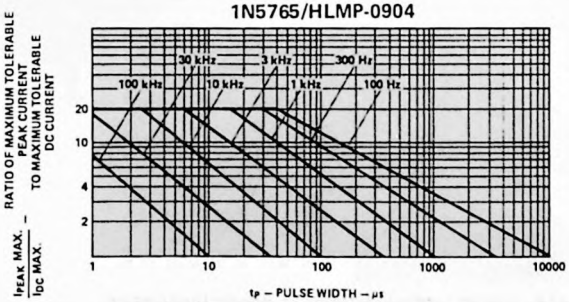


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

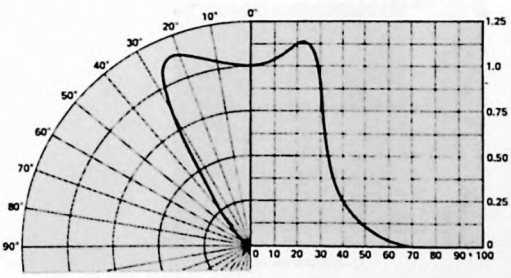


Figure 6. Relative Luminous Intensity vs. Angular Displacement.

Family of High Efficiency Red 1N6092/HLMP-0354

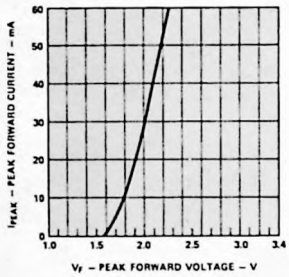


Figure 7. Forward Current vs. Forward Voltage.

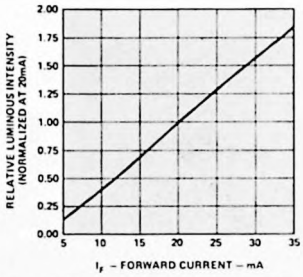


Figure 8. Relative Luminous Intensity vs. Forward Current.

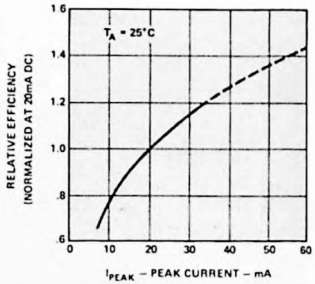


Figure 9. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

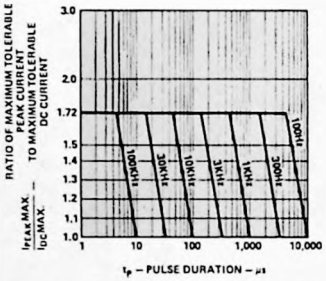


Figure 10. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

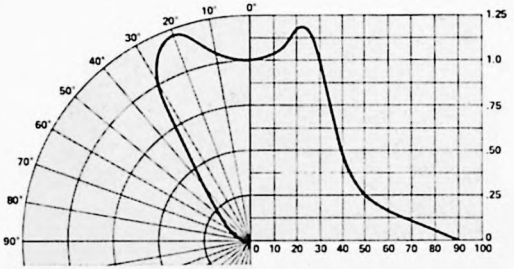


Figure 11. Relative Luminous Intensity vs. Angular Displacement.

Family of Yellow 1N6093/HLMP-0454

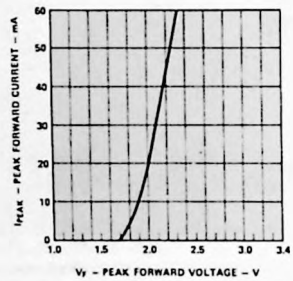


Figure 12. Forward Current vs. Forward Voltage.

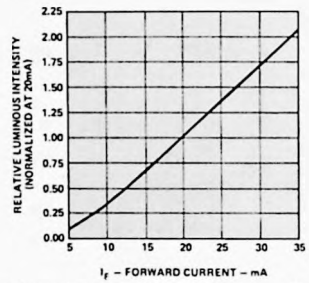


Figure 13. Relative Luminous Intensity vs. Forward Current.

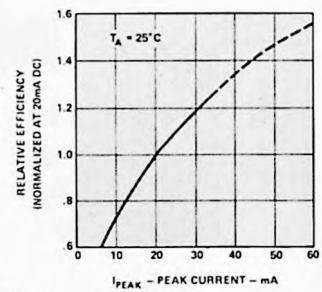


Figure 14. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

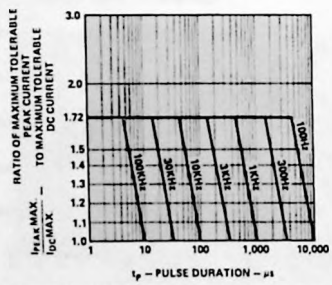


Figure 15. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

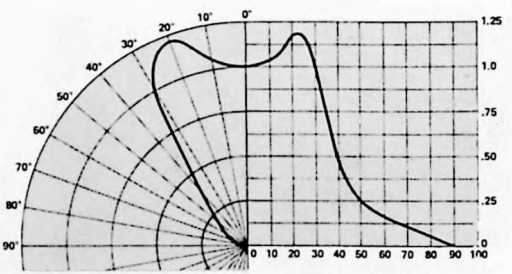


Figure 16. Relative Luminous Intensity vs. Angular Displacement.

Family of Green 1N6094/HLMP-0554

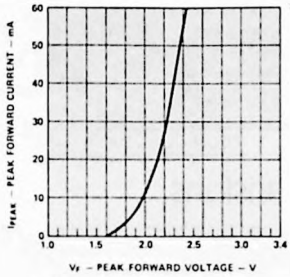


Figure 17. Forward Current vs. Forward Voltage.

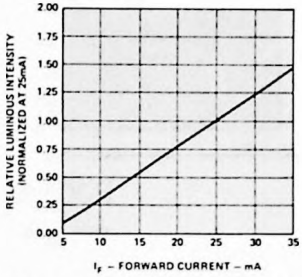


Figure 18. Relative Luminous Intensity vs. Forward Current.

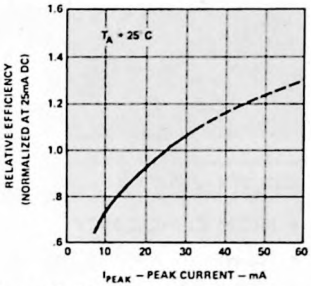


Figure 19. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

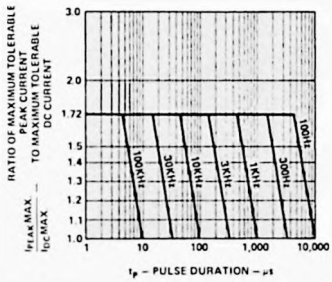


Figure 20. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

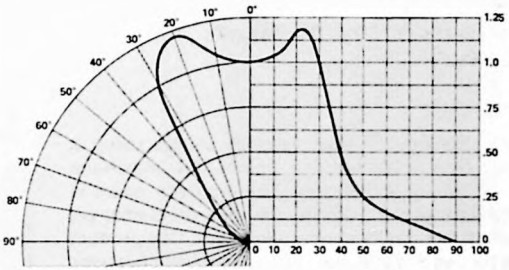


Figure 21. Relative Luminous Intensity vs. Angular Displacement.

HEWLETT PACKARD

670nm HIGH RADIANT INTENSITY EMITTER

HEMT-3300

TECHNICAL DATA JANUARY 1984

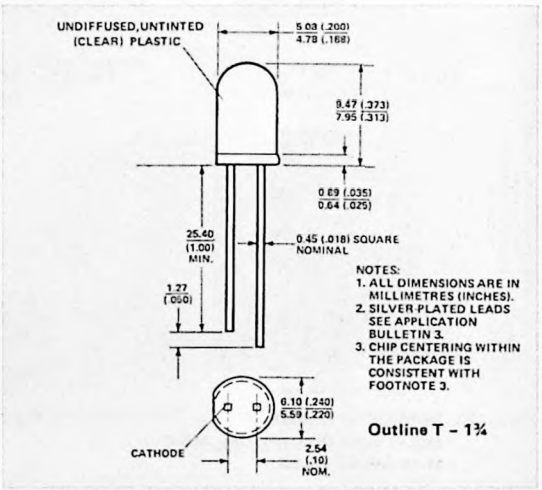
Features

- HIGH EFFICIENCY
- NONSATURATING OUTPUT
- NARROW BEAM ANGLE
- VISIBLE FLUX AIDS ALIGNMENT
- BANDWIDTH: DC TO 3 MHz
- IC COMPATIBLE/LOW CURRENT REQUIREMENT

Description

The HEMT-3300 is a visible, near-IR, source using a GaAsP on GaP LED chip optimized for maximum quantum efficiency at 670 nm. The emitter's beam is sufficiently narrow to minimize stray flux problems, yet broad enough to simplify optical alignment. This product is suitable for use in consumer and industrial applications such as optical transducers and encoders, smoke detectors, assembly line monitors, small parts counters, paper tape readers and fiber optic drivers.

Package Dimensions



Electrical/Optical Characteristics at $T_A = 25°C$

Symbol	Description	Min.	Typ.	Max.	Units	Test Conditions	Figure
I_e	Axial Radiant Intensity	200	500		μW/sr	I_F = 10 mA	3,4
K_e	Temperature Coefficient of Intensity		-0.009		$°C^{-1}$	I_F = 10 mA, Note 1	
η_v	Luminous Efficacy		22		lm/W	Note 2	
$2\Theta_{½}$	Half Intensity Total Angle		22		deg.	Note 3, I_F = 10 mA	6
λ_{PEAK}	Peak Wavelength		670		nm	Measured at Peak	1
$\Delta\lambda_{PEAK}/\Delta T$	Spectral Shift Temperature Coefficient		0.089		nm/°C	Measured at Peak, Note 4	
t_r	Output Rise Time (10% – 90%)		120		ns	I_{PEAK} = 10 mA	
t_f	Output Fall Time (90% – 10%)		50		ns	I_{PEAK} = 10 mA Pulse	
C_O	Capacitance		15		pF	V_F = 0; f = 1 MHz	
BV_R	Reverse Breakdown Voltage	5.0			V	I_R = 100 μA	
V_F	Forward Voltage		1.9	2.5	V	I_F = 10 mA	2
$\Delta V_F/\Delta T$	Temperature Coefficient of V_F		-2.2		mV/°C	I_F = 100 μA	
Θ_{JC}	Thermal Resistance		160		°C/W	Junction to cathode lead at seating plane.	

Notes: 1. $I_e(T) = I_e(25°C)\exp[K_e(T - 25°C)]$ 2. $I_v = \eta_v I_e$ where I_v is in candela, I_e in watts/steradian and η_v in lumen/watt. 3. $\Theta_{½}$ is the off-axis angle at which the radiant intensity is half the axial intensity. The deviation between the mechanical and optical axis is typically within a conical half-angle of five degrees. 4. $\lambda_{PEAK}(T) = \lambda_{PEAK}(25°C) + (\Delta\lambda_{PEAK}/\Delta T)(T - 25°C)$.

Maximum Ratings at T_A=25°C

Power Dissipation ..... 120 mW
(derate linearly from 50°C at 1.6 mW/°C)
Average Forward Current ..... 30 mA
(derate linearly from 50°C at 0.4 mA/°C)
Peak Forward Current ..... See Figure 5
Operating and Storage
Temperature Range ..... -55°C to +100°C
Lead Soldering Temperature ..... 260°C for 5 sec.
(1.6 mm [0.063 inch] from body)

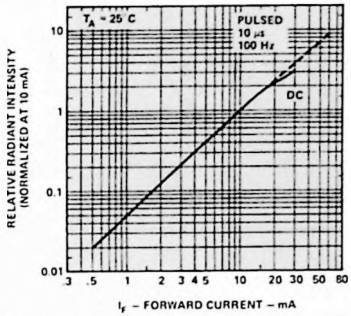


Figure 3. Relative Radiant Intensity versus Forward Current.

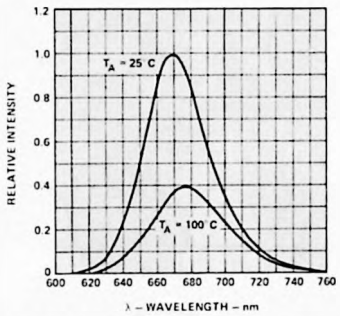


Figure 1. Relative Intensity versus Wavelength.

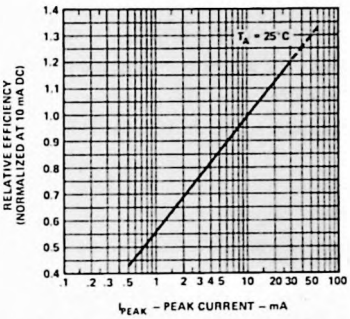


Figure 4. Relative Efficiency (Radiant Intensity per Unit Current) versus Peak Current.

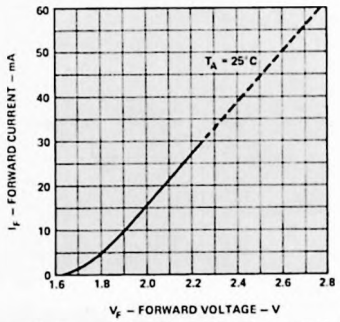


Figure 2. Forward Current versus Forward Voltage.

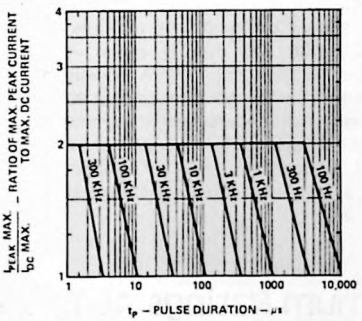


Figure 5. Maximum Tolerable Peak Current versus Pulse Duration. (I_{DC} MAX as per MAX Ratings)

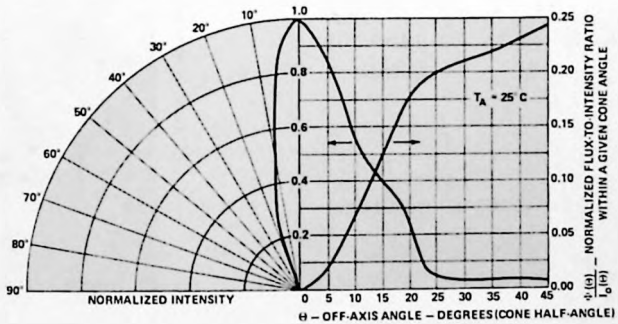


Figure 6. Far-Field Radiation Pattern.

HEWLETT PACKARD

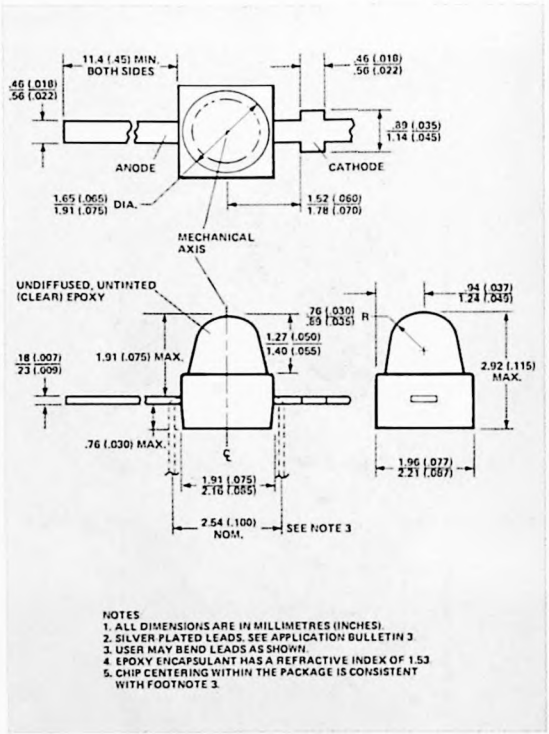
700nm HIGH INTENSITY SUBMINIATURE EMITTER

HEMT-6000

TECHNICAL DATA JANUARY 1984

Features

- HIGH RADIANT INTENSITY
- NARROW BEAM ANGLE
- NONSATURATING OUTPUT
- BANDWIDTH: DC TO 5 MHz
- IC COMPATIBLE/LOW CURRENT REQUIREMENT
- VISIBLE FLUX AIDS ALIGNMENT



NOTES
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. SILVER PLATED LEADS. SEE APPLICATION BULLETIN 3.
3. USER MAY BEND LEADS AS SHOWN.
4. EPOXY ENCAPSULANT HAS A REFRACTIVE INDEX OF 1.53.
5. CHIP CENTERING WITHIN THE PACKAGE IS CONSISTENT WITH FOOTNOTE 3.

Description

The HEMT-6000 uses a GaAsP chip designed for optimum tradeoff between speed and quantum efficiency. This optimization allows a flat modulation bandwidth of 5 MHz without peaking, yet provides a radiant flux level comparable to that of 900nm IREDs. The subminiature package allows operation of multiple closely-spaced channels, while the narrow beam angle minimizes crosstalk. The nominal 700nm wavelength can offer spectral performance advantages over 900nm IREDs, and is sufficiently visible to aid optical alignment. Applications include paper-tape readers, punch-card readers, bar code scanners, optical encoders or transducers, interrupt modules, safety interlocks, tape loop stabilizers and fiber optic drivers.

Maximum Ratings at $T_A = 25°C$

Power Dissipation ..... 50 mW
(derate linearly from 70°C @ 1.0mW/°C)

Average Forward Current ..... 20 mA
(derate linearly from 70°C @ 0.4mA/°C)

Peak Forward Current ..... See Figure 5

Operating and Storage Temperature Range ..... -55° to +100°C

Lead Soldering Temperature ..... 260°C for 5 sec. [1.6 mm (0.063 in.) from body]

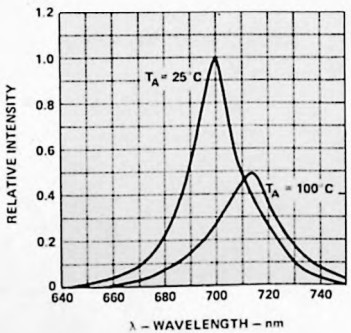


Figure 1. Relative Intensity versus Wavelength.

Electrical/Optical Characteristics at $T_A = 25°C$

Symbol	Description	Min.	Typ.	Max.	Units	Test Conditions	Fig.
I_e	Radiant Intensity along Mechanical Axis	100	250		$\mu W/sr$	I_F = 10 mA	3,4
K_e	Temperature Coefficient of Intensity		-0.005		$°C^{-1}$	Note 1	
η_v	Luminous Efficacy		2.5		lm/W	Note 2	
$2\Theta_{1/2}$	Optical Axis Half Intensity Total Angle		16		deg.	Note 3, I_F = 10 mA	6
λ_{PEAK}	Peak Wavelength (Range)		690-715		nm	Measured @ Peak	1
$\Delta\lambda_{PEAK}/\Delta T$	Spectral Shift Temperature Coefficient		.193		nm/°C	Measured @ Peak, Note 4	
t_r	Output Rise Time (10%-90%)		70		ns	I_{PEAK} = 10 mA	
t_f	Output Fall Time (90%-10%)		40		ns	I_{PEAK} = 10 mA	
C_o	Capacitance		65		pF	V_F = 0; f = 1 MHz	
BV_R	Reverse Breakdown Voltage	5	12		V	I_R = 100 μA	
V_F	Forward Voltage		1.5	1.8	V	I_F = 10 mA	2
$\Delta V_F/\Delta T$	Temperature Coefficient of V_F		-2.1		mV/°C	I_F = 100 μA	
Θ_{JC}	Thermal Resistance		140		°C/W	Junction to cathode lead at 0.79 mm (.031 in) from body	

NOTES:
1. $I_e(T) = I_e\,(25°C)\exp[K_e\,(T - 25°C)]$.
2. $I_v = \eta_v I_e$ where I_v is in candela, I_e in watts/steradian, and η_v in lumen/watt.
3. $\Theta_{1/2}$ is the off-axis angle at which the radiant intensity is half the intensity along the optical axis. The deviation between the mechanical and the optical axis is typically within a conical half-angle of three degrees.
4. $\lambda_{PEAK}\,(T) = \lambda_{PEAK}\,(25°C) + (\Delta\lambda_{PEAK}/\Delta T)\,(T - 25°C)$

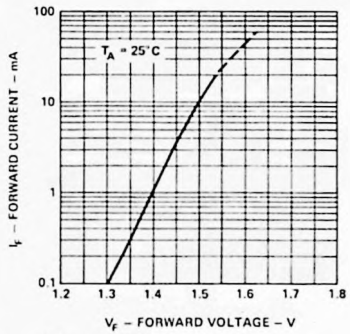


Figure 2. Forward Current versus Forward Voltage.

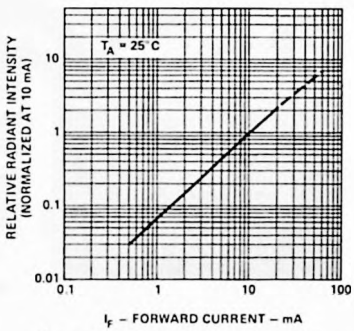


Figure 3. Relative Radiant Intensity versus Forward Current.

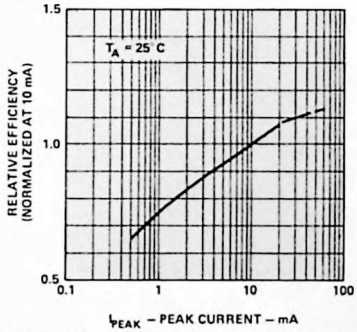


Figure 4. Relative Efficiency (Radiant Intensity per Unit Current) versus Peak Current.

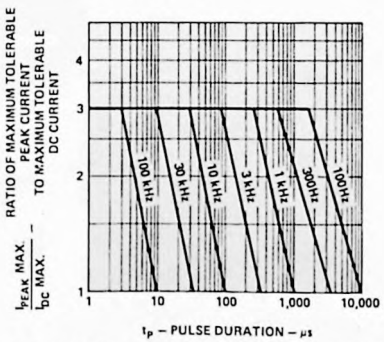


Figure 5. Maximum Tolerable Peak Current versus Pulse Duration. (I_{DC} MAX as per MAX Ratings)

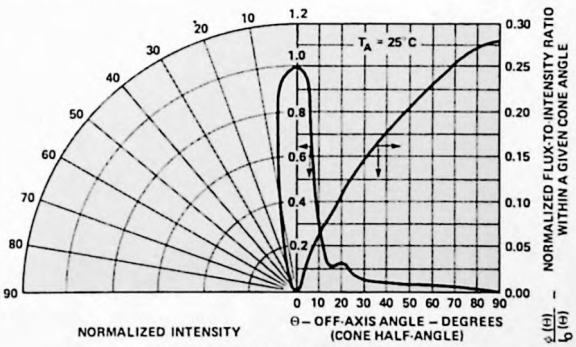
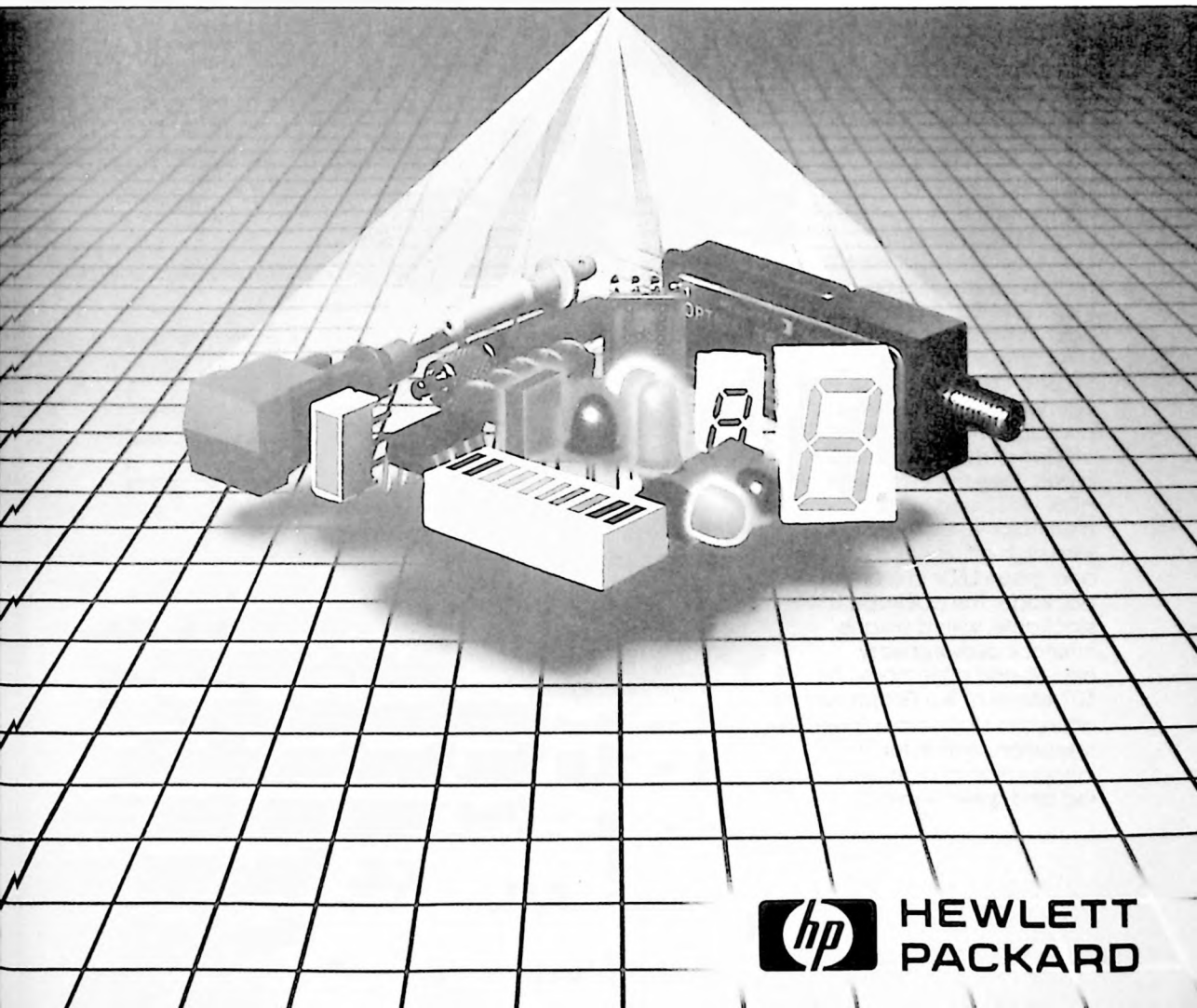


Figure 6. Far-Field Radiation Pattern.

2. Light Bars and Bar Graph Arrays

- LED Light Bars
- LED Bicolor Light Bars —DIP
- Panel and Legend Mounts for Light Bars
- LED 10-Element Bar Graph Array
- LED 101-Element Bar Graph Array

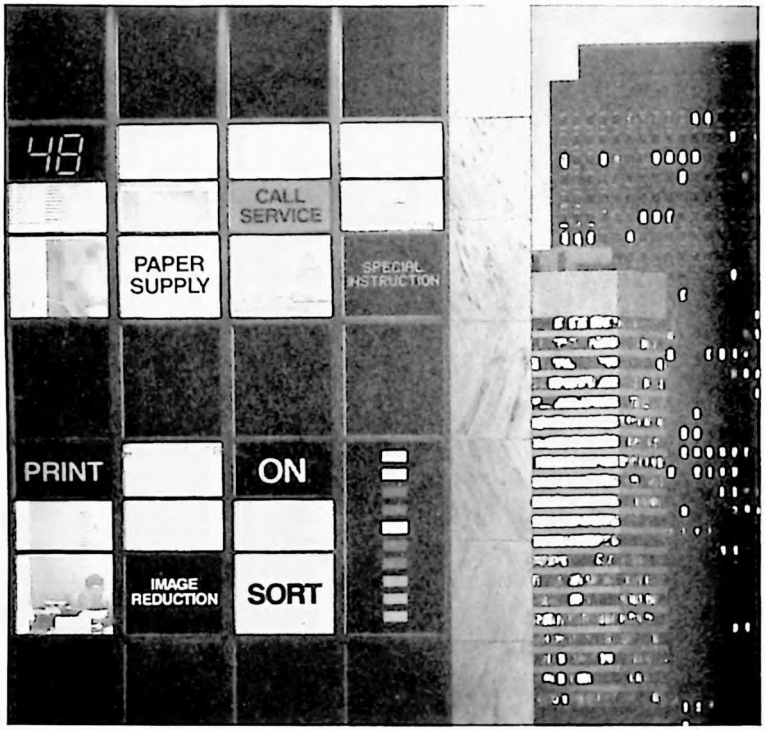


HEWLETT PACKARD

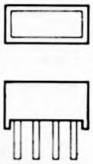
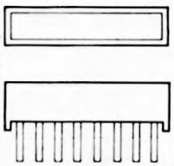
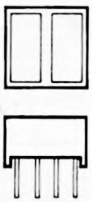
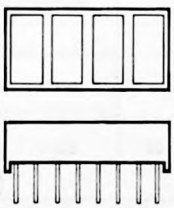
Light Bars and Bar Graph Arrays

LED Light Bars are Hewlett-Packard's innovative solution to fixed message annunciation. The large, uniformly illuminated light emitting surface may be used for backlighting legends or simple indicators. Three distinct colors are offered, high efficiency red, yellow, and high performance green, with two bicolor combinations (see page 2-13). Each of the eight X-Y stackable package styles offers one, two, or four light emitting surfaces. Panel and Legend Mounts are also available for all devices.

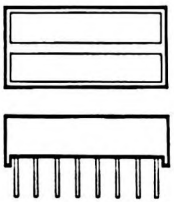
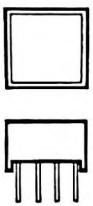
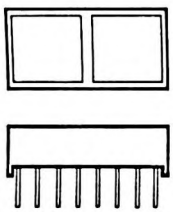
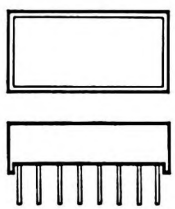
In addition to light bars, HP offers effective analog message annunciation with the new 10-element and 101-element LED Bar Graph Arrays. These bar graph arrays eliminate the matching and alignment problems commonly associated with arrays of discrete LED indicators. Each device offers easy to handle packages that are compatible with standard SIP and DIP sockets. The 10-element Bar Graph Array is available in standard red, high efficiency red, yellow, and green. New this year are the HDSP-4832 and HDSP-4836 multicolor 10-element arrays with high efficiency red, yellow, and green LEDs in a single package. The package is X-Y stackable, with a unique interlock allowing easy end-to-end alignment. The 101-element Bar Graph Array is offered in standard red with 1% resolution. Watch for the introduction of high efficiency red and green versions.



LED Light Bars

Device		Description			Typical Luminous Intensity @ 20 mA	Typical Forward Voltage @ 20 mA	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens			
	HLMP-2300	High Efficiency Red	4 Pin In-Line; .100" Centers; .400"L x .195"W x .240"H	Diffused	20 mcd	2.0 V	2-7
	HLMP-2400	Yellow		Diffused	20 mcd	2.1 V	
	HLMP-2500	Green		Green Diffused	25 mcd	2.2 V	
	HLMP-2350	High Efficiency Red	8 Pin In-Line; .100" Centers; .800"L x .195"W x .240"H	Diffused	35 mcd	2.0 V	
	HLMP-2450	Yellow		Diffused	35 mcd	2.1 V	
	HLMP-2550	Green		Green Diffused	50 mcd	2.2 V	
	HLMP-2600	High Efficiency Red	8 Pin DIP; .100" Centers; .400"L x .400"W x .240"H; Dual Arrangement	Diffused	20 mcd	2.0 V	
	HLMP-2700	Yellow		Diffused	18 mcd	2.1 V	
	HLMP-2800	Green		Green Diffused	25 mcd	2.2 V	
	HLMP-2620	High Efficiency Red	16 Pin DIP; .100" Centers; .800"L x .400"W x .240"H; Quad Arrangement	Diffused	20 mcd	2.0 V	
	HLMP-2720	Yellow		Diffused	18 mcd	2.1 V	
	HLMP-2820	Green		Green Diffused	25 mcd	2.2 V	

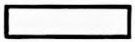
LED Light Bars (Continued)

Device		Description			Typical Luminous Intensity @ 20 mA	Typical Forward Voltage @ 20 mA	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens			
	HLMP-2635	High Efficiency Red	16 Pin DIP; .100" Centers; .800"L x .400"W x .240"H Dual Bar Arrangement	Diffused	35 mcd	2.0 V	2-7
	HLMP-2735	Yellow		Diffused	35 mcd	2.1 V	
	HLMP-2835	Green		Green Diffused	50 mcd	2.2 V	
	HLMP-2655	High Efficiency Red	8 Pin DIP; .100" Centers; .400"L x .400"W x .240"H Square Arrangement	Diffused	35 mcd	2.0 V	
	HLMP-2755	Yellow		Diffused	35 mcd	2.1 V	
	HLMP-2855	Green		Green Diffused	50 mcd	2.2 V	
	HLMP-2670	High Efficiency Red	16 Pin DIP; .100" Centers; .800"L x .400"W x .240"H Dual Square Arrangement	Diffused	35 mcd	2.0 V	
	HLMP-2770	Yellow		Diffused	35 mcd	2.1 V	
	HLMP-2870	Green		Green Diffused	50 mcd	2.2 V	
	HLMP-2685	High Efficiency Red	16 Pin DIP; .100" Centers; .800"L x .400"W x .240"H Single Bar Arrangement	Diffused	70 mcd	2.0 V	
	HLMP-2785	Yellow		Diffused	70 mcd	2.1 V	
	HLMP-2885	Green		Green Diffused	100 mcd	2.2 V	

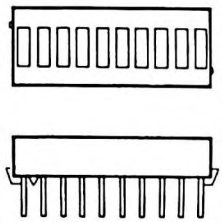
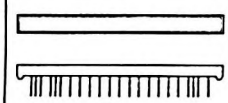
LED Bicolor Light Bars

Device		Description			Typical Luminous Intensity @ 20 mA	Typical Forward Voltage @ 20 mA	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens			
	HLMP-2950	High Efficiency Red/ Yellow	8 Pin DIP; .100" Centers; .400"L x .400"W x .240"H Square Arrangment	Diffused	HER: 20 mcd Yellow: 12 mcd	HER: 2.0 V Yellow: 2.1 V	2-13
	HLMP-2965	High Efficiency Red/ Green		Diffused	HER: 20 mcd Green: 20 mcd	HER: 2.0 V Green: 2.2 V	

Panel and Legend Mounts for LED Light Bars

Device		Corresponding Light Bar Module Part Number HLMP-	Page No.
Package Outline Drawing	Part No.		
	HLMP-2598	2350, 2450, 2550	2-19
	HLMP-2599	2300, 2400, 2500	
	HLMP-2898	2600, 2700, 2800 2655, 2755, 2855 2950, 2965	2-19
	HLMP-2899	2620, 2720, 2820 2635, 2735, 2835 2670, 2770, 2870 2685, 2785, 2885	

LED Bar Graph Arrays

Device		Description			Typical Luminous Intensity @ 20 mA	Typical Forward Voltage @ 20 mA	Page No.
Package Outline Drawing	Part No.	Color	Package	Lens			
	HDSP-4820	Standard Red	20 Pin DIP; .100" Centers; 1.0"L x .400"W x .240"H	Diffused	1250 μcd @ 20 mA DC	1.6 V @ 20 mA DC	2-21
	HDSP-4830	High Efficiency Red		Diffused	2280 μcd @ 10 mA DC	2.1 V @ 20 mA DC	
	HDSP-4840	Yellow		Diffused	1900 μcd @ 10 mA DC	2.2 V @ 20 mA DC	
	HDSP-4850	High Performance Green		Diffused	1900 μcd @ 10 mA DC	2.1 V @ 10 mA DC	
	HDSP-4832	Multicolor		Diffused	1900 μcd @ 10 mA DC		
	HDSP-4836	Multicolor		Diffused	1900 μcd @ 10 mA DC		
	HDSP-8820	Standard Red	22 Pin SIP; .100" Centers; 4.16"L x .390"W x .236"H	Red, Non-Diffused	20 μcd @ 100 mA Pk: 1 of 110 D.F.	1.7 V @ 100 mA Pk: 1 of 110 D.F.	2-27

HEWLETT PACKARD

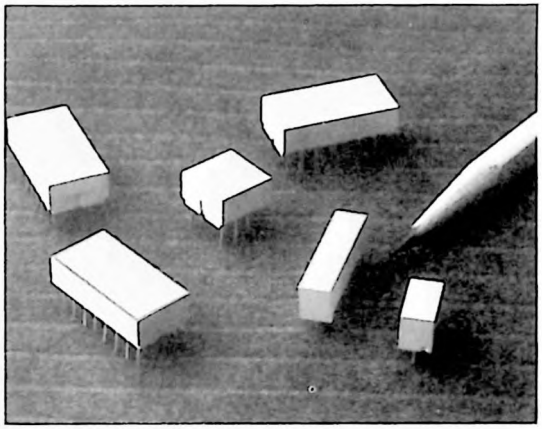
LED LIGHT BARS

HIGH EFFICIENCY RED HLMP-2300/-2600 SERIES
YELLOW HLMP-2400/-2700 SERIES
HIGH PERFORMANCE GREEN HLMP-2500/-2800 SERIES

TECHNICAL DATA JANUARY 1984

Features

- LARGE, BRIGHT, UNIFORM LIGHT EMITTING AREAS
  Approximately Lambertian Radiation Pattern
- CHOICE OF THREE COLORS
- CATEGORIZED FOR LIGHT OUTPUT
- YELLOW AND GREEN CATEGORIZED FOR DOMINANT WAVELENGTH
- EXCELLENT ON-OFF CONTRAST
- EASILY MOUNTED ON P.C. BOARDS OR INDUSTRY STANDARD SIP/DIP SOCKETS
- MECHANICALLY RUGGED
- X-Y STACKABLE
- FLUSH MOUNTABLE
- CAN BE USED WITH PANEL AND LEGEND MOUNTS
- LIGHT EMITTING SURFACE SUITABLE FOR LEGEND ATTACHMENT PER APPLICATION NOTE 1012
- SUITABLE FOR MULTIPLEX OPERATION
- I.C. COMPATIBLE



Applications

- BUSINESS MACHINE MESSAGE ANNUNCIATORS
- TELECOMMUNICATIONS INDICATORS
- FRONT PANEL PROCESS STATUS INDICATORS
- PC BOARD IDENTIFIERS
- BAR GRAPHS

Description

The HLMP-2300/-2400/-2500/-2600/-2700/-2800 series light bars are rectangular light sources designed for a variety of applications where a large, bright source of light is required. These light bars are configured in single-in-line and dual-in-line packages that contain either single or segmented light emitting areas. The -2300/-2400/-2600/-2700 series devices utilize LED chips which are made from GaAsP on a transparent GaP substrate. The -2500/-2800 series devices utilize chips made from GaP on a transparent GaP substrate.

Selection Guide

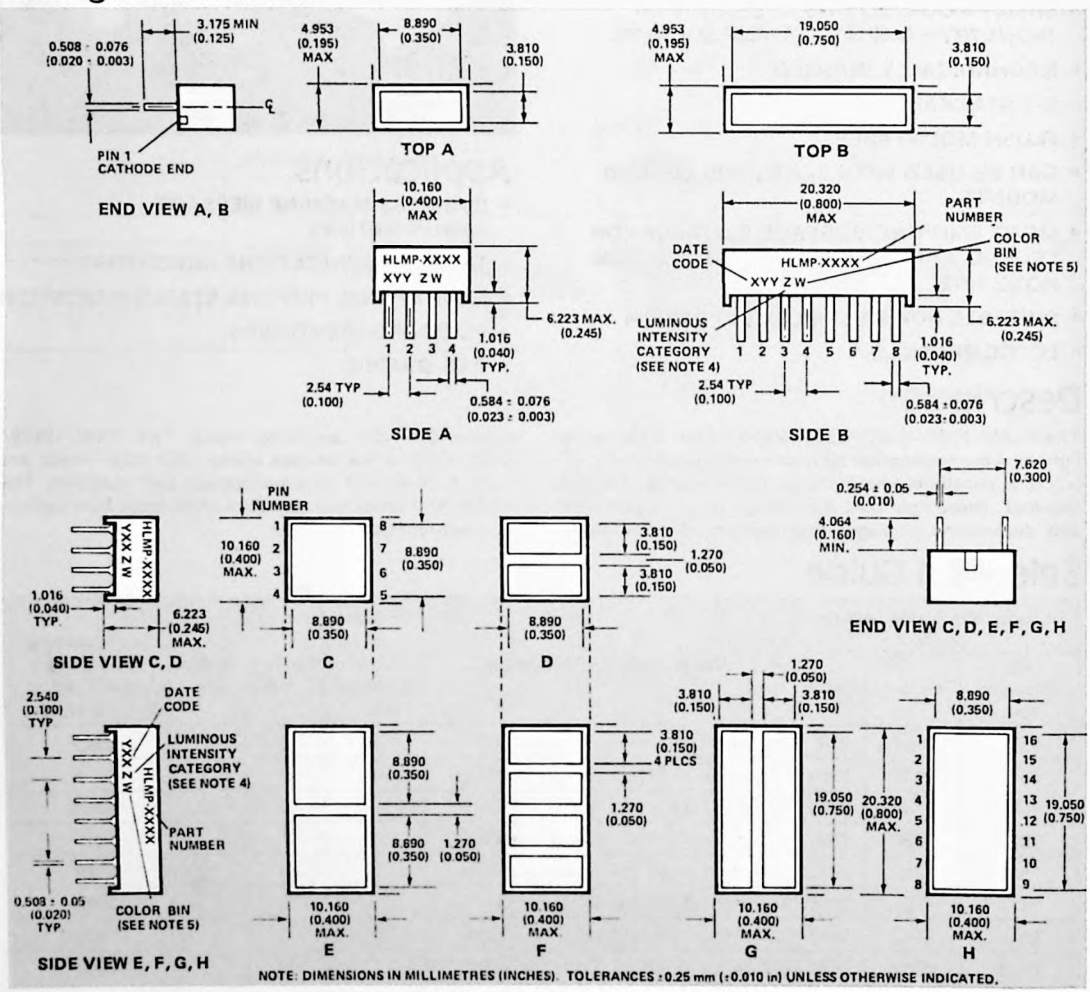
Light Bar Part Number HLMP-			Size of Light Emitting Areas	Number of Light Emitting Areas	Package Outline Outline		Corresponding Panel and Legend Mount Part No. HLMP-
High Efficiency Red	Yellow	Green					
2300	2400	2500	8.89 mm x 3.81 mm (.350 in. x .150 in.)	1	A		2599
2350	2450	2550	19.05 mm x 3.81 mm (.750 in. x .150 in.)	1	B		2598
2600	2700	2800	8.89 mm x 3.81 mm (.350 in. x .150 in.)	2	D		2898
2620	2720	2820	8.89 mm x 3.81 mm (.350 in. x .150 in.)	4	F		2899
2635	2735	2835	8.89 mm x 19.05 mm (.150 in. x .750 in.)	2	G		2899
2655	2755	2855	8.89 mm x 8.89 mm (.350 in. x .350 in.)	1	C		2898
2670	2770	2870	8.89 mm x 8.89 mm (.350 in. x .350 in.)	2	E		2899
2685	2785	2885	8.89 mm x 19.05 mm (.350 in. x .750 in.)	1	H		2899

Absolute Maximum Ratings

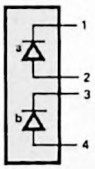
Parameter	HLMP-2300/-2500/ -2600/-2800 Series	HLMP-2400/ -2700 Series
Average Power Dissipation per LED Chip[1]	135 mW	85 mW
Peak Forward Current per LED Chip, T_A = 50°C (Maximum Pulse Width = 2 ms)[1, 2]	90 mA	60 mA
Time Average Forward Current per LED Chip, Pulsed Conditions[2]	25 mA, T_A = 25°C	20 mA, T_A = 50°C
DC Forward Current per LED Chip, T_A = 50°C[3]	30 mA	25 mA
Reverse Voltage per LED Chip	6 V	
Operating Temperature Range	-40°C to +85°C	
Storage Temperature Range	-40°C to +85°C	
Lead Soldering Temperature, 1.6 mm (1/16 inch) Below Seating Plane	260°C for 3 seconds	

NOTES:
1. For HLMP-2300/-2500/-2600/-2800 series, derate above T_A = 25°C at 1.8 mW/°C per LED chip. For HLMP-2400/-2700 series, derate above T_A = 50°C at 1.8 mW/°C per LED chip. See Figure 2.
2. See Figure 1 to establish pulsed operating conditions.
3. For HLMP-2300/-2500/-2600/-2800 series, derate above T_A = 50°C at 0.50 mA/°C per LED chip. For HLMP-2400/-2700 series, derate above T_A = 60°C at 0.50 mA/°C per LED chip. See Figure 3.

Package Dimensions

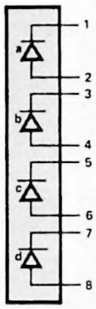


Internal Circuit Diagrams

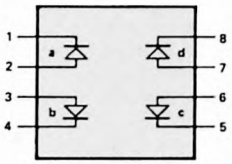


A

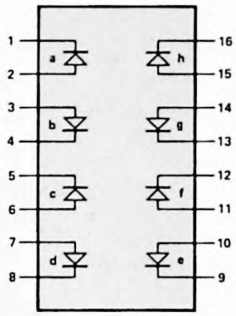
PIN FUNCTION		
PIN	A -2300/-2400 -2500	B -2350/-2450 -2550
1	Cathode — a	Cathode — a
2	Anode — a	Anode — a
3	Cathode — b	Cathode — b
4	Anode — b	Anode — b
5		Cathode — c
6		Anode — c
7		Cathode — d
8		Anode — d



B



C,D



E,F,G,H

PIN	PIN FUNCTION	
	C, D	E, F, G, H
1	CATHODE a	CATHODE a
2	ANODE a	ANODE a
3	ANODE b	ANODE b
4	CATHODE b	CATHODE b
5	CATHODE c	CATHODE c
6	ANODE c	ANODE c
7	ANODE d	ANODE d
8	CATHODE d	CATHODE d
9		CATHODE e
10		ANODE e
11		ANODE f
12		CATHODE f
13		CATHODE g
14		ANODE g
15		ANODE h
16		CATHODE h

Electrical/Optical Characteristics at T_A=25°C

High Efficiency Red HLMP-2300/-2600 Series

Parameter	HLMP-	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Luminous Intensity[4] Per Light Emitting Area	2300	I_V	4.5	20		mcd	20 mA DC
				30		mcd	60 mA Pk: 1 of 3 DF
	2350	I_V	9	35		mcd	20 mA DC
				50		mcd	60 mA Pk: 1 of 3 DF
	2600	I_V	4.5	20		mcd	20 mA DC
				30		mcd	60 mA Pk: 1 of 3 DF
	2620	I_V	4.5	20		mcd	20 mA DC
				30		mcd	60 mA Pk: 1 of 3 DF
	2635	I_V	9	35		mcd	20 mA DC
				50		mcd	60 mA Pk: 1 of 3 DF
	2655	I_V	9	35		mcd	20 mA DC
				50		mcd	60 mA Pk: 1 of 3 DF
	2670	I_V	9	35		mcd	20 mA DC
				50		mcd	60 mA Pk: 1 of 3 DF
	2685	I_V	18	70		mcd	20 mA DC
				100		mcd	60 mA Pk: 1 of 3 DF
Peak Wavelength		λ_{peak}		635		nm	
Dominant Wavelength[5]		λ_d		626		nm	
Forward Voltage Per LED		V_F		2.0	2.6	V	I_F = 20 mA
Reverse Breakdown Voltage Per LED		V_{BR}	6	15		V	I_R = 100μA
Thermal Resistance LED Junction-to-Pin		$R\theta_{J-PIN}$		150		°C/W/ LED Chip	

Yellow HLMP-2400/-2700 Series

Parameter	HLMP-	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Luminous Intensity[4] Per Light Emitting Area	2400	I_V	4	20		mcd	20 mA DC
				33		mcd	60 mA Pk: 1 of 3 DF
	2450	I_V	8	35		mcd	20 mA DC
				60		mcd	60 mA Pk: 1 of 3 DF
	2700	I_V	4	18		mcd	20 mA DC
				30		mcd	60 mA Pk: 1 of 3 DF
	2720	I_V	4	18		mcd	20 mA DC
				30		mcd	60 mA Pk: 1 of 3 DF
	2735	I_V	8	35		mcd	20 mA DC
				60		mcd	60 mA Pk: 1 of 3 DF
	2755	I_V	8	35		mcd	20 mA DC
				60		mcd	60 mA Pk: 1 of 3 DF
	2770	I_V	8	35		mcd	20 mA DC
				60		mcd	60 mA Pk: 1 of 3 DF
	2785	I_V	16	70		mcd	20 mA DC
				115		mcd	60 mA Pk: 1 of 3 DF
Peak Wavelength		λ_{peak}		583		nm	
Dominant Wavelength[5]		λ_d		585		nm	
Forward Voltage Per LED		V_F		2.1	2.6	V	I_F = 20 mA
Reverse Breakdown Voltage Per LED		V_{BR}	6	15		V	I_R = 100 μA
Thermal Resistance LED Junction-to-Pin		$R\theta_{J-PIN}$		150		°C/W/ LED Chip	

High Performance Green HLMP-2500/-2800 Series

Parameter	HLMP-	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Luminous Intensity[4] Per Light Emitting Area	2500	I_V	3.7	25		mcd	20 mA DC
				38		mcd	60 mA Pk: 1 of 3 DF
	2550	I_V	7.5	50		mcd	20 mA DC
				75		mcd	60 mA Pk: 1 of 3 DF
	2800	I_V	3.7	25		mcd	20 mA DC
				38		mcd	60 mA Pk: 1 of 3 DF
	2820	I_V	3.7	25		mcd	20 mA DC
				38		mcd	60 mA Pk: 1 of 3 DF
	2835	I_V	7.5	50		mcd	20 mA DC
				75		mcd	60 mA Pk: 1 of 3 DF
	2855	I_V	7.5	50		mcd	20 mA DC
				75		mcd	60 mA Pk: 1 of 3 DF
	2870	I_V	7.5	50		mcd	20 mA DC
				75		mcd	60 mA Pk: 1 of 3 DF
	2885	I_V	15	100		mcd	20 mA DC
				150		mcd	60 mA Pk: 1 of 3 DF
Peak Wavelength		λ_{peak}		565		nm	
Dominant Wavelength[5]		λ_d		572		nm	
Forward Voltage Per LED		V_F		2.2	2.6	V	I_F = 20 mA
Reverse Breakdown Voltage Per LED		V_{BR}	6	15		V	I_R = 100 μA
Thermal Resistance LED Junction-to-Pin		$R\theta_{J-PIN}$		150		°C/W/ LED Chip	

NOTES:
4. These devices are categorized for luminous intensity with the intensity category designated by a letter code on the side of the package.
5. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and is that single wavelength which defines the color of the device. Yellow and green devices are categorized for dominant wavelength with the color bin designated by a letter code on the side of the package.

Electrical

The HLMP-2300/-2400/-2500/-2600/-2700/-2800 series of light bar devices are composed of two, four or eight light emitting diodes, with the light from each LED optically scattered to form an evenly illuminated light emitting surface. The LED's have a P-N junction diffused into the epitaxial layer on a GaP transparent substrate.

The anode and cathode of each LED is brought out by separate pins. This universal pinout arrangement allows for the wiring of the LED's within a device in any of three possible configurations: parallel, series, or series/parallel.

The typical forward voltage values, scaled from Figure 5, should be used for calculating the current limiting resistor values and typical power dissipation. Expected maximum V_F values for the purpose of driver circuit design and maximum power dissipation may be calculated using the following V_F models:

$$V_F = 1.8V + I_{PEAK}\,(40\Omega)$$
For $I_{PEAK} \geq 20mA$

$$V_F = 1.6V + I_{DC}\,(50\Omega)$$
For $5mA \leq I_{DC} \leq 20mA$

The maximum power dissipation can be calculated for any pulsed or DC drive condition. For DC operation, the maximum power dissipation is the product of the maximum forward voltage and the maximum forward current. For pulsed operation, the maximum power dissipation is the product of the maximum forward voltage at the peak forward current times the maximum average forward current. Maximum allowable power dissipation for any given ambient temperature and thermal resistance ($R\theta_{J-A}$) can be determined by using Figure 2. The solid line in Figure 2 ($R\theta_{J-A}$ of 538°C/W) represents a typical thermal resistance of a device socketed in a printed circuit board. The dashed lines represent achievable thermal resistances that can be obtained through improved thermal design. Once the maximum allowable power dissipation is determined, the maximum pulsed or DC forward current can be calculated.

Optical

The radiation pattern for these light bar devices is approximately Lambertian. The luminous sterance may be calculated using one of the two following formulas:

$$L_V\,(cd/m^2) = \frac{I_V\,(cd)}{A\,(m^2)}$$

$$L_V\,(\text{footlamberts}) = \frac{\pi I_V\,(cd)}{A\,(ft^2)}$$

Size of Light Emitting Area	Surface Area	
	Sq. Metres	Sq. Feet
8.89 mm x 8.89 mm	67.74×10^{-6}	729.16×10^{-6}
8.89 mm x 3.81 mm	33.87×10^{-6}	364.58×10^{-6}
8.89 mm x 19.05 mm	135.48×10^{-6}	1458.32×10^{-6}
3.81 mm x 19.05 mm	72.58×10^{-6}	781.25×10^{-6}

Refresh rates of 1 kHz or faster provide the most efficient operation resulting in the maximum possible time average luminous intensity.

The time average luminous intensity may be calculated using the relative efficiency characteristic of Figure 4, $\eta_{I_{PEAK}}$, and adjusted for operating ambient temperature. The time average luminous intensity at $T_A = 25°C$ is calculated as follows:

$$I_{V\ TIME\ AVG} = \left[\frac{I_{AVG}}{20mA}\right] (\eta_{I_{PEAK}})\,(I_V\ \text{Data Sheet})$$

Example: For HLMP-2735 series

$$\eta_{I_{PEAK}} = 1.18 \text{ at } I_{PEAK} = 48\ mA$$

$$I_{V\ TIME\ AVG} = \left[\frac{12mA}{20mA}\right]\ (1.18)\,(35\ mcd) = 25\ mcd$$

The time average luminous intensity may be adjusted for operating ambient temperature by the following exponential equation:

$$I_V\,(T_A) = I_V\,(25°C)\,e^{[K\,(T_A - 25°C)]}$$

Device	K
-2300/-2600 Series	-0.0131/°C
-2400/-2700 Series	-0.0112/°C
-2500/-2800 Series	-0.0104/°C

Example: $I_V\,(80°C) = (25\ mcd)e^{[-0.0112\,(80-25)]} = 14\ mcd$

These light bar devices may be operated in ambient temperatures above +60°C without derating when installed in a PC board configuration that provides a thermal resistance to ambient value less than 250°C/W/LED. See Figure 3 to determine the maximum allowed thermal resistance for the PC board, $R\theta_{PC-A}$, which will permit nonderated operation in a given ambient temperature.

To optimize device optical performance, specially developed plastics are used which restrict the solvents that may be used for cleaning. It is recommended that only mixtures of Freon (F113) and alcohol be used for vapor cleaning processes, with an immersion time in the vapors of less than two (2) minutes maximum. Some suggested vapor cleaning solvents are Freon TE, Genesolv DI-15 or DE-15, Arklone A or K. A 60°C (140°F) water cleaning process may also be used, which includes a neutralizer rinse (3% ammonia solution or equivalent), a surfactant rinse (1% detergent solution or equivalent), a hot water rinse and a thorough air dry. Room temperature cleaning may be accomplished with Freon T-E35 or T-P35, Ethanol, Isopropanol or water with a mild detergent.

Mechanical

These devices are constructed utilizing a lead frame in a DIP package. The LED dice are attached directly to the lead frame. Therefore, the cathode leads are the direct thermal and mechanical stress paths to the LED dice. The absolute maximum allowed junction temperature, $T_{J\,MAX}$, is 100°C. The maximum power ratings have been established so that the worst case V_F device does not exceed this limit. For most reliable operation, it is recommended that the device pin-to-ambient thermal resistance through the PC board be less than 250°C/W/LED. This will then establish a maximum thermal resistance LED junction-to-ambient of 400°C/W/LED.

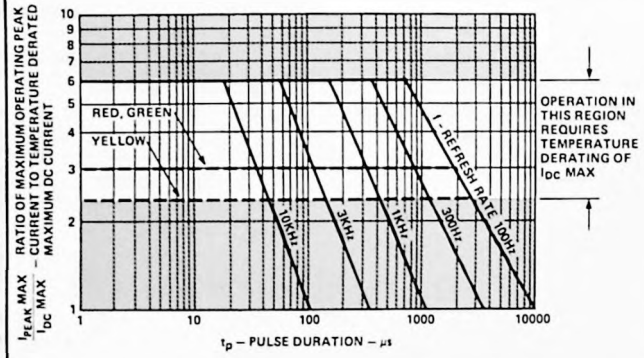


Figure 1. Maximum Allowed Peak Current vs. Pulse Duration.

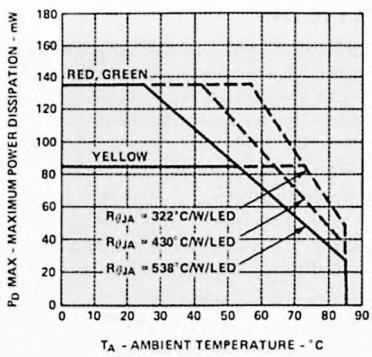


Figure 2. Maximum Allowable Power Dissipation per LED vs. Ambient Temperature Deratings Based on Maximum Allowable Thermal Resistance Values, LED Junction to Ambient on a per LED Basis, Tj MAX = 100° C.

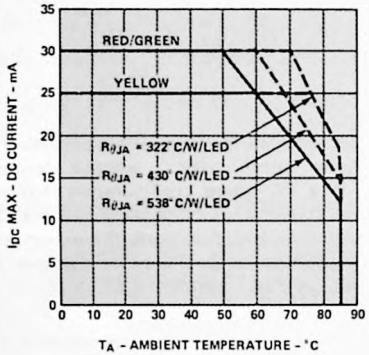


Figure 3. Maximum Allowable DC Current per LED vs. Ambient Temperature, Deratings Based on Maximum Allowable Thermal Resistance Values, LED Junction-to-Ambient on a per LED Basis, Tj MAX = 100° C.

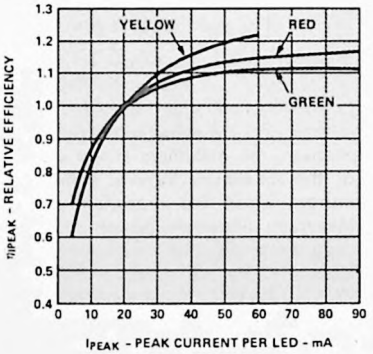


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak LED Current.

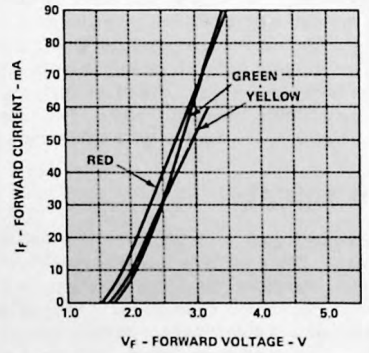


Figure 5. Forward Current vs. Forward Voltage Characteristics.

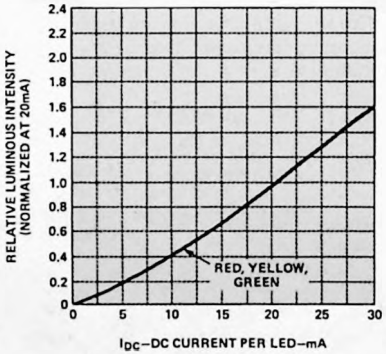


Figure 6. Relative Luminous Intensity vs. DC Forward Current.

For a Detailed Explanation on the Use of Data Sheet Information and Recommended Soldering Procedures, See Application Note 1005.

HEWLETT PACKARD

LED BICOLOR LIGHT BARS

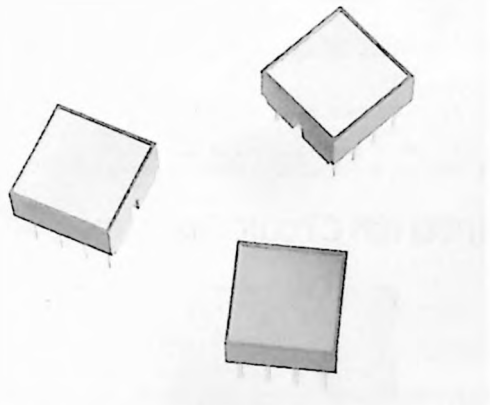
DIP — Single Light Emitting Area

HIGH EFFICIENCY RED/YELLOW HLMP-2950
HIGH EFFICIENCY RED/
HIGH PERFORMANCE GREEN HLMP-2965

TECHNICAL DATA JANUARY 1984

Features

- LARGE, BRIGHT, UNIFORM LIGHT EMITTING AREA
  8.89mm x 8.89mm (0.35 x 0.35 inch)
  Approximately Lambertian Radiation Pattern
- CHOICE OF TWO BICOLOR COMBINATIONS
- CATEGORIZED FOR LIGHT OUTPUT
- YELLOW AND GREEN CATEGORIZED FOR DOMINANT WAVELENGTH
- EXCELLENT ON-OFF CONTRAST
- EASILY MOUNTED ON P.C. BOARDS OR INDUSTRY STANDARD DIP SOCKETS
- MECHANICALLY RUGGED
- X-Y STACKABLE
- FLUSH MOUNTABLE
- CAN BE USED WITH HLMP-2898 PANEL AND LEGEND MOUNT
- LIGHT EMITTING SURFACE SUITABLE FOR LEGEND ATTACHMENT PER APPLICATION NOTE 1012
- I.C. COMPATIBLE



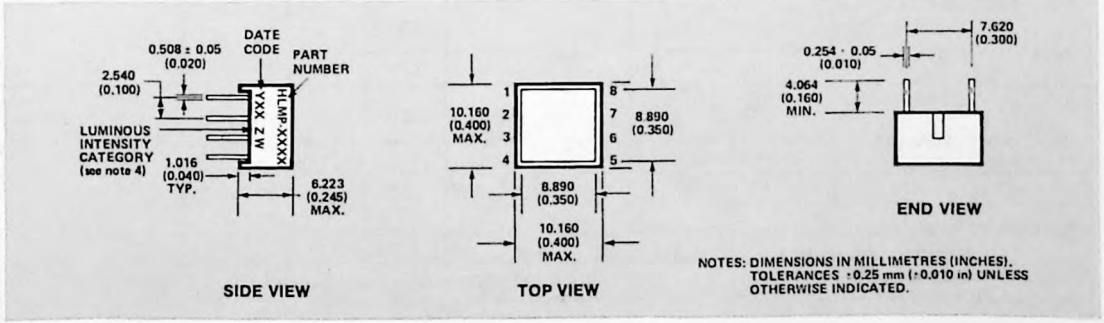
Applications

- TRISTATE LEGEND ILLUMINATION
- SPACE-CONSCIOUS FRONT PANEL STATUS INDICATORS
- BUSINESS MACHINE MESSAGE ANNUNCIATORS
- TELECOMMUNICATIONS INDICATORS
- TWO FUNCTION LIGHTED SWITCHES

Description

The HLMP-2950/-2965 light bars are bicolor light sources designed for a variety of applications where dual state or tristate illumination is required for the same annunciator function. In addition, both devices are capable of emitting a range of colors by pulse width modulation. These light bars are configured in dual-in-line packages which contain a single light emitting area. The high efficiency red (HER) and yellow LED chips utilize GaAsP on a transparent GaP substrate. The green LED chips utilize GaP on a transparent substrate.

Package Dimensions

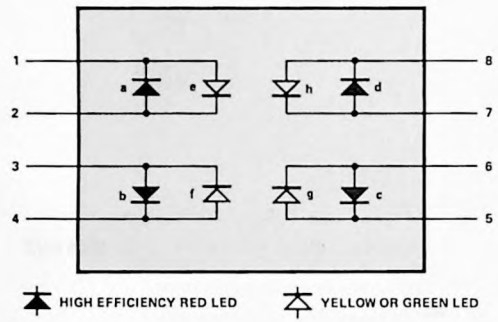


Absolute Maximum Ratings

Parameter	HLMP-2965	HLMP-2950
Average Power Dissipation per LED Chip[1]	135 mW	85 mW
Peak Forward Current per LED Chip, T_A = 50°C (Maximum Pulse Width = 2 ms)[1,2]	90 mA	60 mA
Time Average Forward Current per LED Chip, Pulsed Conditions[2]	25 mA, T_A = 25°C	20 mA, T_A = 50°C
DC Forward Current per LED Chip, T_A = 50°C[3]	30 mA	25 mA
Operating Temperature Range	-40°C to +85°C	
Storage Temperature Range	-40°C to +85°C	
Lead Soldering Temperature, 1.6 mm (1/16 inch) Below Seating Plane	260°C for 3 seconds	

NOTES:
1. For HLMP-2965, derate above T_A = 25°C at 1.8 mW/°C per LED chip. For HLMP-2950 derate above T_A = 50°C at 1.8 mW/°C per LED chip. See Figure 2.
2. See Figure 1 to establish pulsed operating conditions.
3. For HLMP-2965, derate above T_A = 50°C at 0.50 mA/°C per LED chip. For HLMP-2950, derate above T_A = 60°C at 0.50 mA/°C per LED chip. See Figure 3.

Internal Circuit Diagram



PIN	PIN FUNCTION	
	HER	YELLOW or GREEN
1	CATHODE a	ANODE e
2	ANODE a	CATHODE e
3	ANODE b	CATHODE f
4	CATHODE b	ANODE f
5	CATHODE c	ANODE g
6	ANODE c	CATHODE g
7	ANODE d	CATHODE h
8	CATHODE d	ANODE h

Electrical/Optical Characteristics at T_A = 25°C

HIGH EFFICIENCY RED/YELLOW HLMP-2950

Parameter		Symbol	Min.	Typ.	Max.	Units	Test Conditions
Luminous Intensity[4]	HER	I_V	9	20		mcd	20 mA DC
				30		mcd	60 mA Pk: 1 of 3 Duty Factor
	Yellow	I_V	8	12		mcd	20 mA DC
				20		mcd	60 mA Pk: 1 of 3 Duty Factor
Peak Wavelength	HER	λ_{PEAK}		635		nm	
	Yellow			583			
Dominant Wavelength[5]	HER	λ_d		626		nm	
	Yellow			585			
Forward Voltage	HER	V_F		2.1	2.6	V	I_F = 20 mA
	Yellow			2.2	2.6		
Thermal Resistance LED Junction-to-Pin		$R\theta_{J-PIN}$		150		°C/W/LED	

Electrical/Optical Characteristics at $T_A = 25°C$

HIGH EFFICIENCY RED/GREEN HLMP-2965

Parameter		Symbol	Min.	Typ.	Max.	Units	Test Conditions
Luminous Intensity [4]	HER	I_V	9	20		mcd	20 mA DC
				30		mcd	60 mA Pk: 1 of 3 Duty Factor
	Green	I_V	7.5	20		mcd	20 mA DC
				30		mcd	60 mA Pk: 1 of 3 Duty Factor
Peak Wavelength	HER	λ_{PEAK}		635		nm	
	Green			565			
Dominant Wavelength [5]	HER	λ_d		626		nm	
	Green			572			
Forward Voltage	HER	V_F		2.1	2.6	V	$I_F = 20$ mA
	Green			2.2	2.6		
Thermal Resistance LED Junction-to-Pin		$R\theta_{J-PIN}$		150		°C/W/LED	

NOTES:

4. These devices are categorized for luminous intensity with the intensity categorization designated by a two letter combination code located on the side of the package (Z = HER, W = Yellow or Green).
5. The dominant wavelength, λ_d, is derived from the C.I.E. chromaticity diagram and is that single wavelength which defines the color of the device.

Electrical

The HLMP-2950/-2965 bicolor light bar devices are composed of eight light emitting diodes: four High Efficiency Red and four that are either Yellow or Green. The light from each LED is optically scattered to form an evenly illuminated light emitting surface. The LED's are die attached and wire bonded in bicolor pairs, with the anode/cathode of each LED pair brought out by separate pins.

The typical forward voltage values, scaled from Figure 5, should be used for calculating the current limiting resistor values and typical power dissipation. Expected maximum V_F values for the purpose of driver circuit design and maximum power dissipation may be approximated using the following V_F models:

$$V_F = 1.8V + I_{PEAK}\,(40\Omega)$$
$$\text{For } I_{PEAK} \geq 20 \text{ mA}$$

$$V_F = 1.6V + I_{DC}\,(50\Omega)$$
$$\text{For } 5 \text{ mA} \leq I_{DC} \leq 20 \text{ mA}$$

The maximum power dissipation can be calculated for any pulsed or DC drive condition. For DC operation, the maximum power dissipation is the product of the maximum forward voltage and the maximum forward current. For pulsed operation, the maximum power dissipation is the product of the maximum forward voltage at the peak forward current times the maximum average forward current. Maximum allowable power dissipation for any given ambient temperature and thermal resistance ($R\theta_{J-A}$) can be determined by using Figure 2. The solid line in Figure 2 ($R\theta_{J-A}$ of 538° C/W) represents a typical thermal resistance of a device socketed in a printed circuit board. The dashed lines represent achievable thermal resistance that can be obtained through improved thermal design. Once the maximum allowable power dissipation is determined, the maximum pulsed or DC forward current can be calculated.

Optical

The radiation pattern for these light bar devices is approximately Lambertian. The luminous sterance may be calculated using one of the two following formulas:

$$L_V\,(\text{cd/m}^2) = \frac{I_V\,(\text{cd})}{A\,(\text{m}^2)} \qquad L_V\,(\text{footlamberts}) = \frac{\pi I_V\,(\text{cd})}{A\,(\text{ft}^2)}$$

where the area (A) of the light emitting surface is 67.74×10^{-6} m^2 (729.16×10^{-6} ft.^{2}).

For a Detailed Explanation on the Use of Data Sheet Information and Recommended Soldering Procedures, see Application Note 1005.

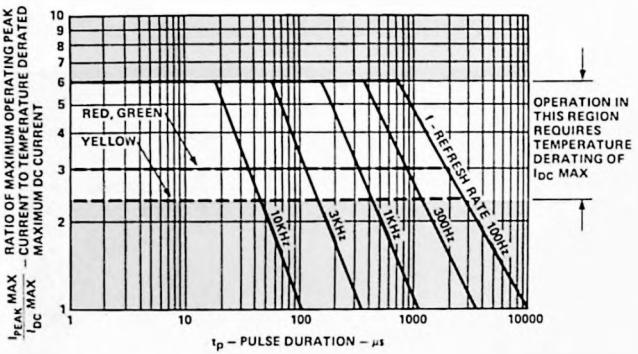


Figure 1. Maximum Allowed Peak Current vs. Pulse Duration.

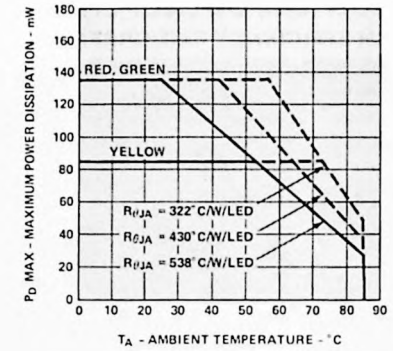


Figure 2. Maximum Allowable Power Dissipation per LED vs. Ambient Temperature. Deratings based on Maximum Allowable Thermal Resistance Values, LED Junction to Ambient on a per LED Basis, Tj MAX = 100° C.

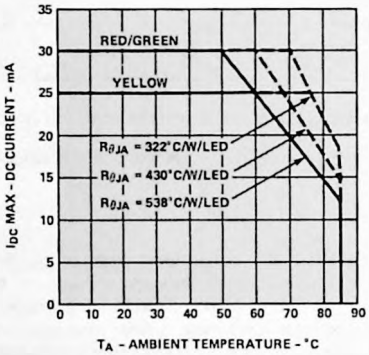


Figure 3. Maximum Allowable DC Current per LED vs. Ambient Temperature, Deratings Based on Maximum Allowable Thermal Resistance Values, LED Junction-to-Ambient on a per LED Basis, Tj MAX = 100° C.

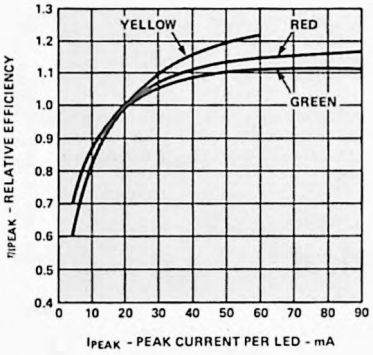


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak LED Current.

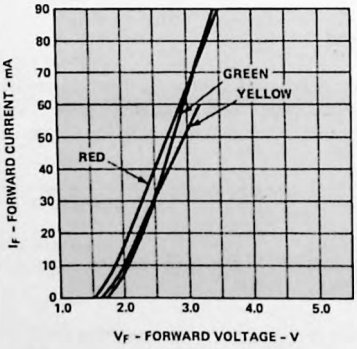


Figure 5. Forward Current vs. Forward Voltage Characteristics.

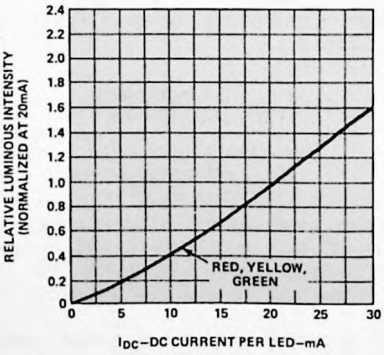


Figure 6. Relative Luminous Intensity vs. DC Forward Current.

Reversing Polarity LED Drivers

Bicolor LED light bar modules require a polarity reversing scheme to turn on the desired LED. Reversing line drivers, timers and memory drivers can be used to drive bicolor LED light bars.

The reversing line driver, which was originally designed to drive a data transmission line, can also be used as a polarity reversing driver for bicolor LED modules. The reversing line driver has a totem pole output structure that differs from most TTL circuits in that the output is designed to source as much current as it is capable of sinking.

Line drivers designed to operate from a single 5V supply are typically specified to source or sink 40 mA. Figure 7 shows the typical output characteristics of three different line drivers connected so that one output sources current across a load and the current is sunk by another output. This circuit is shown in Figure 8. At 40 mA output current, the output voltage typically varies from 2.4V (74128) to 2.9V (DM 8830, 9614) for $V_{CC} = 5.0V$. A basic bicolor LED circuit is shown in Figure 9. Since a line driver can supply 40 mA, it is capable of driving two LED pairs.

Some line drivers like the 9614 are constructed such that the sourcing output is brought out separately from the sinking output. With this type of line driver, the LED currents for each pair can be controlled separately. This technique is shown in Figure 10. Other line drivers provide a tri-state output control or provide other means for turning both LED's off. An example of this circuit technique is shown in Figure 11.

The NE556 dual timer, or two NE555 timers can also be used to drive bicolor light bars, as shown in Figure 12. The outputs at the NE555 timer are able to source or sink up to 200 mA. Connected as shown, each timer acts as an inverting buffer. This circuit has the advantage over the previous line driver circuits of being able to operate at a wide variety of power supply voltages ranging from 4.5 to 16 volts.

Memory drivers can also be used to drive bicolor light bars. Figure 13 shows a 75325 core memory driver being used to drive several pairs of bicolor LEDs. The 75325 is guaranteed to supply up to 600 mA of current with an output voltage considerably higher than 5V line drivers. The 75325 requires an additional 7.5V power supply at about 40 mA to properly bias the sourcing drivers. The 75325 allows tri-state (red, green or yellow, off) operation.

By employing pulse width modulation techniques to any of these circuits a range of colors can be obtained. This technique is illustrated in Figure 14.

Hewlett-Packard cannot assume responsibility for use of any circuitry described other than the circuitry entirely embodied in an HP product.

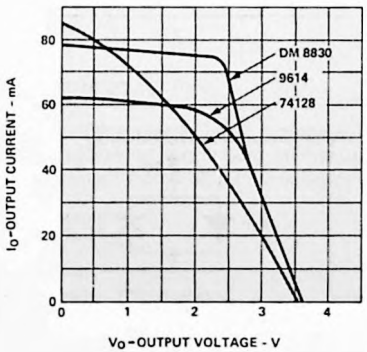


Figure 7. Typical Output Characteristics of Reversing Line Drivers.

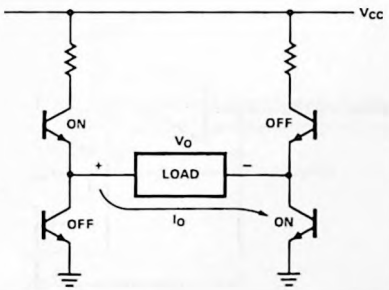


Figure 8. Line Driver Equivalent Circuit.

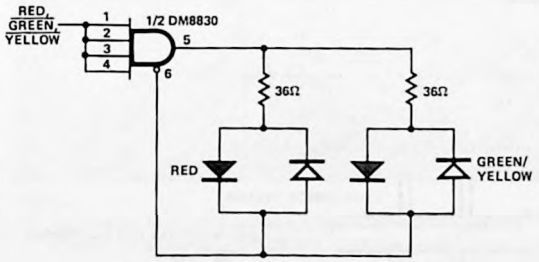


Figure 9. Typical Line Driver Circuit; Approximately 20mA/LED Pair.

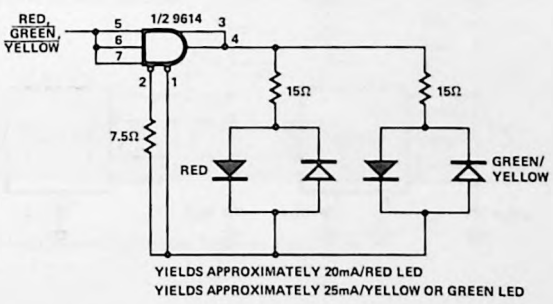


Figure 10. Techniques for Varying the Current of Each LED.

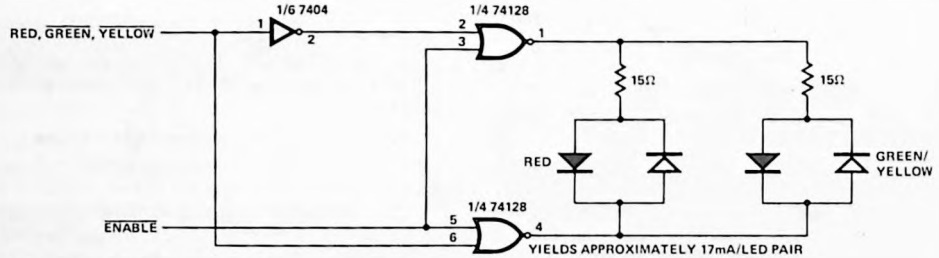


Figure 11. Tristate (Red, Green/Yellow, Off) Bicolor LED Driver.

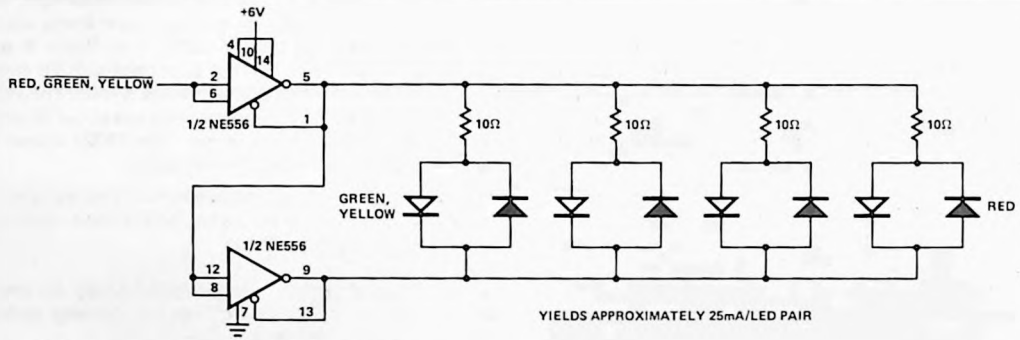


Figure 12. Use of Dual Timer to Drive Bicolor Light Bars

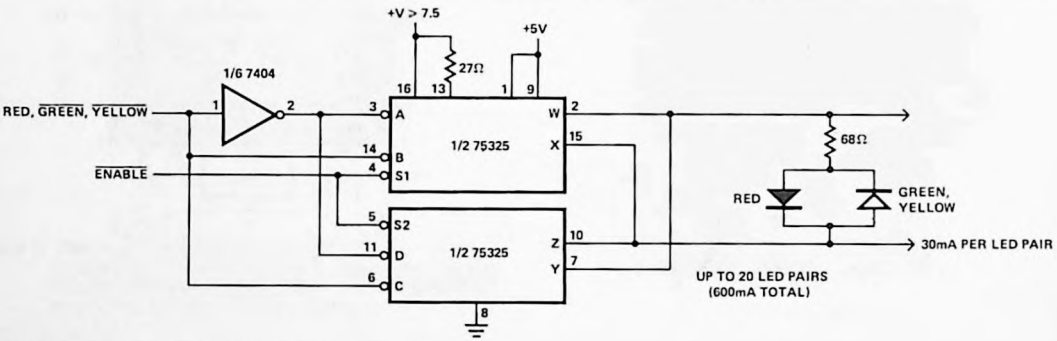


Figure 13. 75325 High Current Bicolor Driver

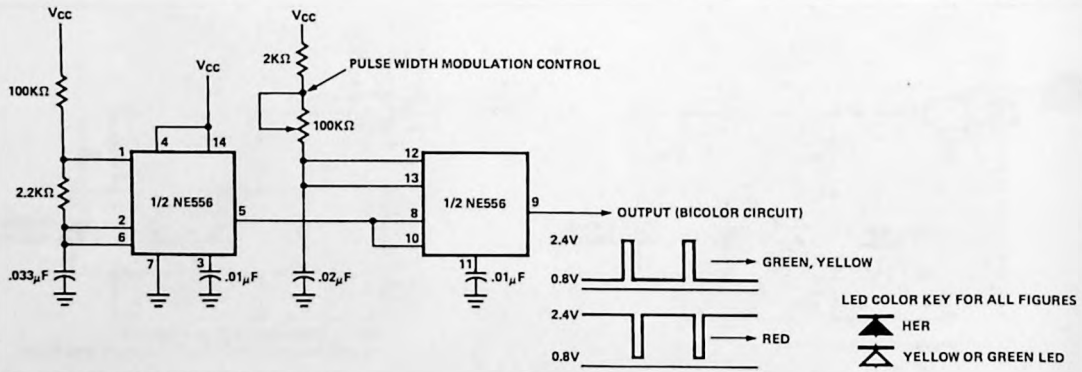


Figure 14. Pulse Width Modulation Technique

HEWLETT PACKARD

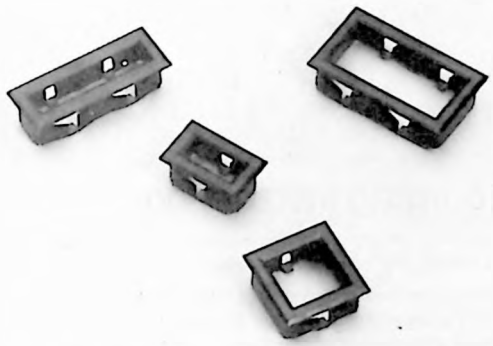
PANEL AND LEGEND MOUNTS FOR LED LIGHT BARS

HLMP-2598
HLMP-2599
HLMP-2898
HLMP-2899

TECHNICAL DATA JANUARY 1984

Features

- FIRMLY MOUNTS LIGHT BARS IN PANELS
- HOLDS LEGENDS FOR FRONT PANEL OR PC BOARD APPLICATIONS[1]
- ONE PIECE, SNAP-IN ASSEMBLY
- MATTE BLACK BEZEL DESIGN ENHANCES PANEL APPEARANCE
- FOUR SIZES AVAILABLE
- MAY BE INSTALLED IN A WIDE RANGE OF PANEL THICKNESSES
- PANEL HOLE EASILY PUNCHED OR MILLED



Description

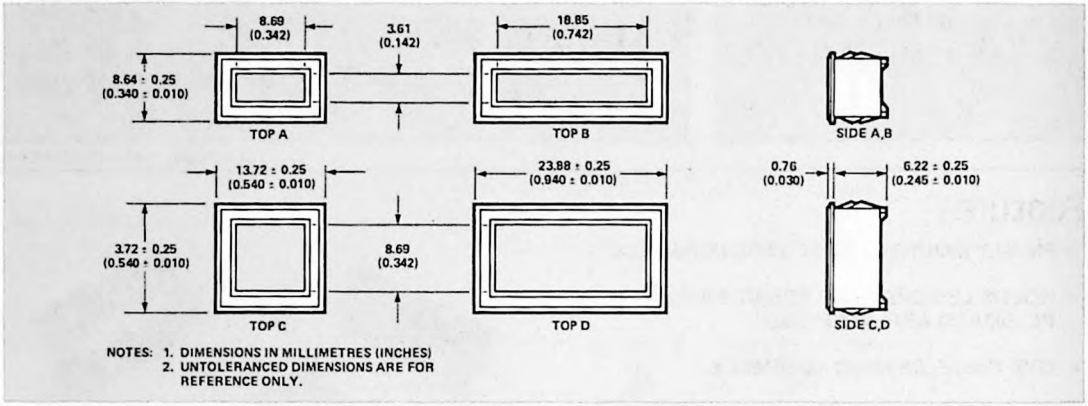
This series of black plastic bezel mounts is designed to install Hewlett-Packard Light Bars in instrument panels ranging in thickness from 1.52 mm (0.060 inch) to 3.18 mm (0.125 inch). A space has been provided for holding a 0.13 mm (0.005 inch) film legend over the light emitting surface of the light bar module.

Selection Guide

Panel and Legend Mount Part No. HLMP-	Corresponding Light Bar Module Part No. HLMP-	Panel Hole Installation Dimensions[2]	Package Outline	
2598	2350, 2450, 2550	7.62 mm (0.300 inch) x 22.86 mm (0.900 inch)		B
2599	2300, 2400, 2500	7.62 mm (0.300 inch) x 12.70 mm (0.500 inch)		A
2898	2600, 2700, 2800 2655, 2755, 2855 2950, 2965	12.70 mm (0.500 inch) x 12.70 mm (0.500 inch)		C
2899	2620, 2720, 2820 2635, 2735, 2835 2670, 2770, 2870 2685, 2785, 2885	12.70 mm (0.500 inch) x 22.86 mm (0.900 inch)		D

Notes:
1. Application Note 1012 addresses legend fabrication options.
2. Allowed hole tolerance: +0.00 mm, -0.13 mm (+0.000 inch, -0.005 inch). Permitted radius: 1.60 mm (0.063 inch).

Package Dimensions



NOTES: 1. DIMENSIONS IN MILLIMETRES (INCHES)
2. UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.

Mounting Instructions

1. Mill[3] or punch a hole in the panel. Deburr, but do not chamfer, the edges of the hole.
2. Place the front of the mount against a solid, flat surface. A film legend with outside dimensions equal to the outside dimensions of the light bar may be placed in the mount or on the light bar light emitting surface. Press the light bar into the mount until the tabs snap over the back of the light bar. (When inserting the HLMP-2898, align the notched sides of the light bar with the mount sides which do not have the tabs). (See Figure 1)
3. Applying even pressure to the top of the mount, press the entire assembly into the hole from the front of the panel.[4] (See Figure 2)

NOTE: For thinner panels, the mount may be pressed into the panel first, then the light bar may be pressed into the mount from the back side of the panel.

Notes:
3. A 3.18 mm (0.125 inch) diameter mill may be used.
4. Repetitive insertion of the mount into the panel will degrade the retention force of the mount.

Suggested Punch Sources

Hole punches may be ordered from one of the following sources:

Danly Machine Corporation
Punchrite Division
15400 Brookpark Road
Cleveland, OH 44135
(216) 267-1444

Ring Division
The Producto Machine Company
Jamestown, NY 14701
(800) 828-2216

Porter Precision Products Company
12522 Lakeland Road
Santa Fe Springs, CA 90670
(213) 946-1531

Di-Acro Division
Houdaille Industries
800 Jefferson Street
Lake City, MN 55041
(612) 345-4571

Installation Sketches

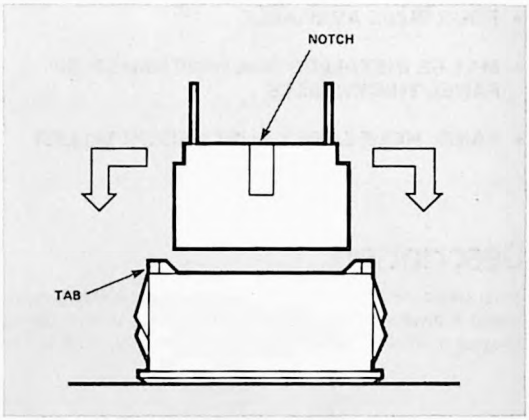


Figure 1. Installation of a Light Bar into a Panel Mount

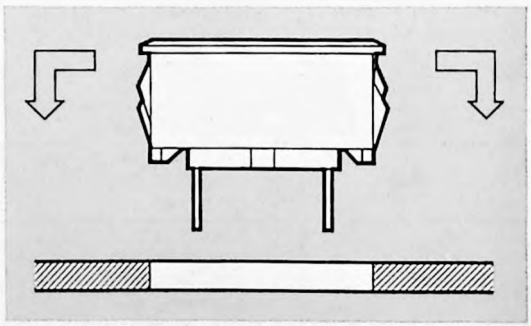


Figure 2. Installation of the Light Bar/Panel Mount Assembly into a Front Panel

HEWLETT PACKARD

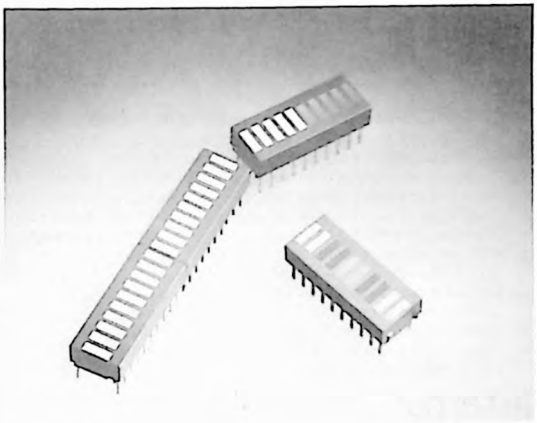
10-ELEMENT BAR GRAPH ARRAY

RED HDSP-4820
HIGH-EFFICIENCY RED HDSP-4830
YELLOW HDSP-4840
HIGH PERFORMANCE GREEN HDSP-4850
MULTICOLOR HDSP-4832
MULTICOLOR HDSP-4836

TECHNICAL DATA JANUARY 1984

Features

- CUSTOM MULTICOLOR ARRAY CAPABILITY
- MATCHED LEDs FOR UNIFORM APPEARANCE
- END STACKABLE
- PACKAGE INTERLOCK ENSURES CORRECT ALIGNMENT
- LOW PROFILE PACKAGE
- RUGGED CONSTRUCTION— RELIABILITY DATA SHEETS AVAILABLE
- LARGE, EASILY RECOGNIZABLE SEGMENTS
- HIGH ON-OFF CONTRAST, SEGMENT TO SEGMENT
- WIDE VIEWING ANGLE
- CATEGORIZED FOR LUMINOUS INTENSITY
- HDSP-4832/-4836/-4840/-4850 CATEGORIZED FOR DOMINANT WAVELENGTH



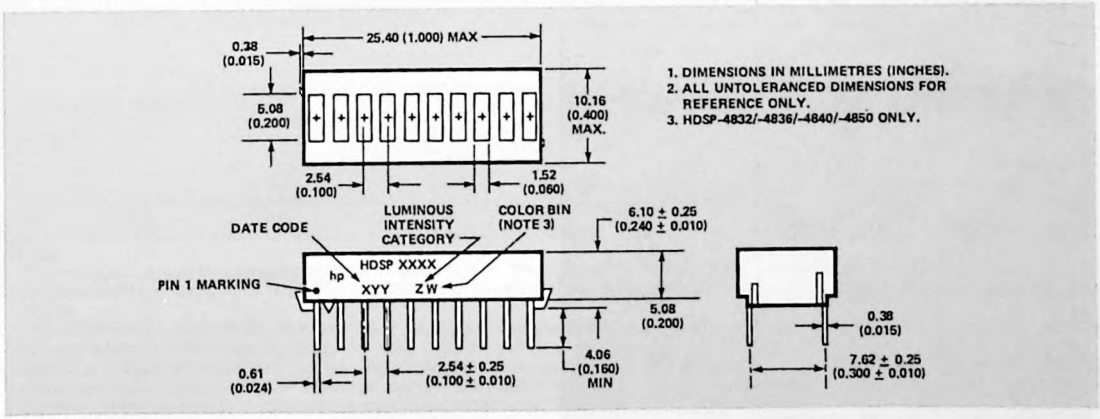
Applications

- INDUSTRIAL CONTROLS
- INSTRUMENTATION
- OFFICE EQUIPMENT
- COMPUTER PERIPHERALS
- CONSUMER PRODUCTS

Description

These 10-element LED arrays are designed to display information in easily recognizable bar graph form. The packages are end stackable and therefore capable of displaying long strings of information. Use of these bar graph arrays eliminates the alignment, intensity, and color matching problems associated with discrete LEDs. The HDSP-4820/-4830/-4840/-4850 each contain LEDs of just one color. The HDSP-4832/-4836 are multicolor arrays with High-Efficiency Red, Yellow, and Green LEDs in a single package. CUSTOM MULTICOLOR ARRAYS ARE AVAILABLE WITH MINIMUM DELIVERY REQUIREMENTS. CONTACT YOUR LOCAL DISTRIBUTOR OR HP SALES OFFICE FOR DETAILS.

Package Dimensions



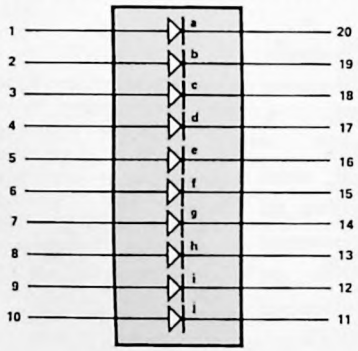
Absolute Maximum Ratings[9]

Parameter	HDSP-4820	HDSP-4830	HDSP-4840	HDSP-4850
Average Power Dissipation per LED (T_A = 25° C)[1]	125 mW	125 mW	125 mW	125 mW
Peak Forward Current per LED	150 mA[2]	90 mA[3]	60 mA[3]	90 mA[3]
DC Forward Current per LED	30 mA[4]	30 mA[5]	20 mA[6]	30 mA[7]
Operating Temperature Range	-40° C to +85° C			
Storage Temperature Range	-40° C to +85° C			
Reverse Voltage per LED	3.0 V			
Lead Soldering Temperature (1.59 mm (1/16 inch) below seating plane)[8]	260° C for 3 sec			

NOTES:

1. Derate maximum average power above T_A = 25° C at 1.67 mW/° C. This derating assumes worst case $R\Theta_{J-A}$ = 600° C/W/LED.
2. See Figure 1 to establish pulsed operating conditions.
3. See Figure 6 to establish pulsed operating conditions.
4. Derate maximum DC current above T_A = 63° C at 0.81 mA/° C per LED. This derating assumes worst case $R\Theta_{J-A}$ = 600° C/W/LED. With an improved thermal design, operation at higher temperatures without derating is possible. See Figure 2.
5. Derate maximum DC current above T_A = 50° C at 0.6 mA/° C per LED. This derating assumes worst case $R\Theta_{J-A}$ = 600° C/W/LED. With an improved thermal design, operation at higher temperatures without derating is possible. See Figure 7.
6. Derate maximum DC current above T_A = 70° C at 0.67 mA/° C per LED. This derating assumes worst case $R\Theta_{J-A}$ = 600° C/W/LED. With an improved thermal design, operation at higher temperatures without derating is possible. See Figure 8.
7. Derate maximum DC current above T_A = 37° C at 0.48 mA/° C per LED. This derating assumes worst case $R\Theta_{J-A}$ = 600° C/W/LED. With an improved thermal design, operation at higher temperatures without derating is possible. See Figure 9.
8. Clean only in water, Isopropanol, Ethanol, Freon TF or TE (or equivalent) and Genesolve DI-15 (or equivalent).
9. Absolute maximum ratings for the HER, Yellow, and Green elements of the multicolor arrays are identical to the HDSP-4830/-4840/-4850 maximum ratings.

Internal Circuit Diagram



Pin	Function	Pin	Function
1	Anode a	11	Cathode j
2	Anode b	12	Cathode i
3	Anode c	13	Cathode h
4	Anode d	14	Cathode g
5	Anode e	15	Cathode f
6	Anode f	16	Cathode e
7	Anode g	17	Cathode d
8	Anode h	18	Cathode c
9	Anode i	19	Cathode b
10	Anode j	20	Cathode a

Multicolor Array Segment Colors

Segment	HDSP-4832 Segment Color	HDSP-4836 Segment Color
a	HER	HER
b	HER	HER
c	HER	Yellow
d	Yellow	Yellow
e	Yellow	Green
f	Yellow	Green
g	Yellow	Yellow
h	Green	Yellow
i	Green	HER
j	Green	HER

Electrical/Optical Characteristics at $T_A = 25°C$[4]

RED HDSP-4820

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity per LED (Unit Average)[1]	I_F	I_F = 20 mA	610	1250		µcd
Peak Wavelength	λ_{PEAK}			655		nm
Dominant Wavelength[2]	λ_d			645		nm
Forward Voltage per LED	V_F	I_F = 20 mA		1.6	2.0	V
Reverse Voltage per LED	V_R	I_R = 100 µA	3	12[5]		V
Temperature Coefficient V_F per LED	$\Delta V_F/°C$			-2.0		mV/°C
Thermal Resistance LED Junction-to-Pin	$R_{\Theta J-PIN}$			300		°C/W/ LED

HIGH-EFFICIENCY RED HDSP-4830

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity per LED (Unit Average)[1]	I_V	I_F = 10 mA	750	2280		µcd
Peak Wavelength	λ_{PEAK}			635		nm
Dominant Wavelength[2]	λ_d			626		nm
Forward Voltage per LED	V_F	I_F = 20 mA		2.1	2.5	V
Reverse Voltage per LED	V_R	I_R = 100 µA	3	30[5]		V
Temperature Coefficient V_F per LED	$\Delta V_F/°C$			-2.0		mV/°C
Thermal Resistance LED Junction-to-Pin	$R_{\Theta J-PIN}$			300		°C/W/ LED

YELLOW HDSP-4840

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity per LED (Unit Average)[1]	I_V	I_F = 10 mA	600	1900		µcd
Peak Wavelength	λ_{PEAK}			583		nm
Dominant Wavelength[2,3]	λ_d		581	585	592	nm
Forward Voltage per LED	V_F	I_F = 20 mA		2.2	2.5	V
Reverse Voltage per LED	V_R	I_R = 100 µA	3	40[5]		V
Temperature Coefficient V_F per LED	$\Delta V_F/°C$			-2.0		mV/°C
Thermal Resistance LED Junction-to-Pin	$R_{\Theta J-PIN}$			300		°C/W/ LED

GREEN HDSP-4850

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity per LED (Unit Average)[1]	I_V	I_F = 10 mA	600	1900		µcd
Peak Wavelength	λ_{PEAK}			566		nm
Dominant Wavelength[2,3]	λ_d			571	577	nm
Forward Voltage per LED	V_F	I_F = 10 mA		2.1	2.5	V
Reverse Voltage per LED	V_R	I_R = 100 µA	3	50[5]		V
Temperature Coefficient V_F per LED	$\Delta V_F/°C$			-2.0		mV/°C
Thermal Resistance LED Junction-to-Pin	$R_{\Theta J-PIN}$			300		°C/W/ LED

NOTES:

1. The bar graph arrays are categorized for luminous intensity. The category is designated by a letter located on the side of the package.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and is that single wavelength which defines the color of the device.
3. The HDSP-4832/-4836/-4840/-4850 bar graph arrays are categorized by dominant wavelength with the category designated by a number adjacent to the intensity category letter. Only the yellow elements of the HDSP-4832/-4836 are categorized for color.
4. Electrical/optical characteristics of the High-Efficiency Red elements of the HDSP-4832/-4836 are identical to the HDSP-4830 characteristics. Characteristics of Yellow elements of the HDSP-4832/-4836 are identical to the HDSP-4840. Characteristics of Green elements of the HDSP-4832/-4836 are identical to the HDSP-4850.
5. Reverse voltage per LED should be limited to 3.0 V Max.

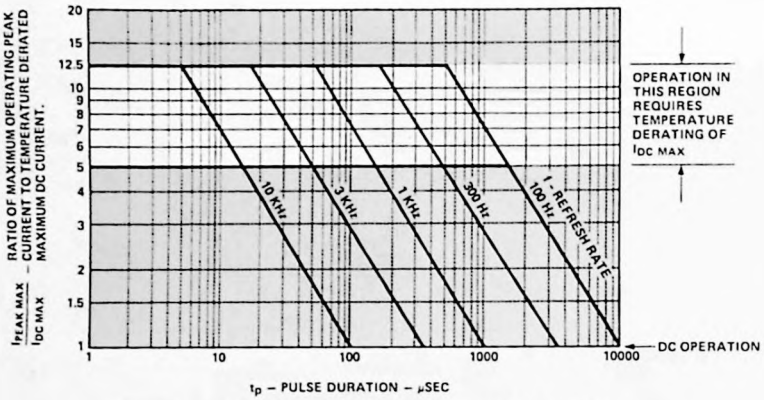


Figure 1. Maximum Tolerable Peak Current vs. Pulse Duration

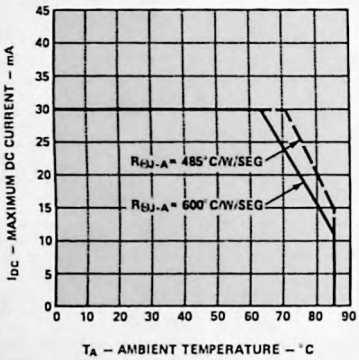


Figure 2. Maximum Allowable D.C. Current per LED vs. Ambient Temperature. Deratings based on Maximum Allowable Thermal Resistance, LED Junction-to-Ambient on a per LED basis. $T_{JMAX} = 100°C$

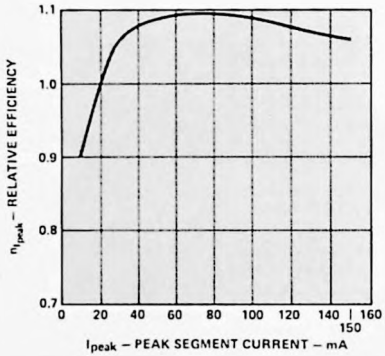


Figure 3. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Segment Current

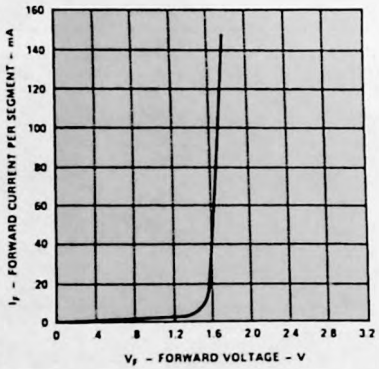


Figure 4. Forward Current vs. Forward Voltage

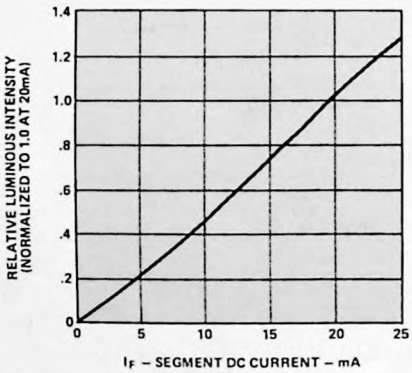


Figure 5. Relative Luminous Intensity vs. D.C. Forward Current

For a Detailed Explanation on the Use of Data Sheet Information and Recommended Soldering Procedures, See Application Note 1005.

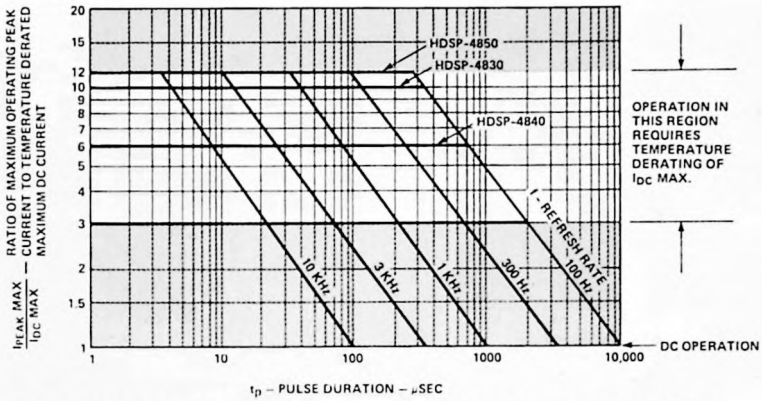


Figure 6. HDSP-4830/-4840/-4850 Maximum Tolerable Peak Current vs. Pulse Duration

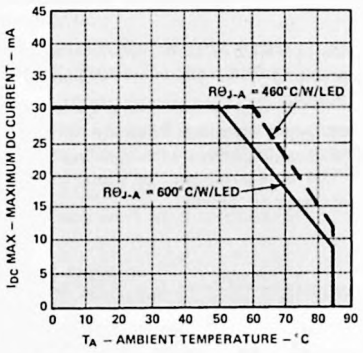


Figure 7. HDSP-4830 Maximum Allowable D.C. Current per LED vs. Ambient Temperature. Deratings Based on Maximum Allowable Thermal Resistance Values, LED Junction-to-Ambient on a per LED basis. $T_{J\ MAX} = 100°C$.

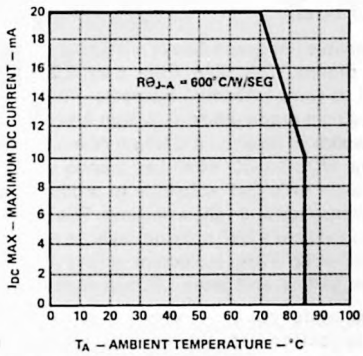


Figure 8. HDSP-4840 Maximum Allowable D.C. Current per LED vs. Ambient Temperature. Deratings Based on Maximum Allowable Thermal Resistance Values, LED Junction-to-Ambient on a per LED basis. $T_{J\ MAX} = 100°C$.

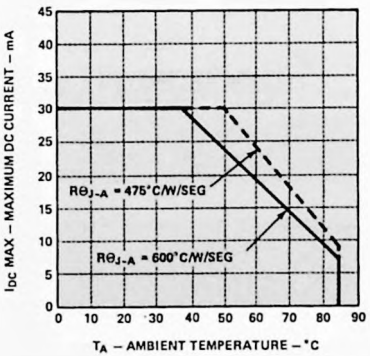


Figure 9. HDSP-4850 Maximum Allowable D.C. Current per LED vs. Ambient Temperature. Deratings Based on Maximum Allowable Thermal Resistance Values, LED Junction-to-Ambient on a per LED basis. $T_{J\ MAX} = 100°C$.

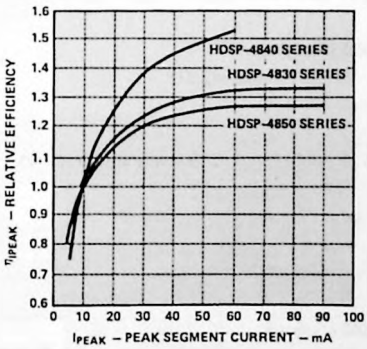


Figure 10. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Segment Current

For a Detailed Explanation on the Use of Data Sheet Information and Recommended Soldering Procedures, See Application Note 1005.

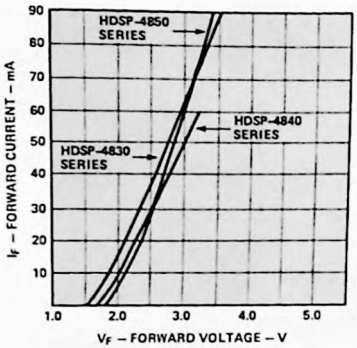


Figure 11. Forward Current vs. Forward Voltage

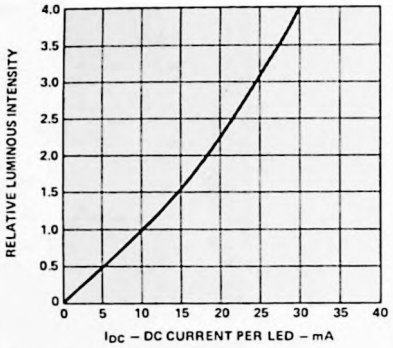


Figure 12. HDSP-4830/-4840/-4850 Relative Luminous Intensity vs. D.C. Forward Current

Electrical

These versatile bar graph arrays are composed of ten light emitting diodes. The light from each LED is optically stretched to form individual elements. The diodes in the HDSP-4820 bar graph utilize a Gallium Arsenide Phosphide (GaAsP) epitaxial layer on a Gallium Arsenide (GaAs) Substrate. The HDSP-4830/-4840 bar graphs utilize a GaAsP epitaxial layer on a GaP substrate to produce the brighter high-efficiency red and yellow displays. The HDSP-4850 bar graph array utilizes a GaP epitaxial layer on a GaP substrate. The HDSP-4832/-4836 multicolor arrays have high efficiency red, yellow, and green LEDs in one package.

These display devices are designed to allow strobed operation. The typical forward voltage values, scaled from Figure 4 or 11, should be used for calculating the current limiting resistor value and typical power dissipation. Expected maximum V_F values, for the purpose of driver circuit design and maximum power dissipation, may be calculated using the following $V_{F\,MAX}$ models.

HDSP-4820 (Red)

$V_{F\,MAX} = 1.75\ V + I_{PEAK}\ (12.5\Omega)$
For: $I_{PEAK} \geq 5$ mA

HDSP-4830/-4840 (High Efficiency Red/Yellow)

$V_{F\,MAX} = 1.75V + I_{PEAK}\ (38\Omega)$
For $I_{PEAK} \geq 20$ mA

$V_{F\,MAX} = 1.6V + I_{DC}\ (45\Omega)$
For: $5\ mA \leq I_{DC} \leq 20$ mA

HDSP-4850 (Green)

$V_{F\,MAX} = 2.0V + I_{PEAK}\ (50\Omega)$
For: $I_{PEAK} > 5$ mA

Refresh rates of 1 KHz or faster provide the most efficient operation resulting in the maximum possible time averaged luminous intensity.

The time averaged luminous intensity may be calculated using the relative efficiency characteristic shown in Figures 3 and 10. The time averaged luminous intensity at $T_A = 25°C$ is calculated as follows:

$$I_{V\,TIME\,AVG} = \left[\frac{I_{F\,AVG}}{I_{F\,SPEC\,AVG}}\right] (\eta I_{PEAK})\ (I_{V\,SPEC})\ .$$

Example: For HDSP-4830 operating at $I_{PEAK} = 50$ mA, 1 of 4 Duty Factor

$$\eta I_{PEAK} = 1.35\ (\text{at } I_{PEAK} = 50\ mA)$$

$$I_{V\,TIME\,AVG} = \left[\frac{12.5\ mA}{10\ mA}\right] (1.35)\ 2280\ \mu cd = 3847\ \mu cd$$

For Further Information Concerning Bar Graph Arrays and Suggested Drive Circuits, Consult HP Application Note 1007 Entitled "Bar Graph Array Applications".

HEWLETT PACKARD

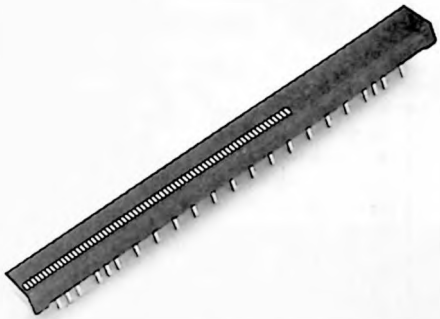
101 ELEMENT BAR GRAPH ARRAY

RED HDSP-8820

TECHNICAL DATA JANUARY 1984

Features

- **EXCELLENT RESOLUTION (1%)**
- **EXCELLENT ELEMENT APPEARANCE**
  Wide, Easily Recognizable Elements
  Matched LEDs for Uniformity
  Excellent Element Alignment
  Easy Readability at 1 Meter
- **SINGLE-IN-LINE PACKAGE DESIGN**
  Sturdy Leads on Industry Standard 2.54mm (0.100") Centers
  Environmentally Rugged Package
  Common Cathode Configuration
- **LOW POWER REQUIREMENTS**
  As low as 1.0 - 1.5 mA average per element depending on Peak Current Levels.
- **SUPPORT ELECTRONICS**
  Easy Interface with Microprocessors



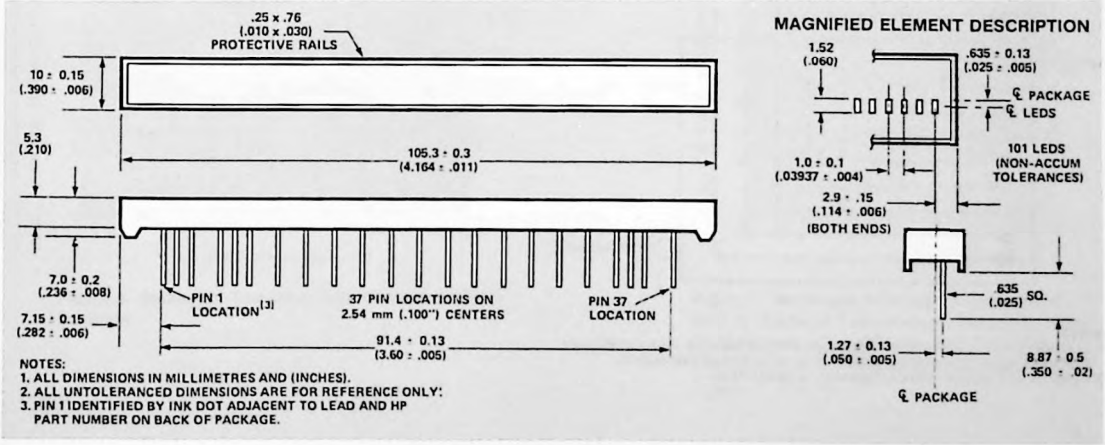
Description

The HDSP-8820 is a 101-element monolithic LED linear array. It is designed to display information in easily recognizable bar graph or position indicator form. The device utilizes GaAsP LED chips assembled on a PC board which is enclosed in a red polycarbonate cover with an epoxy backfill seal. The common cathode chips are addressed via 22 single-in-line pins extending from the back side of the package.

Applications

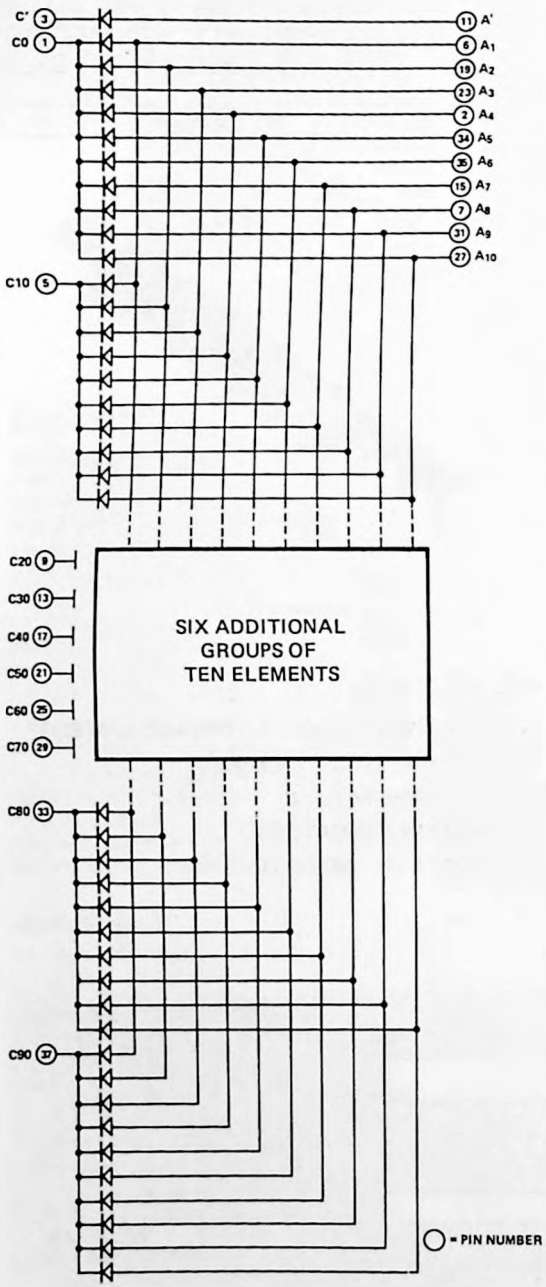
- **INDUSTRIAL PROCESS CONTROL SYSTEMS**
- **EDGEWISE PANEL METERS**
- **INSTRUMENTATION**
- **POSITION INDICATORS**
- **FLUID LEVEL INDICATORS**

Package Dimensions [1, 2]



NOTES:
1. ALL DIMENSIONS IN MILLIMETRES AND (INCHES).
2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
3. PIN 1 IDENTIFIED BY INK DOT ADJACENT TO LEAD AND HP PART NUMBER ON BACK OF PACKAGE.

Internal Circuit Diagram [4, 5]



NOTES:
4. ELEMENT LOCATION NUMBER = COMMON CATHODE NUMBER + ANODE NUMBER. FOR EXAMPLE, ELEMENT 83 IS OBTAINED BY ADDRESSING C80 AND A3.
5. A' AND C' ARE ANODE AND CATHODE OF ELEMENT ZERO.

Device Pin Description

PIN LOCATION	FUNCTION
1	C0
2	A4
3	C' [5]
4	No Pin
5	C10
6	A1
7	A8
8	No Pin
9	C20
10	No Pin
11	A' [5]
12	No Pin
13	C30
14	No Pin
15	A7
16	No Pin
17	C40
18	No Pin
19	A2
20	No Pin
21	C50
22	No Pin
23	A3
24	No Pin
25	C60
26	No Pin
27	A10
28	No Pin
29	C70
30	No Pin
31	A9
32	No Pin
33	C80
34	A5
35	A6
36	No Pin
37	C90

Absolute Maximum Ratings

Parameter	HDSP-8820
Average Power per Element, T_A = 25° C	15 mW
Peak Forward Current per Element, T_A = 25° C (Maximum Pulse Width = 300 μs)[6]	200 mA
Average Forward Current per Element, T_A = 25° C[7]	7 mA
Operating Temperature Range	-40° C to +85° C
Storage Temperature Range	-40° C to +85° C
Reverse Voltage per Element	5V
Lead Solder Temperature, 1.59 mm (1/16 inch) Below Seating Plane[8]	260° C for 3 seconds

NOTE:
6. See Figure 1 to establish pulsed operating conditions.
7. Derate maximum average forward current above T_A = 70° C at 0.16 mA/° C per element. See Figure 2.
8. Clean only in water, Isopropanol, Ethanol, Freon TF or TE (or equivalent), or Genesolv DI-15 or DE-15 (or Equivalent). See mechanical section of this data sheet for information on wave soldering conditions.

Electrical/Optical Characteristics at T_A = 25°C

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Time averaged Luminous Intensity per Element (Unit average)[9]	IV	100 mA Pk.: 1 of 110 Duty Factor	8	20		μcd
Peak Wavelength	λ_{PEAK}			655		nm
Dominant Wavelength[10]	λ_d			640		nm
Forward Voltage per Element	V_F	I_F = 100 mA		1.7	2.1	V
Reverse Voltage per Element	V_R	I_R = 100 μA	3.0			V
Temperature Coefficient V_F per Element	ΔV_F/° C			-2.0		mV/° C
Thermal Resistance LED Junction-to-Pin	$R\Theta_{J-PIN}$			700		° C/W/ LED

Notes:
9. Operation at peak currents of less than 15 mA is not recommended. Display aesthetics are specified at 100 mA, 1 of 110 DF.
10. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and is that single wavelength which defines the color of the device.

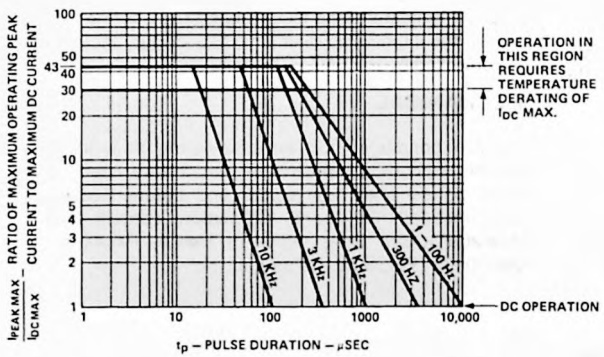


Figure 1. Maximum Tolerable Peak Current vs. Pulse Duration

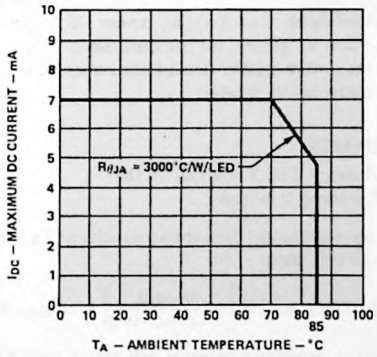


Figure 2. Maximum Allowable D.C. Current per LED vs. Ambient Temperature. Deratings based on Maximum Allowable Thermal Resistance, LED Junction-to-Ambient on a per LED basis. T_{JMAX} = 115° C

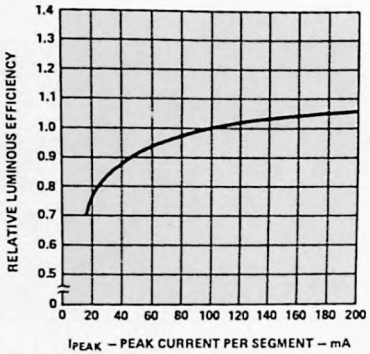


Figure 3. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Segment Current

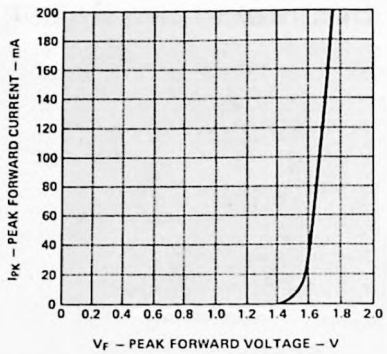


Figure 4. Forward Current vs. Forward Voltage

For A Detailed Explanation on the Use of Data Sheet Information, See Application Note 1005.

Operational Considerations

ELECTRICAL

The HDSP-8820 is a 101 element monolithic bar graph array. The device utilizes GaAsP red LED chips assembled on a PC board which is enclosed in a red polycarbonate cover with an epoxy backfill seal. The linear array is arranged as ten groups of ten LED elements plus one additional element. The ten elements of each group have common cathodes. Like lements in the ten groups have common anodes. The device is addressed via 22 single-in-line pins extending from the back side of the display.

This display is designed specifically for strobed (multiplexed) operation. Minimum peak forward current at which all elements will be illuminated is 15 mA, 1/110 DF. Display aesthetics are specified at 100 mA, 1/110 DF, peak forward current. The typical forward voltage values, scaled from Figure 4, should be used for calculating the current limiting resistor value and typical power dissipation. Expected maximum V_F values, for the purpose of driver circuit design and maximum power dissipation, may be calculated using the following V_F model:

HDSP-8820

$V_{FMAX} = 2.02\ V + I_{PEAK}\ (.8\ \Omega)$
For $I_{PEAK} > 40$ mA

The time averaged luminous intensity at $T_A = 25°C$ may be calculated using:

$$I_V \text{ Time Avg.} = \left[\frac{I_{F\text{-}AVG}}{I_{F\text{-}SPEC\text{-}AVG}}\right] \bullet \eta I_{PEAK} \bullet I_{V\text{-}SPEC}$$

where η, relative luminous efficiency may be determined from Figure 3.

The circuit in Figure 5 displays binary weighted input in bar graph form with 101 bit resolution. Central to the design is a 74390 100 count decade counter. The "1's" output from the counter drives the display element anodes through a 7442 1 of 10 BCD decoder. Sprague UDN 2585 drivers boost peak current. The "10's" output from the counter drives the group cathodes through a 74145 1 of 10 BCD decoder. A 74393 seven bit binary counter follows the decade counter and is reset after each 100 counts. A 74LS85 binary comparator looks at inputs from the binary counter and external circuitry. The comparator output disables the display when the binary count exceeds the binary weighted input. The first display element is DC driven.

The circuit in Figure 6 uses the HDSP-8820 as a 100 bit position indicator. Two BCD input words define the position of the illuminated element. Display duty factor, 1/100, is controlled by the $\overline{\text{ENABLE}}$ signal.

MECHANICAL

Suitable conditions for wave soldering depend on the specific kind of equipment and procedure used. A cool down period after flow solder and before flux rinse is recommended. For more information, consult the local Hewlett-Packard Sales Office or Hewlett-Packard Optoelectronics, Palo Alto, California.

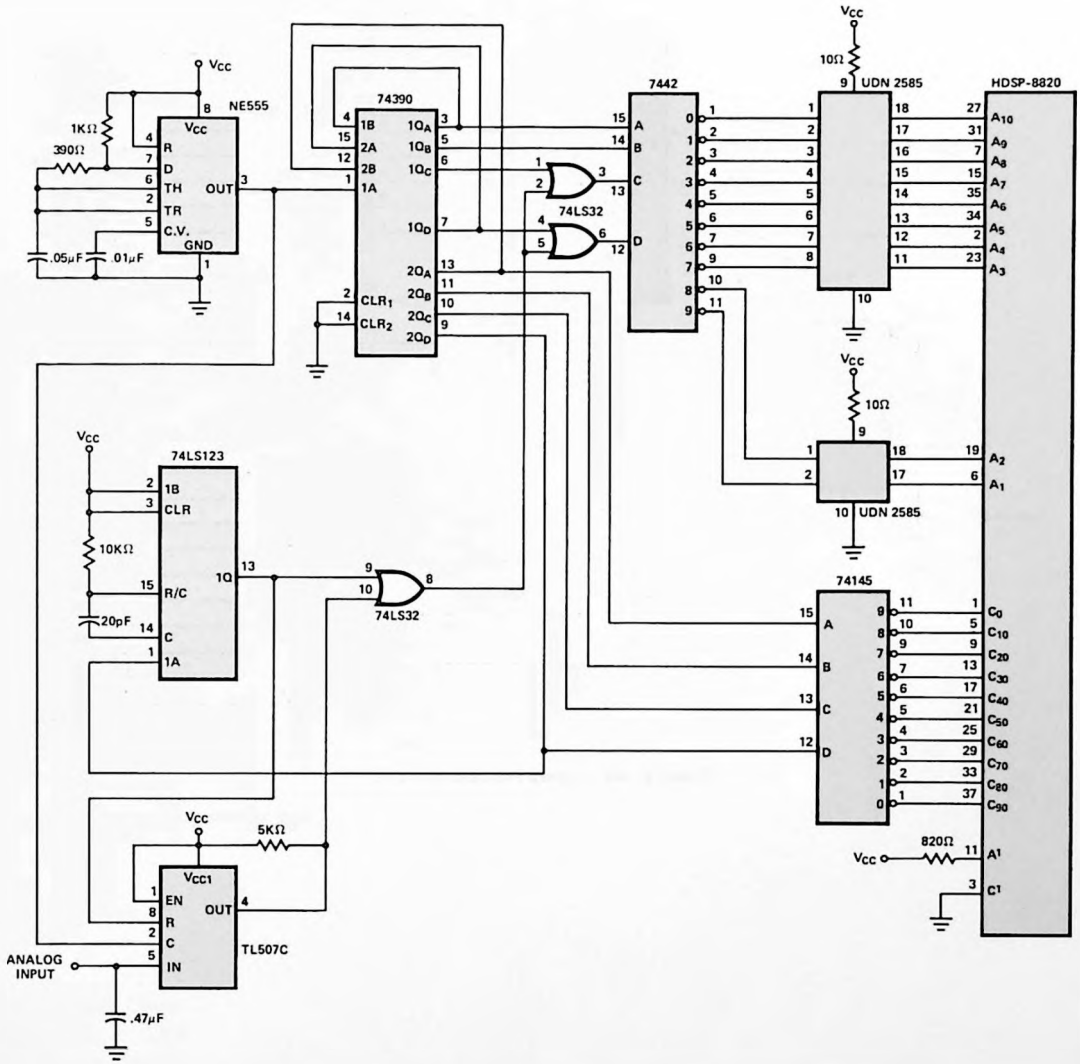


Figure 5. 101 Element Bar Graph

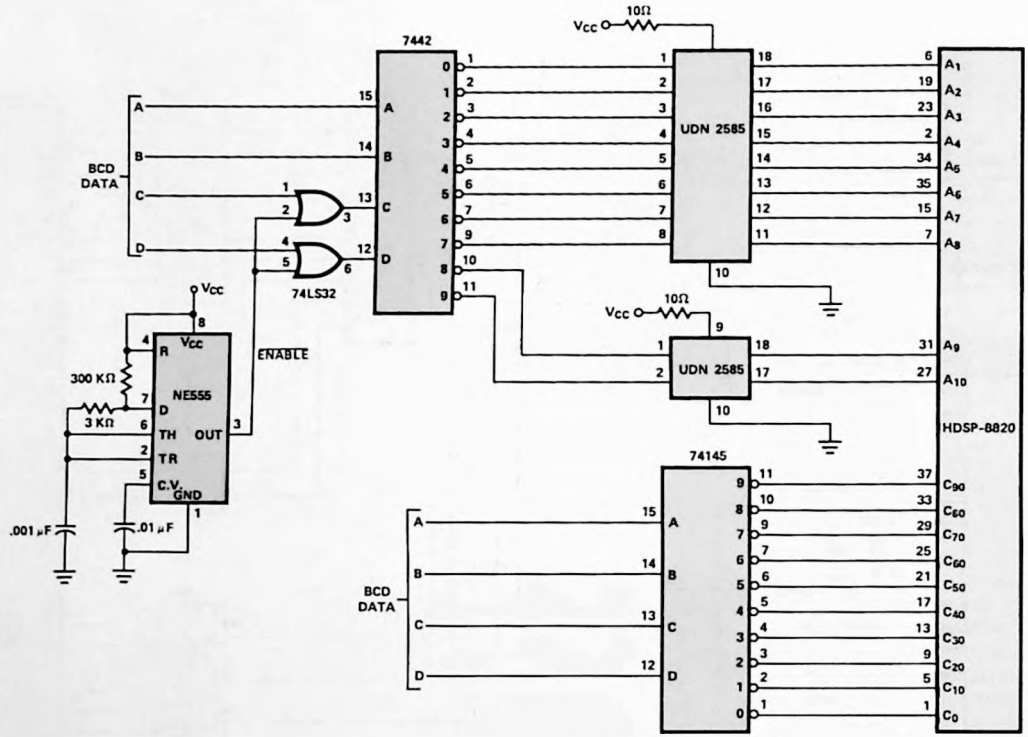
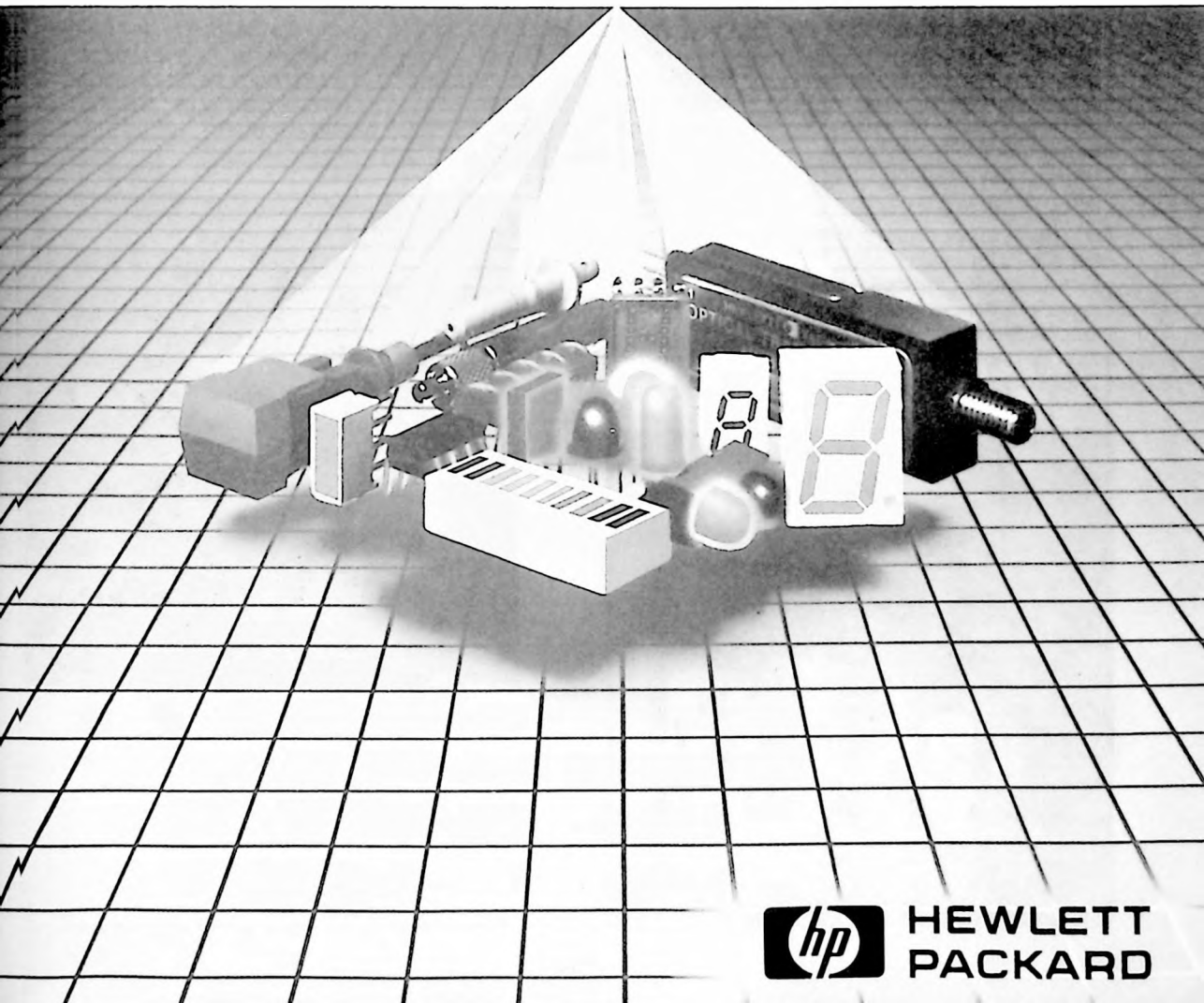


Figure 6. 100 Element Position Indicator

3. Solid State Displays

- Alphanumeric Displays
- Alphanumeric Display Systems
- Red, High Efficiency Red, Yellow and Green Seven Segment Displays
- Red Hexadecimal and Numeric Dot Matrix Displays
- High Efficiency Red, Yellow and Green Hexadecimal and Numeric Displays
- Red Seven Segment Displays



HEWLETT PACKARD

Solid State Displays

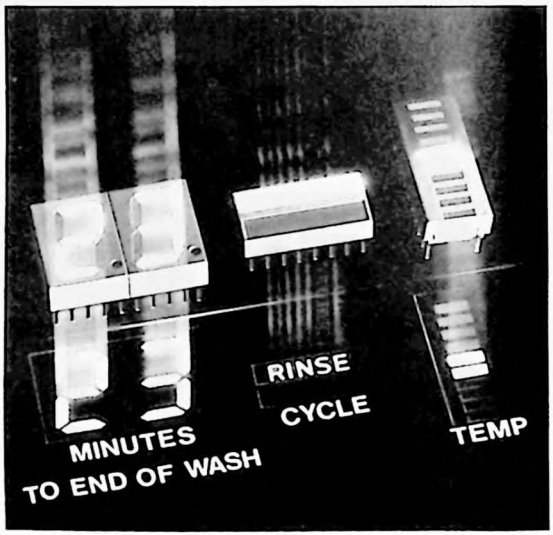
Hewlett-Packard's line of Solid State Displays answers all the needs of the designer. From alphanumeric displays to low cost numeric displays in sizes from 3 mm (.15 in.) to 20 mm (.8 in.) and colors of red, high efficiency red, yellow, and high performance green, the selection is complete.

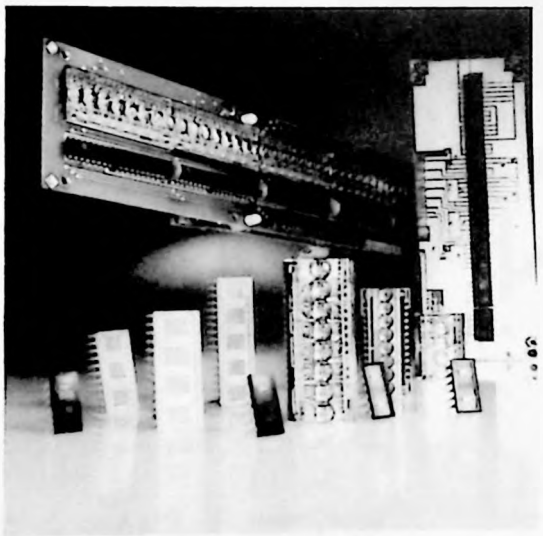
Hewlett-Packard's 5 x 7 dot matrix alphanumeric display line comes in 3 character sizes: 3.8 mm (.15 in.), 5 mm (.2 in.), and 6.9 mm (.27 in.). In turn, there are now 4 colors available for each size: standard red, yellow, high efficiency red, and green. This wide variety of package sizes and colors makes these products ideal for a variety of applications in avionics, industrial control, and instrumentation.

For military applications, we offer 5 x 7 dot matrix alphanumeric displays with extended temperature range capabilities in three package sizes: 3.8 mm (.15 in.), 5 mm (.2 in.), and 6.9 mm (.27 in.). The 5 mm (.2 in.) and 6.9 mm (.27 in.) versions have the additional feature of having a true hermetic seal and an even wider operating temperature range than the 3.8 mm (.15 in.) package. The capability these parts offer truly establishes Hewlett-Packard as a leader in displays for military applications.

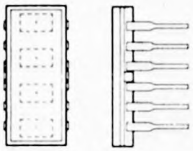
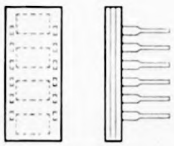
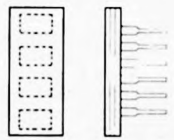
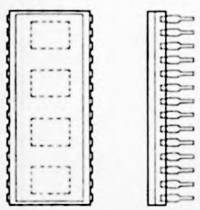
Hewlett-Packard's line of numeric seven segment displays is one of the broadest. From low cost, standard red displays to high light ambient displays producing 7.0 mcd/segment, HP's .3 in., .43 in., .56 in., and .8 in. characters can provide a solution to every display need. HP's latest product offerings include .56 in. dual digit displays and a new line of small package, bright .3 in. displays — the .3 in. Microbright. These displays are ideal for displaying numeric information in electronic instrumentation, point-of-sale equipment, appliance, and automotive instrumentation.

Integrated numeric and hexadecimal displays (with on-board IC's) solve the designer's decoding/driving problem. They are available in plastic packages for general purpose usage, ceramic/glass packages for industrial applications, and hermetic packages for high reliability applications. This family of displays has been designed for ease of use in a wide range of environments.

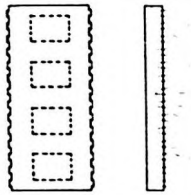
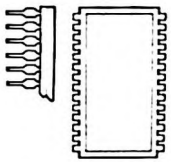
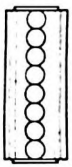
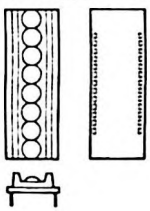




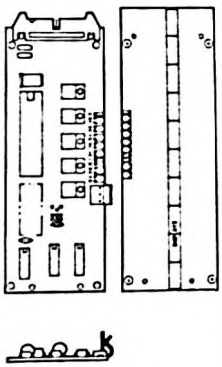
Alphanumeric LED Displays

Device		Description	Color	Application	Page No.
	HDSP-2000	3.7 mm (.15") 5 x 7 Four Character Alphanumeric	Red	• Computer Terminals • Business Machines • Medical Instruments • Portable, Hand-held or mobile data entry, read-out or communications For further information see Application Note 1016.	3-14
	HDSP-2001	12 Pin Ceramic 7.62 mm (.3") DIP with untinted glass lens	Yellow		
	HDSP-2002		High Efficiency Red		
	HDSP-2003		High Performance Green		
	HDSP-2010	Extended Temperature to T_A = -40°C 3.7 mm (.15") 5 x 7 Four Character Alphanumeric	Red, Red Glass Contrast Filter	• Extended temperature applications requiring high reliability. • Avionics For further information see Application Note 1016.	3-18
	HDSP-2010 TXV	TXV Hi Rel Screened			
	HDSP-2010 TXVB	TXVB Hi Rel Screened			
	HDSP-2300	4.87 mm (.19") 5 x 7 Four Character Alphanumeric, 12 Pin Ceramic 6.35 mm (.25") DIP/Low Power	Red	• Medical Equipment • Industrial and Process control • Computer Peripherals and Terminals	3-24
	HDSP-2301		Yellow, High Brightness		
	HDSP-2302		High Efficiency Red, High Brightness		
	HDSP-2303		High Performance Green, High Brightness		
	HDSP-2310	Hermetic Extended Temperature Range 5.0 mm (.20") 5 x 7 Alpha-numeric, 12 Pin Ceramic 6.35 mm (.25") DIP/Low Power	Standard Red	• Military Equipment • Avionics • High Rel Industrial Equipment • Ground Support, Cockpit, Shipboard Systems	3-30
	HDSP-2310 TXV		TXV — High Rel Screened		
	HDSP-2310 TXVB		TXVB — High Rel Screened to Level A MIL-D-87157		
	HDSP-2311		Yellow		
	HDSP-2311 TXV		TXV — High Rel Screened		
	HDSP-2311 TXVB		TXVB — High Rel Screened to Level A MIL-D-87157		
	HDSP-2312		High Efficiency Red		
	HDSP-2312 TXV		TXV — High Rel Screened		
	HDSP-2312 TXVB		TXVB — High Rel Screened to Level A MIL-D-87157		
	HDSP-2450	Hermetic Extended Temperature Range to T_A = -55°C 6.9 mm (.27") 5 x 7 Four Character Alphanumeric 28 Pin Ceramic 15.24 mm (.6") DIP	Red	• Military Equipment • High Reliability Applications • Avionics • Ground Support, Cockpit, Shipboard Systems	3-41
	HDSP-2450 TXV		TXV — Hi Rel Screened		
	HDSP-2450 TXVB		TXVB — Hi Rel Screened to Level A MIL-D-87157		
	HDSP-2451		Yellow		
	HDSP-2451 TXV		TXV — Hi Rel Screened		
	HDSP-2451 TXVB		TXVB — Hi Rel Screened to Level A MIL-D-87157		
	HDSP-2452		High Efficiency Red		
	HDSP-2452 TXV		TXV — Hi Rel Screened		
	HDSP-2452 TXVB		TXVB — Hi Rel Screened to Level A MIL-D-87157		

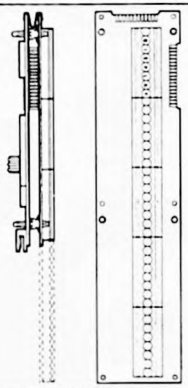
Alphanumeric LED Displays (continued)

Device		Description	Color	Application	Page No.
	HDSP-2490 HDSP-2491 HDSP-2492 HDSP-2493	6.9 mm (.27") 5 x 7 Four Character Alphanumeric 28 Pin Ceramic 15.24 mm (.6") DIP	Red Yellow, High Brightness High Efficiency Red, High Brightness High Performance Green, High Brightness	• Computer Base Mobile Units • High Brightness Ambient Systems • Industrial and Process Control For further information see Application Note 1016.	3-37
	5082-7100	6.9 mm (.27") 5 x 7 Three Digit Alphanumeric 22 Pin Ceramic 15.2 mm (.6") DIP	Red, Untinted Glass Lens	General Purpose Market • Business Machines • Calculators • Solid State CRT • High Reliability Applications	3-48
	5082-7101	6.9 mm (.27") 5 x 7 Four Digit Alphanumeric 28 Pin Ceramic 15.2 mm (.6") DIP			
	5082-7102	6.9 mm (.27") 5 x 7 Five Digit Alphanumeric 36 Pin Ceramic 15.2 mm (.6") DIP			
	HDSP-6504	3.8 mm (.15") Sixteen Segment Four Character Alphanumeric 22 Pin 15.2 mm (.6") DIP	Red	• Computer Terminals • Hand Held Instruments • In-Plant Control Equipment • Diagnostic Equipment	3-52
	HDSP-6508	3.8 mm (.15") Sixteen Segment Eight Character Alphanumeric 26 Pin 15.2 mm (.6") DIP			
	HDSP-6300	3.56 mm (.14") Sixteen Segment Eight Character Alphanumeric 26 Pin 15.2 mm (.6") DIP		• Computer Peripherals and Terminals • Computer Base Emergency Mobile Units • Automotive Instrument Panels • Desk Top Calculators • Hand-Held Instruments For further information ask for Application Note 1003.	3-58

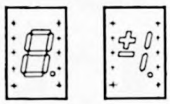
Alphanumeric Display Systems

Device		Description	Package	Application	Page No.
	HDSP-2416	Single-Line 16 Character Display Panel Utilizing the HDSP-2000 Display	162.56 mm (6.4") L x 58.42 mm (2.3") H x 7.11 mm (28") D	• Data Entry Terminals • Instrumentation	3-63
	HDSP-2424	Single-Line 24 Character Display Panel Utilizing the HDSP-2000 Display			
	HDSP-2432	Single-Line 32 Character Display Panel Utilizing the HDSP-2000 Display			
	HDSP-2440	Single-Line 40 Character Display Panel Utilizing the HDSP-2000 Display	177.80 mm (7.0") L x 58.42 mm (2.3") H x 7.11 mm (.28") D		
	HDSP-2470	HDSP-2000 Display Interface Incorporating a 64 Character ASCII Decoder	171.22 mm (6.74") L x 58.42 mm (2.3") H x 16.51 mm (.65") D		
	HDSP-2471	HDSP-2000 Display Interface Incorporating a 128 Character ASCII Decoder			

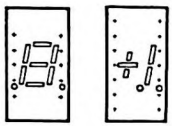
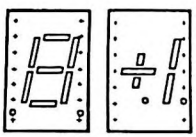
Alphanumeric Display Systems (continued)

Device		Description	Package	Application	Page No.
(See previous page)	HDSP-2472	HDSP-2000 Display Interface without ASCII Decoder. Instead, a 24 Pin Socket is Provided to Accept a Custom 128 Character Set from a User Programmed 1K x 8 PROM			3-63
	HDSP-8716	Single-line 16 Character Alphanumeric Display System Utilizing the HDSP-6508 Display	167.64 mm (6.6") L x 58.42 mm (2.3") H x 33 mm (1.3") D	• Data Entry Terminals • Instrumentation	3-75
	HDSP-8724	Single-line 24 Character Alphanumeric Display System Utilizing the HDSP-6508 Display			
	HDSP-8732	Single-line 32 Character Alphanumeric Display System Utilizing the HDSP-6508 Display	218.44 mm (8.6") L x 58.42 mm (2.3") H x 33 mm (1.3") D		
	HDSP-8740	Single-line 40 Character Alphanumeric Display System Utilizing the HDSP-6508 Display	269.24 mm (10.6") L x 58.42 mm (2.3") H x 33 mm (1.3") D		

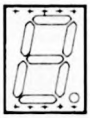
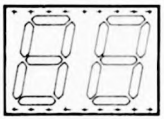
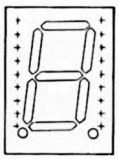
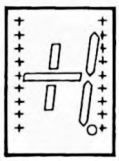
Red, High Efficiency Red, Yellow, and High Performance Green Seven Segment LED Displays

Package	Device	Description	Typical I_V @ 20 mA DC	Page No.
 7.62 mm (.3") Microbright Dual-in-Line .5" H x .3" W x .24" D	HDSP-7301	Red, Common Anode, RHDP	1000 μcd/seg	3-87
	HDSP-7302	Red, Common Anode, RHDP, Colon		
	HDSP-7303	Red, Common Cathode, RHDP		
	HDSP-7304	Red, Common Cathode, RHDP, Colon		
	HDSP-7307	Red, Overflow, ±1, Common Anode		
	HDSP-7308	Red, Overflow, ±1, Common Cathode		
	HDSP-7311	Bright Red, Common Anode, RHDP	1350 μcd/seg	
	HDSP-7313	Bright Red, Common Cathode, RHDP		
	HDSP-7317	Bright Red, Overflow, ±1, Common Anode		
	HDSP-7318	Bright Red, Overflow, ±1, Common Cathode		
	HDSP-7401	Yellow, Common Anode, RHDP	2750 μcd/seg	
	HDSP-7402	Yellow, Common Anode, RHDP, Colon		
	HDSP-7403	Yellow, Common Cathode, RHDP		
	HDSP-7404	Yellow, Common Cathode, RHDP, Colon		
	HDSP-7407	Yellow, Overflow, ±1, Common Anode		
	HDSP-7408	Yellow, Overflow, ±1, Common Cathode		
	HDSP-7501	High Efficiency Red, Common Anode, RHDP	3600 μcd/seg	
	HDSP-7502	High Efficiency Red, Common Anode, RHDP, Colon		
	HDSP-7503	High Efficiency Red, Common Cathode, RHDP		
	HDSP-7504	High Efficiency Red, Common Cathode, RHDP, Colon		
	HDSP-7507	High Efficiency Red, Overflow, ±1, Common Anode		
	HDSP-7508	High Efficiency Red, Overflow, ±1, Common Cathode		
	HDSP-7801	High Performance Green, Common Anode, RHDP	3250 μcd/seg	
	HDSP-7802	High Performance Green, Common Anode, RHDP, Colon		
	HDSP-7803	High Performance Green, Common Cathode, RHDP		
	HDSP-7804	High Performance Green, Common Cathode, RHDP, Colon		
	HDSP-7807	High Performance Green, Overflow, ±1, Common Anode		
	HDSP-7808	High Performance Green, Overflow, ±1, Common Cathode		

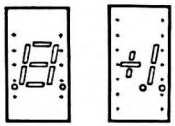
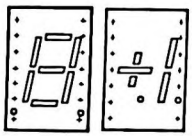
Red, High Efficiency Red, Yellow, and High Performance Green Seven Segment LED Displays (continued)

Package	Device	Description	Typical I_V @ 20 mA DC	Page No.
 7.62 mm (.3") Dual-in-line .75" H x .4" W x .18" D	5082-7730 5082-7731 5082-7736 5082-7740	Red, Common Anode, LHDP Red, Common Anode, RHDP Red, Common Anode, Polarity and Overflow Indicator Red, Common Cathode, RHDP	700 μcd/seg	3-93
	5082-7610 5082-7611 5082-7613 5082-7616	High Efficiency Red, Common Anode, LHDP High Efficiency Red, Common Anode, RHDP High Efficiency Red, Common Cathode, RHDP High Efficiency Red, Universal Polarity Overflow Indicator, RHDP	3000 μcd/seg	3-97
	5082-7620 5082-7621 5082-7623 5082-7626	Yellow, Common Anode, LHDP Yellow, Common Anode, RHDP Yellow, Common Cathode, RHDP Yellow, Universal Polarity and Overflow Indicator, RHDP	2300 μcd/seg	
	HDSP-3600 HDSP-3601 HDSP-3603 HDSP-3606	High Performance Green, Common Anode, LHDP High Performance Green, Common Anode, RHDP High Performance Green, Common Cathode, RHDP High Performance Green, Universal Overflow Indicator	2750 μcd/seg	
 10.92 mm (.43") Dual-in-line .75" H x .5" W x .25" D	5082-7750 5082-7751 5082-7756 5082-7760	Red, Common Anode, LHDP Red, Common Anode, RHDP Red, Universal Polarity and Overflow Indicator, RHDP Red, Common Cathode, RHDP	700 μcd/seg	3-93
	5082-7650 5082-7651 5082-7653 5082-7656	High Efficiency Red, Common Anode, LHDP High Efficiency Red, Common Anode, RHDP High Efficiency Red, Common Cathode, RHDP High Efficiency Red, Universal Polarity and Overflow Indicator, RHDP	3000 μcd/seg	3-97
	5082-7660 5082-7661 5082-7663 5082-7666	Yellow, Common Anode, LHDP Yellow, Common Anode, RHDP Yellow, Common Cathode, RHDP Yellow, Universal Polarity and Overflow Indicator, RHDP	2300 μcd/seg	
	HDSP-4600 HDSP-4601 HDSP-4603 HDSP-4606	High Performance Green, Common Anode, LHDP High Performance Green, Common Anode, RHDP High Performance Green, Common Cathode, RHDP High Performance Green, Universal Overflow Indicator	3100 μcd/seg	

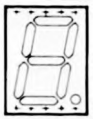
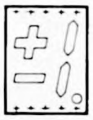
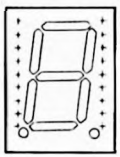
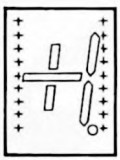
Red, High Efficiency Red, Yellow, and High Performance Green Seven Segment LED Displays (continued)

Package	Device	Description	Typical I_V @ 20 mA DC	Page No.
 14.2 mm (.56") Dual-in-Line (Single Digit) .67" H x .49" W x .31" D	HDSP-5301	Red, Common Anode, RHDP	1200 μcd/seg	3-104
	HDSP-5303	Red, Common Cathode, RHDP		
	HDSP-5307	Red ±1, Common Anode		
	HDSP-5308	Red ±1, Common Cathode		
	HDSP-5321	Red, Common Anode, Dual Digit, RHDP		
	HDSP-5323	Red, Common Cathode, Dual Digit, RHDP		
	HDSP-5501	High Efficiency Red, Common Anode, RHDP	5800 μcd/seg	
	HDSP-5503	High Efficiency Red, Common Cathode, RHDP		
	HDSP-5507	High Efficiency Red ±1, Common Anode		
	HDSP-5508	High Efficiency Red ±1, Common Cathode		
	HDSP-5521	High Efficiency Red, Common Anode, Dual Digit, RHDP		
	HDSP-5523	High Efficiency Red, Common Cathode, Dual Digit, RHDP		
	HDSP-5601	High Performance Green, Common Anode, RHDP	3450 μcd/seg	
	HDSP-5603	High Performance Green, Common Cathode, RHDP		
	HDSP-5607	High Performance Green, Common Anode Overflow Indicator		
	HDSP-5608	High Performance Green, Common Cathode Overflow Indicator		
 14.2 mm (.56") Dual-in-Line (Dual Digit) .67" H x 1.0" W x .31" D	HDSP-5621	High Performance Green, Common Anode, Dual Digit, RHDP		
	HDSP-5623	High Performance Green, Common Cathode, Dual Digit, RHDP		
	HDSP-5701	Yellow, Common Anode, RHDP	4200 μcd/seg	
	HDSP-5703	Yellow, Common Cathode, RHDP		
	HDSP-5707	Yellow ±1, Common Anode		
	HDSP-5708	Yellow ±1, Common Cathode		
	HDSP-5721	Yellow, Common Anode, Dual Digit, RHDP		
	HDSP-5723	Yellow, Common Cathode, Dual Digit, RHDP		
  20 mm (.8") Dual-in-Line 1.09" H x .78" W x .33" D	HDSP-3400	Red, Common Anode, LHDP	1200 μcd/seg	3-112
	HDSP-3401	Red, Common Anode, RHDP		
	HDSP-3403	Red, Common Cathode, RHDP		
	HDSP-3405	Red, Common Cathode, LHDP		
	HDSP-3406	Red, Universal Polarity Overflow Indicator, RHDP		
	HDSP-3900	High Efficiency Red, Common Anode, LHDP	4800 μcd/seg	
	HDSP-3901	High Efficiency Red, Common Anode, RHDP		
	HDSP-3903	High Efficiency Red, Common Cathode, RHDP		
	HDSP-3905	High Efficiency Red, Common Cathode, LHDP		
	HDSP-3906	High Efficiency Red, Universal Polarity Overflow Indicator, RHDP		
	HDSP-4200	Yellow, Common Anode, LHDP	3400 μcd/seg	
	HDSP-4201	Yellow, Common Anode, RHDP		
	HDSP-4203	Yellow, Common Cathode, RHDP		
	HDSP-4205	Yellow, Common Cathode, LHDP		
	HDSP-4206	Yellow, Universal Polarity Overflow Indicator, RHDP		
	HDSP-8600	High Performance Green, Common Anode, LHDP	3600 μcd/seg	
	HDSP-8601	High Performance Green, Common Anode, RHDP		
	HDSP-8603	High Performance Green, Common Cathode, RHDP		
	HDSP-8605	High Performance Green, Common Cathode, LHDP		
	HDSP-8606	High Performance Green, Universal Overflow Indicator		

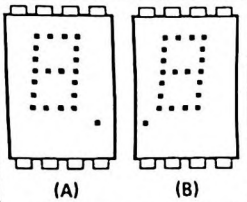
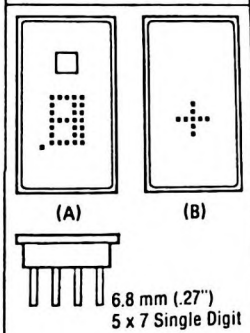
High Ambient Light, High Efficiency Red, Yellow, and High Performance Green Seven Segment Displays

Package	Device	Description	Typical I_V @ 100 mA Peak 1/5 Duty Factor	Page No.
 7.62 mm (.3") Dual-in-Line .75" H x .4" W x .18" D	HDSP-3530	High Efficiency Red, Common Anode, LHDP	4500 μcd/seg	3-119
	HDSP-3531	High Efficiency Red, Common Anode, RHDP		
	HDSP-3533	High Efficiency Red, Common Cathode, RHDP		
	HDSP-3536	High Efficiency Red, Universal Polarity Overflow Indicator, RHDP		
	HDSP-4030	Yellow, Common Anode, LHDP	4500μcd/seg	
	HDSP-4031	Yellow, Common Anode, RHDP		
	HDSP-4033	Yellow, Common Cathode, RHDP		
	HDSP-4036	Yellow, Universal Polarity Overflow Indicator, RHDP		
	HDSP-3600	High Performance Green, Common Anode, LHDP	5000μcd/seg (90 mA Peak 1/3 Duty Factor)	3-97
	HDSP-3601	High Performance Green, Common Anode, RHDP		
	HDSP-3603	High Performance Green, Common Cathode, RHDP		
	HDSP-3606	High Performance Green, Universal Overflow Indicator, RHDP		
 10.92 mm (.43") Dual-in-Line .75" H x .5" W x .25" D	HDSP-3730	High Efficiency Red, Common Anode, LHDP	5000μcd/seg	3-119
	HDSP-3731	High Efficiency Red, Common Anode, RHDP		
	HDSP-3733	High Efficiency Red, Common Cathode, RHDP		
	HDSP-3736	High Efficiency Red, Universal Polarity Overflow Indicator, RHDP		
	HDSP-4130	Yellow, Common Anode, LHDP	5000μcd/seg	
	HDSP-4131	Yellow, Common Anode, RHDP		
	HDSP-4133	Yellow, Common Cathode, RHDP		
	HDSP-4136	Yellow, Universal Polarity Overflow Indicator, RHDP		
	HDSP-4600	High Performance Green, Common Anode, LHDP	5000μcd/seg (90 mA Peak 1/3 Duty Factor)	3-97
	HDSP-4601	High Performance Green, Common Anode, RHDP		
	HDSP-4603	High Performance Green, Common Cathode, RHDP		
	HDSP-4606	High Performance Green, Universal Overflow Indicator		

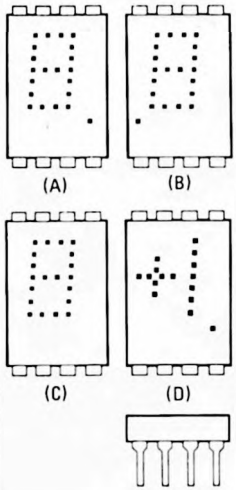
High Ambient Light, High Efficiency Red, Yellow, and High Performance Green Seven Segment Displays (continued)

Package	Device	Description	Typical I_V @ 100 mA Peak 1/5 Duty Factor	Page No.
  14.2 mm (.56") Dual-in-Line .67" H x .49" W x .31" D	HDSP-5531	High Efficiency Red, Common Anode, RHDP	7000μcd/seg	3-119
	HDSP-5533	High Efficiency Red, Common Cathode, RHDP		
	HDSP-5537	High Efficiency Red ±1, Common Anode		
	HDSP-5538	High Efficiency Red ±1, Common Cathode		
	HDSP-5731	Yellow, Common Anode, RHDP	7000μcd/seg	
	HDSP-5733	Yellow, Common Cathode, RHDP		
	HDSP-5737	Yellow ±1, Common Anode		
	HDSP-5738	Yellow ±1, Common Cathode		
	HDSP-5601	High Performance Green, Common Anode, RHDP	5800μcd/seg (90 mA Peak 1/3 Duty Factor)	3-104
	HDSP-5603	High Performance Green, Common Cathode, RHDP		
	HDSP-5607	High Performance Green, Common Anode Overflow Indicator		
	HDSP-5608	High Performance Green, Common Cathode Overflow Indicator		
  20 mm (.8") Dual-in-Line 1.09" H x .78" W x .33" D	HDSP-3900	High Efficiency Red, Common Anode, LHDP	7000μcd/seg	3-119
	HDSP-3901	High Efficiency Red, Common Anode, RHDP		
	HDSP-3903	High Efficiency Red, Common Cathode, RHDP		
	HDSP-3905	High Efficiency Red, Common Cathode, LHDP		
	HDSP-3906	High Efficiency Red, Universal Overflow Indicator, RHDP		
	HDSP-4200	Yellow, Common Anode, LHDP	7000μcd/seg	
	HDSP-4201	Yellow, Common Anode, RHDP		
	HDSP-4203	Yellow, Common Cathode, RHDP		
	HDSP-4205	Yellow, Common Cathode, LHDP		
	HDSP-4206	Yellow, Universal Polarity Overflow Indicator, RHDP		
	HDSP-8600	High Performance Green, Common Anode, LHDP	5800μcd/seg (90 mA Peak 1/3 Duty Factor)	3-112
	HDSP-8601	High Performance Green, Common Anode, RHDP		
	HDSP-8603	High Performance Green, Common Cathode, RHDP		
	HDSP-8605	High Performance Green, Common Cathode, LHDP		
	HDSP-8606	High Performance Green, Universal Overflow Indicator, RHDP		

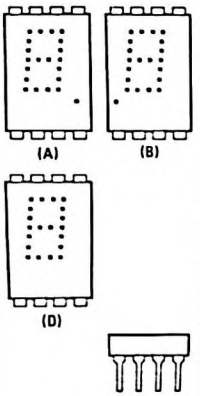
Red Hexadecimal and Numeric Dot Matrix Displays

Device		Description	Package	Application	Page No.
 (A) (B) (C) (D) 7.4 mm (.29") 4 x 7 Single Digit	5082-7300 (A)	Numeric RHDP Built-in Decoder/Driver/Memory	8 Pin Epoxy 15.2 mm (.6") DIP	General Purpose Market • Test Equipment • Business Machines • Computer Peripherals • Avionics	3-127
	5082-7302 (B)	Numeric LHDP Built-in Decoder/Driver/Memory			
	5082-7340 (C)	Hexadecimal Built-in Decoder/Driver/Memory			
	5082-7304 (D)	Character Plus/Minus Sign			
	5082-7356 (A)	Numeric RHDP Built-in Decoder/Driver/Memory	8 Pin Glass Ceramic 15.2 mm (.6") DIP	• Medical Equipment • Industrial and Process Control Equipment • Computers • Where Ceramic Package IC's required • High Reliability Applications	3-131
	5082-7357 (B)	Numeric LHDP Built-in Decoder/Driver/Memory			
	5082-7359 (C)	Hexadecimal Built-in Decoder/Driver/Memory			
	5082-7358 (D)	Character Plus/Minus Sign			
	4N51 (5082-7391) 4N51TXV 4N51TXVB (A)	Numeric RHDP Built-in Decoder/Driver/Memory TXV — Hi Rel Screened TXVB — Hi Rel Screened with Group B data	8 Pin Hermetic 15.2 mm (.6") DIP with gold plated leads	• Ground, Airborne, Shipboard Equipment • Fire Control Systems • Space Flight Systems • Other High Reliability Applications	3-136
	4N52 (5082-7392) 4N52TXV 4N52TXVB (B)	Numeric LHDP Built-in Decoder/Driver/Memory TXV — Hi Rel Screened TXVB — Hi Rel Screened with Group B data			
	4N54 (5082-7395) 4N54TXV 4N54TXVB (C)	Hexadecimal Built-in Decoder/Driver/Memory TXV — Hi Rel Screened TXVB — Hi Rel Screened with Group B data			
	4N53 (5082-7393) 4N53TXV 4N53TXVB (D)	Character Plus/Minus Sign TXV — Hi Rel Screened TXVB — Hi Rel Screened with Group B data			
 (A) (B) 6.8 mm (.27") 5 x 7 Single Digit	5082-7010 (A)	Numeric LHDP Built-in Decoder/Driver/Memory	8 Pin Metal can 2.54 mm (.100") Pin Centers	• Ground, Airborne, Shipboard Equipment • Fire Control Systems • Space Flight Systems	3-158
	5082-7011 (B)	Plus/Minus Sign			

High Efficiency Red, Yellow, and Green Hexadecimal and Numeric Displays

Device and Package		Description	Color	Application	Page No.
 (A) (B) (C) (D) 7.4 mm (.29") 4 x 7 Single Digit Package: 8 Pin Glass Ceramic 15.2 mm (.6") DIP	HDSP-0760 (A)	Numeric RHDP Built in Decoder/Driver/Memory	High Efficiency Red Low Power	• Military Equipment • Ground Support Equipment • Avionics • High Reliability Applications	3-144
	HDSP-0761 (B)	Numeric LHDP Built in Decoder/Driver/Memory			
	HDSP-0762 (C)	Hexadecimal Built in Decoder/Driver/Memory			
	HDSP-0763 (D)	Over Range ± 1			
	HDSP-0770 (A)	Numeric RHDP Built in Decoder/Driver/Memory	High Efficiency Red High Brightness	• High Brightness Ambient Systems • Cockpit, Shipboard Equipment • High Reliability Applications	
	HDSP-0771 (B)	Numeric LHDP Built in Decoder/Driver/Memory			
	HDSP-0772 (C)	Hexadecimal Built in Decoder/Driver/Memory			
	HDSP-0763 (D)	Over Range ± 1			
	HDSP-0860 (A)	Numeric RHDP Built in Decoder/Driver/Memory	Yellow	• Business Machines • Fire Control Systems • Military Equipment • High Reliability Applications	
	HDSP-0861 (B)	Numeric LHDP Built in Decoder/Driver/Memory			
	HDSP-0862 (C)	Hexadecimal Built in Decoder/Driver/Memory			
	HDSP-0863 (D)	Over Range ± 1			
	HDSP-0960 (A)	Numeric RHDP Built in Decoder/Driver/Memory	High Performance Green	• Business Machines • Fire Control Systems • Military Equipment • High Reliability Applications	
	HDSP-0961 (B)	Numeric LHDP Built in Decoder/Driver/Memory			
	HDSP-0962 (C)	Hexadecimal Built in Decoder/Driver/Memory			
	HDSP-0963 (D)	Over Range ± 1			

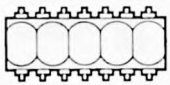
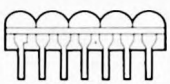
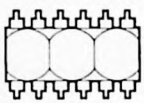
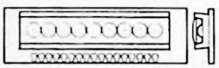
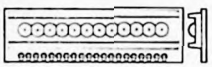
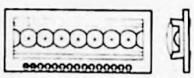
High Efficiency Red, Yellow, and Green Hexadecimal and Numeric Displays (continued)

Device		Description	Color	Application	Page No.
 7.4 mm (.29") 4 x 7 Single Digit	HDSP-0781 HDSP-0781 TXV HDSP-0781 TXVB	Numeric RHDP, Built-in Decoder/Driver Memory	High Efficiency Red, Low Power	• Ground, Airborne, Shipboard Equipment • Fire Control Systems • Space Flight Systems • Other High Reliability Uses	3-150
	HDSP-0782 HDSP-0782 TXV HDSP-0782 TXVB	Numeric LHDP, Built-in Decoder/Driver Memory			
	HDSP-0783 HDSP-0783 TXV HDSP-0783 TXVB	Overrange ±1			
	HDSP-0784 HDSP-0784 TXV HDSP-0784 TXVB	Hexadecimal, Built-in Decoder/Driver Memory			
	HDSP-0791 HDSP-0791 TXV HDSP-0791 TXVB	Numeric RHDP, Built-in Decoder/Driver Memory	High Efficiency Red, High Brightness	• Ground, Airborne, Shipboard Equipment • Fire Control Systems • Space Flight Systems • Other High Reliability Uses	
	HDSP-0792 HDSP-0792 TXV HDSP-0792 TXVB	Numeric LHDP, Built-in Decoder/Driver Memory			
	HDSP-0783 HDSP-0783 TXV HDSP-0783 TXVB	Overrange ±1			
	HDSP-0794 HDSP-0794 TXV HDSP-0794 TXVB	Hexadecimal, Built-in Decoder/Driver Memory			
	HDSP-0881 HDSP-0881 TXV HDSP-0881 TXVB	Numeric RHDP, Built-in Decoder/Driver Memory	Yellow	• Ground, Airborne, Shipboard Equipment • Fire Control Systems • Space Flight Systems • Other High Reliability Uses	
	HDSP-0882 HDSP-0882 TXV HDSP-0782 TXVB	Numeric LHDP, Built-in Decoder/Driver Memory			

High Efficiency Red, Yellow, and Green Hexadecimal and Numeric Displays (continued)

Device		Description	Color	Application	Page No.
(See previous page)	HDSP-0883 HDSP-0883 TXV HDSP-0883 TXVB	Overrange ±1			3-150
	HDSP-0884 HDSP-0884 TXV HDSP-0884 TXVB	Hexadecimal, Built-in Decoder/Driver Memory			

Red Seven Segment LED Displays

Device		Description	Package	Application	Page No.
	5082-7404	2.79 mm (.11") Red, 4 Digits Centered D.P.	12 Pin Epoxy, 7.62 mm (.3") DIP	Small Display Market • Portable/Battery Power Instruments • Portable Calculators • Digital Counters • Digital Thermometers • Digital Micrometers • Stopwatchs • Cameras • Copiers • Digital Telephone Peripherals • Data Entry Terminals • Taxi Meters For further information ask for Application Note 937.	3-164
	5082-7405	2.79 mm (.11") Red, 5 Digits, Centered D.P.	14 Pin Epoxy, 7.62 mm (.3") DIP		
	5082-7414	2.79 mm (.11") Red, 4 Digits, RHDP	12 Pin Epoxy, 7.62 mm (.3") DIP		
	5082-7415	2.79 mm (.11") Red, 5 Digits, RHDP	14 Pin Epoxy, 7.62 mm (.3") DIP		
	5082-7432	2.79 mm (.11") Red, 2 Digits, Right, RHDP	12 Pin Epoxy, 7.62 mm (.3") DIP		
	5082-7433	2.79 mm (.11") Red, 3 Digits, RHDP			
	5082-7441	2.67 mm (.105") Red, 9 Digits, Mounted on P.C. Board	50.8 mm (2") PC Bd., 17 Term. Edge Con.		
	5082-7446	2.92 mm (.115") Red, 16 Digits, Mounted on P.C. Board	69.85 mm (2.750") PC Bd., 24 Term. Edge Con.		
	5082-7285	4.45 mm (.175") Red, 5 Digits, Mounted on P.C. Board. RHDP	50.8 mm (2") PC Bd., 15 Term. Edge Con.		
	5082-7295	4.45 mm (.175") Red, 15 Digits, Mounted on P.C. Board. RHDP	91.2 mm (3.59") PC Bd., 23 Term. Edge Con.		

HEWLETT PACKARD

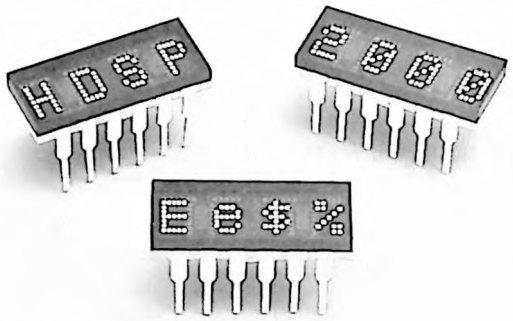
FOUR CHARACTER 3.8 mm (0.15 INCH) 5x7 ALPHANUMERIC DISPLAYS

STANDARD RED	HDSP-2000
YELLOW	HDSP-2001
HIGH EFFICIENCY RED	HDSP-2002
HIGH PERFORMANCE GREEN	HDSP-2003

TECHNICAL DATA JANUARY 1984

Features

- FOUR COLORS
  Standard Red
  Yellow
  High Efficiency Red
  High Performance Green
- INTEGRATED SHIFT REGISTERS WITH CONSTANT CURRENT DRIVERS
- COMPACT CERAMIC PACKAGE
- WIDE VIEWING ANGLE
- END STACKABLE FOUR CHARACTER PACKAGE
- TTL COMPATIBLE
- 5 x 7 LED MATRIX DISPLAYS FULL ASCII SET
- CATEGORIZED FOR LUMINOUS INTENSITY
- HDSP-2001/2003 CATEGORIZED FOR COLOR



Typical Applications

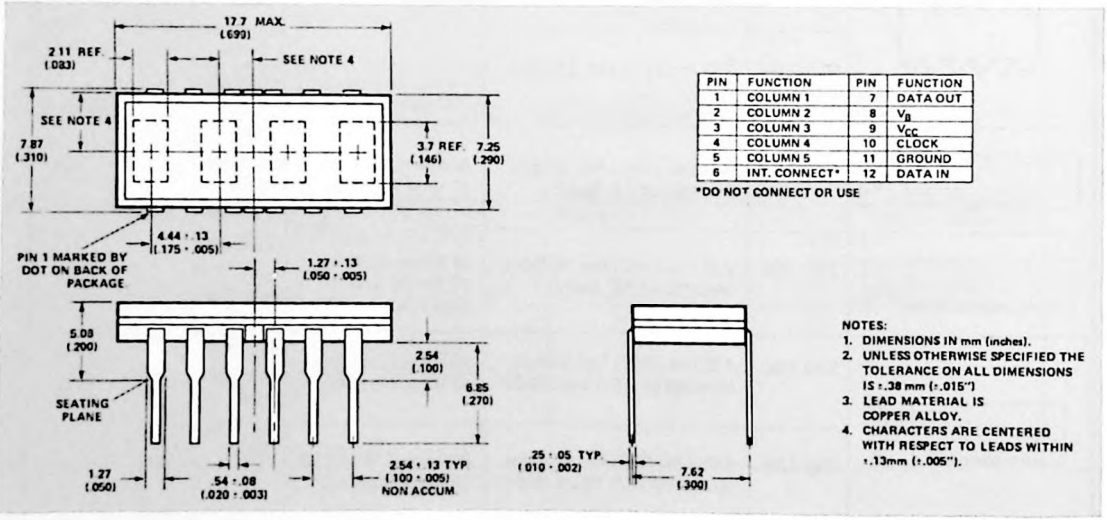
- Portable Data Entry Devices
- Business Machines
- Programmable Legend Switches
- Medical Instruments

Description

The HDSP-2000/-2001/-2002/-2003 series of displays are 3.8 mm (0.15 inch) 5 x 7 LED arrays for display of alphanumeric information. These devices are available in standard red, yellow, high efficiency red, and high performance green.

Each four character cluster is contained in a 12 pin dual-in-line package. An on-board SIPO (Serial-In-Parallel-Out) 7-bit shift register associated with each digit controls constant current LED row drivers. Full character display is achieved by external column strobing.

Package Dimensions



PIN	FUNCTION	PIN	FUNCTION
1	COLUMN 1	7	DATA OUT
2	COLUMN 2	8	V_B
3	COLUMN 3	9	V_{CC}
4	COLUMN 4	10	CLOCK
5	COLUMN 5	11	GROUND
6	INT. CONNECT*	12	DATA IN

*DO NOT CONNECT OR USE

NOTES:
1. DIMENSIONS IN mm (inches).
2. UNLESS OTHERWISE SPECIFIED THE TOLERANCE ON ALL DIMENSIONS IS ±.38 mm (±.015").
3. LEAD MATERIAL IS COPPER ALLOY.
4. CHARACTERS ARE CENTERED WITH RESPECT TO LEADS WITHIN ±.13mm (±.005").

Absolute Maximum Ratings (HDSP-2000/-2001/-2002/-2003)

Supply Voltage V_{CC} to Ground ..... −0.5V to 6.0V
Inputs, Data Out and V_B ..... −0.5V to V_{CC}
Column Input Voltage, V_{COL} ..... −0.5V to +6.0V
Free Air Operating
Temperature Range, T_A[1,2] ..... −20°C to +85°C
Storage Temperature Range, Ts ..... −55°C to +100°C
Maximum Allowable Package Dissipation
at T_A = 25°C[1,2,3] ..... 1.24 Watts
Maximum Solder Temperature 1.59 mm (0.063")
Below Seating Plane t < 5 sec ..... 260°C

Recommended Operating Conditions (HDSP-2000/-2001/-2002/-2003)

Parameter	Symbol	Min.	Nom.	Max.	Units	Fig.
Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
Data Out Current, Low State	I_{OL}			1.6	mA	
Data Out Current, High State	I_{OH}			-0.5	mA	
Column Input Voltage, Column On HDSP-2000	V_{COL}	2.4		3.5	V	4
Column Input Voltage, Column On, HDSP-2001/-2002/-2003	V_{COL}	2.75		3.5	V	4
Setup Time	t_{setup}	70	45		ns	1
Hold Time	t_{hold}	30	0		ns	1
Width of Clock	$t_{w(Clock)}$	75			ns	1
Clock Frequency	f_{clock}	0		3	MHz	1
Clock Transition Time	t_{THL}			200	ns	1
Free Air Operating Temperature Range[1,2]	T_A	-20		85	°C	2

Electrical Characteristics Over Operating Temperature Range

(Unless otherwise specified)

Description		Symbol	Test Conditions		Min.	Typ.*	Max.	Units	Fig.
Supply Current		I_{CC}	V_{CC} = 5.25V, V_{CLOCK} = V_{DATA} = 2.4V, All SR Stages = Logical 1	V_B = 0.4V		45	60	mA	
				V_B = 2.4V		73	95	mA	
Column Current at any Column Input		I_{COL}	V_{CC} = 5.25 V, V_{COL} = 3.5V	V_B = 0.4V			500	µA	4
Column Current at any Column Input		I_{COL}	All SR Stages = Logical 1	V_B = 2.4V		335	410	mA	
V_B, Clock or Data Input Threshold High		V_{IH}	V_{CC} = V_{COL} = 4.75V		2.0			V	
V_B, Clock or Data Input Threshold Low		V_{IL}					0.8	V	
Input Current Logical 1	V_B, Clock	I_{IH}	V_{CC} = 5.25V, V_{IH} = 2.4V			20	80	µA	
	Data In	I_{IH}				10	40	µA	
Input Current Logical 0	V_B, Clock	I_{IL}	V_{CC} = 5.25V, V_{IL} = 0.4V			-500	-800	µA	
	Data In	I_{IL}				-250	-400	µA	
Data Out Voltage		V_{OH}	V_{CC} = 4.75V, I_{OH} = -0.5 mA, I_{COL} = 0 mA		2.4	3.4		V	
		V_{OL}	V_{CC} = 4.75V, I_{OL} = 1.6 mA, I_{COL} = 0 mA			0.2	0.4	V	
Power Dissipation Per Package**		P_D	V_{CC} = 5.0V, V_{COL} = 3.5V, 17.5% DF 15 LEDs on per character, V_B = 2.4V			0.72		W	2
Thermal Resistance IC Junction-to-Case		$R\theta_{J-C}$				25		°C/W/ Device	2

*All typical values specified at V_{CC} = 5.0V and T_A = 25°C unless otherwise noted.

**Power dissipation per package with four characters illuminated.

Notes:

1. Operation above 85°C ambient is possible provided the following conditions are met. The junction should not exceed 125°C T_J and the case temperature (as measured at pin 1 or the back of the display) should not exceed 100°C Tc.
2. The device should be derated linearly above 50°C at 16.7 mW/°C. This derating is based on a device mounted in a socket having a thermal resistance from case to ambient at 35°C/W per device. See Figure 2 for power deratings based on a lower thermal resistance.
3. Maximum allowable dissipation is derived from V_{CC} = 5.25V, V_B = 2.4V, V_{COL} = 3.5V 20 LEDs on per character, 20% DF.

Optical Characteristics

STANDARD RED HDSP-2000

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED[4,8] (Character Average)	I_{vPeak}	V_{CC} = 5.0V, V_{COL} = 3.5V T_i = 25° C[6], V_B = 2.4V	105	200		µcd	3
Peak Wavelength	λ_{PEAK}			655		nm	
Dominant Wavelength[7]	λ_d			639		nm	

YELLOW HDSP-2001

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED[4,8] (Character Average)	I_{vPeak}	V_{CC} = 5.0V, V_{COL} = 3.5V T_i = 25° C[6], V_B = 2.4V	400	750		µcd	3
Peak Wavelength	λ_{PEAK}			583		nm	
Dominant Wavelength[5,7]	λ_d			585		nm	

HIGH EFFICIENCY RED HDSP-2002

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED[4,8] (Character Average)	I_{vPeak}	V_{CC} = 5.0V, V_{COL} = 3.5V T_i = 25° C[6], V_B = 2.4V	400	1430		µcd	3
Peak Wavelength	λ_{PEAK}			635		nm	
Dominant Wavelength[7]	λ_d			626		nm	

HIGH PERFORMANCE GREEN HDSP-2003

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED[4,8] (Character Average)	I_{vPeak}	V_{CC} = 5.0V, V_{COL} = 3.5V T_i = 25° C[6], V_B = 2.4V	850	1550		µcd	3
Peak Wavelength	λ_{PEAK}			568		nm	
Dominant Wavelength[5,7]	λ_d			574		nm	

*All typical values specified at V_{CC} = 5.0V and T_A = 25° C unless otherwise noted.

**Power dissipation per package with four characters illuminated.

Notes:

4. The characters are categorized for luminous intensity with the intensity category designated by a letter code on the bottom of the package.
5. The HDSP-2001/-2003 are categorized for color with the color category designated by a number code on the bottom of the package.
6. T_i refers to the initial case temperature of the device immediately prior to the light measurement.
7. Dominant wavelength λ_d, is derived from the CIE chromaticity diagram, and represents the single wavelength which defines the color of the device.
8. The luminous sterance of the LED may be calculated using the following relationships:
   L_v (cd/m²) = I_v (Candela)/A (Metre)²
   L_v (Footlamberts) = πIv (Candela)/A (Foot)²
   A = 5.3 x 10^{-8} M² = 5.8 x 10^{-7} Foot²

Electrical Description

The HDSP-200X series of four character alphanumeric displays have been designed to allow the user maximum flexibility in interface electronics design. Each four character display module features Data In and Data Out terminals arrayed for easy PC board interconnection. Data Out represents the output of the 7th bit of digit number 4 shift register. Shift register clocking occurs on the high to low transition of the clock input. The like columns of each character in a display cluster are tied to a single pin. Figure 5 is the block diagram for the displays. High true data in the shift register enables the output current mirror driver stage associated with each row of LEDs in the 5 x 7 diode array.

The TTL compatible V_B input may either be tied to V_{CC} for maximum display intensity or pulse width modulated to achieve intensity control and reduction in power consumption.

The normal mode of operation input data for digit 4, column 1 is loaded into the 7 on-board shift register locations 1 through 7 . Column 1 data for digits 3, 2, and 1 is similarly shifted into the display shift register locations. The column 1 input is now enabled for an appropriate period of time, T. A similar process is repeated for columns 2, 3, 4 and 5. If the time necessary to decode and load data into the shift register is t, then with 5 columns, each column of the display is operating at a duty factor of:

$$D.F. = \frac{T}{5\,(t+T)}$$

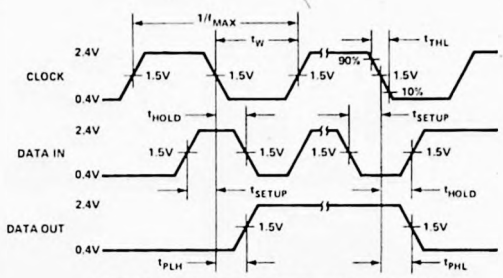
The time frame, t + T, alloted to each column of the display is generally chosen to provide the maximum duty factor consistent with the minimum refresh rate necessary to achieve a flicker free display. For most strobed display systems, each column of the display should be refreshed (turned on) at a minimum rate of 100 tirnes per second.

With columns to be addressed, this refresh rate then gives a value for the time t + T of:

$$1/[5 \times (100)] = 2 \text{ msec}$$

If the device is operated at 3.0 MHz clock rate maximum, it is possible to maintain t << T. For short display strings, the duty factor will then approach 20%.

For further applications information, refer to HP Application Note 1016.



Parameter	Condition	Min.	Typ.	Max.	Units
f_{clock} CLOCK Rate				3	MHz
t_{PLH}, t_{PHL} Propagation delay CLOCK to DATA OUT	C_l = 15pF R_L=2.4kΩ			125	ns

Figure 1. Switching Characteristics HDSP-2000/-2001/-2002/-2003 (T_A = -20° C to +85° C)

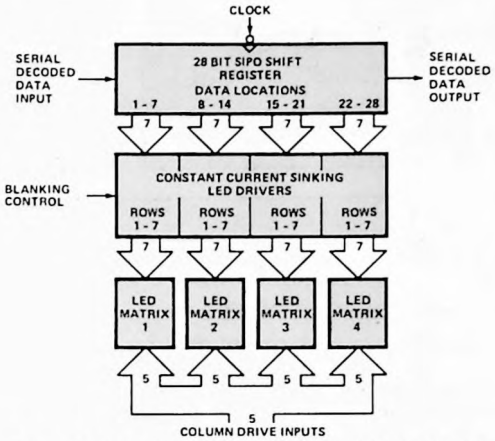


Figure 5. Block Diagram of HDSP-2000/-2001/-2002/-2003

Mechanical and Thermal Considerations

The HDSP-2000/-2001/-2002/-2003 are available in standard ceramic dual-in-line packages. They are designed for plugging into sockets or soldering into PC boards. The packages may be horizontally or vertically stacked for character arrays of any desired size. Full power operation (V_{CC} = 5.25V, V_B = 2.4V, V_{COL} = 3.5V) with worst case thermal resistance from IC junction to ambient of 60° C/watt/device is possible up to ambient temperature of 50° C. For operation above 50° C, the maximum device dissipation should be derated linearly at 16.7 mW/° C (see Figure 2). With an improved thermal design, operation at higher ambient temperatures without derating is possible.

Power derating for this family of displays can be achieved in several ways. The power supply voltage can be lowered to a minimum of 4.75V. Column Input Voltage, V_{COL}, can be decreased to the recommended minimum values of 2.4V for the HDSP-2000 and 2.75V for the HDSP-2001/-2002/-2003. Also, the average drive current can be decreased through pulse width modulation of V_B.

The HDSP-2000/-2001/-2002/-2003 displays have glass windows. A front panel contrast enhancement filter is desirable in most actual display applications. Some suggested filter materials are provided in Figure 6. Additional information on filtering and constrast enhancement can be found in HP Application Note 1015.

Post solder cleaning may be accomplished using water or Freon/alcohol mixtures formulated for vapor cleaning processing or Freon/alcohol mixtures formulated for room temperature cleaning. Freon/alcohol vapor cleaning processing for up to 2 minutes in vapors at boiling is permissible. Suggested solvents include Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15, and water.

Display Color	Ambient Lighting		
	Dim	Moderate	Bright
HDSP-2000 Std. Red	Panelgraphic Dark Red 63 Ruby Red 60 Chequers Red 118 Plexiglass 2423		
HDSP-2001 Yellow	Panelgraphic Yellow 27 Chequers Amber 107	Polaroid HNCP37 3M Light Control Film Panelgraphic Gray 10	Note 1
HDSP-2002 HER	Panelgraphic Ruby Red 60 Chequers Red 112	Chequers Grey 105	
HDSP-2003 HP Green	Panelgraphic Green 48 Chequers Green 107		

Note: 1. Optically coated circular polarized filters, such as Polaroid HNCP10.

Figure 6. Contrast Enhancement Filters

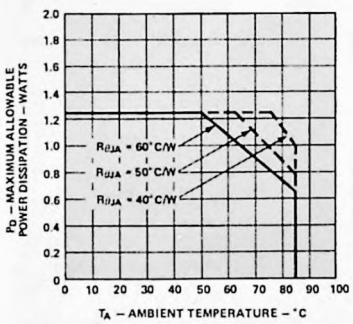


Figure 2. Maximum Allowable Power Dissipation vs. Temperature

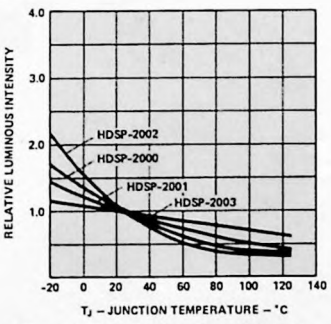


Figure 3. Relative Luminous Intensity vs. Temperature

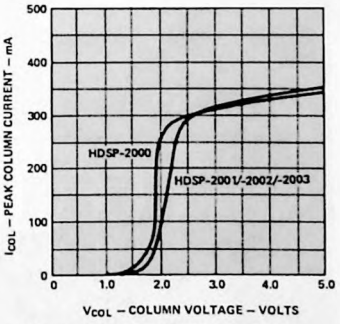


Figure 4. Peak Column Current vs. Column Voltage

HEWLETT PACKARD

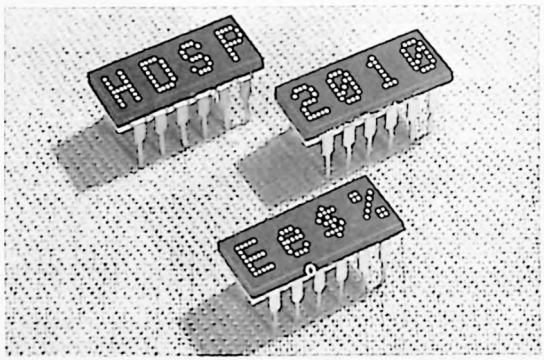
FOUR CHARACTER RED ALPHANUMERIC DISPLAY FOR EXTENDED TEMPERATURE APPLICATIONS

HDSP-2010
HDSP-2010TXV
HDSP-2010TXVB

TECHNICAL DATA JANUARY 1984

Features

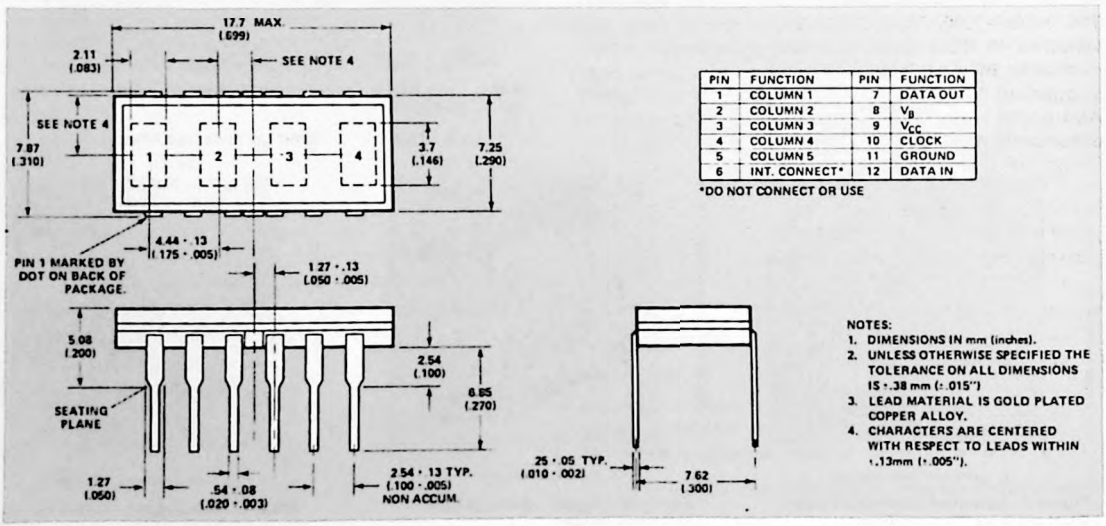
- OPERATION GUARANTEED TO T_A = -40°C
- LEAK RATE GUARANTEED
- QUALITY LEVEL A OF MIL-D-87157
- 100% TEMPERATURE CYCLED -55°C to +100°C
- GOLD PLATED LEADS
- INTEGRATED SHIFT REGISTERS WITH CONSTANT CURRENT DRIVERS
- CERAMIC 7.62mm (.3 in.) DIP Integral Red Glass Contrast Filter
- WIDE VIEWING ANGLE
- END STACKABLE 4 CHARACTER PACKAGE
- PIN ECONOMY 12 Pins for 4 Characters
- TTL COMPATIBLE
- 5 x 7 LED MATRIX DISPLAYS FULL ASCII CODE
- RUGGED, LONG OPERATING LIFE
- CATEGORIZED FOR LUMINOUS INTENSITY Assures Ease of Package to Package Brightness Matching



Description

The HDSP-2010 display is designed for use in applications requiring high reliability. The character font is a 3.8mm (0.15 inch) 5 x 7 red LED array for displaying alphanumeric information. The device is available in 4 character clusters and is packaged in a 12-pin dual-in-line type package. An on-board SIPO (serial-in-parallel-out) 7-bit shift register associated with each digit controls constant current LED row drivers. Full character display is achieved by external column strobing. The constant current LED drivers are externally programmable and typically capable of sinking 13.5mA peak per diode. Applications include interactive I/O terminals, avionics, portable telecommunications gear, and hand held equipment requiring alphanumeric displays.

Package Dimensions



PIN	FUNCTION	PIN	FUNCTION
1	COLUMN 1	7	DATA OUT
2	COLUMN 2	8	V_B
3	COLUMN 3	9	V_{CC}
4	COLUMN 4	10	CLOCK
5	COLUMN 5	11	GROUND
6	INT. CONNECT*	12	DATA IN

*DO NOT CONNECT OR USE

NOTES:
1. DIMENSIONS IN mm (inches).
2. UNLESS OTHERWISE SPECIFIED THE TOLERANCE ON ALL DIMENSIONS IS ±.38 mm (±.015").
3. LEAD MATERIAL IS GOLD PLATED COPPER ALLOY.
4. CHARACTERS ARE CENTERED WITH RESPECT TO LEADS WITHIN ±.13mm (±.005").

Absolute Maximum Ratings

Supply Voltage V_{CC} to Ground ..... −0.5V to 6.0V
Inputs, Data Out and V_B ..... −0.5V to V_{CC}
Column Input Voltage, V_{COL} ..... −0.5V to +6.0V
Free Air Operating Temperature Range, T_A[2] ..... −40°C to +85°C
Storage Temperature Range, T_S ..... -55°C to +100°C
Maximum Allowable Package Dissipation at $T_A = 25°C$[1,2,6] ..... 1.29 Watts
Maximum Solder Temperature 1.59mm (.063") Below Seating Plane t<5 secs ..... 260°C

Recommended Operating Conditions

Parameter	Symbol	Min.	Nom.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Data Out Current, Low State	I_{OL}			1.6	mA
Data Out Current, HighState	I_{OH}			−0.5	mA
Column Input Voltage, Column On	V_{COL}	2.6		3.5	V
Setup Time	t_{setup}	70	45		ns
Hold Time	t_{hold}	30	0		ns
Width of Clock	$t_{w(Clock)}$	75			ns
Clock Frequency	f_{clock}	0		3	MHz
Clock Transition Time	t_{THL}			200	ns
Free Air Operating Temperature Range	T_A	-40		85	°C

Electrical Characteristics Over Operating Temperature Range

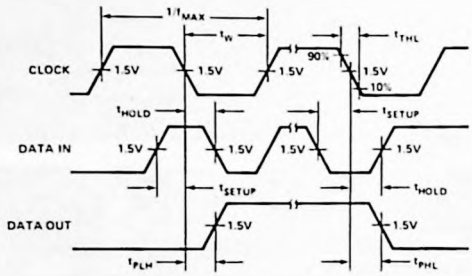
(Unless otherwise specified.)

Description		Symbol	Test Conditions		Min.	Typ.*	Max.	Units
Supply Current		I_{CC}	V_{CC} = 5.25V, V_{CLOCK} = V_{DATA} = 2.4V, All SR Stages = Logical 1	V_B = 0.4V		45	60	mA
				V_B = 2.4V		73	95	mA
Column Current at any Column Input		I_{COL}	V_{CC} = 5.25V, V_{COL} = 3.5V, All SR Stages = Logical 1	V_B = 0.4V			1.5	mA
Column Current at any Column Input		I_{COL}		V_B = 2.4V		350	435	mA
Peak Luminous Intensity per LED[3,7] (Character Average)		I_{VPEAK}	V_{CC} = 5.0V, V_{COL} = 3.5V, T_j = 25°C[4], V_B = 2.4V		105	200		µcd
V_B, Clock or Data Input Threshold High		V_{IH}	V_{CC} = V_{COL} = 4.75V		2.0			V
V_B, Data Input Threshold Low		V_{IL}					0.8	V
Clock Threshold Low		V_{IL}					0.6	V
Input Current Logical 1	V_B, Clock	I_{IH}	V_{CC} = 5.25V, V_{IH} = 2.4V			20	80	µA
	Data In	I_{IH}				10	40	µA
Input Current Logical 0	V_B, Clock	I_{IL}	V_{CC} = 5.25V, V_{IL} = 0.4V			-500	-800	µA
	Data In	I_{IL}				-250	-400	µA
Data Out Voltage		V_{OH}	V_{CC} = 4.75V, I_{OH} = -0.5mA, V_{COL} = 0V		2.4	3.4		V
		V_{OL}	V_{CC} = 4.75V, I_{OL} = 1.6mA, V_{COL} = 0V			0.2	0.4	V
Power Dissipation Per Package**		P_D	V_{CC} = 5.0V, V_{COL} = 2.6V, 15 LEDs on per character, V_B = 2.4V			0.66		W
Peak Wavelength		λ_{PEAK}				655		nm
Dominant Wavelength[5]		λ_d				640		nm
Thermal Resistance IC Junction-to-Case		$R\theta_{J-C}$				25		°C/W/ Device
Leak Rate							$5x10^{-7}$	cc/s

*All typical values specified at V_{CC} = 5.0V and T_A = 25°C unless otherwise noted.

**Power dissipation per package with 4 characters illuminated.

1. Operation above 85°C ambient is possible provided the following conditions are met. The junction temperature should not exceed 125°C T_J and the case temperature as measured at pin 1 or the back of the display should not exceed 100°C T_C.
2. The device should be derated linearly above 50°C at 16.7 mW/°C. This derating is based on a device mounted in a socket having a thermal resistance from case to ambient at 35° C/W per device. See Figure 2 for power deratings based on a lower thermal resistances.
3. The characters are categorized for Luminous Intensity with the category designated by a letter code on the bottom of the package.
4. T_j refers to the initial case temperature of the device immediately prior to the light measurement.
5. Dominant wavelength λ_d, is derived from the CIE chromaticity diagram, and represents the single wavelength which defines the color of the device.
6. Maximum allowable dissipation is derived from V_{CC} = V_B = 5.25 Volts, V_{COL} = 3.5V, 20 LEDs on per character, 20% DF.
7. The luminous stearance of the LED may be calculated using the following relationships:
   L_v (Lux) = I_v (Candela)/A (Metre)^2
   L_v (Footlamberts) = πI_v (Candela)/A (Foot)^2
   A = 5.3 x 10^{-8} M^2 = 5.8 x 10^{-7} (Foot)^2



Parameter	Condition	Min.	Typ.	Max.	Units
f_{clock} CLOCK Rate				3	MHz
t_{PLH}, t_{PHL} Propagation delay CLOCK to DATA OUT	C_L = 15pF R_L=2.4KΩ			125	ns

Figure 1. Switching Characteristics. (V_{CC} = 5V, T_A = -40°C to +70°C)

Mechanical and Thermal Considerations

The HDSP-2010 is available in a standard 12 lead ceramic-glass dual in-line package. It is designed for plugging into DIP sockets or soldering into PC boards. The packages may be horizontally or vertically stacked for character arrays of any desired size.

The HDSP-2010 can be operated over a wide range of temperature and supply voltages. Power reduction can be achieved by either decreasing V_{COL} or decreasing the average drive current through pulse width modulation of V_B.

The HDSP-2010 display has a glass lens. A front panel contrast filter is desirable in most actual display applications. Some suggested filters are Panel graphic Ruby Red 60, SGL Homalite H100-1605 Red and 3M Light Control Film (louvered filters). OCLI Sungard optically coated glass filters offer superior contrast enhancement.

Post solder cleaning may be accomplished using water, Freon/alcohol mixtures formulated for vapor cleaning processing (up to 2 minutes in vapors at boiling) or Freon/alcohol mixtures formulated for room temperature cleaning. Suggested solvents: Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15.

Electrical Description

The HDSP-2010 display provides on-board storage of decoded column data and constant current sinking row drivers for each of 28 rows in the 4 character display. The device consists of four LED matrices and two integrated circuits that form a 28-bit serial input-parallel output (SIPO) shift register, see Figure 5. Each character is a 5 x 7 diode array arranged with the cathodes of each row connected to one constant current sinking output of the SIPO shift register. The anodes of each column are connected together, with the same column of each of the 4 characters connected together (i.e. column 1 of all four characters are connected to pin 1). Any LED within any character may be addressed by shifting data to the appropriate shift register location and applying a voltage to the appropriate column.

Associated with each shift register location is a constant current sinking LED driver, capable of sinking a nominal 13.5 mA. A logical 1 loaded into a shift register location enables the current source at that location. A voltage applied to the appropriate column input turns on the desired LED.

The display is column strobed on a 1 of 5 basis by loading 7 bits of row data per character for a selected column. The data is shifted through the SIPO shift register, one bit location for each high-to-low transition of the clock. When the HDSP-2010 display is operated with pin 1 in the lower left hand corner, the first bit that is loaded into the SIPO shift register will be the information for row 7 of the right most character. The 28th bit loaded into the SIPO shift register will be the information for row 1 of the left most character. When the 28 bits of row data for column 1 have been loaded into the SIPO shift register, the first column is energized for a time period, T, illuminating column 1 in all four characters. Column 1 is turned off and the process is repeated for columns 2 through 5.

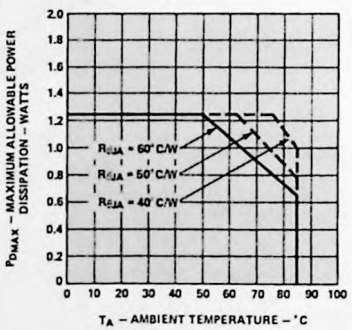


Figure 2. Maximum Allowable Power Dissipation vs. Temperature.

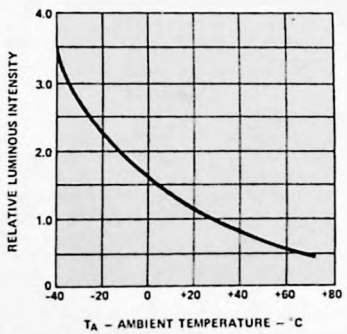


Figure 3. Relative Luminous Intensity vs. Temperature.

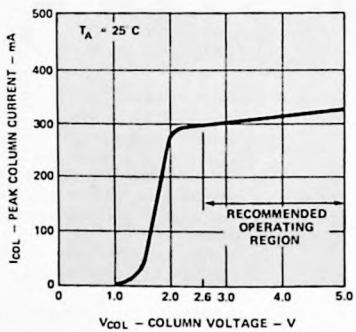


Figure 4. Peak Column Current vs. Column Voltage.

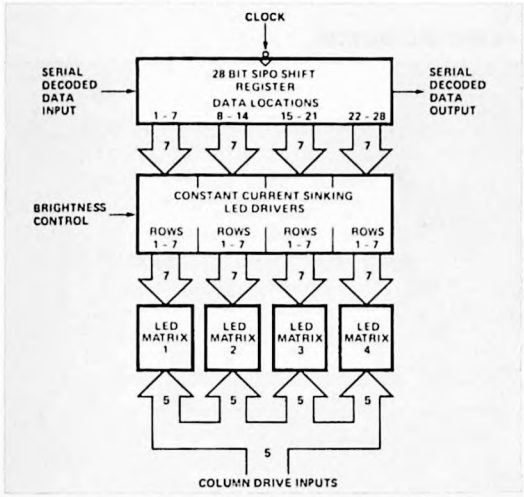


Figure 5. Block Diagram of the HDSP-2010 Display

The time frame allotted per column is $(t + T)$ and the minimum recommended refresh rate for a flicker free display is 100 Hz, so that $(t + T) \leq 2$ ms. If the display is operated at the 3 MHz maximum clock rate, it is possible to maintain $t << T$. For display strings of 24 characters or less, the LED on time DF will be approximately 19.4%. For longer display strings, operation of the display with DF approximately 10% will provide adequate light output for indoor applications.

The 28th stage of the SIPO shift register is connected to the Data Output, which is designed to interface directly to the Data Input of the next HDSP-2010 in the display string.

The V_B input may be used to control the apparent brightness of the display. A logic high applied to the V_B input enables the display to be turned ON, and a logic low blanks the display by disabling the constant current LED drivers. Therefore, the time average luminous intensity of the display can be varied by pulse width modulation of V_B. For application and drive circuit information refer to HP Application Note 1016.

High Reliability Testing

Two standard reliability testing programs are available. The TXVB program is in conformance with Quality Level A of MIL-D-87157 for hermetically sealed displays with 100% screening tests. A TXVB product is tested to Tables I, II, IIIa, and IVa. A second program is an HP modification to the full conformance program and offers the 100% screening portion of Level A, Table I, and Group A, Table II.

PART MARKING SYSTEM

Standard Product	With Table I and II	With Tables I, II, IIIa, and IVa
HDSP-2010	HDSP-2010 TXV	HDSP-2010 TXVB

100% Screening

TABLE I. QUALITY LEVEL A OF MIL-D-87157

Test Screen	MIL-STD-750 Method	Conditions
1. Precap Visual	—	HP Procedure 5956-7512-52
2. High Temperature Storage	1032	$T_A = 100°C$, Time = 24 hours
3. Temperature Cycling	1051	$T_A = -55°C$ to $+100°C$, 10 cycles, 15 min. dwell
4. Constant Acceleration	2006	10,000 G's at Y_1 orientation
5. Fine Leak	1071	Condition H, Leak Rate $\leq 5 \times 10^{-7}$ cc/s
6. Gross Leak	1071	Condition C, except fluid temperature shall be $+100°C$
7. Interim Electrical/Optical Tests[2]	—	I_{CC} (at $V_B = 0.4V$ and $2.4V$), I_{COL} (at $V_B = 0.4V$ and $2.4V$) I_{IH} (V_B, Clock and Data In), I_{IL} (V_B, Clock and Data In), I_{OH}, I_{OL}, Visual Function and I_V Peak. V_{IH} and V_{IL} inputs are guaranteed by the electronic shift register test. $T_A = 25°C$
8. Burn-In[1]	1015	Condition B at $V_{CC} = V_B = 5.25V$, $V_{COL} = 3.5V$, $T_A = +85°C$ LED ON-Time Duty Factor = 5%, t = 168 hours
9. Final Electrical Test[2]	—	Same as Step 7
10. Delta Determinations	—	$\Delta I_{CC} = \pm 6$ mA, ΔI_{IH} (clock) $= \pm 10\ \mu A$ ΔI_{IH} (Data In) $= \pm 10\ \mu A$ $\Delta I_{OH} = \pm 10\%$ of initial value and $\Delta I_V = -20\%$
11. External Visual	2009	

Notes:
1. MIL-STD-883 Test Method applies.
2. Limits and conditions are per the electrical/optical characteristics. The I_{OH} and I_{OL} tests are the inverse of V_{OH} and V_{OL} specified in the electrical characteristics.

TABLE II
GROUP A ELECTRICAL TESTS MIL-D-87157

Test	Parameters	LTPD
Subgroup 1 DC Electrical Tests at 25° C[1]	I_{CC} (at V_B = 0.4V and 2.4V), I_{COL} (at V_B = 0.4V and 2.4V) I_{IH} (V_B, Clock and Data In), I_{IL} (V_B, Clock and Data In), I_{OH}, I_{OL} Visual Function and Iv peak. V_{IH} and V_{IL} inputs are guaranteed by the electronic shift register test.	5
Subgroup 2 DC Electrical Tests at High Temperature[1]	Same as Subgroup 1, except delete Iv and visual function. T_A = +85° C	7
Subgroup 3 DC Electrical Tests at Low Temperature[1]	Same as Subgroup 1, except delete Iv and visual function. T_A = -40° C	7
Subgroup 4, 5, and 6 not tested		
Subgroup 7 Optical and Functional Tests at 25° C	Satisfied by Subgroup 1	5
Subgroup 8 External Visual		7

1. Limits and conditions are per the electrical/optical characteristics. The I_{OH} and I_{OL} tests are the inverse of V_{OH} and V_{OL} specified in the electrical characteristics.

TABLE IIIa
GROUP B, CLASS A AND B OF MIL-D-87157

Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1 Resistance to Solvents	1022		4 Devices/ 0 Failures
Internal Visual and Mechanical[3]	2014		1 Device/ 0 Failures
Subgroup 2[1,2] Solderability	2026	T_A = 260° C for 5 seconds	LTPD = 15
Subgroup 3 Thermal Shock (Temp. Cycle)	1051	T_A = -55° C to +100° C, 10 cycles, 15 min. dwell	LTPD = 15
Moisture Resistance	1021		
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C, except fluid temperature shall be +100° C	
Electrical/Optical Endpoints[4]	—	I_{CC} (at V_B = 0.4V and 2.4V), I_{COL} (at V_B = 0.4V and 2.4V), I_{IH} (V_B, Clock and Data In), I_{IL} (V_B, Clock and Data In), I_{OH}, I_{OL} Visual Function and Iv peak. V_{IH} and V_{IL} inputs are guaranteed by the electronic shift register test. T_A = 25° C	
Subgroup 4 Operating Life Test (340 hrs.)	1027	T_A = +85° C at V_{CC} = V_B = 5.25V, V_{COL} = 3.5V, LED ON-Time Duty Factor = 5%	LTPD = 10
Electrical/Optical Endpoints[4]	—	Same as Subgroup 3	
Subgroup 5 Non-operating (Storage) Life Test (340 hrs.)	1032	T_A = +100° C	LTPD = 10
Electrical/Optical Endpoints[4]	—	Same as Subgroup 3	

1. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
2. The LTPD applies to the number of leads inspected except in no case shall less than 3 displays be used to provide the number of leads required.
3. MIL-STD-883 methods apply.
4. Limits and conditions are per the electrical/optical characteristics. The I_{OH} and I_{OL} tests are the inverse of V_{OH} and V_{OL} specified in the electrical characteristics.

TABLE IVa
GROUP C, CLASS A AND B OF MIL-D-87157

Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1[1]			
Physical Dimensions	2066		2 Devices/ 0 Failures
Subgroup 2[2,7]			LTPD = 15
Lead Integrity	2004	Condition B2	
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C, except fluid temperature shall be +100°C	
Subgroup 3			
Shock	2016	1500G, Time = 0.5 ms, 5 blows in each orientation X_1, Y_1, Y_2	LTPD = 15
Vibration, Variable Frequency	2056		
Constant Acceleration	2006	10,000G at Y_1 orientation	
External Visual[4]	1010 or 1011		
Electrical/Optical Endpoints[8]	—	I_{CC} (at V_B = 0.4V and 2.4V) I_{COL} (at V_B = 0.4V and 2.4V) I_{IH} (V_B, Clock and Data In) I_{IL} (V_B, Clock and Data In) I_{OH}, I_{OL}, Visual Function and Iv peak. V_{IH} and V_{IL} inputs are guaranteed by the electronic shift register test. T_A = 25°C.	
Subgroup 4[1,3]			
Salt Atmosphere	1041		LTPD = 15
External Visual[4]	1010 or 1011		
Subgroup 5			
Bond Strength[5]	2037	Condition A	LTPD = 20 (C = 0)
Subgroup 6			
Operating Life Test[6]	1026	T_A = +85°C at V_{CC} = V_B = 5.25V, V_{COL} = 3.5V	λ = 10
Electrical/Optical Endpoints[8]	—	Same as Subgroup 3	

1. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
2. The LTPD applies to the number of leads inspected except in no case shall less than three displays be used to provide the number of leads required.
3. Solderability samples shall not be used.
4. Visual requirements shall be as specified in MIL-STD-883, Methods 1010 or 1011.
5. Displays may be selected prior to seal.
6. If a given inspection lot undergoing Group B inspection has been selected to satisfy Group C inspection requirements, the 340 hour life tests may be continued on test to 1000 hours in order to satisfy the Group C life test requirements. In such cases, either the 340 hour endpoint measurements shall be made a basis for Group B lot acceptance or the 1000 hour endpoint measurement shall be used as the basis for both Group B and Group C acceptance.
7. MIL-STD-883 test method applies.
8. Limits and conditions are per the electrical/optical characteristics. The I_{OH} and I_{OL} tests are the inverse of V_{OH} and V_{OL} specified in the electrical characteristics.

HEWLETT PACKARD

FOUR CHARACTER 5.0 mm (0.20 INCH) 5x7 ALPHANUMERIC DISPLAYS

STANDARD RED	HDSP-2300
YELLOW	HDSP-2301
HIGH EFFICIENCY RED	HDSP-2302
HIGH PERFORMANCE GREEN	HDSP-2303

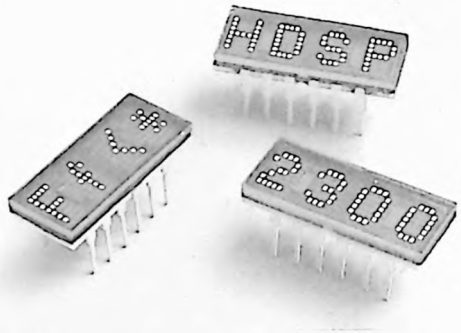
TECHNICAL DATA JANUARY 1984

Features

- FOUR COLORS

Standard Red	Low Power
Yellow	High Brightness
High Efficiency Red	High Brightness
High Performance Green	High Brightness

- INTEGRATED SHIFT REGISTERS WITH CONSTANT CURRENT DRIVERS
- COMPACT CERAMIC PACKAGE
- WIDE VIEWING ANGLE
- END STACKABLE FOUR CHARACTER PACKAGE
- TTL COMPATIBLE
- 5 x 7 LED MATRIX DISPLAYS FULL ASCII SET
- CATEGORIZED FOR LUMINOUS INTENSITY
- HDSP-2301/2303 CATEGORIZED FOR COLOR



Typical Applications

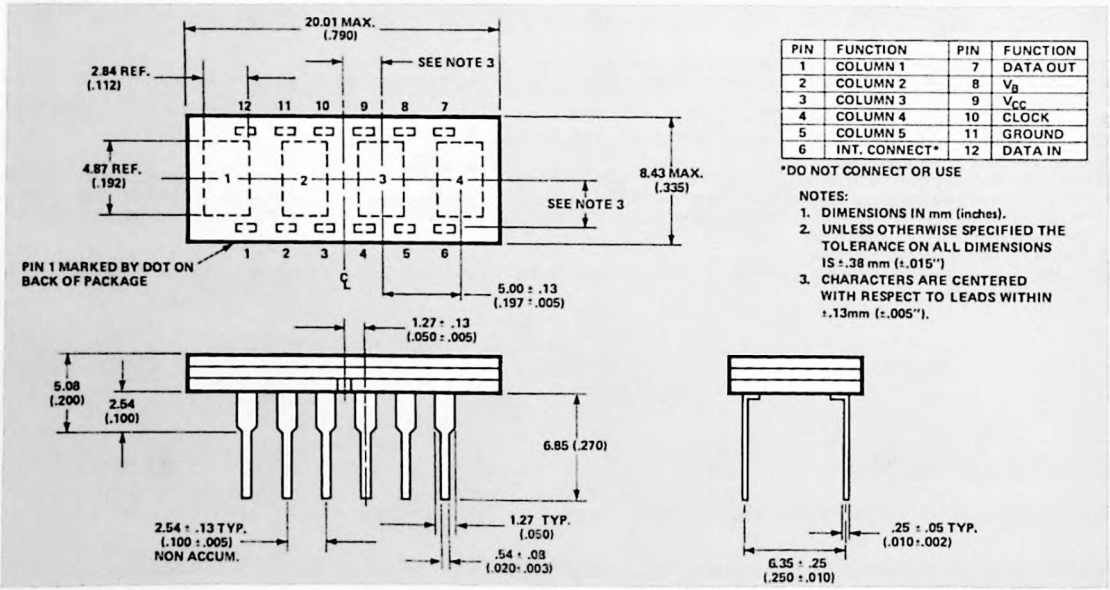
- Avionics
- Business Machines
- Medical Instruments
- Portable Data Entry Devices

Description

The HDSP-2300/-2301/-2302/-2303 series of displays are 5.0 mm (0.20 inch) 5 x 7 LED arrays for display of alphanumeric information. These devices are available in standard red, yellow, high efficiency red, and high performance green.

Each four character cluster is contained in a 12 pin dual-in-line package. An on-board SIPO (Serial-In-Parallel-Out) 7-bit shift register associated with each digit controls constant current LED row drivers. Full character display is achieved by external column strobing.

Package Dimensions



PIN	FUNCTION	PIN	FUNCTION
1	COLUMN 1	7	DATA OUT
2	COLUMN 2	8	V_B
3	COLUMN 3	9	V_{CC}
4	COLUMN 4	10	CLOCK
5	COLUMN 5	11	GROUND
6	INT. CONNECT*	12	DATA IN

*DO NOT CONNECT OR USE

NOTES:
1. DIMENSIONS IN mm (inches).
2. UNLESS OTHERWISE SPECIFIED THE TOLERANCE ON ALL DIMENSIONS IS ±.38 mm (±.015")
3. CHARACTERS ARE CENTERED WITH RESPECT TO LEADS WITHIN ±.13mm (±.005").

Absolute Maximum Ratings (HDSP-2300/-2301/-2302/-2303)

Supply Voltage V_{CC} to Ground ..... −0.5V to 6.0V
Inputs, Data Out and V_B ..... −0.5V to V_{CC}
Column Input Voltage, V_{COL} ..... −0.5V to +6.0V
Free Air Operating
Temperature Range, T_A[1,2] ..... −20°C to +85°C
Storage Temperature Range, T_S ..... −55°C to +100°C

Maximum Allowable Package Dissipation
at T_A = 25°C[1,2,3]
HDSP-2300 ..... 1.24 Watts
HDSP-2301/-2302/-2303 ..... 1.46 Watts
Maximum Solder Temperature 1.59 mm (0.063")
Below Seating Plane t < 5 sec ..... 260°C

Recommended Operating Conditions (HDSP-2300/-2301/-2302/-2303)

Parameter	Symbol	Min.	Nom.	Max.	Units	Fig.
Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
Data Out Current, Low State	I_{OL}			1.6	mA	
Data Out Current, High State	I_{OH}			-0.5	mA	
Column Input Voltage, Column On HDSP-2300	V_{COL}	2.4		3.5	V	4
Column Input Voltage, Column On HDSP-2301/-2302/-2303	V_{COL}	2.75		3.5	V	7
Setup Time	t_{setup}	70	45		ns	1
Hold Time	t_{hold}	30	0		ns	1
Width of Clock	$t_{w(Clock)}$	75			ns	1
Clock Frequency	f_{clock}	0		3	MHz	1
Clock Transition Time	t_{THL}			200	ns	1
Free Air Operating Temperature Range[1,2]	T_A	-20		85	°C	3, 5

Electrical Characteristics Over Operating Temperature Range

(Unless otherwise specified)

STANDARD RED HDSP-2300

Description		Symbol	Test Conditions		Min.	Typ.*	Max.	Units	Fig.
Supply Current		I_{CC}	V_{CC} = 5.25V, V_{CLOCK} = V_{DATA} = 2.4V, All SR Stages = Logical 1	V_B = 0.4V		45	60	mA	
				V_B = 2.4V		73	95	mA	
Column Current at any Column Input		I_{COL}	V_{CC} = 5.25 V, V_{COL} = 3.5V	V_B = 0.4V			500	µA	4
Column Current at any Column Input		I_{COL}	All SR Stages = Logical 1	V_B = 2.4V		335	410	mA	
V_B, Clock or Data Input Threshold High		V_{IH}	V_{CC} = V_{COL} = 4.75V		2.0			V	
V_B, Clock or Data Input Threshold Low		V_{IL}					0.8	V	
Input Current Logical 1	V_B, Clock	I_{IH}	V_{CC} = 5.25V, V_{IH} = 2.4V			20	80	µA	
	Data In	I_{IH}				10	40	µA	
Input Current Logical 0	V_B, Clock	I_{IL}	V_{CC} = 5.25V, V_{IL} = 0.4V			-500	-800	µA	
	Data In	I_{IL}				-250	-400	µA	
Data Out Voltage		V_{OH}	V_{CC} = 4.75V, I_{OH} = -0.5 mA, I_{COL} = 0 mA		2.4	3.4		V	
		V_{OL}	V_{CC} = 4.75V, I_{OL} = 1.6 mA, I_{COL} = 0 mA			0.2	0.4	V	
Power Dissipation Per Package**		P_D	V_{CC} = 5.0V, V_{COL} = 3.5V, 17.5% DF, 15 LEDs on per character, V_B = 2.4V			0.72		W	2
Thermal Resistance IC Junction-to-Case		$R\theta_{J-C}$				25		°C/W/ Device	2

*All typical values specified at V_{CC} = 5.0V and T_A = 25°C unless otherwise noted.

**Power dissipation per package with four characters illuminated.

Notes:

1. Operation above 85°C ambient is possible provided the following conditions are met. The junction temperature should not exceed 125°C T_J and the case temperature (as measureed at pin 1 or the back of the display) should not exceed 100°C T_C.
2. The HDSP-2300 should be derated linearly above 50°C at 16.7 mW/°C. The HDSP-2301/-2302/-2303 should be derated linearly above 37°C at 16.7 mW/°C. This derating is based on a device mounted in a socket having a thermal resistance from case to ambient at 35°** C/W per device. See Figure 2 for power deratings based on a lower thermal resistance.
3. Maximum allowable dissipation is derived from V_{CC} = 5.25V, V_B = 2.4V, V_{COL} = 3.5V 20 LEDs on per character, 20% DF.

YELLOW HDSP-2301/HIGH EFFICIENCY RED HDSP-2302/HIGH PERFORMANCE GREEN HDSP-2303

Description		Symbol	Test Conditions		Min.	Typ.*	Max.	Units	Fig.
Supply Current		I_{CC}	V_{CC} = 5.25V, V_{CLOCK} = V_{DATA} = 2.4V, All SR Stages = Logical 1	V_B = 0.4V		45	60	mA	
				V_B = 2.4V		73	95	mA	
Column Current at any Column Input		I_{COL}	V_{CC} = 5.25 V, V_{COL} = 3.5V	V_B = 0.4V			500	µA	7
Column Current at any Column Input		I_{COL}	All SR Stages = Logical 1	V_B = 2.4V		380	520	mA	
V_B, Clock or Data Input Threshold High		V_{IH}	V_{CC} = V_{COL} = 4.75V		2.0			V	
V_B, Clock or Data Input Threshold Low		V_{IL}					0.8	V	
Input Current Logical 1	V_B, Clock	I_{IH}	V_{CC} = 5.25V, V_{IH} = 2.4V			20	80	µA	
	Data In	I_{IH}				10	40	µA	
Input Current Logical 0	V_B, Clock	I_{IL}	V_{CC} = 5.25V, V_{IL} = 0.4V			-500	-800	µA	
	Data In	I_{IL}				-250	-400	µA	
Data Out Voltage		V_{OH}	V_{CC} = 4.75V, I_{OH} = -0.5 mA, I_{COL} = 0 mA		2.4	3.4		V	
		V_{OL}	V_{CC} = 4.75V, I_{OL} = 1.6 mA, I_{COL} = 0 mA			0.2	0.4	V	
Power Dissipation Per Package**		P_D	V_{CC} = 5.0V, V_{COL} = 3.5V, 17.5% DF, 15 LEDs on per character, V_B = 2.4V			0.78		W	5
Thermal Resistance IC Junction-to-Case		$R\theta_{J-C}$				25		°C/W/ Device	5

Optical Characteristics

STANDARD RED HDSP-2300

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED [4,8] (Character Average)	I_{VPeak}	V_{CC} = 5.0V, V_{COL} = 3.5V, T_i = 25°C[6], V_B = 2.4V	130	300		µcd	3
Peak Wavelength	λ_{PEAK}			655		nm	
Dominant Wavelength[7]	λ_d			639		nm	

YELLOW HDSP-2301

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED [4,8] (Character Average)	I_{VPeak}	V_{CC} = 5.0V, V_{COL} = 3.5V, T_i = 25°C[6], V_B = 2.4V	650	1140		µcd	6
Peak Wavelength	λ_{PEAK}			583		nm	
Dominant Wavelength[5,7]	λ_d			585		nm	

HIGH EFFICIENCY RED HDSP-2302

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED [4,8] (Character Average)	I_{VPeak}	V_{CC} = 5.0V, V_{COL} = 3.5V, T_i = 25°C[6], V_B = 2.4V	650	1430		µcd	6
Peak Wavelength	λ_{PEAK}			635		nm	
Dominant Wavelength[7]	λ_d			626		nm	

HIGH PERFORMANCE GREEN HDSP-2303

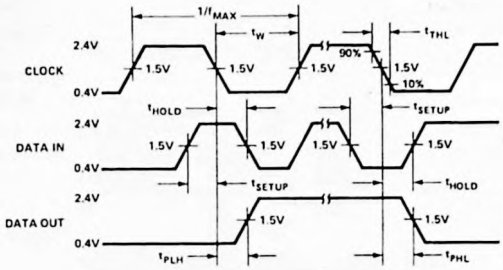
Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED [4,8] (Character Average)	I_{VPeak}	V_{CC} = 5.0V, V_{COL} = 3.5V, T_i = 25°C[6], V_B = 2.4V	1280	2410		µcd	6
Peak Wavelength	λ_{PEAK}			568		nm	
Dominant Wavelength [5,7]	λ_d			574		nm	

*All typical values specified at V_{CC} = 5.0V and T_A = 25°C unless otherwise noted.

**Power dissipation per package with four characters illuminated.

Notes:

4. The characters are categorized for luminous intensity with the intensity category designated by a letter code on the bottom of the package.
5. The HDSP-2301/-2303 are categorized for color with the color category designated by a number code on the bottom of the package.
6. T_i refers to the initial case temperature of the device immediately prior to the light measurement.
7. Dominant wavelength λ_d, is derived from the CIE chromaticity diagram, and represents the single wavelength which defines the color of the device.
8. The luminous sterance of the LED may be calculated using the following relationships:
   L_v (cd/m²) = I_v (Candela)/A (Metre)²
   L_v (Footlamberts) = πI_v (Candela)/A (Foot)²
   A = 5.3 x 10^{-8} M² = 5.8 x 10^{-7} (Foot)²



Parameter	Condition	Min.	Typ.	Max.	Units
f_{clock} CLOCK Rate				3	MHz
t_{PLH}, t_{PHL} Propagation delay CLOCK to DATA OUT	C_L = 15pF R_L=2.4KΩ			125	ns

Figure 1. Switching Characteristics HDSP-2300/-2301/-2302/-2303 (T_A = -20° C to +85° C)

HDSP-2300

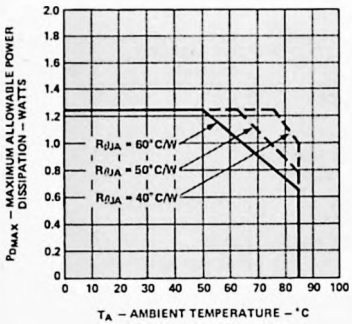


Figure 2. Maximum Allowable Power Dissipation vs. Temperature

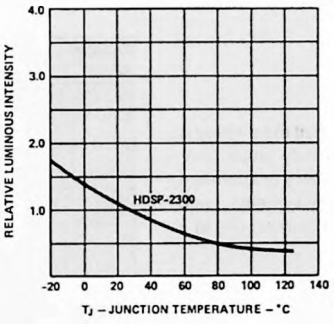


Figure 3. Relative Luminous Intensity vs. Temperature

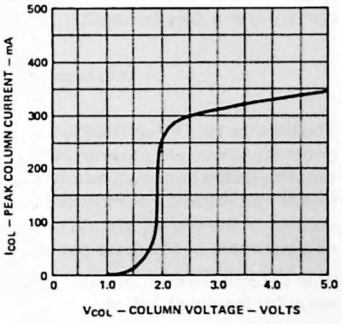


Figure 4. Peak Column Current vs. Column Voltage

HDSP-2301/-2302/-2303

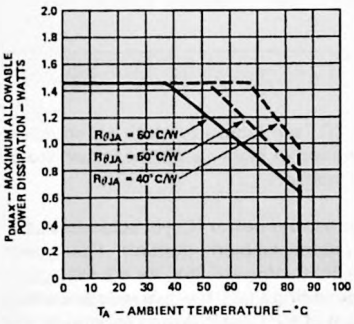


Figure 5. Maximum Allowable Power Dissipation vs. Temperature

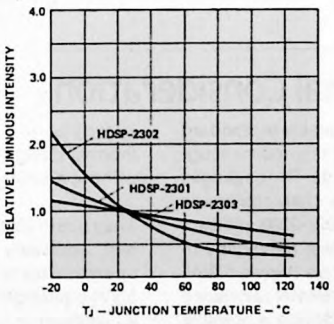


Figure 6. Relative Luminous Intensity vs. Temperature

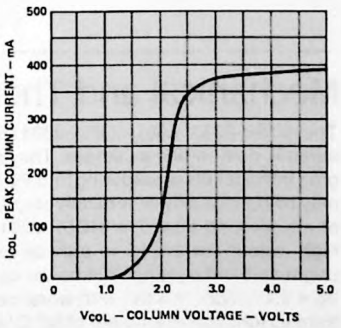


Figure 7. Peak Column Current vs. Column Voltage

Electrical Description

The HDSP-230X series of four character alphanumeric displays have been designed to allow the user maximum flexibility in interface electronics design. Each four character display module features Data In and Data Out terminals arrayed for easy PC board interconnection. Data Out represents the output of the 7th bit of digit number 4 shift register. Shift register clocking occurs on the high to low transition of the Clock input. The like columns of each character in a display cluster are tied to a single pin. Figure 8 is the block diagram for the displays. High true data in the shift register enables the output current mirror driver stage associated with each row of LEDs in the 5 x 7 diode array.

The TTL compatible V_B input may either be tied to V_{CC} for maximum display intensity or pulse width modulated to achieve intensity control and reduction in power consumption.

The normal mode of operation input data for digit 4, column 1 is loaded into the 7 on-board shift register locations 1 through 7 . Column 1 data for digits 3, 2, and 1 is similarly shifted into the display shift register locations. The column 1 input is now enabled for an appropriate period of time, T. A similar process is repeated for columns 2, 3, 4 and 5. If the time necessary to decode and load data into the shift register is t, then with 5 columns, each column of the display is operating at a duty factor of:

$$D.F. = \frac{T}{5\,(t+T)}$$

The time frame, t + T, alloted to each column of the display is generally chosen to provide the maximum duty factor consistent with the minimum refresh rate necessary to achieve a flicker free display. For most strobed display systems, each column of the display should be refreshed (turned on) at a minimum rate of 100 times per second.

With columns to be addressed, this refresh rate then gives a value for the time t + T of:

$$1/[5 \times (100)] = 2 \text{ msec}$$

If the device is operated at 3.0 MHz clock rate maximum, it is possible to maintain $t << T$. For short display strings, the duty factor will then approach 20%.

For further applications information, refer to HP Application Note 1016.

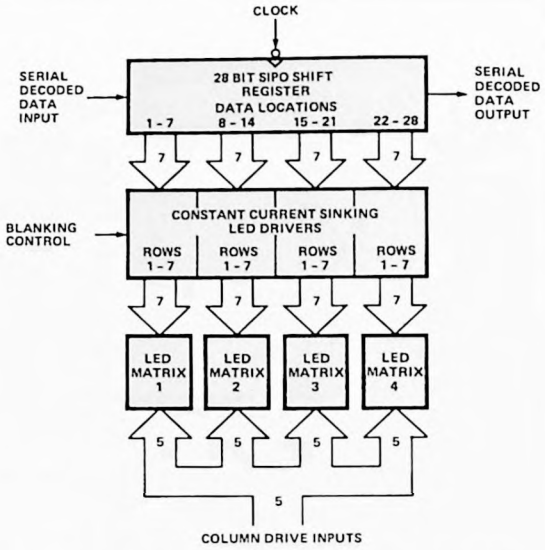


Figure 8. Block Diagram of HDSP-2300/-2301/-2302/-2303

Display Color	Ambient Lighting		
	Dim	Moderate	Bright
HDSP-2300 Std. Red	Panelgraphic Dark Red 63 Ruby Red 60 Chequers Red 118 Plexiglass 2423		
HDSP-2301 (Yellow)	Panelgraphic Yellow 27 Chequers Amber 107	Polaroid HNCP37 3M Light Control Film Panelgraphic Gray 10	Note 1
HDSP-2302 (HER)	Panelgraphic Ruby Red 60 Chequers Red 112	Chequers Grey 105	
HDSP-2303 (HP Green)	Panelgraphic Green 48 Chequers Green 107		

Note: 1. Optically coated circular polarized filters, such as Polaroid HNCP10.

Figure 9. Contrast Enhancement Filters

Mechanical and Thermal Considerations

The HDSP-2300/-2301/-2302/-2303 are available in standard ceramic dual-in-line packages. They are designed for plugging into sockets or soldering into PC boards. The packages may be horizontally or vertically stacked for character arrays of any desired size. The HDSP-2301/-2302/-2303 utilize a high output current IC to provide excellent readability in bright ambient lighting. Full power operation (V_{CC} = 5.25V, V_B = 2.4V, V_{COL} = 3.5V) with worst case thermal resistance from IC junction to ambient of 60° C/watt/device is possible up to ambient temperature of 37° C. For operation above 37° C, the maximum device dissipation should be derated linearly at 16.7 mW/° C (see Figure 5). With an improved thermal design, operation at higher ambient temperatures without derating is possible.

The HDSP-2300 uses a lower power IC, yet achieves excellent readabilty in indoor ambient lighting. Full power operation up to T_A = 50° C (V_{CC} = 5.25V, V_B = 2.4V, V_{COL} = 3.5V) is possible by providing a total thermal resistance from IC junction to ambient of 60° C/watt/device maximum. For operation above 50° C, the maximum device dissipation should be derated at 16.7 mW/° C/device (see Figure 2).

Power derating for this family of displays can be achieved in several ways. The power supply voltage can be lowered to a minimum of 4.75V. Column Input Voltage, V_{COL}, can be decreased to the recommended minimum values of 2.6V for the HDSP-2300 and 2.75V for the HDSP-2301/-2302/-2303. Also, the average drive current can be decreased through pulse width modulation of V_B.

The HDSP-2300/-2301/-2302/-2303 displays have glass windows. A front panel contrast enhancement filter is desirable in most actual display applications. Some suggested filter materials are provided in Figure 9. Additional information on filtering and constrast enhancement can be found in HP Application Note 1015.

Post solder cleaning may be accomplished using water or Freon/alcohol mixtures formulated for vapor cleaning processing or Freon/alcohol mixtures formulated for room temperature cleaning. Freon/alcohol vapor cleaning processing for up to 2 minutes in vapors at boiling is permissible. Suggested solvents include Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15, and water.

HEWLETT PACKARD

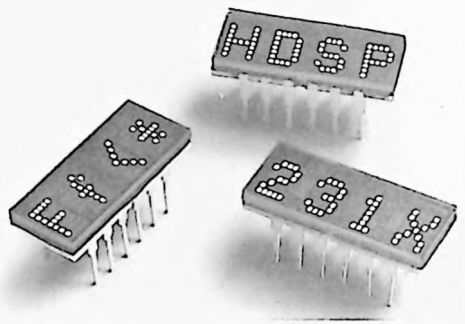
HERMETIC, EXTENDED TEMPERATURE RANGE 5.0mm (.20") 5x7 ALPHANUMERIC DISPLAYS

STANDARD RED	HDSP-2310/2310TXV/2310TXVB
YELLOW	HDSP-2311/2311TXV/2311TXVB
HIGH EFFICIENCY RED	HDSP-2312/2312TXV/2312TXVB

TECHNICAL DATA JANUARY 1984

Features

- WIDE OPERATING TEMPERATURE RANGE -55° C TO +85° C
- TRUE HERMETIC PACKAGE
- CAPABLE OF LEVEL A MIL-D-87157
- THREE COLORS
  Standard Red
  High Efficiency Red
  Yellow
- CATEGORIZED FOR LUMINOUS INTENSITY
- YELLOW DISPLAYS CATEGORIZED FOR COLOR
- INTEGRATED SHIFT REGISTERS WITH CONSTANT CURRENT DRIVERS
- 5x7 LED MATRIX DISPLAYS FULL ASCII CHARACTER SET
- WIDE VIEWING ANGLE
- END STACKABLE
- TTL COMPATIBLE



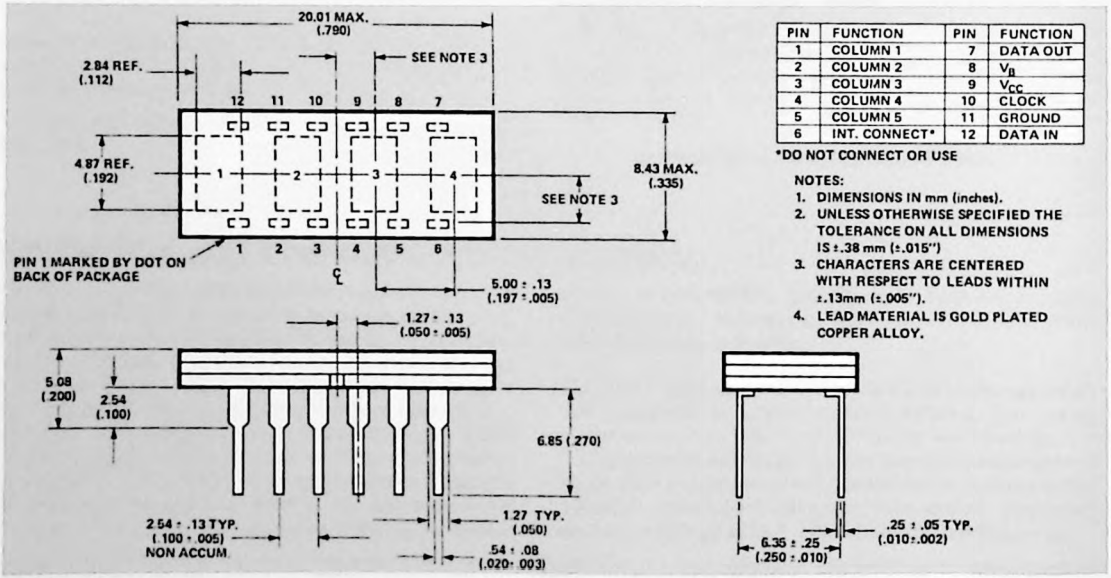
Typical Applications

- MILITARY EQUIPMENT
- AVIONICS
- HIGH RELIABILITY INDUSTRIAL EQUIPMENT

Description

The HDSP-2310 series displays are 5.0mm (0.20 in.) 5x7 LED arrays for display of alphanumeric information. These devices are available in standard red, yellow and high efficiency red. Each four character cluster is contained in a hermetic 12 pin dual-in-line, solder glass sealed ceramic package. An on-board SIPO (Serial-In-Parallel-Out) 7-bit shift register associated with each digit controls constant current LED row drivers. Full character display is achieved by external column strobing.

Package Dimensions



PIN	FUNCTION	PIN	FUNCTION
1	COLUMN 1	7	DATA OUT
2	COLUMN 2	8	V_B
3	COLUMN 3	9	V_{CC}
4	COLUMN 4	10	CLOCK
5	COLUMN 5	11	GROUND
6	INT. CONNECT*	12	DATA IN

*DO NOT CONNECT OR USE

NOTES:
1. DIMENSIONS IN mm (inches).
2. UNLESS OTHERWISE SPECIFIED THE TOLERANCE ON ALL DIMENSIONS IS ±.38 mm (±.015").
3. CHARACTERS ARE CENTERED WITH RESPECT TO LEADS WITHIN ±.13mm (±.005").
4. LEAD MATERIAL IS GOLD PLATED COPPER ALLOY.

Absolute Maximum Ratings (HDSP-2310/-2311/-2312)

Supply Voltage V_{CC} to Ground ..... −0.5V to 6.0V
Inputs, Data Out and V_B ..... −0.5V to V_{CC}
Column Input Voltage, V_{COL} ..... −0.5V to +6.0V
Free Air Operating
Temperature Range, T_A [1,2] ..... −55°C to +85°C
Storage Temperature Range, T_S ..... −65°C to +125°C
Maximum Allowable Package Dissipation
at T_A = 25°C [1,2,3] ..... 1.46 Watts
Maximum Solder Temperature 1.59 mm (.063")
Below Seating Plane t < 5 secs ..... 260°C

Recommended Operating Conditions (HDSP-2310/-2311/-2312)

Parameter	Symbol	Min.	Nom.	Max.	Units	Fig.
Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
Data Out Current, Low State	I_{OL}			1.6	mA	
Data Out Current, High State	I_{OH}			-0.5	mA	
Column Input Voltage, Column On HDSP-2310	V_{COL}	2.4		3.5	V	4
Column Input Voltage, Column On HDSP-2311/-2312/-2313	V_{COL}	2.75		3.5	V	4
Setup Time	t_{setup}	70	45		ns	1
Hold Time	t_{hold}	30	0		ns	1
Width of Clock	$t_{w(Clock)}$	75			ns	1
Clock Frequency	f_{clock}	0		3	MHz	1
Clock Transition Time	t_{THL}			200	ns	1
Free Air Operating Temperature Range [1,2]	T_A	-55		85	°C	

Electrical Characteristics Over Operating Temperature Range

(Unless otherwise specified)

Description		Symbol	Test Conditions		Min.	Typ.*	Max.	Units	Fig.
Supply Current		I_{CC}	V_{CC} = 5.25V, V_{CLOCK} = V_{DATA} = 2.4V, All SR Stages = Logical 1	V_B = 0.4V		45	60	mA	
				V_B = 2.4V		73	95	mA	
Column Current at any Column Input		I_{COL}	V_{CC} = 5.25 V, V_{COL} = 3.5V	V_B = 0.4V			500	µA	4
Column Current at any Column Input		I_{COL}	All SR Stages = Logical 1	V_B = 2.4V		380	520	mA	
V_B, Clock or Data Input Threshold High		V_{IH}	V_{CC} = 4.75V		2.0			V	
V_B, Data Input Threshold Low		V_{IL}					0.8	V	
Clock Input Threshold Low		V_{IL}					0.6	V	
Input Current Logical 1	V_B, Clock	I_{IH}	V_{CC} = 5.25V, V_{IH} = 2.4V			20	80	µA	
	Data In	I_{IH}				10	40	µA	
Input Current Logical 0	V_B, Clock	I_{IL}	V_{CC} = 5.25V, V_{IL} = 0.4V			-500	-800	µA	
	Data In	I_{IL}				-250	-400	µA	
Data Out Voltage		V_{OH}	V_{CC} = 4.75V, I_{OH} = -0.5 mA, I_{COL} = 0 mA		2.4	3.4		V	
		V_{OL}	V_{CC} = 4.75V, I_{OL} = 1.6 mA, I_{COL} = 0 mA			0.2	0.4	V	
Power Dissipation Per Package**		P_D	V_{CC} = 5.0V, V_{COL} = 3.5V, 17.5% DF, 15 LEDs on per character, V_B = 2.4V			0.78		W	2
Thermal Resistance IC Junction-to-Case		$R\theta_{J-C}$				25		°C/W/ Device	2
Leak Rate							$5x10^{-8}$	cc/sec	

*All typical values specified at V_{CC} = 5.0V and T_A = 25°C unless otherwise noted.

**Power dissipation per package with four characters illuminated.

Notes:

1. Operation above 85°C ambient is possible provided the IC junction temperature, T_J, does not exceed 125°C.
2. The device should be derated linearly above 37°C at 16.7 mW/°C. This derating is based on a device mounted in a socket having a thermal resistance from case to ambient at 35° C/W per device. See Figure 2 for power deratings based on a lower thermal resistance.
3. Maximum allowable dissipation is derived from V_{CC} = 5.25V, V_B = 2.4V, V_{COL} = 3.5V 20 LEDs on per character, 20% DF.

Optical Characteristics

STANDARD RED HDSP-2310

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED[4,8] (Character Average)	I_{vPeak}	V_{CC} = 5.0V, V_{COL} = 3.5V T_J = 25°C[6], V_B = 2.4V	220	370		µcd	3
Peak Wavelength	λ_{PEAK}			655		nm	
Dominant Wavelength[7]	λ_d			639		nm	

YELLOW HDSP-2311

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED[4,8] (Character Average)	I_{vPeak}	V_{CC} = 5.0V, V_{COL} = 3.5V T_J = 25°C[6], V_B = 2.4V	650	1140		µcd	3
Peak Wavelength	λ_{PEAK}			583		nm	
Dominant Wavelength[5,7]	λ_d			585		nm	

HIGH EFFICIENCY RED HDSP-2312

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED[4,8] (Character Average)	I_{vPeak}	V_{CC} = 5.0V, V_{COL} = 3.5V T_J = 25°C[6], V_B = 2.4V	650	1430		µcd	3
Peak Wavelength	λ_{PEAK}			635		nm	
Dominant Wavelength[7]	λ_d			626		nm	

*All typical values specified at V_{CC} = 5.0V and T_A = 25°C unless otherwise noted.

**Power dissipation per package with four characters illuminated.

Notes:

4. The characters are categorized for luminous intensity with the intensity category designated by a letter code on the bottom of the package.
5. The HDSP-2311 is categorized for color with the color category designated by a number code on the bottom of the package.
6. The luminous intensity is measured at $T_A = T_J$ = 25°C. No time is allowed for the device to warm-up prior to measurement.
7. Dominant wavelength λ_d, is derived from the CIE chromaticity diagram, and represents the single wavelength which defines the color of the device.
8. The luminous sterance of the LED may be calculated using the following relationships:

   L_V (cd/m²) = I_V (Candela)/A (Metre)²

   L_V (Footlamberts) = πI_V = (Candela)/A (Foot)²

   A = 5.3 x 10^{-8} M^2 = 5.8 x 10^{-7} (Foot)²

Electrical Description

The HDSP-2310 series of four charater alphanumeric displays have been designed to allow the user maximum flexibility in interface electronics design. Each four character module is arranged as a 28 bit serial in parallel out shift register as is shown in Figure 5. The display module features Data In and Data Out terminals arrayed for easy PC board interconnection. Data Out represents the output of the 7th bit of digit number 4 shift register. Shift register clocking occurs on the high to low transition of the Clock input. The like columns of each character in a display cluster are tied to a single pin. Figure 5 is the block diagram for the displays. High true data in the shift register enables the output current mirror driver stage associated with each row of LEDs in the 5x7 diode array.

The TTL compatible V_B input may either be tied to V_{CC} for maximum display intensity or pulse width modulated to achieve intensity control and reduction in power consumption.

In the normal mode of operation, input data for digit 4, column 1 is loaded into the 7 on-board shift register locations 1 through 7. Column 1 data for digits 3, 2, and 1 is similarly shifted into the display shift register locations. The column 1 input is now enabled for an appropriate period of time, T. A similar process is repeated for columns 2, 3, 4 and 5. If the time necessary to decode and load data into the shift register is t, then with 5 columns, each column of the display is operating at a duty factor of:

$$D.F. = \frac{T}{5(t+T)}$$

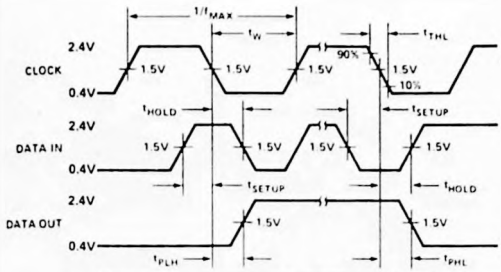
The time rrame, t + T, alloted to each column of the display is generally chosen to provide the maximum duty factor consistent with the minimum refresh rate necessary to achieve a flicker free display. For most strobed display systems, each column of the display should be refreshed (turned on) at a minimum rate of 100 times per second.

With five columns to be addressed, this refresh rate then gives a value for the time t + T of:

$$1/[5 \times (100)] = 2 \text{ msec}$$

If the device is operated at 3.0 MHz clock rate maximum, it is possible to maintain t<<T. For short display strings, the duty factor will then approach 20%.

For further applications information, refer to HP Application Note 1016.



Parameter	Condition	Min.	Typ.	Max.	Units
f_{clock} CLOCK Rate				3	MHz
t_{PLH}, t_{PHL} Propagation delay CLOCK to DATA OUT	C_L = 15pF R_L=2.4KΩ			125	ns

Figure 1. Switching Characteristics HDSP-2310/2311/-2312 (T_A = -55°C to +85°C)

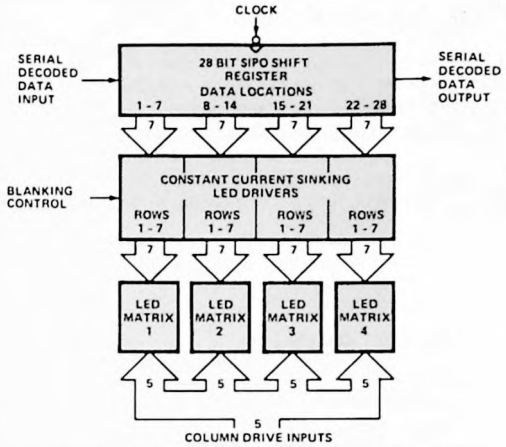


Figure 5. Block Diagram of HDSP-2310/-2311/-2312

Mechanical and Thermal Considerations

The HDSP-2310 series displays are available in standard ceramic dual-in-line packages. They are designed for plugging into sockets or soldering into PC boards. The packages may be horizontally or vertically stacked for character arrays of any desired size. HDSP-2310 series displays utilize a high output current IC to provide excellent readability in bright ambient lighting. Full power operation (V_{CC} = 5.25V, V_B = 2.4V, V_{COL} = 3.5V) with worst case thermal resistance from IC junction to ambient of 60°C/watt/device is possible up to ambient temperature of 37°C. For operation above 37°C, the maximum device dissipation should be derated linearly at 16.7 mW/°C (see Figure 2). With an improved thermal design, operation at higher ambient temperatures without derating is possible.

Power derating for this family of displays can be achieved in several ways. The power supply voltage can be lowered to a minimum of 4.75V. Column Input Voltage, V_{COL}, can be decreased to the recommended minimum values of 2.4V for the HDSP-2310 and 2.75V for the HDSP-2311/-2312. Also, the average drive current can be decreased through pulse width modulation of V_B.

The HDSP-2310 series displays have integral glass windows. A front panel contrast enhancement filter is desirable in most actual display applications. Some suggested filter materials are provided in Figure 6. Additional information on filtering and contrast enhancement can be found in HP Application Note 1015.

Post solder cleaning may be accomplished using water or Freon/alcohol mixtures formulated for vapor cleaning processing or Freon/alcohol mixtures formulated for room temperature cleaning. Freon/alcohol vapor cleaning processing for up to 2 minutes in vapors at boiling is permissible. Suggested solvents include Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15, and water.

Display Color	Ambient Lighting		
	Dim	Moderate	Bright
HDSP-2310 Std. Red	Panelgraphic Dark Red 63 Ruby Red 60 Chequers Red 118 Plexiglass 2423	Polaroid HNCP37 3M Light Control Film Panelgraphic Gray 10	
HDSP-2311 (Yellow)	Panelgraphic Yellow 27 Chequers Amber 107	Chequers Grey 105	Polaroid HNCP10
HDSP-2312 (HER)	Panelgraphic Ruby Red 60 Chequers Red 112		

Figure 6. Contrast Enhancement Filters

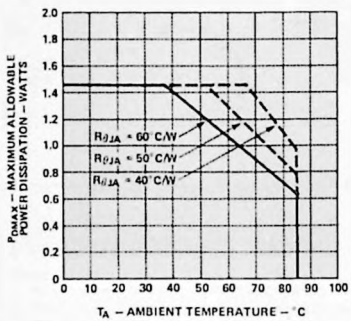


Figure 2. Maximum Allowable Power Dissipation vs. Temperature

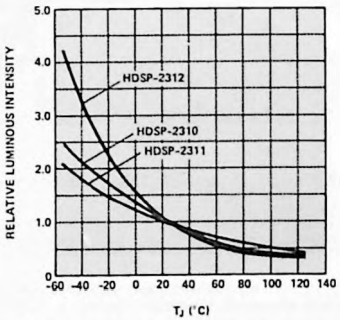


Figure 3. Relative Luminous Intensity vs. Temperature

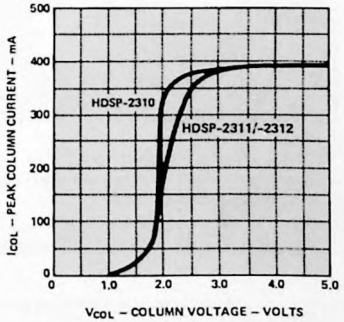


Figure 4. Peak Column Current vs. Column Voltage

High Reliability Testing

Two standard reliability testing programs are available. The TXVB program is in conformance with Quality Level A of MIL-D-87157 for hermetically sealed LED displays with 100% screening tests. A TXVB product is tested to Tables I, II, IIIa, and IVa. The TXV program is an HP modification to the full conformance program and offers the 100% screening of Quality Level A, Table I, and Group A, Table II.

Part Marking System

Standard Product	With Table I and II	With Tables I, II, IIIa, IVa
HDSP-2310 HDSP-2311 HDSP-2312	HDSP-2310 TXV HDSP-2311 TXV HDSP-2312 TXV	HDSP-2310 TXVB HDSP-2311 TXVB HDSP-2312 TXVB

100% Screening

Table I. Quality Level A of MIL-D-87157

Test Screen	Method	Conditions
1. Precap Visual	—	HP Procedure 5956-7512-52, based on MIL-STD-883B
2. High Temperature Storage	MIL-STD-750 Method 1032	T_A = 125° C, Time = 24 hours
3. Temperature Cycling	MIL-STD-750 Method 1051	Condition B, 10 cycles, 15 min. dwell
4. Constant Acceleration	MIL-STD-750 Method 2006	10,000 G's at Y_1 orientation
5. Fine Leak	MIL-STD-750 Method 1071	Condition H
6. Gross Leak	MIL-STD-750 Method 1071	Condition C
7. Interim Electrical/Optical Tests[2]	—	I_{CC} (at V_B = 0.4V and 2.4V), I_{COL} (at V_B = 0.4V and 2.4V) I_{IH} (V_B, Clock and Data In), I_{IL} (V_B, Clock and Data In), I_{OH}, I_{OL}, Visual Function and Iv Peak. V_{IH} and V_{IL} inputs are guaranteed by the electronic shift register test. T_A = 25° C
8. Burn-In[1]	MIL-STD-883 Method 1015	Condition B at V_{CC} = V_B = 5.25V, V_{COL} = 3.5V, T_A = +85° C, LED ON-Time Duty Factor = 5%, 35 Dots On; t = 168 hours
9. Final Electrical Test[2]	—	Same as Step 7
10. Delta Determinations	—	ΔI_{CC} = ±6 mA, ΔI_{IH} (clock) = ±10 μA, ΔI_{IH} (Data In) = ±10 μA ΔI_{OH} = ±10% of initial value, and ΔIv = -20%, T_A = 25° C
11. External Visual	MIL-STD-883 Method 2009	

Notes:
1. MIL-STD-883 Test Method Applies
2. Limits and conditions are per the electrical optical characteristics. The I_{OH} and I_{OL} tests are the inverse of V_{OH} and V_{OL} specified in the electrical characteristics.

Table II. Group A Electrical Tests — MIL-D-87157

Subgroup/Test	Parameters	LTPD
Subgroup 1 DC Electrical Tests at 25°C[1]	I_{CC} (at V_B = 0.4V and 2.4V), I_{COL} (at V_B = 0.4V and 2.4V) I_{IH} (V_B, Clock and Data In), I_{IL} (V_B, Clock and Data In), I_{OH}, I_{OL} Visual Function and Iv peak. V_{IH} and V_{IL} inputs are guaranteed by the electronic shift register test.	5
Subgroup 2 DC Electrical Tests at High Temperature[1]	Same as Subgroup 1, except delete Iv and visual function, T_A = +85°C	7
Subgroup 3 DC Electrical Tests at Low Temperature[1]	Same as Subgroup 1, except delete Iv and visual function, T_A = -55°C	7
Subgroup 4, 5, and 6 not tested		
Subgroup 7 Optical and Functional Tests at 25°C	Satisfied by Subgroup 1	5
Subgroup 8 External Visual		7

Note:
1. Limits and conditions are per the electrical/optical characteristics. The I_{OH} and I_{OL} tests are the inverse of V_{OH} and V_{OL} specified in the electrical characteristics.

Table IIIa. Group B, Class A and B of MIL-D-87157

Subgroup/Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1 Resistance to Solvents	1022		4 Devices/ 0 Failures
Internal Visual and Mechanical[3]	2014		1 Device/ 0 Failures
Subgroup 2[1,2] Solderability	2026	T_A = 260°C for 5 seconds	LTPD = 15
Subgroup 3 Thermal Shock (Temp. Cycle)	1051	Condition B, 10 cycles, 15 min. dwell	LTPD = 15
Moisture Resistance	1021		
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C	
Electrical/Optical Endpoints[4]	—	I_{CC} (at V_B = 0.4V and 2.4V), I_{COL} (at V_B = 0.4V and 2.4V), I_{IH} (V_B, Clock and Data In), I_{IL} (V_B, Clock and Data In), I_{OH}, I_{OL} Visual Function and Iv peak. V_{IH} and V_{IL} inputs are guaranteed by the electronic shift register test. T_A = 25°C	
Subgroup 4 Operating Life Test (340 hrs.)	1027	T_A = +85°C at V_{CC} = V_B = 5.25V, V_{COL} = 3.5V, LED ON-Time Duty Factor = 5%, 35 Dots On	LTPD = 10
Electrical/Optical Endpoints[4]	—	Same as Subgroup 3	
Subgroup 5 Non-operating (Storage) Life Test (340 hrs.)	1032	T_A = +125°C	LTPD = 10
Electrical/Optical Endpoints[4]	—	Same as Subgroup 3	

Notes:
1. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
2. The LTPD applies to the number of leads inspected except in no case shall less than 3 displays be used to provide the number of leads required.
3. MIL-STD-883 test methods apply.
4. Limits and conditions are per the electrical/optical characteristics. The I_{OH} and I_{OL} tests are the inverse of V_{OH} and V_{OL} specified in the electrical characteristics.

Table IVa. Group C, Class A and B of MIL-D-87157

Subgroup/Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1			
Physical Dimensions	2066		2 Devices/ 0 Failures
Subgroup 2[2,7]			
Lead Integrity	2004	Condition B2	LTPD = 15
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C	
Subgroup 3			
Shock	2016	1500G, Time = 0.5 ms, 5 blows in each orientation X_1, Y_1, Y_2	LTPD = 15
Vibration, Variable Frequency	2056		
Constant Acceleration	2006	10,000G at Y_1 orientation	
External Visual[4]	1010 or 1011		
Electrical/Optical Endpoints[8]	—	I_{CC} (at V_B = 0.4V and 2.4V) I_{COL} (at V_B = 0.4V and 2.4V) I_{IH} (V_B, Clock and Data In) I_{IL} (V_B, Clock and Data In) I_{OH}, I_{OL}, Visual Function and Iv peak. V_{IH} and V_{IL} inputs are guaranteed by the electronic shift register test. T_A = 25°C.	
Subgroup 4[1,3]			
Salt Atmosphere	1041		LTPD = 15
External Visual[4]	1010 or 1011		
Subgroup 5			
Bond Strength[5]	2037	Condition A	LTPD = 20 (C = 0)
Subgroup 6			
Operating Life Test[6]	1026	T_A = +85°C at V_{CC} = V_B = 5.25V, V_{COL} = 3.5V, 35 Dots On	λ = 10
Electrical/Optical Endpoints[8]	—	Same as Subgroup 3	

Notes:

1. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
2. The LTPD applies to the number of leads inspected except in no case shall less than three displays be used to provide the number of leads required.
3. Solderability samples shall not be used.
4. Visual requirements shall be as specified in MIL-STD-883, Methods 1010 or 1011.
5. Displays may be selected prior to seal.
6. If a given inspection lot undergoing Group B inspection has been selected to satisfy Group C inspection requirements, the 340 hour life tests may be continued on test to 1000 hours in order to satisfy the Group C life test requirements. In such cases, either the 340 hour endpoint measurements shall be made a basis for Group B lot acceptance or the 1000 hour endpoint measurement shall be used as the basis for both Group B and Group C acceptance.
7. MIL-STD-883 test method applies.
8. Limits and conditions are per the electrical/optical characteristics. The I_{OH} and I_{OL} tests are the inverse of V_{OH} and V_{OL} specified in the electrical characteristics.

HEWLETT PACKARD

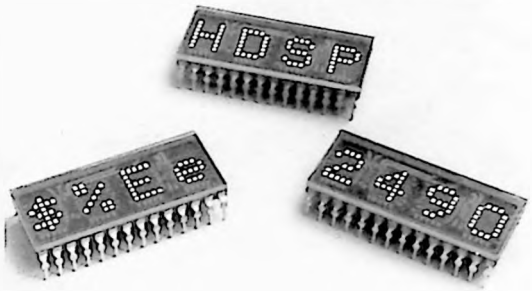
FOUR CHARACTER 6.9 mm (0.27 INCH) 5x7 ALPHANUMERIC DISPLAYS

STANDARD RED	HDSP-2490
YELLOW	HDSP-2491
HIGH EFFICIENCY RED	HDSP-2492
HIGH PERFORMANCE GREEN	HDSP-2493

TECHNICAL DATA JANUARY 1984

Features

- FOUR COLORS
  Standard Red
  Yellow
  High Efficiency Red
  High Performance Green
- INTEGRATED SHIFT REGISTERS WITH CONSTANT CURRENT DRIVERS
- COMPACT CERAMIC PACKAGE
- WIDE VIEWING ANGLE
- END STACKABLE FOUR CHARACTER PACKAGE
- TTL COMPATIBLE
- 5 x 7 LED MATRIX DISPLAYS FULL ASCII SET
- CATEGORIZED FOR LUMINOUS INTENSITY
- HDSP-2491/2493 ALSO CATEGORIZED FOR COLOR



Typical Applications

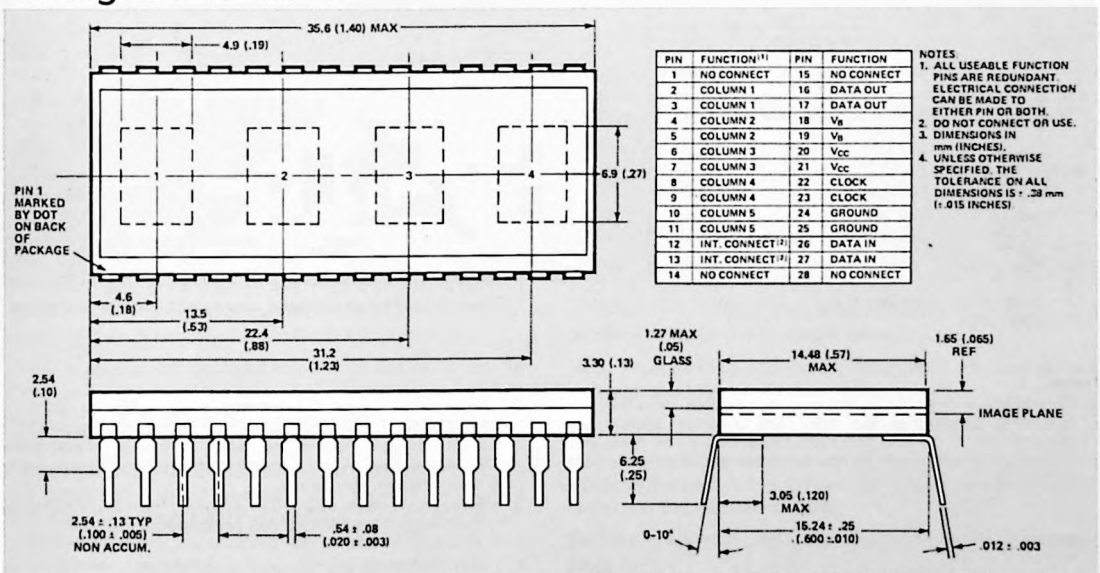
- Instruments
- Business Machines
- Industrial Process Control Equipment
- Medical Instruments

Description

The HDSP-2490/-2491/-2492/-2493 series of displays are 6.9 mm (0.27 inch) 5 x 7 LED arrays for display of alphanumeric information. These devices are available in standard red, yellow, high efficiency red, and high performance green.

Each four character cluster is contained in a 28 pin dual-in-line package. An on-board SIPO (Serial-In-Parallel-Out) 7-bit shift register associated with each digit controls constant current LED row drivers. Full character display is achieved by external column strobing.

Package Dimensions



PIN	FUNCTION[1]	PIN	FUNCTION
1	NO CONNECT	15	NO CONNECT
2	COLUMN 1	16	DATA OUT
3	COLUMN 1	17	DATA OUT
4	COLUMN 2	18	V_B
5	COLUMN 2	19	V_B
6	COLUMN 3	20	V_{CC}
7	COLUMN 3	21	V_{CC}
8	COLUMN 4	22	CLOCK
9	COLUMN 4	23	CLOCK
10	COLUMN 5	24	GROUND
11	COLUMN 5	25	GROUND
12	INT. CONNECT[2]	26	DATA IN
13	INT. CONNECT[2]	27	DATA IN
14	NO CONNECT	28	NO CONNECT

NOTES:
1. ALL USEABLE FUNCTION PINS ARE REDUNDANT. ELECTRICAL CONNECTION CAN BE MADE TO EITHER PIN OR BOTH.
2. DO NOT CONNECT OR USE.
3. DIMENSIONS IN mm (INCHES).
4. UNLESS OTHERWISE SPECIFIED, THE TOLERANCE ON ALL DIMENSIONS IS ± .38 mm (± .015 INCHES).

Absolute Maximum Ratings (HDSP-2490/-2491/-2492/-2493)

Supply Voltage V_{CC} to Ground ..... −0.5V to 6.0V
Inputs, Data Out and V_B ..... −0.5V to V_{CC}
Column Input Voltage, V_{COL} ..... −0.5V to +6.0V
Free Air Operating
Temperature Range, T_A [1,2] ..... −20°C to +85°C

Storage Temperature Range, T_S ..... −55°C to +100°C
Maximum Allowable Package Dissipation
at T_A = 25°C [1,2,3] ..... 1.46 Watts
Maximum Solder Temperature 1.59 mm (0.63") Below Seating Plane t < 5 sec ..... 260°C

Recommended Operating Conditions (HDSP-2490/-2491/-2492/-2493)

Parameter	Symbol	Min.	Nom.	Max.	Units	Fig.
Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
Data Out Current, Low State	I_{OL}			1.6	mA	
Data Out Current, High State	I_{OH}			-0.5	mA	
Column Input Voltage, Column On HDSP-2490	V_{COL}	2.4		3.5	V	4
Column Input Voltage, Column On HDSP-2491/-2492/-2493	V_{COL}	2.75		3.5	V	4
Setup Time	t_{setup}	70	45		ns	1
Hold Time	t_{hold}	30	0		ns	1
Width of Clock	$t_{w(Clock)}$	75			ns	1
Clock Frequency	f_{clock}	0		3	MHz	1
Clock Transition Time	t_{THL}			200	ns	1
Free Air Operating Temperature Range [1,2]	T_A	-20		85	°C	2

Electrical Characteristics Over Operating Temperature Range

(Unless otherwise specified)

Description		Symbol	Test Conditions		Min.	Typ.*	Max.	Units	Fig.
Supply Current		I_{CC}	V_{CC} = 5.25V, V_{CLOCK} = V_{DATA} = 2.4V, All SR Stages = Logical 1	V_B = 0.4V		45	60	mA	
				V_B = 2.4V		73	95	mA	
Column Current at any Column Input		I_{COL}	V_{CC} = 5.25 V, V_{COL} = 3.5V	V_B = 0.4V			500	µA	4
Column Current at any Column Input		I_{COL}	All SR Stages = Logical 1	V_B = 2.4V		380	520	mA	
V_B, Clock or Data Input Threshold High		V_{IH}	V_{CC} = V_{COL} = 4.75V		2.0			V	
V_B, Clock or Data Input Threshold Low		V_{IL}					0.8	V	
Input Current Logical 1	V_B, Clock	I_{IH}	V_{CC} = 5.25V, V_{IH} = 2.4V			20	80	µA	
	Data In	I_{IH}				10	40	µA	
Input Current Logical 0	V_B, Clock	I_{IL}	V_{CC} = 5.25V, V_{IL} = 0.4V			-500	-800	µA	
	Data In	I_{IL}				-250	-400	µA	
Data Out Voltage		V_{OH}	V_{CC} = 4.75V, I_{OH} = -0.5 mA, I_{COL} = 0 mA		2.4	3.4		V	
		V_{OL}	V_{CC} = 4.75V, I_{OL} = 1.6 mA, I_{COL} = 0 mA			0.2	0.4	V	
Power Dissipation Per Package**		P_D	V_{CC} = 5.0V, V_{COL} = 3.5V, 17.5% DF, 15 LEDs on per character, V_B = 2.4V			0.78		W	2
Thermal Resistance IC Junction-to-Case		$R\theta_{J-C}$				20		°C/W/ Device	2

*All typical values specified at V_{CC} = 5.0V and T_A = 25°C unless otherwise noted.

**Power dissipation per package with four characters illuminated.

Notes:

1. Operation above 85°C ambient is possible provided the following conditions are met. The junction should not exceed 125°C T_J and the case temperature (as measured at pin 1 or the back of the display) should not exceed 100°C T_C.
2. The device should be derated linearly above 60°C at 22.2 mW/°C. This derating is based on a device mounted in a socket having a thermal resistance from case to ambient at 25°C/W per device. See Figure 2 for power deratings based on a lower thermal resistance.
3. Maximum allowable dissipation is derived from V_{CC} = 5.25V, V_B = 2.4V, V_{COL} = 3.5V 20 LEDs on per character, 20% DF.

Optical Characteristics

STANDARD RED HDSP-2490

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED[4,8] (Character Average)	I_{VPeak}	V_{CC} = 5.0V, V_{COL} = 3.5V T_j = 25° C[6], V_B = 2.4V	220	370		µcd	3
Peak Wavelength	λ_{PEAK}			655		nm	
Dominant Wavelength[7]	λ_d			639		nm	

YELLOW HDSP-2491

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED[4,8] (Character Average)	I_{VPeak}	V_{CC} = 5.0V, V_{COL} = 3.5V T_j = 25° C[6], V_B = 2.4V	850	1400		µcd	3
Peak Wavelength	λ_{PEAK}			583		nm	
Dominant Wavelength[5,7]	λ_d			585		nm	

HIGH EFFICIENCY RED HDSP-2492

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED[4,8] (Character Average)	I_{VPeak}	V_{CC} = 5.0V, V_{COL} = 3.5V T_j = 25° C[6], V_B = 2.4V	850	1530		µcd	3
Peak Wavelength	λ_{PEAK}			635		nm	
Dominant Wavelength[7]	λ_d			626		nm	

HIGH PERFORMANCE GREEN HDSP-2493

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED[4,8] (Character Average)	I_{VPeak}	V_{CC} = 5.0V, V_{COL} = 3.5V T_j = 25° C[6], V_B = 2.4V	1280	2410		µcd	3
Peak Wavelength	λ_{PEAK}			568		nm	
Dominant Wavelength[5,7]	λ_d			574		nm	

*All typical values specified at V_{CC} = 5.0V and T_A = 25° C unless otherwise noted.

**Power dissipation per package with four characters illuminated.

Notes:

4. The characters are categorized for luminous intensity with the intensity category designated by a letter code on the bottom of the package.
5. The HDSP-2491/-2493 are categorized for color with the color category designated by a number code on the bottom of the package.
6. T_j refers to the initial case temperature of the device immediately prior to the light measurement.
7. Dominant wavelength λ_d, is derived from the CIE chromaticity diagram, and represents the single wavelength which defines the color of the device.
8. The luminous sterance of the LED may be calculated using the following relationships:
   L_v (cd/m^2) = I_v (Candela)/A (Metre)^2
   L_v (Footlamberts) = πI_v (Candela)/A (Foot)^2
   A = 5.3 x 10^{-8} M^2 = 5.8 x 10^{-7} (Foot)^2

Electrical Description

The HDSP-249X series of four character alphanumeric displays have been designed to allow the user maximum flexibility in interface electronics design. Each four character display module features Data In and Data Out terminals arrayed for easy PC board interconnection. Data Out represents the output of the 7th bit of digit number 4 shift register. Shift register clocking occurs on the high to low transition of the clock input. The like columns of each character in a display cluster are tied to a single pin. Figure 5 is the block diagram for the displays. High true data in the shift register enables the output current mirror driver stage associated with each row of LEDs in the 5 x 7 diode array.

The TTL compatible V_B input may either be tied to V_{CC} for maximum display intensity or pulse width modulated to achieve intensity control and reduction in power consumption.

The normal mode of operation input data for digit 4, column 1 is loaded into the 7 on-board shift register locations 1 through 7 . Column 1 data for digits 3, 2, and 1 is similarly shifted into the display shift register locations. The column 1 input is now enabled for an appropriate period of time, T. A similar process is repeated for columns 2, 3, 4 and 5. If the time necessary to decode and load data into the shift register is t, then with 5 columns, each column of the display is operating at a duty factor of:

$$D.F. = \frac{T}{5\,(t+T)}$$

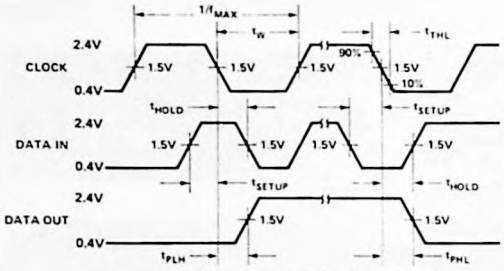
The time frame, t + T, alloted to each column of the display is generally chosen to provide the maximum duty factor consistent with the minimum refresh rate necessary to achieve a flicker free display. For most strobed display systems, each column of the display should be refreshed (turned on) at a minimum rate of 100 times per second.

With columns to be addressed, this refresh rate then gives a value for the time t + T of:

$$1/[5 \times (100)] = 2 \text{ msec}$$

If the device is operated at 3.0 MHz clock rate maximum, it is possible to maintain t << T. For short display strings, the duty factor will then approach 20%.

For further applications information, refer to HP Application Note 1016.



Parameter	Condition	Min.	Typ.	Max.	Units
f_{clock} CLOCK Rate				3	MHz
t_{PLH}, t_{PHL} Propagation delay CLOCK to DATA OUT	C_L = 15pF R_L=2.4KΩ			125	ns

Figure 1. Switching Characteristics HDSP-2490/-2491/-2492/-2493 (T_A = -20°C to +85°C)

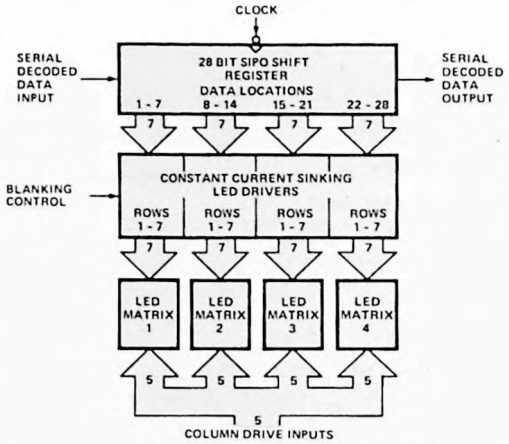


Figure 5. Block Diagram of HDSP-2490/-2491/-2492/-2493

Mechanical and Thermal Considerations

The HDSP-2490/-2491/-2492/-2493 are available in standard ceramic dual-in-line packages. They are designed for plugging into sockets or soldering into PC boards. The packages may be horizontally or vertically stacked for character arrays of any desired size. The HDSP-2490/-2491/-2492/-2493 utilize a high output current IC to provide excellent readability in bright ambient lighting. Full power operation (V_{CC} = 5.25V, V_B = 2.4V, V_{COL} = 3.5V) with worst case thermal resistance from IC junction to ambient of 45° C/watt/device is possible up to ambient temperature of 60° C. For operation above 60°C, the maximum device dissipation should be derated linearly at 22.2 mW/°C (see Figure 2). With an improved thermal design, operation at higher ambient temperatures without derating is possible.

Power derating for this family of displays can be achieved in several ways. The power supply voltage can be lowered to a minimum of 4.75V. Column Input Voltage, V_{COL}, can be decreased to the recommended minimum values of 2.4V for the HDSP-2490 and 2.75V for the HDSP-2491/-2492/-2493. Also, the average drive current can be decreased through pulse width modulation of V_B.

The HDSP-2490/-2491/-2492/-2493 displays have glass windows. A front panel contrast enhancement filter is desirable in most actual display applications. Some suggested filter materials are provided in Figure 6. Additional information on filtering and contrast enhancement can be found in HP Application Note 1015.

Post solder cleaning may be accomplished using water or Freon/alcohol mixtures formulated for vapor cleaning processing or Freon/alcohol mixtures formulated for room temperature cleaning. Freon/alcohol vapor cleaning processing for up to 2 minutes in vapors at boiling is permissible. Suggested solvents include Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15, and water.

Display Color	Ambient Lighting		
	Dim	Moderate	Bright
HDSP-2490 Std. Red	Panelgraphic Dark Red 63 Ruby Red 60 Chequers Red 118 Plexiglass 2423		
HDSP-2491 Yellow	Panelgraphic Yellow 27 Chequers Amber 107	Polaroid HNCP37 3M Light Control Film Panelgraphic Gray 10	Note 1
HDSP-2492 HER	Panelgraphic Ruby Red 60 Chequers Red 112	Chequers Grey 105	
HDSP-2493 HP Green	Panelgraphic Green 48 Chequers Green 107		

Note: 1. Optically coated circular polarized filters, such as Polaroid HNCP10.

Figure 6. Contrast Enhancement Filters

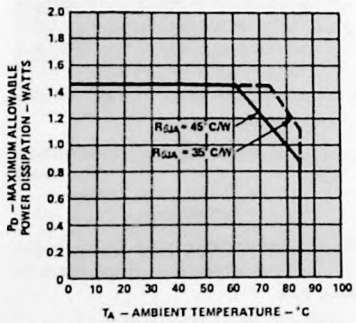


Figure 2. Maximum Allowable Power Dissipation vs. Temperature

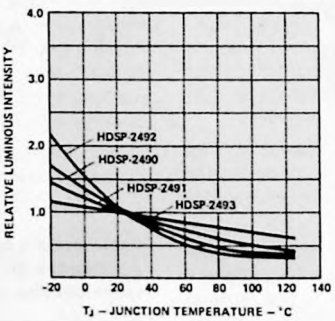


Figure 3. Relative Luminous Intensity vs. Temperature

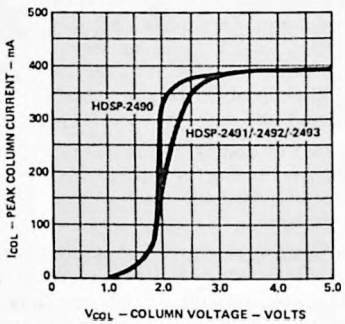


Figure 4. Peak Column Current vs. Column Voltage

HEWLETT PACKARD

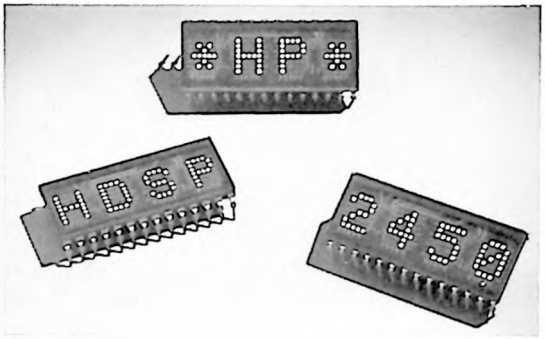
HERMETIC, EXTENDED TEMPERATURE RANGE 6.9mm (.27") 5x7 ALPHANUMERIC DISPLAYS

STANDARD RED	HDSP-2450/2450TXV/2450TXVB
YELLOW	HDSP-2451/2451TXV/2451TXVB
HIGH EFFICIENCY RED	HDSP-2452/2452TXV/2452TXVB

TECHNICAL DATA JANUARY 1984

Features

- WIDE OPERATING TEMPERATURE RANGE -55° C TO +85° C
- TRUE HERMETIC PACKAGE
- CAPABLE OF LEVEL A MIL-D-87157
- THREE COLORS
  Standard Red
  High Efficiency Red
  Yellow
  High Performance Green
- CATEGORIZED FOR LUMINOUS INTENSITY
- YELLOW DISPLAYS CATEGORIZED FOR COLOR
- INTEGRATED SHIFT REGISTERS WITH CONSTANT CURRENT DRIVERS
- 5x7 LED MATRIX DISPLAYS FULL ASCII CHARACTER SET
- WIDE VIEWING ANGLE
- END STACKABLE
- TTL COMPATIBLE



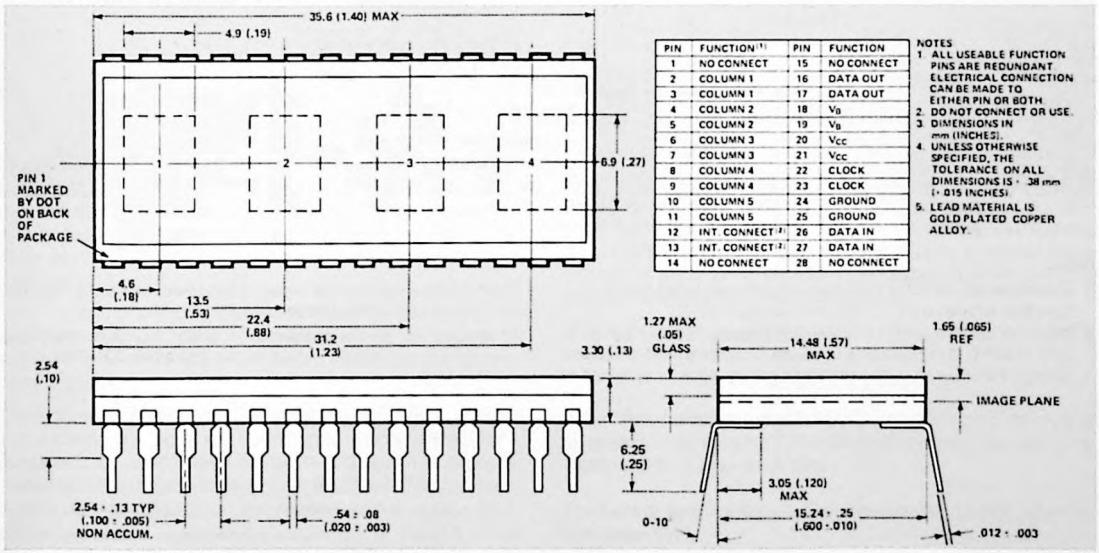
Typical Applications

- MILITARY EQUIPMENT
- AVIONICS
- HIGH RELIABILITY INDUSTRIAL EQUIPMENT

Description

The HDSP-2450 series displays are 6.9mm (0.27 in.) 5x7 LED arrays for display of alphanumeric information. These devices are available in standard red, yellow, high efficiency red and high performance green. Each four character cluster is contained in a hermetic 28 pin dual-in-line, solder glass sealed ceramic package. An on-board SIPO (Serial-In-Parallel-Out) 7-bit shift register associated with each digit controls constant current LED row drivers. Full character display is achieved by external column strobing.

Package Dimensions



PIN	FUNCTION[1]	PIN	FUNCTION
1	NO CONNECT	15	NO CONNECT
2	COLUMN 1	16	DATA OUT
3	COLUMN 1	17	DATA OUT
4	COLUMN 2	18	V_B
5	COLUMN 2	19	V_B
6	COLUMN 3	20	V_{CC}
7	COLUMN 3	21	V_{CC}
8	COLUMN 4	22	CLOCK
9	COLUMN 4	23	CLOCK
10	COLUMN 5	24	GROUND
11	COLUMN 5	25	GROUND
12	INT. CONNECT[2]	26	DATA IN
13	INT. CONNECT[2]	27	DATA IN
14	NO CONNECT	28	NO CONNECT

NOTES
1. ALL USEABLE FUNCTION PINS ARE REDUNDANT ELECTRICAL CONNECTION CAN BE MADE TO EITHER PIN OR BOTH.
2. DO NOT CONNECT OR USE.
3. DIMENSIONS IN mm (INCHES).
4. UNLESS OTHERWISE SPECIFIED, THE TOLERANCE ON ALL DIMENSIONS IS ± .38 mm (± .015 INCHES).
5. LEAD MATERIAL IS GOLD PLATED COPPER ALLOY.

Absolute Maximum Ratings (HDSP-2450/-2451/-2452)

Supply Voltage V_{CC} to Ground ..... −0.5V to 6.0V
Inputs, Data Out and V_B ..... −0.5V to V_{CC}
Column Input Voltage, V_{COL} ..... −0.5V to +6.0V
Free Air Operating
Temperature Range, T_A[1,2] ..... −55°C to +85°C
Storage Temperature Range, Ts ..... −65°C to +125°C
Maximum Allowable Package Dissipation
at T_A = 25°C[1,2,3] ..... 1.46 Watts
Maximum Solder Temperature 1.59 mm (0.63")
Below Seating Plane t < 5 secs ..... 260°C

Recommended Operating Conditions (HDSP-2450/-2451/-2452)

Parameter	Symbol	Min.	Nom.	Max.	Units	Fig.
Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
Data Out Current, Low State	I_{OL}			1.6	mA	
Data Out Current, High State	I_{OH}			-0.5	mA	
Column Input Voltage, Column On HDSP-2450	V_{COL}	2.4		3.5	V	4
Column Input Voltage, Column On HDSP-2451/2452/2453	V_{COL}	2.75		3.5	V	4
Setup Time	t_{setup}	70	45		ns	1
Hold Time	t_{hold}	30	0		ns	1
Width of Clock	$t_{w(Clock)}$	75			ns	1
Clock Frequency	f_{clock}	0		3	MHz	1
Clock Transition Time	t_{THL}			200	ns	1
Free Air Operating Temperature Range[1,2]	T_A	-55		85	°C	

Electrical Characteristics Over Operating Temperature Range

(Unless otherwise specified)

Description		Symbol	Test Conditions		Min.	Typ.*	Max.	Units	Fig.
Supply Current		I_{CC}	V_{CC} = 5.25V, V_{CLOCK} = V_{DATA} = 2.4V, All SR Stages = Logical 1	V_B = 0.4V		45	60	mA	
				V_B = 2.4V		73	95	mA	
Column Current at any Column Input		I_{COL}	V_{CC} = 5.25 V, V_{COL} = 3.5V	V_B = 0.4V			500	µA	4
Column Current at any Column Input		I_{COL}	All SR Stages = Logical 1	V_B = 2.4V		380	520	mA	
V_B, Clock or Data Input Threshold High		V_{IH}	V_{CC} = 4.75V		2.0			V	
V_B, Data Input Threshold Low		V_{IL}					0.8	V	
Clock Input Threshold Low		V_{IL}					0.6	V	
Input Current Logical 1	V_B, Clock	I_{IH}	V_{CC} = 5.25V, V_{IH} = 2.4V			20	80	µA	
	Data In	I_{IH}				10	40	µA	
Input Current Logical 0	V_B, Clock	I_{IL}	V_{CC} = 5.25V, V_{IL} = 0.4V			-500	-800	µA	
	Data In	I_{IL}				-250	-400	µA	
Data Out Voltage		V_{OH}	V_{CC} = 4.75V, I_{OH} = -0.5 mA, I_{COL} = 0 mA		2.4	3.4		V	
		V_{OL}	V_{CC} = 4.75V I_{OL} = 1.6 mA, I_{COL} = 0 mA			0.2	0.4	V	
Power Dissipation Per Package**		P_D	V_{CC} = 5.0V, V_{COL} = 3.5V, 17.5% DF, 15 LEDs on per character, V_B = 2.4V			0.78		W	2
Thermal Resistance IC Junction-to-Case		$R\theta_{J-C}$				20		°C/W/ Device	2
Leak Rate							$5x10^{-8}$	cc/sec	

*All typical values specified at V_{CC} = 5.0V and T_A = 25°C unless otherwise noted.

**Power dissipation per package with four characters illuminated.

Notes:

1. Operation above 85°C ambient is possible provided the IC junction temperature, T_J, does not exceed 125°C.
2. The device should be derated linearly above 60°C at 22.2 mW/°C. This derating is based on a device mounted in a socket having a thermal resistance from case to ambient at 25° C/W per device. See Figure 2 for power deratings based on a lower thermal resistance.
3. Maximum allowable dissipation is derived from V_{CC} = 5.25V, V_B = 2.4V, V_{COL} = 3.5V 20 LEDs on per character, 20% DF.

Optical Characteristics (continued)

STANDARD RED HDSP-2450

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED[4,8] (Character Average)	I_{vPeak}	V_{CC} = 5.0V, V_{COL} = 3.5V T_j = 25°C[6], V_B = 2.4V	220	370		µcd	3
Peak Wavelength	λ_{PEAK}			655		nm	
Dominant Wavelength[7]	λ_d			639		nm	

YELLOW HDSP-2451

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED[4,8] (Character Average)	I_{vPeak}	V_{CC} = 5.0V, V_{COL} = 3.5V T_j = 25°C[6], V_B = 2.4V	850	1400		µcd	3
Peak Wavelength	λ_{PEAK}			583		nm	
Dominant Wavelength[5,7]	λ_d			585		nm	

HIGH EFFICIENCY RED HDSP-2452

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED[4,8] (Character Average)	I_{vPeak}	V_{CC} = 5.0V, V_{COL} = 3.5V T_j = 25°C[6], V_B = 2.4V	850	1530		µcd	3
Peak Wavelength	λ_{PEAK}			635		nm	
Dominant Wavelength[7]	λ_d			626		nm	

*All typical values specified at V_{CC} = 5.0V and T_A = 25°C unless otherwise noted.

**Power dissipation per package with four characters illuminated.

Notes:

4. The characters are categorized for luminous intensity with the intensity category designated by a letter code on the bottom of the package.
5. The HDSP-2451 is categorized for color with the color category designated by a number code on the bottom of the package.
6. The luminous intensity is measured at $T_A = T_j = 25°C$. No time is allowed for the device to warm-up prior to measurement.
7. Dominant wavelength λ_d, is derived from the CIE chromaticity diagram, and represents the single wavelength which defines the color of the device.
8. The luminous sterance of the LED may be calculated using the following relationships:

   L_v (cd/m^2) = I_v (Candela)/A (Metre^2)

   L_v (Footlamberts) = πI_v (Candela)/A (Foot)^2

   A = 5.3 x 10^{-8} M^2 = 5.8 x 10^{-7} Foot^2

Electrical Description

The HDSP-2450 series of four character alphanumeric displays have been designed to allow the user maximum flexibility in interface electronics design. Each four character display module features Data In and Data Out terminals arrayed for easy PC board interconnection. Data Out represents the output of the 7th bit of digit number 4 shift register. Shift register clocking occurs on the high to low transition of the Clock input. The like columns of each character in a display cluster are tied to a single pin. Figure 5 is the block diagram for the displays. High true data in the shift register enables the output current mirror driver stage associated with each row of LEDs in the 5x7 diode array.

The TTL compatible V_B input may either be tied to V_{CC} for maximum display intensity or pulse width modulated to achieve intensity control and reduction in power consumption.

The normal mode of operation input data for digit 4, column 1 is loaded into the 7 on-board shift register locations 1 through 7. Column 1 data for digits 3, 2, and 1 is similarly shifted into the display shift register locations. The column 1 input is now enabled for an appropriate period of time, T. A similar process is repeated for columns 2, 3, 4 and 5. If the time necessary to decode and load data into the shift register is t, then with 5 columns, each column of the display is operating at a duty factor of:

$$D.F. = \frac{T}{5(t+T)}$$

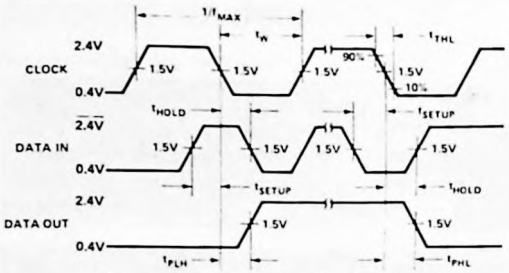
The time frame, t + T, alloted to each column of the display is generally chosen to provide the maximum duty factor consistent with the minimum refresh rate necessary to achieve a flicker free display. For most strobed display systems, each column of the display should be refreshed (turned on) at a minimum rate of 100 times per second.

With columns to be addressed, this refresh rate then gives a value for the time t + T of:

$$1/[5 \times (100)] = 2 \text{ msec}$$

If the device is operated at 3.0 MHz clock rate maximum, it is possible to maintain t<<T. For short display strings, the duty factor will then approach 20%.

For further applications information, refer to HP Application Note 1016.



Parameter	Condition	Min.	Typ.	Max.	Units
f_{clock} CLOCK Rate				3	MHz
t_{PLH}, t_{PHL} Propagation delay CLOCK to DATA OUT	C_L = 15pF R_L = 2.4KΩ			125	ns

Figure 1. Switching Characteristics HDSP-2450/-2451/-2452 (T_A = -55°C to +85°C)

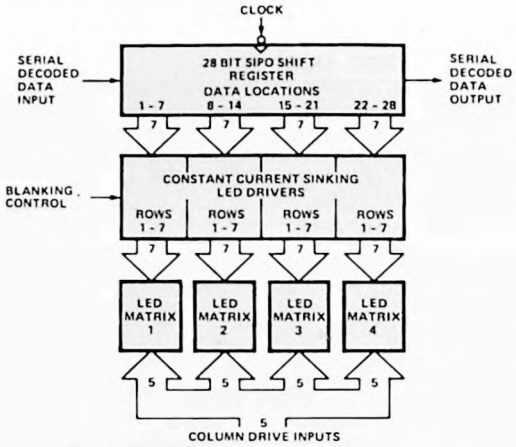


Figure 5. Block Diagram of HDSP-2450/-2451/-2452

Mechanical and Thermal Considerations

The HDSP-2450 series displays are available in standard ceramic dual-in-line packages. They are designed for plugging into sockets or soldering into PC boards. The packages may be horizontally or vertically stacked for character arrays of any desired size. HDSP-2450 series displays utilize a high output current IC to provide excellent readability in bright ambient lighting. Full power operation (V_{CC} = 5.25V, V_B = 2.4V, V_{COL} = 3.5V) with worst case thermal resistance from IC junction to ambient of 45° C/watt/device is possible up to ambient temperature of 60° C. For operation above 60° C, the maximum device dissipation should be derated linearly at 22.2 mW/° C (see Figure 2). With an improved thermal design, operation at higher ambient temperatures without derating is possible.

Power derating for this family of displays can be achieved in several ways. The power supply voltage can be lowered to a minimum of 4.75V. Column Input Voltage, V_{COL}, can be decreased to the recommended minimum values of 2.4V for the HDSP-2450 and 2.75V for the HDSP-2451/-2452. Also, the average drive current can be decreased through pulse width modulation of V_B.

The HDSP-2450 series displays have glass windows. A front panel contrast enhancement filter is desirable in most actual display applications. Some suggested filter materials are provided in Figure 6. Additional information on filtering and contrast enhancement can be found in HP Application Note 1015.

Post solder cleaning may be accomplished using water or Freon/alcohol mixtures formulated for vapor cleaning processing or Freon/alcohol mixtures formulated for room temperature cleaning. Freon/alcohol vapor cleaning processing for up to 2 minutes in vapors at boiling is permissible. Suggested solvents include Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15, and water.

Display Color	Ambient Lighting		
	Dim	Moderate	Bright
HDSP-2450 Std. Red	Panelgraphic Dark Red 63 Ruby Red 60 Chequers Red 118 Plexiglass 2423	Polaroid HNCP37 3M Light Control Film Panelgraphic Gray 10	
HDSP-2451 (Yellow)	Panelgraphic Yellow 27 Chequers Amber 107	Chequers Grey 105	Polaroid HNCP10
HDSP-2452 (HER)	Panelgraphic Ruby Red 60 Chequers Red 112		

Figure 6. Contrast Enhancement Filters

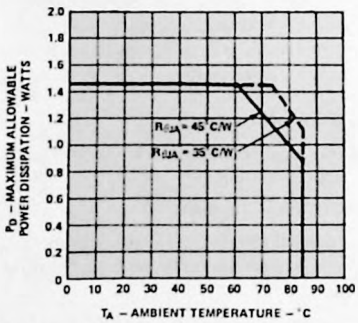


Figure 2. Maximum Allowable Power Dissipation vs. Temperature

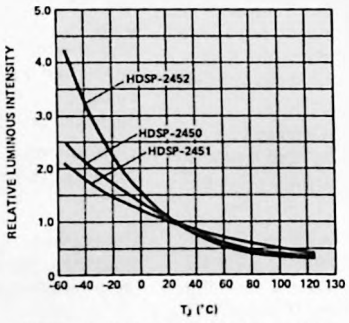


Figure 3. Relative Luminous Intensity vs. Temperature

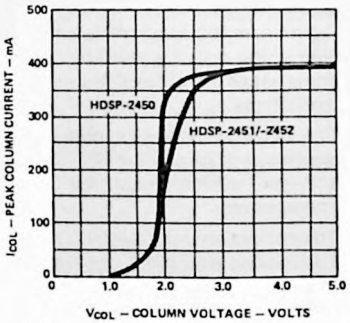


Figure 4. Peak Column Current vs. Column Voltage

High Reliability Testing

Two standard reliability testing programs are available. The TXVB program is in conformance with Quality Level A of MIL-D-87157 for hermetically sealed LED displays with 100% screening tests. A TXVB product is tested to Tables I, II, IIIa, and IVa. The TXV program is an HP modification to the full conformance program and offers the 100% screening of Quality Level A, Table I, and Group A, Table II.

Part Marking System

Standard Product	With Table I and II	With Tables I, II, IIIa, IVa
HDSP-2450	HDSP-2450 TXV	HDSP-2450 TXVB
HDSP-2451	HDSP-2451 TXV	HDSP-2451 TXVB
HDSP-2452	HDSP-2452 TXV	HDSP-2452 TXVB

100% Screening

Table I. Quality Level A of MIL-D-87157

Test Screen	Method	Conditions
1. Precap Visual	—	HP Procedure 5956-7512-52, based on MIL-STD-883B
2. High Temperature Storage	MIL-STD-750 Method 1032	T_A = 125°C, Time = 24 hours
3. Temperature Cycling	MIL-STD-750 Method 1051	Condition B, 10 cycles
4. Constant Acceleration	MIL-STD-750 Method 2006	10,000 G's at Y_1 orientation
5. Fine Leak	MIL-STD-750 Method 1071	Condition H
6. Gross Leak	MIL-STD-750 Method 1071	Condition C
7. Interim Electrical/Optical Tests[2]	—	I_{CC} (at V_B = 0.4V and 2.4V), I_{COL} (at V_B = 0.4V and 2.4V) I_{IH} (V_B, Clock and Data In), I_{IL} (V_B, Clock and Data In), I_{OH}, I_{OL}, Visual Function and I_V Peak. V_{IH} and V_{IL} inputs are guaranteed by the electronic shift register test. T_A = 25°C
8. Burn-In	MIL-STD-883 Method 1015	Condition B at V_{CC} = V_B = 5.25V, V_{COL} = 3.5V, T_A = +85°C, LED ON-Time Duty Factor = 5%, 35 dots On; t = 168 hours
9. Final Electrical Test[2]	—	Same as Step 7
10. Delta Determinations	—	ΔI_{CC} = ±6 mA, ΔI_{IH} (clock) = ±8 μA, Δi_{IH} (Data In) = ±5 μA ΔI_{OH} = ±50 μA, and ΔI_V = -20%, T_A = 25°C
11. External Visual	MIL-STD-883 Method 2009	

Notes:
1. MIL-STD-883 Test Method Applies
2. Limits and conditions are per the electrical optical characteristics. The I_{OH} and I_{OL} tests are the inverse of V_{OH} and V_{OL} specified in the electrical characteristics.

Table II. Group A Electrical Tests — MIL-D-87157

Subgroup/Test	Parameters	LTPD
Subgroup 1 DC Electrical Tests at 25°C[1]	I_{CC} (at V_B = 0.4V and 2.4V), I_{COL} (at V_B = 0.4V and 2.4V) I_{IH} (V_B, Clock and Data In), I_{IL} (V_B, Clock and Data In), I_{OH}, I_{OL} Visual Function and I_V peak. V_{IH} and V_{IL} inputs are guaranteed by the electronic shift register test.	5
Subgroup 2 DC Electrical Tests at High Temperature[1]	Same as Subgroup 1, except delete I_V and visual function, T_A = +85°C	7
Subgroup 3 DC Electrical Tests at Low Temperature[1]	Same as Subgroup 1, except delete I_V and visual function, T_A = -55°C	7
Subgroup 4, 5, and 6 not tested		
Subgroup 7 Optical and Functional Tests at 25°C	Satisfied by Subgroup 1	5
Subgroup 8 External Visual		7

Note:
1. Limits and conditions are per the electrical/optical characteristics. The I_{OH} and I_{OL} tests are the inverse of V_{OH} and V_{OL} specified in the electrical characteristics.

Table IIIa. Group B, Class A and B of MIL-D-87157

Subgroup/Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1			
Resistance to Solvents	1022		4 Devices/ 0 Failures
Internal Visual and Mechanical[3]	2014		1 Device/ 0 Failures
Subgroup 2[1,2]			
Solderability	2026	T_A = 260°C for 5 seconds	LTPD = 15
Subgroup 3			
Thermal Shock (Temp. Cycle)	1051	Condition B, 10 cycles, 15 min. dwell	LTPD = 15
Moisture Resistance	1021		
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C	
Electrical/Optical Endpoints[4]	—	I_{CC} (at V_B = 0.4V and 2.4V), I_{COL} (at V_B = 0.4V and 2.4V), I_{IH} (V_B, Clock and Data In), I_{IL} (V_B, Clock and Data In), I_{OH}, I_{OL} Visual Function and I_V peak. V_{IH} and V_{IL} inputs are guaranteed by the electronic shift register test. T_A = 25°C	
Subgroup 4			
Operating Life Test (340 hrs.)	1027	T_A = +85°C at V_{CC} = V_B = 5.25V, V_{COL} = 3.5V, LED ON-Time Duty Factor = 5%, 35 Dots On	LTPD = 10
Electrical/Optical Endpoints[4]	—	Same as Subgroup 3	
Subgroup 5			
Non-operating (Storage) Life Test (340 hrs.)	1032	T_A = +125°C	LTPD = 10
Electrical/Optical Endpoints[4]	—	Same as Subgroup 3	

Notes:
1. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
2. The LTPD applies to the number of leads inspected except in no case shall less than 3 displays be used to provide the number of leads required.
3. MIL-STD-883 test methods apply.
4. Limits and conditions are per the electrical/optical characteristics. The I_{OH} and I_{OL} tests are the inverse of V_{OH} and V_{OL} specified in the electrical characteristics.

Table IVa. Group C, Class A and B of MIL-D-87157

Subgroup/Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1			
Physical Dimensions	2066		2 Devices/ 0 Failures
Subgroup 2[2,7]			
Lead Integrity	2004	Condition B2	LTPD = 15
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C	
Subgroup 3			
Shock	2016	1500G, Time = 0.5 ms, 5 blows in each orientation X_1, Y_1, Y_2	LTPD = 15
Vibration, Variable Frequency	2056		
Constant Acceleration	2006	10,000G at Y_1 orientation	
External Visual[4]	1010 or 1011		
Electrical/Optical Endpoints[8]	—	I_{CC} (at V_B = 0.4V and 2.4V) I_{COL} (at V_B = 0.4V and 2.4V) I_{IH} (V_B, Clock and Data In) I_{IL} (V_B, Clock and Data In) I_{OH}, I_{OL}, Visual Function and Iv peak. V_{IH} and V_{IL} inputs are guaranteed by the electronic shift register test. T_A = 25°C.	
Subgroup 4[1,3]			
Salt Atmosphere	1041		LTPD = 15
External Visual[4]	1010 or 1011		
Subgroup 5			
Bond Strength[5]	2037	Condition A	LTPD = 20 (C = 0)
Subgroup 6			
Operating Life Test[6]	1026	T_A = +85°C at V_{CC} = V_B = 5.25V, V_{COL} = 3.5V, 35 Dots On	λ = 10
Electrical/Optical Endpoints[8]	—	Same as Subgroup 3	

Notes:
1. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
2. The LTPD applies to the number of leads inspected except in no case shall less than three displays be used to provide the number of leads required.
3. Solderability samples shall not be used.
4. Visual requirements shall be as specified in MIL-STD-883, Methods 1010 or 1011.
5. Displays may be selected prior to seal.
6. If a given inspection lot undergoing Group B inspection has been selected to satisfy Group C inspection requirements, the 340 hour life tests may be continued on test to 1000 hours in order to satisfy the Group C life test requirements. In such cases, either the 340 hour endpoint measurements shall be made a basis for Group B lot acceptance or the 1000 hour endpoint measurement shall be used as the basis for both Group B and Group C acceptance.
7. MIL-STD-883 test method applies.
8. Limits and conditions are per the electrical/optical characteristics. The I_{OH} and I_{OL} tests are the inverse of V_{OH} and V_{OL} specified in the electrical characteristics.

HEWLETT PACKARD

LED SOLID STATE ALPHANUMERIC INDICATOR

5082-7100
5082-7101
5082-7102

TECHNICAL DATA JANUARY 1984

Features

- 5 x 7 LED MATRIX CHARACTER
- LARGE 6.9 mm (.27 INCH) CHARACTER HEIGHT
- EXTREMELY WIDE TEMP. RANGE
- COMPACT 15.2 mm (.600 INCH) GLASS/CERAMIC DIP
- WIDE VIEWING ANGLE
- RUGGED, SHOCK RESISTANT

Description

The Hewlett-Packard 5082-7100 Series is an X-Y addressable, 5 x 7 LED Matrix capable of displaying the full alphanumeric character set. This alphanumeric indicator series is available in 3, 4, or 5 character end-stackable clusters. The clusters permit compact presentation of information, ease of character alignment, minimum number of interconnections, and compatibility with multiplexing driving schemes.

Alphanumeric applications include computer terminals, calculators, military equipment and space flight readouts.

The **5082-7100** is a three character cluster.
The **5082-7101** is a four character cluster.
The **5082-7102** is a five character cluster.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Peak Forward Current Per LED (Duration < 1 ms)	I_{PEAK}		100	mA
Average Current Per LED	I_{AVG}		10	mA
Power Dissipation Per Character (All diodes lit) [1]	P_D		700	mW
Operating Temperature, Case	T_C	–55	95	°C
Storage Temperature	T_S	–55	100	°C
Reverse Voltage Per LED	V_R		4	V

Note 1: At 25°C Case Temperature; derate 8.5 mW/°C above 25°C.

Electrical / Optical Characteristics at T_C=25°C

Parameter	Symbol	Min.	Typ.	Max.	Units
Peak Luminous Intensity Per LED (Character Average) @ Pulse Current of 100mA/LED	$I_{V\ (PEAK)}$	1.0	2.2		mcd
Reverse Current Per LED @ V_R = 4V	I_R		10		μA
Peak Forward Voltage @ Pulse Current of 50mA/LED	V_F		1.7	2.0	V
Peak Wavelength	λ_{PEAK}		655		nm
Spectral Line Halfwidth	$\Delta\lambda_{1/2}$		30		nm
Rise and Fall Times [1]	t_r, t_f		10		ns

Note 1. Time for a 10% - 90% change of light intensity for step change in current.

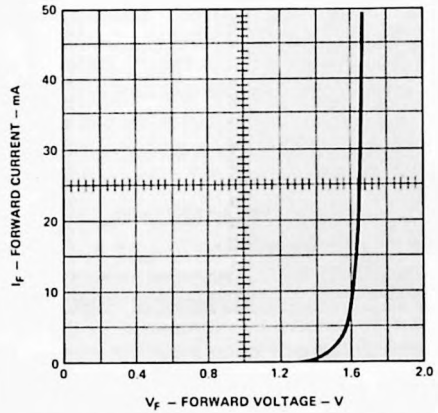


Figure 1. Forward Current-Voltage Characteristic.

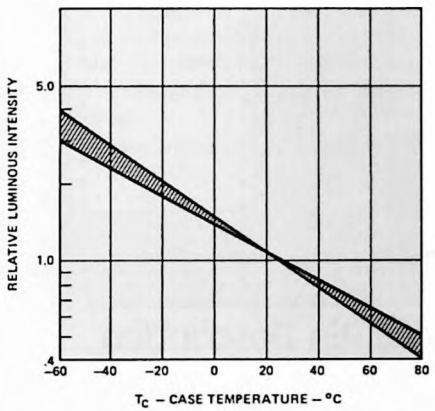


Figure 2. Relative Luminous Intensity vs. Case Temperature at Fixed Current Level.

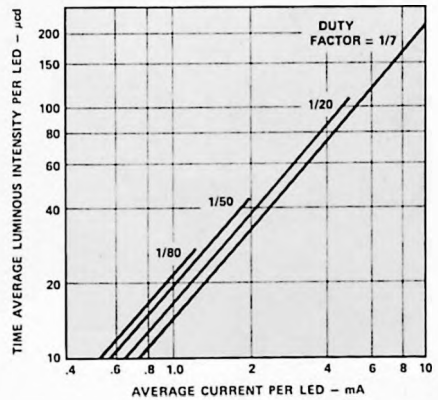


Figure 3. Typical Time Average Luminous Intensity per LED vs. Average Current per LED.

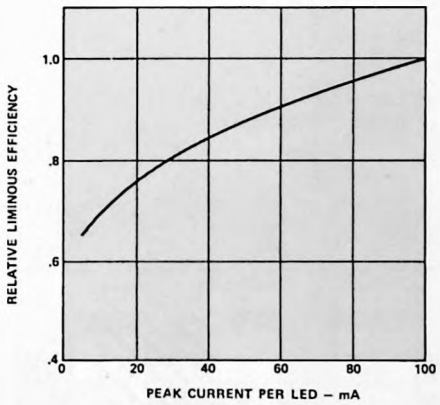
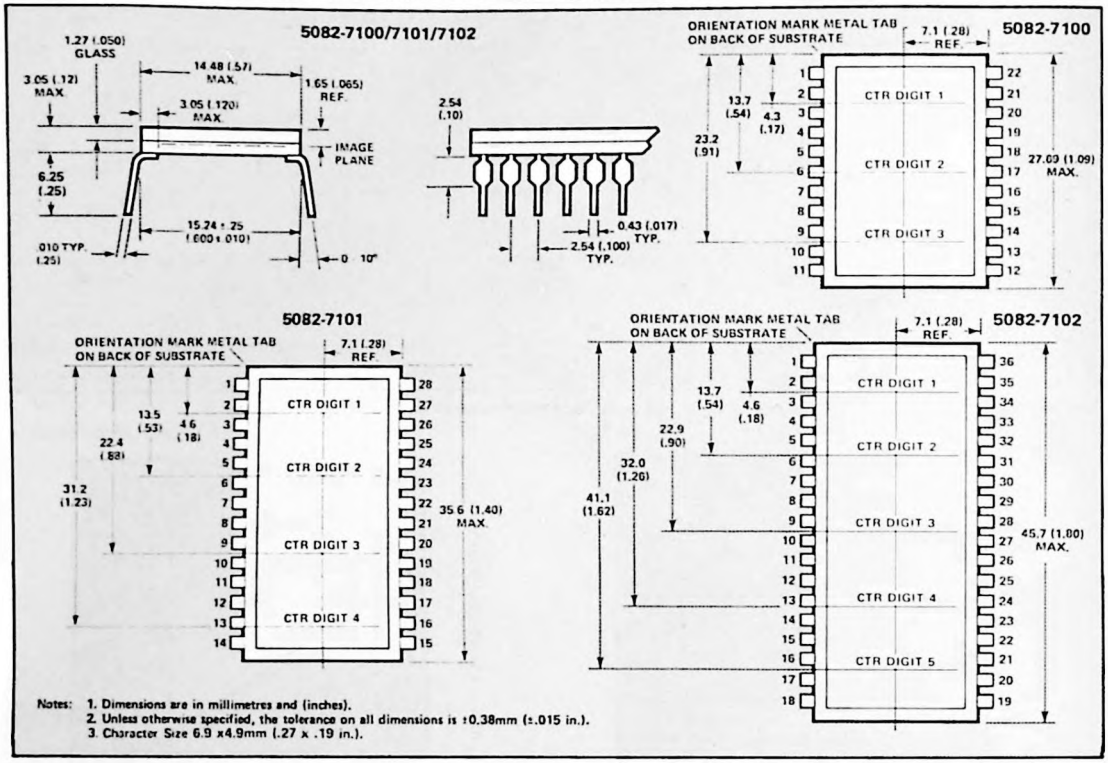


Figure 4. Typical Relative Luminous Efficiency vs. Peak Current per LED.

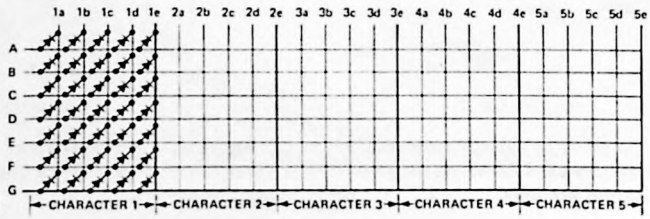
Package Dimensions and Pin Configurations



Notes: 1. Dimensions are in millimetres and (inches).
2. Unless otherwise specified, the tolerance on all dimensions is ±0.38mm (±.015 in.).
3. Character Size 6.9 x4.9mm (.27 x .19 in.).

Device Pin Description

5082-7100				5082-7101				5082-7102			
Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	Anode G	12	Anode B	1	N/C	15	Anode C	1	N/C	19	5e
2	1c	13	3d	2	1c	16	4c	2	1c	20	5c
3	1d	14	3b	3	1e	17	4a	3	1e	21	5a
4	Anode F	15	Anode A	4	Anode G	18	Anode B	4	Anode F	22	Anode D
5	Anode E	16	2e	5	2b	19	3e	5	2b	23	4e
6	2b	17	2c	6	2d	20	3b	6	2d	24	4c
7	2d	18	2a	7	Anode D	21	3a	7	2e	25	N/C
8	Anode C	19	Anode D	8	Anode E	22	2e	8	Anode E	26	Anode C
9	3a	20	1e	9	3c	23	2c	9	3c	27	3d
10	3c	21	1b	10	3d	24	2a	10	3e	28	3b
11	3e	22	1a	11	Anode F	25	Anode A	11	Anode G	29	3a
				12	4b	26	1d	12	4a	30	Anode B
				13	4d	27	1b	13	4b	31	2c
				14	4e	28	1a	14	4d	32	2a
								15	N/C	33	Anode A
								16	5b	34	1d
								17	5d	35	1b
								18	N/C	36	1a



5082-7100/7101/7102
Schematic Wiring Diagram

Operating Considerations

ELECTRICAL

The 5 x 7 matrix of LED's, which make up each character, are X-Y addressable. This allows for a simple addressing, decoding and driving scheme between the display module and customer furnished logic.

There are three main advantages to the use of this type of X-Y addressable array:

1. It is an elementary addressing scheme and provides the least number of interconnection pins for the number of diodes addressed. Thus, it offers maximum flexibility toward integrating the display into particular applications.
2. This method of addressing offers the advantage of sharing the Read-Only-Memory character generator among several display elements. One character generating ROM can be shared over 25 or more 5 x 7 dot matrix characters with substantial cost savings.
3. In many cases equipments will already have a portion of the required decoder/driver (timing and clock circuitry plus buffer storage) logic circuitry available for the display.

To form alphanumeric characters a method called "scanning" or "strobing" is used. Information is addressed to the display by selecting one row of diodes at a time, energizing the appropriate diodes in that row and then proceeding to the next row. After all rows have been excited one at a time, the process is repeated. By scanning through all rows at least 100 times a second, a flicker free character can be produced. When information moves sequentially from row to row of the display (top to bottom) this is row scanning, as illustrated in Figure 5. Information can also be moved from column to column (left to right across the display) in a column scanning mode. For most applications (5 or more characters to share the same ROM) it is more economical to use row scanning.

A much more detailed description of general scanning techniques along with specific circuit recommendations is contained in HP Application Note 931.

MECHANICAL/THERMAL MOUNTING

The solid state display typically operates with 200 mW power dissipation per character. However, if the operating conditions are such that the power dissipation exceeds the derated maximum allowable value, the device should be heat sunk. The usual mounting technique combines mechanical support and thermal heat sinking in a common structure. A metal strap or bar can be mounted behind the display using silicone grease to insure good thermal control. A well-designed heat sink can limit the case temperature to within 10°C of ambient.

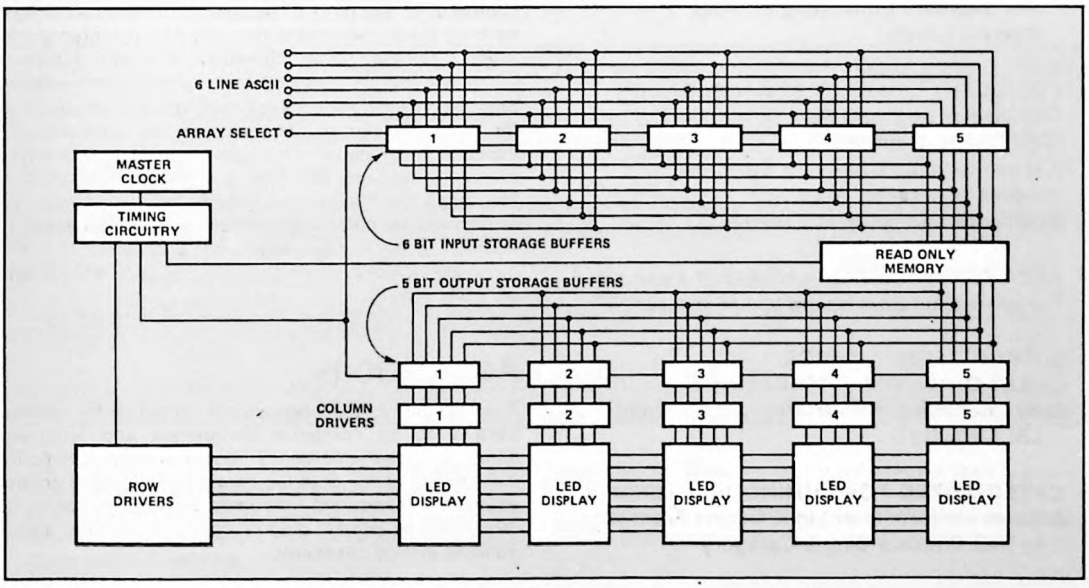


Figure 5. Row Scanning Block Diagram.

HEWLETT PACKARD

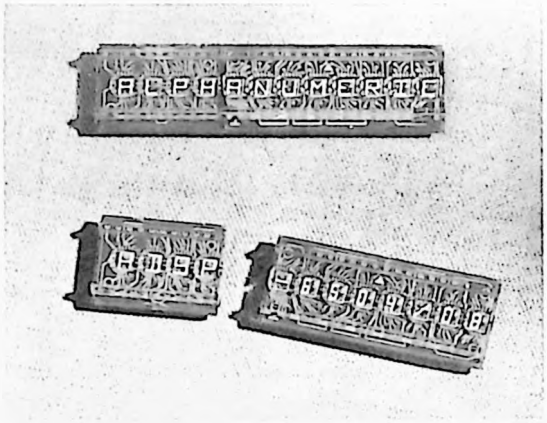
16 SEGMENT SOLID STATE ALPHANUMERIC DISPLAY

HDSP-6504
HDSP-6508

TECHNICAL DATA JANUARY 1984

Features

- **ALPHANUMERIC**
  Displays 64 Character ASCII Set and Special Characters
- **16 SEGMENT FONT PLUS CENTERED D.P. AND COLON**
- **3.81mm (0.150") CHARACTER HEIGHT**
- **APPLICATION FLEXIBILITY WITH PACKAGE DESIGN**
  4 and 8 Character Dual-In-Line Packages
  End Stackable-On Both Ends for 8 Character and On One End for 4 Character
  Sturdy Gold-Plated Leads on 2.54mm (0.100") Centers
  Environmentally Rugged Package
  Common Cathode Configuration
- **LOW POWER**
  As Low as 1.0-1.5mA Average Per Segment Depending on Peak Current Levels
- **EXCELLENT CHARACTER APPEARANCE**
  Continuous Segment Font
  High On/Off Contrast
  6.35mm (0.250") Character Spacing
  Excellent Character Alignment
  Excellent Readability at 2 Metres
- **SECONDARY BARREL MAGNIFIER AVAILABLE**
  Increases Character Height to 4.45 mm (0.175")
- **SUPPORT ELECTRONICS**
  Can Be Driven With ROM Decoders and Drivers
  Easy Interfacing With Microprocessors and LSI Circuitry
- **CATEGORIZED FOR LUMINOUS INTENSITY**
  Assures Uniformity of Light Output From Unit to Unit Within a Single Category



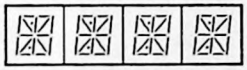
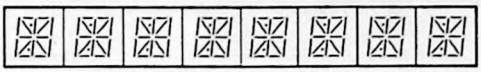
Description

The HDSP-6504 and HDSP-6508 are 3.81mm (0.150") sixteen segment GaAsP red alphanumeric displays mounted in 4 character and 8 character dual-in-line package configurations that permit mounting on PC boards or in standard IC sockets. The monolithic light emitting diode character is magnified by the integral lens which increases both character size and luminous intensity, thereby making low power consumption possible. The rugged package construction, enhanced by the back fill design, offers extended environmental capabilities compared to the standard PC board/lens type of display package. Its temperature cycling capability is the result of the air gap which exists between the semiconductor chip/wire bond assembly and the lens. In addition to the sixteen segments, a centered D.P. and colon are included. Character spacing yields 4 characters per inch.

Applications

These alphanumeric displays are attractive for applications such as computer peripherals and terminals, computer base emergency mobile units, automotive instrument panels, desk top calculators, in-plant control equipment, hand-held instruments and other products requiring low power, display compactness and alphanumeric display capability.

Device Selection Guide

Characters Per Display	Configuration		Part No. HDSP-
	Device	Package	
4		(Figure 6)	6504
8		(Figure 7)	6508

Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Units
I_{PEAK}	Peak Forward Current Per Segment or DP (Duration ≤ 312μs)		200	mA
I_{AVG}	Average Current Per Segment or DP[1]		7	mA
P_D	Average Power Dissipation Per Character[1,2]		138	mW
T_A	Operating Temperature, Ambient	-40	85	°C
T_S	Storage Temperature	-40	100	°C
V_R	Reverse Voltage		5	V
	Solder Temperature at 1.59mm (1/16 inch) below seating plane, t ≤ 3 Seconds		260	°C

NOTES:
1. Maximum allowed drive conditions for strobed operation are derived from Figures 1 and 2. See electrical section of operational considerations.
2. Derate linearly above T_A = 50°C at 2.17mW/°C. P_D Max. (T_A = 85°C) = 62mW.

Electrical/Optical Characteristics at T_A=25°C

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
I_V	Luminous Intensity, Time Average, Character Total with 16 Segments Illuminated [3,4]	I_{PEAK} = 30mA 1/16 Duty Factor	0.40	1.65		mcd
V_F	Forward Voltage Per Segment or DP	I_F = 30mA (One Segment On)		1.6	1.9	V
λ_{PEAK}	Peak Wavelength			655		nm
λ_d	Dominant Wavelength [5]			640		nm
I_R	Reverse Current Per Segment or DP	V_R = 5V		10		μA
$\Delta V_F/\Delta°C$	Temperature Coefficient of Forward Voltage			-2		mV/°C
$R\theta_{J-PIN}$	Thermal Resistance LED Junction-to-Pin			232		°C/W/ Seg

NOTES:
3. The luminous intensity ratio between segments within a digit is designed so that each segment will have the same luminous sterance. Thus each segment will appear with equal brightness to the eye.
4. Each character of the display is matched for luminous intensity at the test conditions shown. Operation of the display at lower peak currents may cause intensity mismatch within the display. Operation at peak currents less than 7 mA will cause objectionable display segment matching.
5. The dominant wavelength, λd, is derived from the C.I.E. chromaticity diagram and represents that single wavelength which defines the color of the device, standard red.

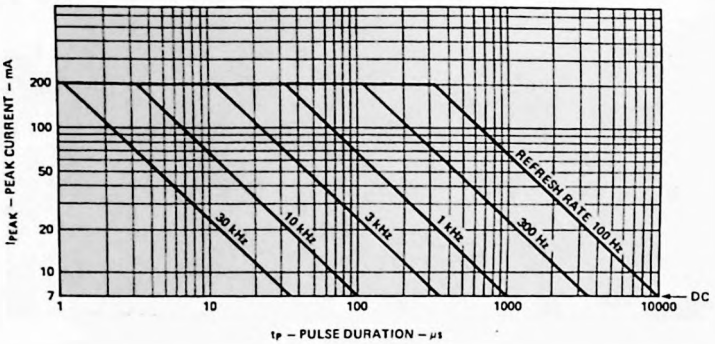


Figure 1. Maximum Allowed Peak Current vs. Pulse Duration. Derate derived operating conditions above T_A = 50°C using Figure 2.

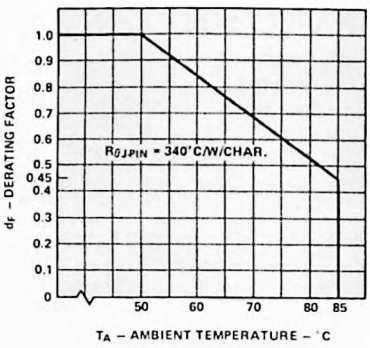


Figure 2. Temperature Derating Factor For Peak Current per Segment vs. Ambient Temperature. T_JMAX = 110°C

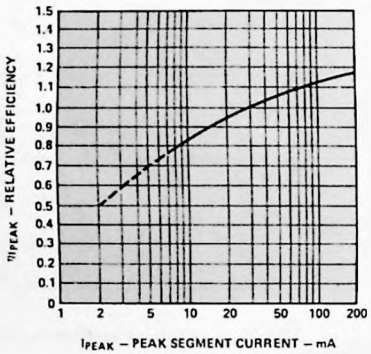


Figure 3. Relative Luminous Efficiency (Luminous Intensity Per Unit Current) vs. Peak Segment Current.

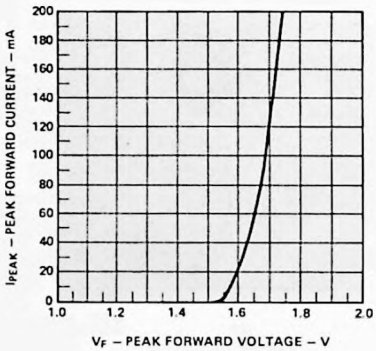
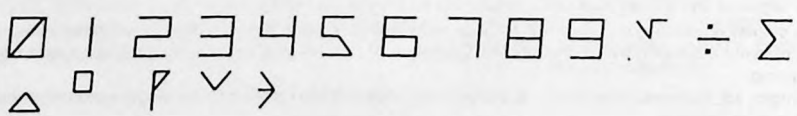


Figure 4. Peak Forward Segment Current vs. Peak Forward Voltage.

For a Detailed Explanation on the Use of Data Sheet Information and Recommended Soldering Procedures, See Application Note 1005.

Figure 5. Typical 64 Character ASCII Set.



Additional Character Font

Package Dimensions

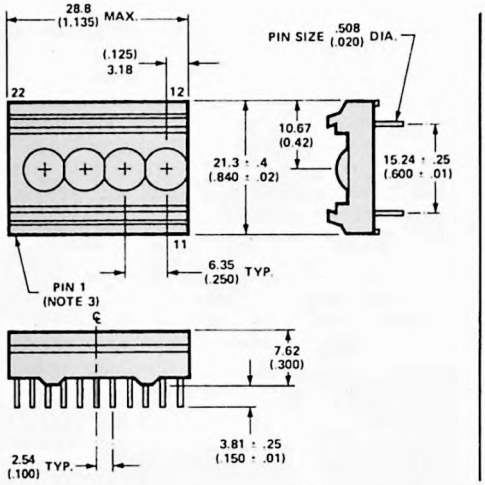


Figure 6. HDSP-6504

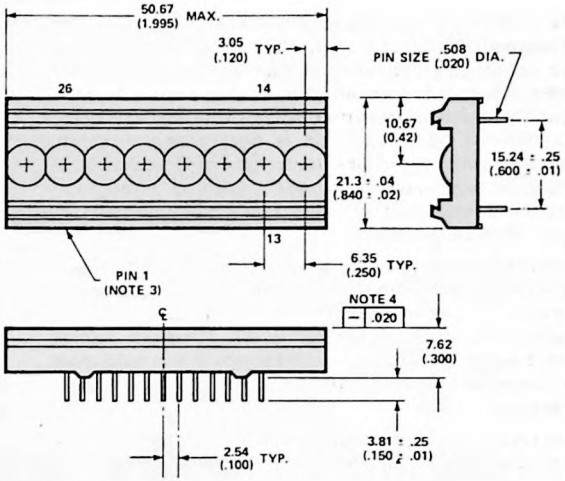


Figure 7. HDSP-6508

NOTES:
1. ALL DIMENSIONS IN MILLIMETRES AND (INCHES).
2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
3. PIN 1 IDENTIFIED BY INK DOT ADJACENT TO LEAD.

Magnified Character Font Description

DEVICES
HDSP-6504
HDSP-6508

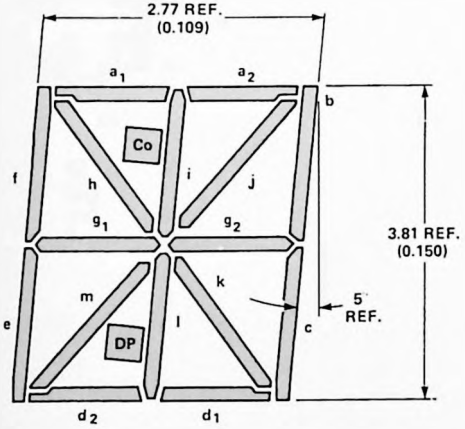


Figure 8.

Device Pin Description

Pin No.	Function			
	HDSP-6504		HDSP-6508	
1	Anode	Segment g_1	Anode	Segment g_1
2	Anode	Segment DP	Anode	Segment DP
3	Cathode	Digit 1	Cathode	Digit 1
4	Anode	Segment d_2	Anode	Segment d_2
5	Anode	Segment l	Anode	Segment l
6	Cathode	Digit 3	Cathode	Digit 3
7	Anode	Segment e	Anode	Segment e
8	Anode	Segment m	Anode	Segment m
9	Anode	Segment k	Anode	Segment k
10	Cathode	Digit 4	Cathode	Digit 4
11	Anode	Segment d_1	Anode	Segment d_1
12	Anode	Segment j	Cathode	Digit 6
13	Anode	Segment C_O	Cathode	Digit 8
14	Anode	Segment g_2	Cathode	Digit 7
15	Anode	Segment a_2	Cathode	Digit 5
16	Anode	Segment i	Anode	Segment j
17	Cathode	Digit 2	Anode	Segment C_O
18	Anode	Segment b	Anode	Segment g_2
19	Anode	Segment a_1	Anode	Segment a_2
20	Anode	Segment c	Anode	Segment i
21	Anode	Segment h	Cathode	Digit 2
22	Anode	Segment f	Anode	Segment b
23			Anode	Segment a_1
24			Anode	Segment c
25			Anode	Segment h
26			Anode	Segment f

Operational Considerations

ELECTRICAL

The HDSP-6504 and -6508 devices utilize large monolithic 16 segment GaAsP LED chips with centered decimal point and colon. Like segments of each digit are electrically interconnected to form an 18 by N array, where N is the quantity of characters in the display. In the driving scheme the decimal point or colon is treated as a separate character with its own time frame. A detailed discussion of character font capabilities, ASCII code to 18 segment decoding and display drive techniques appears in Application Note 1003.

These displays are designed specifically for strobed (multiplexed) operation. Under normal operating situations the maximum number of illuminated segments needed to represent a given characcter is 10. Therefore, except where noted, the information presented in this data sheet is for a maximum of 10 segments illuminated per character.*

The typical forward voltage values, scaled from Figure 4, should be used for calculating the current limiting resistor values and typical power dissipation. Expected maximum V_F values for the purpose of driver circuit design may be calculated using the following V_F model:

$V_F = 1.85V + I_{PEAK}\ (1.8\Omega)$
For: $30mA \leq I_{PEAK} \leq 200mA$
$V_F = 1.58V + I_{PEAK}\ (10.7\Omega)$
For: $10mA \leq I_{PEAK} \leq 30mA$

OPTICAL AND CONTRAST ENHANCEMENT

Each large monolithic chip is positioned under a separate element of a plastic aspheric magnifying lens, producing a magnified character height of 3.810mm (.150 inch). The aspheric lens provides wide included viewing angles of typically 75 degrees horizontal and 75 degrees vertical with low off axis distortion. These two features, coupled with the very high segment luminous sterance, provide to the user a display with excellent readability in bright ambient light for viewing distances in the range of 2 metres. Effective contrast enhancement can be obtained by employing any of the following optical filter products: Panelgraphic: Ruby Red 60, Dark Red 63 or Purple 90; SGL Homalite: H100-1605 Red or H100-1804 Purple, Plexiglas 2423. For very bright ambients, such as indirect sunlight, the 3M Light Control Film is recommended: Red 655, Violet, Purple or Neutral Density.

For those applications requiring only 4 or 8 characters, a secondary barrel magnifier, HP part number HDSP-6505 (four character) and -6509 (eight character), may be inserted into support grooves on the primary magnifier. This secondary magnifier increases the character height to 4.45mm (.175 inch) without loss of horizontal viewing angle (see below).

MECHANICAL

These devices are constructed by LED die attaching and wire bonding to a high temperature PC board substrate. A precision molded plastic lens is attached to the PC board and the resulting assembly is backfilled with a sealing epoxy to form an environmentally sealed unit.

The four character and eight character devices can be end stacked to form a character string which is a multiple of a basic four character grouping. As an example, one -6504 and two -6508 devices will form a 20 character string. These devices may be soldered onto a printed circuit board or inserted into 24 and 28 pin DIP LSI sockets. The socket spacing must allow for device end stacking.

Suitable conditions for wave soldering depend upon the specific kind of equipment and procedure used. For more information, consult the local HP Sales Office or Hewlett-Package Components, Palo Alto, California.

*More than 10 segments may be illuminated in a given character, provided the maximum allowed character power dissipation, temperature derated, is not exceeded.

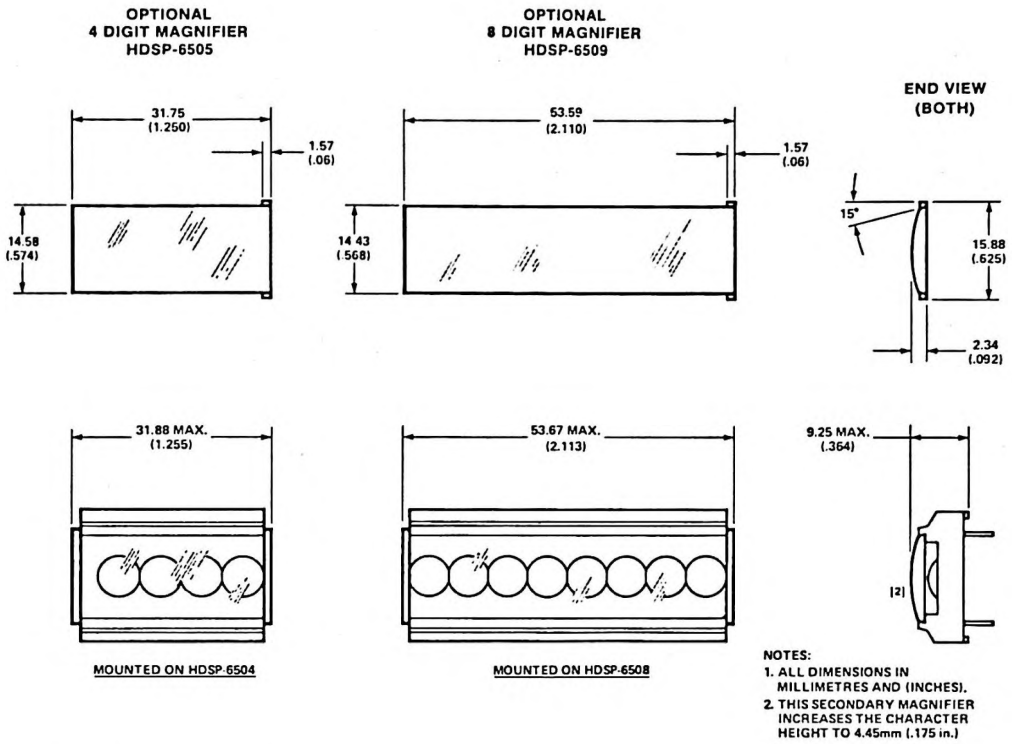


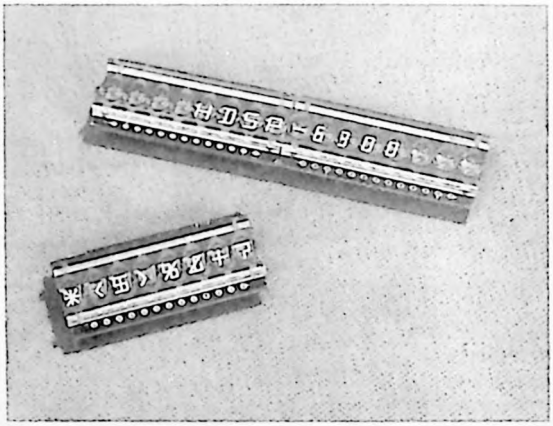
Figure 9. Design Data for Optional Barrel Magnifier in Single Display Applications.

HEWLETT PACKARD

16 SEGMENT SOLID STATE ALPHANUMERIC DISPLAY

HDSP-6300

TECHNICAL DATA JANUARY 1984



Features

- **ALPHANUMERIC**
  Displays 64 Character ASCII Set and Special Characters
- **16 SEGMENT FONT PLUS CENTERED D.P. AND COLON**
- **3.56mm (0.140") CHARACTER HEIGHT**
- **APPLICATION FLEXIBILITY WITH PACKAGE DESIGN**
  8 Character Dual-In-Line Package
  End Stackable
  Sturdy Leads on 2.54mm (0.100") Centers
  Common Cathode Configuration
- **LOW POWER**
  As Low as 1.0-1.5mA Average Per Segment Depending on Peak Current Levels
- **EXCELLENT CHARACTER APPEARANCE**
  Continuous Segment Font
  High On/Off Contrast
  5.08mm (0.200") Character Spacing
  Excellent Character Alignment
  Excellent Readability at 1.5 Metres
- **SUPPORT ELECTRONICS**
  Can Be Driven With ROM Decoders and Drivers
  Easy Interfacing With Microprocessors and LSI Circuitry
- **CATEGORIZED FOR LUMINOUS INTENSITY**
  Assures Uniformity of Light Output From Unit to Unit Within a Single Category

Description

The HDSP-6300 is a sixteen segment GaAsP red alphanumeric display mounted in an 8 character dual-in-line package configuration that permits mounting on PC boards or in standard IC sockets. The monolithic light emitting diode character is magnified by the integral lens which increases both character size and luminous intensity, thereby making low power consumption possible. The sixteen elements consist of sixteen segments for alphanumeric and special characters plus centered decimal point and colon for good visual aesthetics. Character spacing yields 5 characters per inch.

Applications

These alphanumeric displays are attractive for applications such as computer peripherals and mobile terminals, desk top calculators, in-plant control equipment, hand-held instruments and other products requiring low power, display compactness and alphanumeric display capability.

Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Units
I_{PEAK}	Peak Forward Current Per Segment or DP (Duration ≤ 417μs)		150	mA
I_{AVG}	Average Current Per Segment or DP[1]		6.25	mA
P_D	Average Power Dissipation Per Character[1,2]		133	mW
T_A	Operating Temperature, Ambient	-40	85	°C
T_S	Storage Temperature	-40	100	°C
V_R	Reverse Voltage		5	V
	Solder Temperature at 1.59mm (1/16 inch) below seating plane, t ≤ 5 Seconds		260	°C

NOTES:
1. Maximum allowed drive conditions for strobed operation are derived from Figures 1 and 2. See electrical section of operational considerations.
2. Derate linearly above T_A = 50°C at 2.47 mW/°C. P_D Max. (T_A = 85°C) = 47 mW.

Electrical/Optical Characteristics at T_A=25°C

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
I_V	Luminous Intensity, Time Average, Character Total with 16 Segments Illuminated [3,4]	I_{PEAK} = 24mA 1/16 Duty Factor	400	1200		μcd
V_F	Forward Voltage Per Segment or DP	I_F = 24mA (One Segment On)		1.6	1.9	V
λ_{PEAK}	Peak Wavelength			655		nm
λ_d	Dominant Wavelength [5]			640		nm
I_R	Reverse Current Per Segment or DP	V_R = 5V		10		μA
$R\theta_{J-PIN}$	Thermal Resistance LED Junction-to-Pin per Character			250		°C/W/ Char.

NOTES:
3. The luminous intensity ratio between segments within a digit is designed so that each segment will have the same luminous sterance. Thus each segment will appear with equal brightness to the eye.
4. Each character of the display is matched for luminous intensity at the test conditions shown. Operation of the display at lower peak currents may cause intensity mismatch within the display. Operation at peak currents less than 7 mA will cause objectionable display segment matching.
5. The dominant wavelength, λd, is derived from the C.I.E. chromaticity diagram and represents that single wavelength which defines the color of the device, standard red.

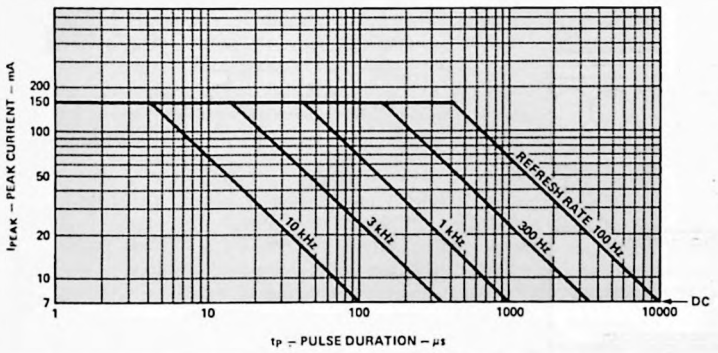


Figure 1. Maximum Allowed Peak Current vs. Pulse Duration. Derate derived operating conditions above T_A = 50°C using Figure 2.

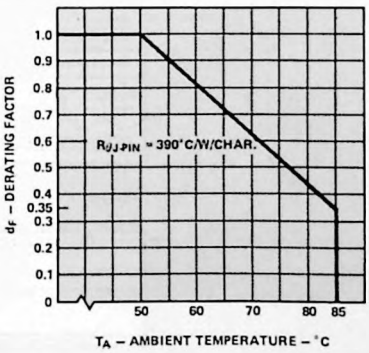


Figure 2. Temperature Derating Factor For Peak Current per Segment vs. Ambient Temperature. T_JMAX = 110°C

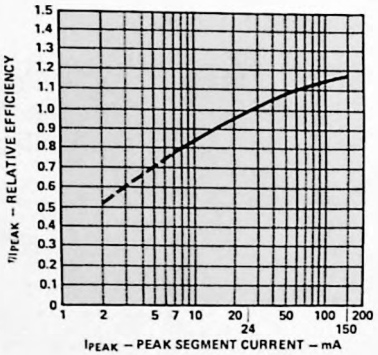


Figure 3. Relative Luminous Efficiency (Luminous Intensity Per Unit Current) vs. Peak Segment Current.

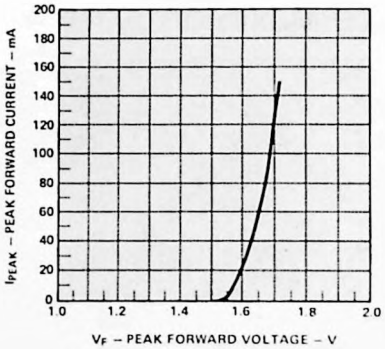
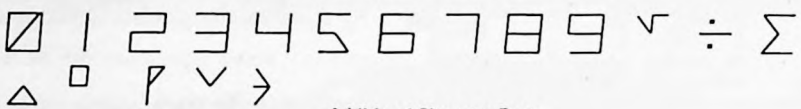


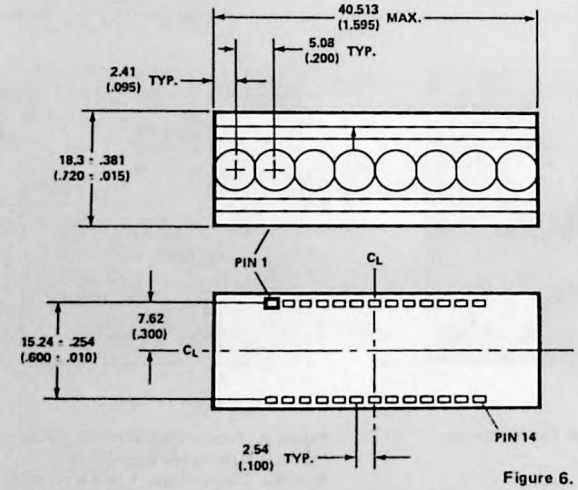
Figure 4. Peak Forward Segment Current vs. Peak Forward Voltage.

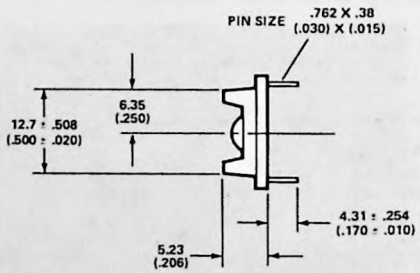
For a Detailed Explanation on the Use of Data Sheet Information and Recommended Soldering Procedures, See Application Note 1005.

Figure 5. Typical 64 Character ASCII Set.



Additional Character Font





NOTES
1. ALL DIMENSIONS IN MILLIMETRES AND (INCHES).
2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
3. PIN 1 IDENTIFIED BY DOT ADJACENT TO LEAD.

Figure 6.

Magnified Character Font Description

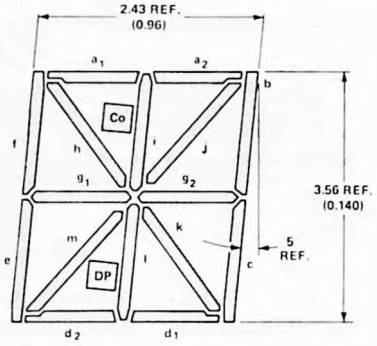


Figure 7.

Device Pin Description

Pin No.	Function	
1	Anode	Segment K
2	Anode	Segment D_1
3	Anode	Segment C
4	Cathode	Digit 1
5	Cathode	Digit 2
6	Cathode	Digit 3
7	Cathode	Digit 4
8	Anode	Segment L
9	Anode	Segment G_2
10	Anode	Segment E
11	Anode	Segment M
12	Anode	Segment D_2
13	Anode	Segment DP
14	Anode	Segment A_2
15	Anode	Segment I
16	Anode	Segment J
17	Cathode	Digit 8
18	Cathode	Digit 7
19	Cathode	Digit 6
20	Cathode	Digit 5
21	Anode	Segment C_o
22	Anode	Segment G_1
23	Anode	Segment B
24	Anode	Segment F
25	Anode	Segment H
26	Anode	Segment A_1

Operational Considerations

ELECTRICAL

The HDSP-6300 device utilizes large monolithic 16 segment plus centered decimal point and colon GaAsP LED chips. Like segments of each digit are electrically interconnected to form an 18 by N array, where N is the quantity of characters in the display. In the driving scheme the decimal point or colon is treated as a separate character with its own time frame. A detailed discussion of character font capabilities, ASCII code to 18 segment decoding and display drive techniques appears in Application Note 1003.

This display is designed specifically for strobed (multiplexed) operation. Under normal operating situations the maximum number of illuminated segments needed to represent a given character is 10. Therefore, except where noted, the information presented in this data sheet is for a maximum of 10 segments illuminated per character.*

The typical forward voltage values, scaled from Figure 4, should be used for calculating the current limiting resistor values and typical power dissipation. Expected maximum V_F values for the purpose of driver circuit design may be calculated using the following V_F model:

$V_F = 1.85V + I_{PEAK}\ (1.8\Omega)$
For $30mA \leq I_{PEAK} \leq 150mA$
$V_F = 1.58V + I_{PEAK}\ (10.7\Omega)$
For $10mA \leq I_{PEAK} \leq 30mA$

*More than 10 segments may be illuminated in a given character, provided the maximum allowed character power dissipation, temperature derated, is not exceeded.

OPTICAL AND CONTRAST ENHANCEMENT

Each large monolithic chip is positioned under a separate element of a plastic aspheric magnifying lens producing a magnified character height of 3.56mm (0.140 inch). The aspheric lens provides wide included viewing angles of 60 degrees horizontal and 55 degrees vertical with low off axis distortion. These two features, coupled with the very high segment luminous sterance, provide to the user a display with excellent readability in bright ambient light for viewing distances in the range of 1.5 metres. Effective contrast enhancement can be obtained by employing an optical filter product such as Panelgraphic Ruby Red 60, Dark Red 63 or Purple 90; SGL Homalite H100-1605 Red or H100-1804 Purple; or Plexiglas 2423. For very bright ambients, such as indirect sunlight, the 3M Red 655 or Neutral Density Light Control Film is recommended.

MECHANICAL

This device is constructed by LED die attaching and wire bonding to a high temperature PC board substrate. A precision molded plastic lens is attached to the PC board.

The HDSP-6300 can be end stacked to form a character string which is a multiple of a basic eight character grouping. These devices may be soldered onto a printed circuit board or inserted into 28 pin DIP LSI sockets. The socket spacing must allow for device end stacking.

Suitable conditions for wave soldering depend upon the specific kind of equipment and procedure used. It is recommended that a non-activated rosin core wire solder or a low temperature deactivating flux and solid wire solder be used in soldering operations. For more information, consult the local HP Sales Office or Hewlett-Packard Components, Palo Alto, California.

HEWLETT PACKARD

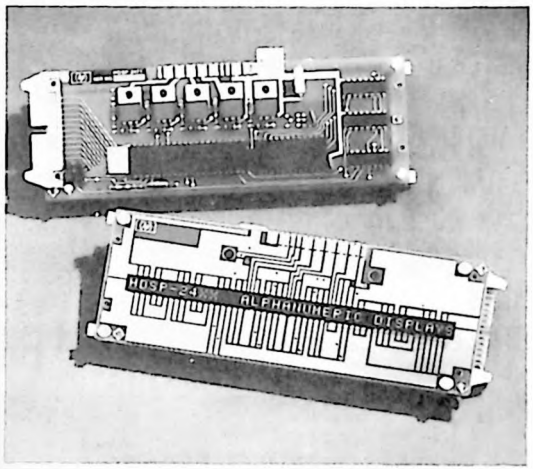
5 x 7 DOT MATRIX ALPHANUMERIC DISPLAY SYSTEM

HDSP - 2416
HDSP - 2424
HDSP - 2432
HDSP - 2440
HDSP - 2470
HDSP - 2471
HDSP - 2472

TECHNICAL DATA JANUARY 1984

Features

- **COMPLETE ALPHANUMERIC DISPLAY SYSTEM UTILIZING THE HDSP-2000 DISPLAY**
- **CHOICE OF 64, 128, OR USER DEFINED ASCII CHARACTER SET**
- **CHOICE OF 16, 24, 32, or 40 ELEMENT DISPLAY PANEL**
- **MULTIPLE DATA ENTRY FORMATS — Left, Right, RAM, or Block Entry**
- **EDITING FEATURES THAT INCLUDE CURSOR, BACKSPACE, FORWARDSPACE, INSERT, DELETE, AND CLEAR**
- **DATA OUTPUT CAPABILITY**
- **SINGLE 5.0 VOLT POWER SUPPLY**
- **TTL COMPATIBLE**
- **EASILY INTERFACED TO A KEYBOARD OR A MICROPROCESSOR**



Description

The HDSP-24XX series of alphanumeric display systems provides the user with a completely supported 5 x 7 dot matrix display panel. These products free the user's system from display maintenance and minimize the interaction normally required for alphanumeric displays. Each alphanumeric display system is composed of two component parts:

1. An alphanumeric display controller which consists of a preprogrammed microprocessor plus associated logic, which provides decode, memory, and drive signals necessary to properly interface a user's system to an HDSP-2000 display. In addition to these basic display support operations, the controller accepts data in any of four data entry formats and incorporates several powerful editing routines.
2. A display panel which consists of HDSP-2000 displays matched for luminous intensity and mounted on a P.C. board designed to have low thermal resistance.

These alphanumeric display systems are attractive for applications such as data entry terminals, instrumentation, electronic typewriters, and other products which require an easy to use 5 x 7 dot matrix alphanumeric display system.

PART NUMBER	DESCRIPTION
Display Boards	
HDSP-2416	Single-line 16 character display panel utilizing the HDSP-2000 display
HDSP-2424	Single-line 24 character display panel utilizing the HDSP-2000 display
HDSP-2432	Single-line 32 character display panel utilizing the HDSP-2000 display
HDSP-2440	Single-line 40 character display panel utilizing the HDSP-2000 display
Controller Boards	
HDSP-2470	HDSP-2000 display interface incorporating a 64 character ASCII decoder
HDSP-2471	HDSP-2000 display interface incorporating a 128 character ASCII decoder
HDSP-2472	HDSP-2000 display interface without ASCII decoder. Instead, a 24 pin socket is provided to accept a custom 128 character set from a user programmed 1K x 8 PROM.

When ordering, specify one each of the Controller Board and the Display Board for each complete system.

Absolute Maximum Ratings

V_{CC} ..... -0.5V to 6.0V

Operating Temperature Range, Ambient (T_A) ..... 0°C to 70°C

Storage Temperature Range (T_S) .... -55°C to 100°C

Voltage Applied to any Input or Output ..-0.5V to 6.0V

I_{SOURCE} Continuous for any Column Driver ..... 5.0 Amps (60 sec. max. duration)

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Data Out	I_{OL}		0.4	mA
	I_{OH}		-20	μA
Ready, Data Valid, Column On, Display Data	I_{OL}		1.6	mA
	I_{OH}		-40	μA
Clock	I_{OL}		10.0	mA
	I_{OH}		-1.0	mA
$Column_{1-5}$	I_{SOURCE}		-5.0	A

Electrical Characteristics Over Operating Temperature Range

(Unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	
Supply Current[1]	I_{CC}			400	mA	V_{CC} = 5.25V Column On and All Outputs Open	
Input Threshold High (except Reset)	V_{IH}	2.0			V	V_{CC} = 5.0V ± .25V	
Input Threshold High — Reset[2]	V_{IH}	3.0			V	V_{CC} = 5.0V ± .25V	
Input Threshold Low — All Inputs	V_{IL}			0.8	V	V_{CC} = 5.0V ± .25V	
Data Out Voltage	V_{OH}Data	2.4			V	I_{OH} = -20μA	V_{CC} = 4.75V
	V_{OL}Data			0.5	V	I_{OL} = 0.4mA	V_{CC} = 4.75V
Clock Output Voltage	V_{OH}Clk	2.4			V	I_{OH} = -1000μA	V_{CC} = 4.75V
	V_{OL}Clk			0.5	V	I_{OL} = 10.0mA	V_{CC} = 4.75V
Ready, Display Data, Data Valid, Column on Output Voltage	V_{OH}	2.4			V	I_{OH} = -40μA	V_{CC} = 4.75V
	V_{OL}			0.5	V	I_{OL} = 1.6mA	V_{CC} = 4.75V
Input Current,[3] All Inputs Except Reset, Chip Select, D_7	I_{IH}			-0.3	mA	V_{IH} = 2.4V	V_{CC} = 5.25V
	I_{IL}			-0.6	mA	V_{IL} = 0.5V	V_{CC} = 5.25V
$\overline{\text{Reset}}$ Input Current	I_{IH}			-0.3	mA	V_{IH} = 3.0V	V_{CC} = 5.25V
	I_{IL}			-0.6	mA	V_{IL} = 0.5V	V_{CC} = 5.25V
Chip Select, D_7 Input Current	I_I	-10		+10	μA	0 < V_I < V_{CC}	
Column Output Voltage	V_{OL}COL	2.6	3.2		V	I_{OUT} = -5.0A	V_{CC} = 5.00V

NOTES:

1. See Figure 11 for total system supply current.
2. External reset may be initiated by grounding Reset with either a switch or open collector TTL gate for a minimum time of 50ms. For Power On Reset to function properly, V_{CC} power supply should turn on at a rate > 100V/s.
3. Momentary peak surge currents may exist on these lines. However, these momentary currents will not interfere with proper operation of the HDSP-2470/1/2.

Absolute Maximum Ratings

Supply Voltage V_{CC} to Ground ..... -0.5V to 6.0V
Inputs, Data Out and V_B ..... -0.5V to V_{CC}
Column Input Voltage, V_{COL} ..... -0.5V to +6.0V
Free Air Operating Temperature Range, T_A[1] ..... 0°C to +55°C
Storage Temperature Range, T_S .... -55°C to +100°C

Recommended Operating Conditions

Parameter	Symbol	Min.	Norm.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Column Input Voltage, Column On	V_{COL}	2.6			V
Setup Time	t_{SETUP}	70	45		ns
Hold Time	t_{HOLD}	30	0		ns
Width of Clock	$t_{W(CLOCK)}$	75			ns
Clock Frequency	f_{CLOCK}	0		3	MHz
Clock Transition Time	t_{THL}			200	ns
Free Air Operating[1] Temperature Range	T_A	0		55	°C

Electrical Characteristics Over Operating Temperature Range

(Unless otherwise specified)

Parameter		Symbol	Min.	Typ.*	Max.	Units	Conditions	
Supply Current		I_{CC}		45n	60n[2]	mA	V_{CC} = 5.25V, V_{CLOCK}=V_{DATA}=2.4V, All SR Stages = Logical 1	V_B = 0.4V
				73n	95n	mA		V_B = 2.4V
Column Current at any Column Input		I_{COL}			1.5n	mA	V_{CC} = V_{COL} = 5.25V, All SR Stages = Logical 1	V_B = 0.4V
		I_{COL}		335n	410n	mA		V_B = 2.4V
Peak Luminous Intensity per LED (Character Average)		$I_{V\ PEAK}$	105	200		µcd	V_{CC} = 5.0V, V_{COL} = 3.5V, T_j = 25°C[3], V_B = 2.4V	
V_B, Clock or Data Input Threshold High		V_{IH}	2.0			V	V_{CC} = V_{COL} = 4.75V	
V_B, Clock or Data Input Threshold Low		V_{IL}			0.8	V		
Input Current Logical 1	V_B, Clock	I_{IH}			80	µA	V_{CC} = 5.25V, V_{IH} = 2.4V	
	Data In	I_{IH}			40	µA		
Input Current Logical 0	V_B, Clock	I_{IL}		-500	-800	µA	V_{CC} = 5.25V, V_{IL} = 0.4V	
	Data In	I_{IL}		-250	-400	µA		
Power Dissipation Per Board[4]		P_D		0.66n		W	V_{CC} = 5.0V, V_{COL} = 2.6V, 15 LED's on per Character, V_B = 2.4V	

*All typical values specified at V_{CC} = 5.0V and T_A = 25°C unless otherwise noted.

NOTES:

1. Operation above 55°C (70°C MAX) may be achieved by the use of forced air (150 fpm normal to component side of HDSP-247X controller board at sea level). Operation down to -20°C is possible in applications that do not require the use of HDSP-2470/-2471/-2472 controller boards.
2. n = number of HDSP-2000 packages
   HDSP-2416 n = 4
   HDSP-2424 n = 6
   HDSP-2432 n = 8
   HDSP-2440 n = 10
3. Tj refers to initial case temperature immediately prior to the light measurement.
4. Power dissipation with all characters illuminated.

System Overview

The HDSP-2470/-2471/-2472 Alphanumeric Display Controllers provide the interface between any ASCII based Alphanumeric System and the HDSP-2000 Alphanumeric Display. ASCII data is loaded into the system by means of any one of four data entry modes — Left, Right, RAM or Block Entry. This ASCII data is stored in the internal RAM memory of the system. The system refreshes HDSP-2000 displays from 4 to 48 characters with the decoded data.

The user interfaces to any of the systems through eight DATA IN inputs, five ADDRESS inputs (RAM mode), a CHIP SELECT input, RESET input, seven DATA OUT outputs, a READY output, DATA VALID output, and a COLUMN ON output. A low level on the RESET input clears the display and initializes the system. A low level on the CHIP SELECT input causes the system to load data from the DATA IN and ADDRESS inputs into the system. The controller outputs a status word, cursor address and 32 ASCII data characters through the DATA OUT outputs and DATA VALID output during the time the system is waiting to refresh the next column of the display. The COLUMN ON output can be used to synchronize the DATA OUT function. A block diagram for the HDSP-2470/-2471/-2472 systems is shown in Figure 1.

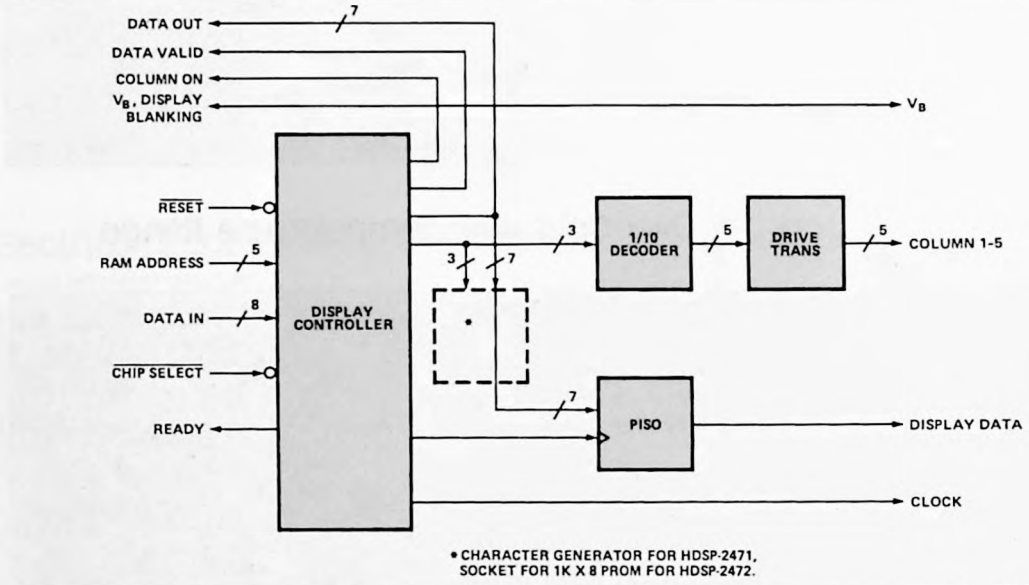


Figure 1. Block Diagram for the HDSP-2470/-2471/-2472 Alphanumeric Display Controller.

The system interfaces to the HDSP-2000 display through five COLUMN outputs, a CLOCK output, DISPLAY DATA output, and the COLUMN ON output. The user should connect DISPLAY DATA to DATA IN of the leftmost HDSP-2000 cluster and cascade DATA OUT to DATA IN of all HDSP-2000 clusters. COLUMN outputs from the system are connected to the COLUMN inputs of all HDSP-2000 clusters. The HDSP-24XX Series display boards are designed to interconnect directly with the HDSP-247X Series display controllers. The COLUMN outputs can source enough current to drive up to 48 characters of the HDSP-2000 display. Pulse width modulation of display luminous intensity can be provided by connecting COLUMN ON to the input of a monostable multivibrator and the output of the monostable multivibrator to the V_B inputs of the HDSP-2000 displays. The system is designed to refresh the display at a fixed refresh rate of 100 Hz. COLUMN ON time is optimized for each display length in order to maximize light output as shown in Figure 2.

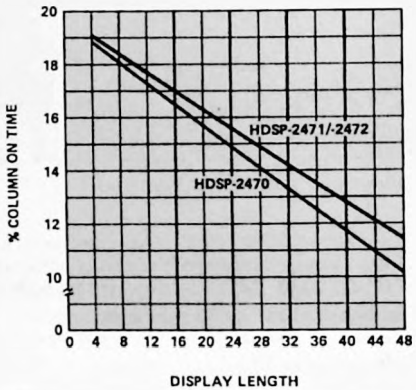


Figure 2. Column on Time vs. Display Length for the HDSP-2470/-2471/-2472 Alphanumeric Display Controller.

Control Mode/Data Entry

User interface to the HDSP-247X Series controller is via an 8 bit word which provides to the controller either a control word or standard ASCII data input. In addition to this user provided 8 bit word, two additional control lines, CHIP SELECT and READY, allow easily generated "handshake" signals for interface purposes.

A logic low applied to the CHIP SELECT input (minimum six microseconds) causes the controller to read the 8 DATA IN lines and determine whether a control word or ASCII data word is present, as determined by the logic state of the most significant bit (D_7). If the controller detects a logic high at D_7, the state of D_6-D_0 will define the data entry mode and the number of alphanumeric characters to be displayed.

The 8 bit control data word format is outlined in Figure 3. For the control word (D_7 high), bits D_6 and D_5 define the selected data entry mode (Left entry, Right entry, etc.) and bits D_3 to D_0 define display length. Bit D_4 is ignored.

Control word inputs are first checked to verify that the control word is valid. The system ignores display lengths greater than 1011 for left block or right, or 0111 for RAM. If the word is valid, the present state—next state table shown in Figure 4 is utilized to determine whether or not to clear the display. For display lengths of up to 32 characters, RAM entry can be used as a powerful editing tool, or can be used to preload the cursor. With other transitions, the internal data memory is cleared.

CONTROL WORD: $D_7D_6D_5D_4D_3D_2D_1D_0$

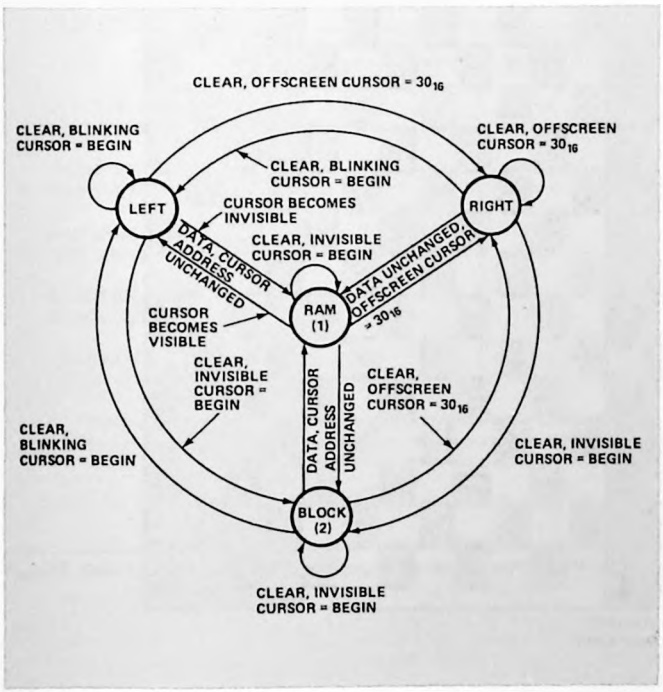
1	X	X	–	Y	Y	Y	Y

Y Y Y Y	DISPLAY LENGTH:
0 0 0 0	4 DIGITS
0 0 0 1	8 "
0 0 1 0	12 "
0 0 1 1	16 "
0 1 0 0	20 "
0 1 0 1	24 "
0 1 1 0	28 "
0 1 1 1	32* "
1 0 0 0	36 "
1 0 0 1	40 "
1 0 1 0	44 "
1 0 1 1	48 "

*maximum for RAM data entry mode

X X	DATA ENTRY MODES
0 0	RAM DATA ENTRY
0 1	LEFT DATA ENTRY
1 0	RIGHT DATA ENTRY
1 1	BLOCK DATA ENTRY

Figure 3. Control Word Format for the HDSP-2470/-2471/-2472 Alphanumeric Display Controller.



(1) RAM ENTRY MODE IS VALID FOR DISPLAYS OF 32 CHARACTERS OR LESS IN LENGTH.
(2) FOLLOWING A TRANSITION FROM RAM TO BLOCK, WHEN THE CURSOR ADDRESS IS 48 (30_{16}) DURING THE TRANSITION, THE FIRST VALID ASCII CHARACTER WILL BE IGNORED AND THE SECOND VALID ASCII CHARACTER WILL BE LOADED IN THE LEFT-MOST DISPLAY LOCATION.

WHERE BEGIN IS DEFINED AS FOLLOWS:

DISPLAY LENGTH	CURSOR ADDRESS OF BEGIN
4	$2C_{16}$, 44_{10}
8	28_{16}, 40_{10}
12	24_{16}, 36_{10}
16	20_{16}, 32_{10}
20	$1C_{16}$, 28_{10}
24	18_{16}, 24_{10}
28	14_{16}, 20_{10}
32	10_{16}, 16_{10}
36	$0C_{16}$, 12_{10}
40	08_{16}, 8_{10}
44	04_{16}, 4_{10}
48	00_{16}

Figure 4. Present State-Next State Diagram for the HDSP-2470/-2471/-2472 Alphanumeric Display Controller.

If D_7 is a logic low when the DATA IN lines are read, the controller will interpret D_6-D_0 as standard ASCII data to be stored, decoded and displayed. The system accepts seven bit ASCII for all three versions. However, the HDSP-2470 system displays only the 64 character subset [20_{16} (space) to $5F_{16}$ (_)] and ignores all ASCII characters outside this subset with the exception of those characters defined as display commands. These display commands are shown in Figure 5. Displayed character sets for the HDSP-2470/-2471 systems are shown in Figure 6.

DATA WORD:	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
ASCII ASSIGNMENT	0	A	A	A	A	A	A	A	DISPLAY COMMAND	
LF	0	0	0	1	0	1	0		CLEAR	Valid in Right Entry Mode
BS	0	0	0	1	0	0	0		BACKSPACE CURSOR	Valid in Left Entry Mode
HT	0	0	0	1	0	0	1		FORWARDSPACE CURSOR	
US	0	0	1	1	1	1	1		INSERT CHARACTER	
DEL	1	1	1	1	1	1	1		DELETE CHARACTER	

Figure 5. Display Commands for the HDSP-2470/-2471/-2472 Alphanumeric Display Controller.

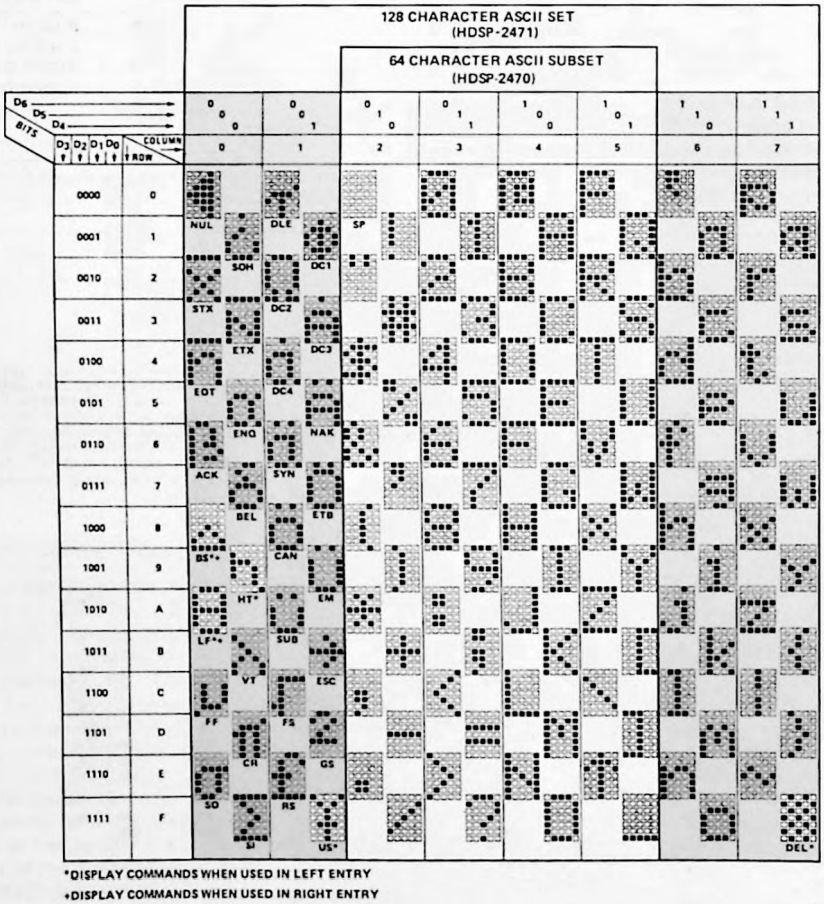
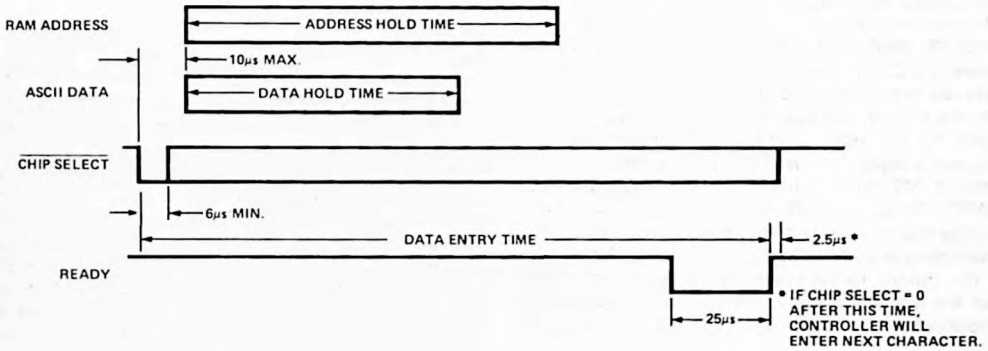


Figure 6. Display Font for the HDSP-2470 (64 Character ASCII Subset), and HDSP-2471 (128 Character ASCII Set) Alphanumeric Display Controller.

Regardless of whether a control word or ASCII data word is presented by the user, a READY signal is generated by the controller after the input word is processed. This READY signal goes low for 25μs and upon a positive transition, a new CHIP SELECT may be accepted by the controller. Data Entry Timing is shown in Figure 7.

DATA ENTRY TIMING



MAXIMUM DATA ENTRY TIMES OVER OPERATING TEMPERATURE RANGE

DATA ENTRY MODE			FUNCTION					
HDSP-	DATA HOLD TIME*		DATA ENTRY	BACK SPACE	CLEAR	FORWARD SPACE	DELETE	INSERT
LEFT (2471/2)	135μs		235μs	195μs	505μs	205μs	725μs	725μs
LEFT (2470)	150μs		245μs	215μs	530μs	225μs	745μs	735μs
RIGHT (2471/2)	85μs		480μs	470μs	465μs			
RIGHT (2470)	105μs		490μs	490μs	485μs			
RAM (2471/2)	55μs	120μs**	190μs					
RAM (2470)	55μs	130μs**	200μs					
BLOCK (2471/2)	55μs		120μs	(155μs FOR RIGHTMOST CHARACTER)				
BLOCK (2470)	55μs		130μs	(165μs FOR RIGHTMOST CHARACTER)				
LOAD CONTROL (2471/2)	50μs		505μs					
LOAD CONTROL (2470)	50μs		505μs					

*Minimum time that data inputs must remain valid after Chip Select goes low.
**Minimum time that RAM address inputs must remain valid after Chip Select goes low.

Figure 7. Data Entry Timing and Data Entry Times for the HDSP-2470/-2471/-2472 Alphanumeric Display Controller.

Left Entry Mode

With Left entry, characters are entered in typewriter fashion, i.e., to the right of all previous characters. Left entry uses a blinking cursor to indicate the location where the next character is to be entered. CLEAR loads the display with spaces and resets the cursor to the leftmost display location. BACKSPACE and FORWARDSPACE move the cursor without changing the character string. Thus, the user can backspace to the character to be edited, enter a character and then forward space the cursor. The DELETE function deletes the displayed character at the cursor location and then shifts the character string following the cursor one location to the left to fill the void of the deleted character. The INSERT CHARACTER sets a flag inside the system that causes subsequent ASCII characters to be inserted to the left of the character at the cursor location. As new characters are entered, the cursor, the character at the cursor, and all characters to the right of the cursor are shifted one location to the right. The INSERT function is terminated by a second INSERT CHARACTER, or by BACKSPACE, FORWARDSPACE, CLEAR or DELETE. In Left entry mode, after the display is filled, the system ignores all characters except BACKSPACE and CLEAR. The system allows the cursor to be positioned only in the region between the leftmost display character and immediately to the right (offscreen) of the rightmost display character.

Right Entry Mode

In Right entry mode, characters are entered at the right hand side of the display and shifted to the left as new characters are entered. In this mode, the system stores 48 ASCII characters, although only the last characters entered are displayed. CLEAR loads the display with spaces. BACKSPACE shifts the display one location to the right, deleting the last character entered and displaying the next character in the 48 character buffer. Right entry mode is a simple means to implement the walking or "Times-Square" display. FORWARDSPACE, INSERT, and DELETE have character assignments in this mode since they are not treated as editing characters. In this mode, the cursor is located immediately to the right (offscreen) of the rightmost displayed character.

Block Entry Mode

Block entry allows the fastest data entry rate of all four modes. In this mode, characters are loaded from left to right as with Left entry. However, with Block entry, after the display is completely loaded, the next ASCII character is loaded in the leftmost display location, replacing the previous displayed character. While Block entry has a nonvisible cursor, the cursor is always loaded with the address of the next character to be entered. In this entry mode, the system can display the complete 128 character ASCII set. The display can be cleared and the cursor reset to the leftmost display location by loading in a new BLOCK control word.

RAM Entry Mode

In RAM entry, ASCII characters are loaded at the address specified by the five bit RAM address. Due to the limitation of only five address lines, RAM data entry is allowed only for displays less than or equal to 32 characters. Regardless of display length, address 00 is the leftmost display character. Out of range RAM addresses are ignored. While RAM entry has a non-visible cursor, the cursor is always preloaded with the address to the right of the last character entered. This allows the cursor to be preloaded with an address prior to going into any other entry mode. In RAM entry, the system can display the complete 128 character ASCII set because it does not interpret any of the characters as control functions. The display can be cleared by loading in a new RAM control word.

Data Out

For display lengths of 32 characters or less, the data stored in the internal RAM is available to the user during the time between display refresh cycles. The system outputs a STATUS WORD, CURSOR ADDRESS, and 32 ASCII data characters. The STATUS WORD specifies the data entry mode and the display length of the system. The STATUS WORD output differs slightly from the CONTROL WORD input. This difference is depicted in Figure 8. Regardless of display length, the CURSOR ADDRESS of the rightmost character location is address 47 ($2F_{16}$) and the offscreen address of the cursor is address 48 (30_{16}). The CURSOR ADDRESS of the leftmost location is defined as address 48 minus the display length. A general formula for CURSOR ADDRESS is:

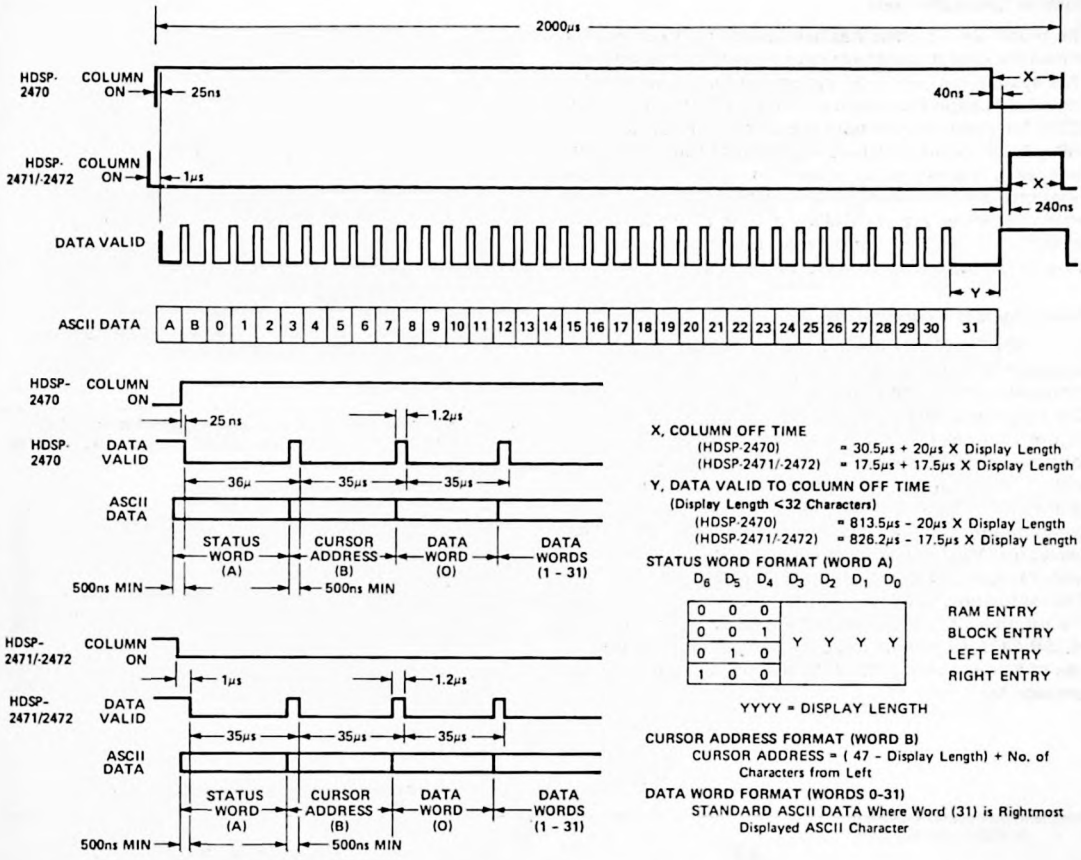
CURSOR ADDRESS =

(47 - Display Length) + Number of Characters from Left.

For example, suppose the alphanumeric display is 16 characters long and the cursor was blinking at the third digit from the left. Then the CURSOR ADDRESS would be 47 - 16 + 3 or 34 (22_{16}) and the 18th ASCII data word would correspond to the ASCII character at the location of the display cursor. In Left and Block entry, the CURSOR ADDRESS specifies the location where the next ASCII data character is to be entered. In RAM entry, the CURSOR ADDRESS specifies the location to the right of the last character entered. In Right entry, the CURSOR ADDRESS is always 48 (30_{16}). The negative edge of the DATA VALID output can be used to load the 34 DATA OUT words into the user's system. The DATA OUT timing for the HDSP-247X systems are summarized in Figure 8. For displays longer than 32 characters, the system only outputs the STATUS WORD between refresh cycles.

Master/Power On Reset

When power is first applied to the system, the system clears the display and tests the state of the DATA INPUT, D_7. If $D_7 > 2.0V$, the systems loads the control word on the DATA INPUTS into the system. If $D_7 \leq .8V$ or the system sees an invalid control word, the system initializes as Left entry for a 32 character display with a flashing cursor in the leftmost location. For POWER ON RESET to function properly, the power supply must turn on at a rate > 100 V/s. In addition, the system can be reset by pulling the RESET input low for a minimum of 50 milliseconds. POWER ON/MASTER RESET timing is shown in Figure 9.



X, COLUMN OFF TIME
(HDSP-2470) = 30.5µs + 20µs X Display Length
(HDSP-2471/-2472) = 17.5µs + 17.5µs X Display Length

Y, DATA VALID TO COLUMN OFF TIME
(Display Length <32 Characters)
(HDSP-2470) = 813.5µs - 20µs X Display Length
(HDSP-2471/-2472) = 826.2µs - 17.5µs X Display Length

STATUS WORD FORMAT (WORD A)

D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	0	0	Y	Y	Y	Y	RAM ENTRY
0	0	1					BLOCK ENTRY
0	1	0					LEFT ENTRY
1	0	0					RIGHT ENTRY

YYYY = DISPLAY LENGTH

CURSOR ADDRESS FORMAT (WORD B)
CURSOR ADDRESS = (47 - Display Length) + No. of Characters from Left

DATA WORD FORMAT (WORDS 0-31)
STANDARD ASCII DATA Where Word (31) is Rightmost Displayed ASCII Character

Figure 8. Data Out Timing and Format for the HDSP-2470/-2471/-2472 Alphanumeric Display Controller.

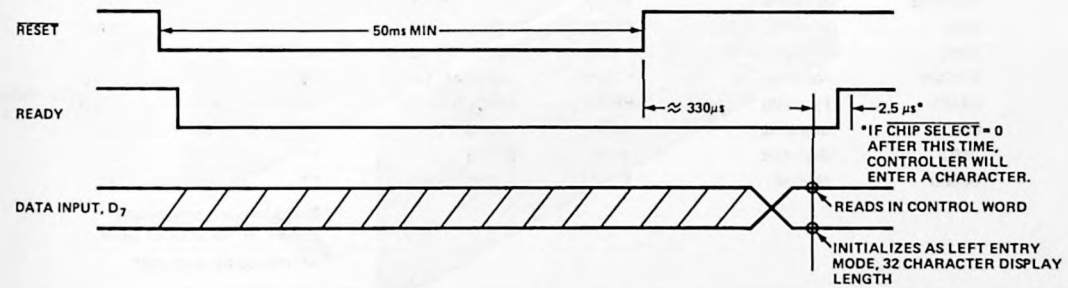


Figure 9. Power-On/Master Reset Timing for the HDSP-2470/-2471/-2472 Alphanumeric Display Controller.

Custom Character Sets

The HDSP-2472 system has been specifically designed to permit the user to insert a custom 128 ASCII character set. This system features a 24 pin socket that is designed to accept a custom programmed 1K X 8 PROM, EPROM, or ROM. The read only memory should have an access time ≤ 500ns, $I_{IL} \leq |-.4mA|$ and $I_{IH} \leq 40\mu A$. A list of pin compatible read only memories is shown in Figure 10. Jumper locations are provided on the HDSP-2472 P.C. board which allow the use of ROM's requiring chip enables tied either to 0 or 5V. For further information on ROM programming, please contact the factory.

Power Supply Requirements

The HDSP-247X Alphanumeric Display System is designed to operate from a single 5 volt supply. Total I_{CC} requirements for the HDSP-247X Alphanumeric Display Controller and HDSP-24XX Display Panel are shown in Figure 11. Peak I_{CC} is the instantaneous current required for the system. Maximum Peak I_{CC} occurs for $V_{CC} = 5.25V$ with 7 dots ON in the same Column in all display characters. This current must be supplied by a combination of the power supply and supply filter capacitor. Maximum Average I_{CC} occurs for $V_{CC} = 5.25V$ with 21 dots ON per character in all display characters. The inclusion of a 375 X microfarad capacitor (where X is the number of characters in the display) adjacent to the HDSP-247X Alphanumeric Display System will permit the use of a power supply capable of supplying the maximum average I_{CC}.

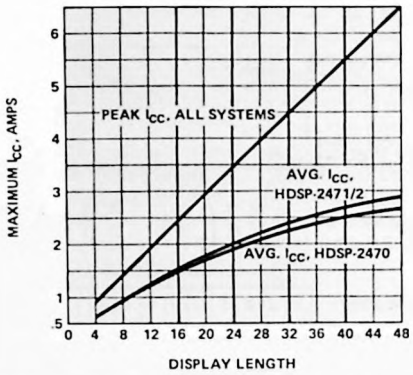


Figure 11. Maximum Peak and Average I_{CC} for the HDSP-2470/71/72 Alphanumeric Display Controller and HDSP-2000 Display.

CONNECTORS

FUNCTION	TYPE OF CONNECTOR	SUGGESTED MANUFACTURER
CONTROL/DATA ENTRY	26 Pin Ribbon Cable	3M P/N 3399-X000 Series
POWER(1)	3 Pin With Locking Ramp	Molex P/N 09-50-3031 with 08-50-0106 Terminals
DISPLAY DRIVE(2,3)	17 Lead Board to Board	Amp P/N 1-530500-7, also available in board to cable and other configurations

NOTES:
(1) Power leads should be 18-20 gauge stranded wire.
(2) The maximum lead length from the controller board to the display should not exceed 1 metre.
(3) The suggested Amp connector is supplied with the controller.

PART NUMBER	MANUFACTURER	TYPE	CONSTRUCTION	EXTERNAL CONNECTION* X	Y	Z
2758	Intel	EPROM	NMOS	GND	GND	+5
7608	Harris	PROM	BIPOLAR-NiCr	NC	NC	NC
3628-4	Intel	PROM	BIPOLAR-Si	+5	+5	GND
82S2708	Signetics	PROM	BIPOLAR-NiCr	NC	NC	NC
6381	Monolithic Mem.	PROM	BIPOLAR-NiCr	+5	+5	GND
6385	Monolithic Mem.	PROM	BIPOLAR-NiCr	NC	NC	NC
87S228	National	PROM	BIPOLAR-TiW	+5	+5	GND
93451	Fairchild	PROM	BIPOLAR-NiCr	+5	+5	GND
68308	Motorola	ROM	NMOS	**	NC	NC
2607	Signetics	ROM	NMOS	**	NC	NC
30000	Mostek	ROM	NMOS	**	+5	NC

*Board jumpers correspond to pins 18, 19 & 21 of ROM.
**As defined by customer

Figure 10. Pin Compatible 1K x 8 Read Only Memories for the HDSP-2472 Alphanumeric Display Controller.

Display Boards/Hardware

The mechanical layout of the HDSP-247X Series allows direct mating of the controller P.C. board to a compatible series of display boards available from Hewlett-Packard. These display boards consist of matched and tested HDSP-2000 clusters soldered to a P.C. board.

Included with the controller board are: 1 each Amp P/N 1-530500-7 board to board connector, and 4 each locking circuit board support nylon standoffs (Richco LCBS-4). This hardware allows the controller board to interconnect with any of the standard display boards. Figure 12 depicts correct assembly technique.

Assembly Steps

1. Insert the standoffs into .151 diameter holes (noted as "S" on Figure 12. The long end of the standoffs should protrude through the controller board side.
2. Position the controller board and display board with the components and displays facing out. The HP logo should be in the upper left corner when viewed facing the boards. Insert the standoffs through the mating holes on the display board and press the boards together so that the standoffs lock in place.
3. After the standoffs are secured, the Amp connector should be placed on the edge connect pads (marked "A" through "Q" Figure 12) at the top of the boards. Visual alignment of this connector may be done on the controller board by determining that the first connector contact finger is centered on the pad labeled "A".

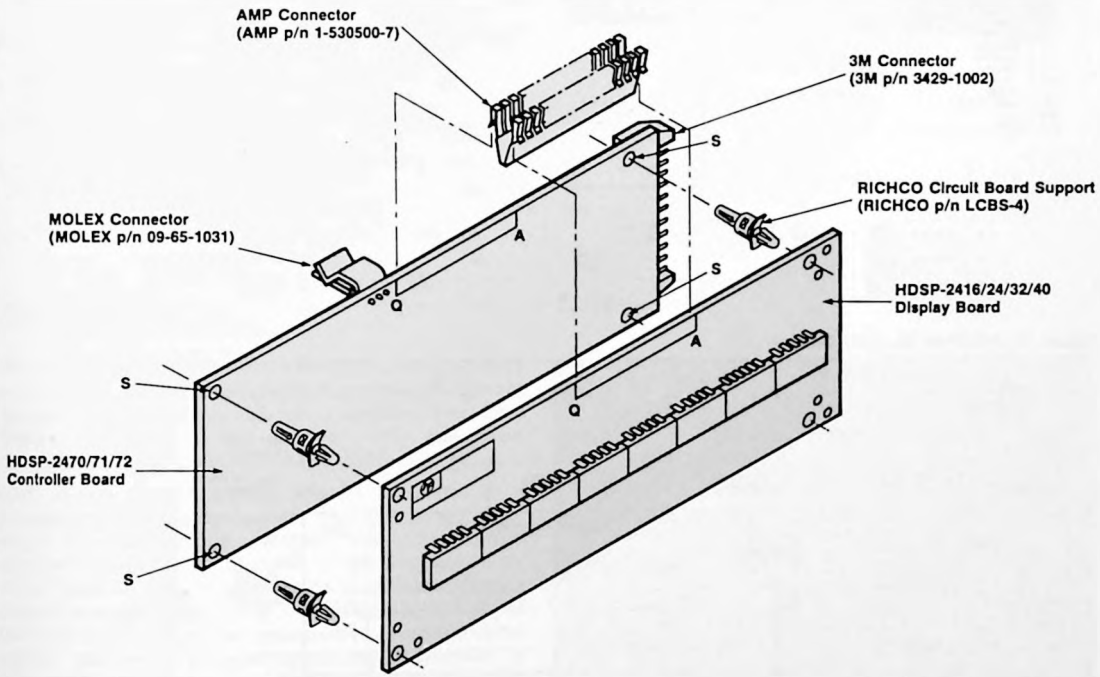


Figure 12. Assembly Drawing.

Package Dimensions

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN mm AND (INCHES)

HDSP 2470, 2471/2472

PIN	DESCRIPTION
1	CHIP SELECT
2	DATA VALID
3	RAM ADDRESS, A_0
4	DATA IN, D_7
5	RAM ADDRESS, A_1
6	RESET
7	RAM ADDRESS, A_2
8	DATA OUT, DO_6
9	RAM ADDRESS, A_3
10	DATA OUT, DO_5
11	DATA IN, D_6
12	DATA OUT DO_4
13	DATA IN, D_5
14	DATA OUT, DO_3
15	DATA IN, D_4
16	DATA OUT, DO_2
17	DATA IN, D_3
18	DATA OUT, DO_1
19	DATA IN, D_2
20	DATA OUT, DO_0
21	DATA IN, D_1
22	READY
23	DATA IN, D_0
24	COLUMN ON
25	RAM ADDRESS, A_4
26	DISPLAY BLANK, V_B

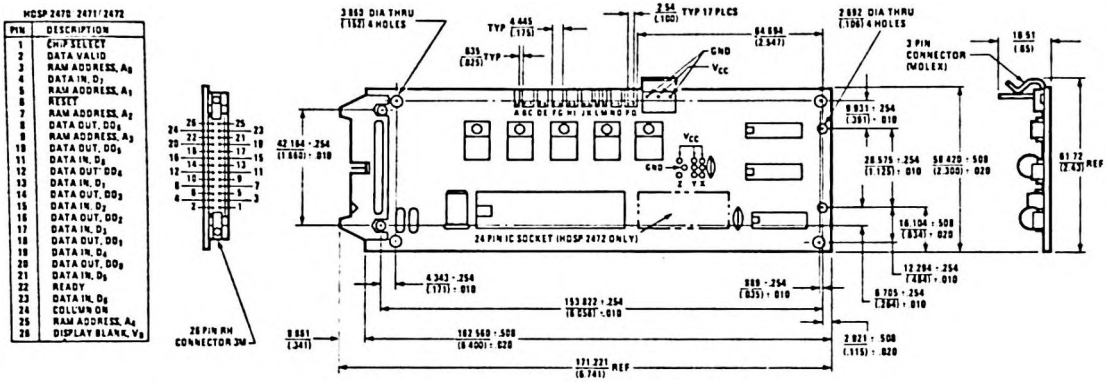


Figure 13. HDSP-2470/-2471/-2472

HDSP 2416, 2424, 2432, 2440
HDSP 2470, 2471/2472

PIN	DESCRIPTION
A	DISPLAY BLANK, V_B
B,C	COLUMN$_1$
D,E	COLUMN$_2$
F,G	COLUMN$_3$
H,I	COLUMN$_4$
J,K	COLUMN$_5$
L	CLOCK
M	DISPLAY DATA
N,O	V_{CC}
P,Q	GND

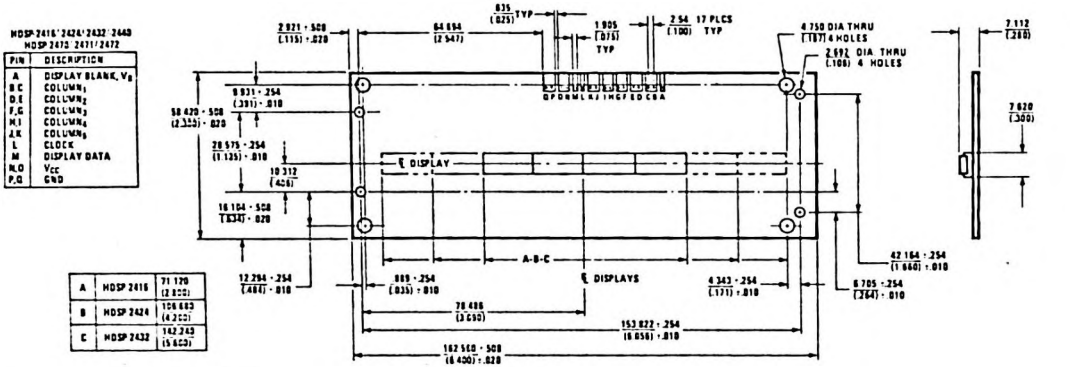


Figure 14. HDSP-2416/-2424/-2432

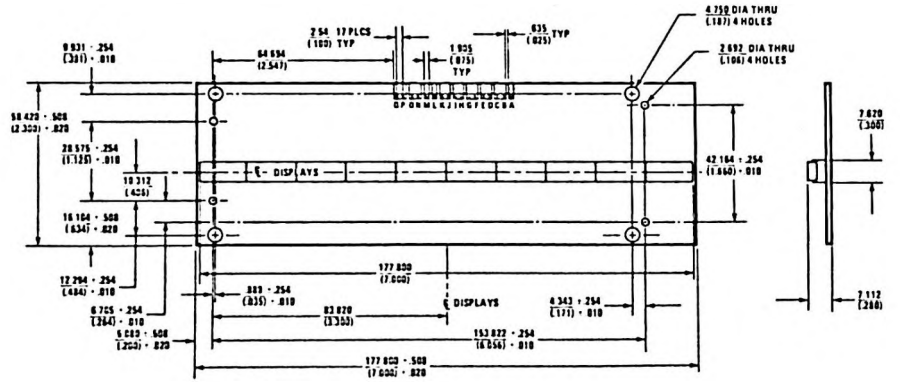


Figure 15. HDSP-2440

HEWLETT PACKARD

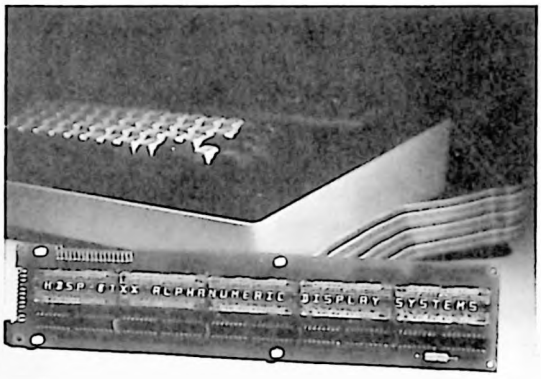
16 SEGMENT ALPHANUMERIC DISPLAY SYSTEM

HDSP-8716
HDSP-8724
HDSP-8732
HDSP-8740

TECHNICAL DATA JANUARY 1984

Features

- COMPLETE ALPHANUMERIC DISPLAY SYSTEM UTILIZING THE HDSP-6508 DISPLAY
- DISPLAYS 64 CHARACTER ASCII SET
- CHOICE OF 16, 24, 32, OR 40 ELEMENT DISPLAY PANEL
- MULTIPLE DATA ENTRY FORMATS Left, Right, RAM, or Block Entry
- EDITING FEATURES THAT INCLUDE CURSOR, BACKSPACE, FORWARDSPACE, INSERT, DELETE, CARRIAGE RETURN, AND CLEAR
- DATA OUTPUT CAPABILITY
- SINGLE 5.0 VOLT POWER SUPPLY
- TTL COMPATIBLE
- EASILY INTERFACED TO A KEYBOARD OR A MICROPROCESSOR



Description

The HDSP-87XX series of alphanumeric display systems provides the user with a completely supported 16 segment display panel. These products free the user's system from display maintenance and minimize the interaction normally required for alphanumeric displays.

Each alphanumeric display system consists of a preprogrammed microprocessor plus associated logic, which provides decode, memory, and drive signals necessary to properly interface a user's system to an HDSP-6508 display. In addition to these basic display support operations, the controller accepts data in any of four data entry formats and incorporates several powerful editing routines. This microprocessor controller is mounted behind a single line display panel consisting of HDSP-6508 displays matched for luminous intensity.

These alphanumeric display systems are attractive for applications such as data entry terminals, instrumentation,, electronic typewriters, and other products which require an easy to use 16 segment alphanumeric display system.

Part Number	Description
HDSP-8716	Single-line 16 Character Alphanumeric Display System utilizing the HDSP-6508 Display
HDSP-8724	Single-line 24 Character Alphanumeric Display System utilizing the HDSP-6508 Display
HDSP-8732	Single-line 32 Character Alphanumeric Display System utilizing the HDSP-6508 Display
HDSP-8740	Single-line 40 Character Alphanumeric Display System utilizing the HDSP-6508 Display

HDSP-8716/-8724/-8732/-8740

Absolute Maximum Ratings

V_{CC} ..... -0.5V to 6.0V
Operating Temperature Range,
Ambient (T_A) ..... 0°C to 70°C
Storage Temperature Range (T_S) ..... -40°C to 85°C
Voltage Applied to any
Input or Output ..... -0.5V to 6.0V

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Data Out, Data Valid Ready, $\overline{\text{Refresh}}$	I_{OL}		3.2	mA
	I_{OH}		-80	μA
$\overline{\text{Active}}$, Clock	I_{OL}		1.6	mA
	I_{OH}		-40	μA

Electrical Characteristics Over Operating Temperature Range

(Unless otherwise specified)

Parameter		Symbol	Min.	Typ.[5]	Max.	Units	Conditions
Supply Current	HDSP-8716/-8724	I_{CC}		560	1150	mA	V_{CC}=5.25V, "$" Displayed in All
	HDSP-8732/-8740	I_{CC}		700	1320	mA	Character Locations, All Outputs Open
Time Average Luminous Intensity Per Digit, 10 Segments on[1]		I_V	.24	.70		mcd	V_{CC}=5.0V, Digit Average '$' Displayed In All Character Locations, T_A=25°C
Input Threshold High (except $\overline{\text{Reset}}$)		V_{IH}	2.0			V	V_{CC}=5.0V ± .25V
Input Threshold High — $\overline{\text{Reset}}$[2]		V_{IH}	3.0			V	
Input Threshold Low — All Inputs		V_{IL}			0.8	V	
Data Out, Data Valid, Ready, $\overline{\text{Refresh}}$, Output Voltage		V_{OH}	2.4			V	I_{OH}=-80μA, V_{CC} = 4.75V
		V_{OL}			0.5	V	I_{OL}=3.2 mA, V_{CC}=4.75V
$\overline{\text{Active}}$, Clock Output Voltage		V_{OH}	2.4			V	I_{OH}=-40μA, V_{CC}=4.75V
		V_{OL}			0.5	V	I_{OL}=1.6mA, V_{CC}=4.75V
Address,[3] $\overline{\text{Expand}}$, Input Current		I_{IH}			-0.3	mA	V_{IH}=2.4V, V_{CC}=5.25V
		I_{IL}			-0.6	mA	V_{IL}=0.5V, V_{CC}=5.25V
$\overline{\text{Blank}}$ Input Current		I_{IH}			-0.5	mA	V_{IH}=2.4V, V_{CC}=5.25V
		I_{IL}			-1.0	mA	V_{IL}=0.5V, V_{CC}=5.25V
$\overline{\text{Reset}}$ Input Current		I_{IH}			-0.5	mA	V_{IH}=3.0V, V_{CC}=5.25V
		I_{IL}			-1.0	mA	V_{IL}=0.5V, V_{CC}=5.25V
Data In, $\overline{\text{Chip Select}}$, Input Current		I_I	-10		+10	μA	0<V_I<V_{CC}
Peak Wavelength		λ_{PEAK}		655		nm	
Dominant Wavelength[4]		λ_d		640		nm	

NOTES:
1. The luminous intensity ratio between segments within a digit is designed so that each segment will have the same luminous sterance. Thus, each segment will appear with equal brightness to the eye.
2. External reset may be initiated by grounding $\overline{\text{Reset}}$ with either a switch or open collector TTL gate for a minimum time of 50ms. For Power On Reset to function properly, V_{CC} power supply should turn on at a rate > 100V/S.
3. Momentary peak surge currents may exist on these lines. However, these momentary currents will not interfere with proper operation of the HDSP-8716/-8724/-8732/-8740.
4. The dominant wavelength, λ_d, is derived from the C.I.E. chromaticity diagram and represents that single wavelength which defines the color of the device, standard red.
5. All typical values at V_{CC} = 5.0V and T_A = 25°C unless otherwise noted.

System Overview

The HDSP-8716/-8724/-8732/-8740 Alphanumeric Display Controllers provide the interface between any ASCII based Alphanumeric System and the HDSP-6508 Alphanumeric Display. ASCII data is loaded into the system by means of any one of four data entry modes — Left, Right, RAM, or Block Entry. This ASCII data is stored in the internal RAM memory of the system. The system may also be expanded to form multiple line panels with system to system control signals.

The user interfaces to any of the system through eight DATA IN inputs, six ADDRESS inputs (RAM mode), a $\overline{\text{CHIP SELECT}}$ input, $\overline{\text{RESET}}$ input, $\overline{\text{BLANK}}$ input, $\overline{\text{EXPAND}}$ input, six DATA OUT outputs, a READY output, DATA VALID output, $\overline{\text{REFRESH}}$ output, and CLOCK output. A low level on the $\overline{\text{RESET}}$ input clears the display and initializes the system. A low level on the $\overline{\text{CHIP SELECT}}$ input causes the system to load data from the DATA IN and ADDRESS inputs into the system. A special control word causes the controller to output a STATUS WORD, CURSOR ADDRESS, and a string of ASCII characters through the DATA OUT outputs and DATA VALID output. A low level on the $\overline{\text{EXPAND}}$ input allows two or more systems to be configured for multiple line display panels. Pulse width modulation of display luminous intensity can be provided by connecting $\overline{\text{REFRESH}}$ to the input of a monostable multivibrator and the output of the monostable multivibrator to the $\overline{\text{BLANK}}$ input. A 400kHz clock is provided on the CLOCK output. A system block diagram for the HDSP-8716/-8724/-8732/-8740 systems is shown in Figure 1. The system is designed to refresh the display at a fixed refresh rate of 100Hz. The display duty factor is optimized for each display length in order to maximize light output.

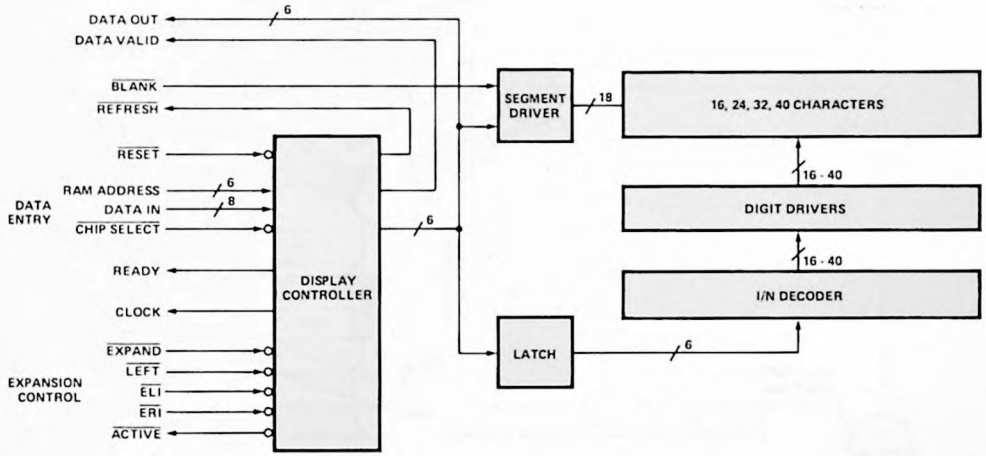


Figure 1. Block Diagram of the HDSP-8716/-8724/-8732/-8740 Alphanumeric Display System.

Control Mode/Data Entry

User interface to the HDSP-87XX series controller is via an 8-bit word which provides to the controller either a control word or standard ASCII data input. In addition to this user provided 8-bit word, two additional control lines, $\overline{\text{CHIP SELECT}}$ and READY, allow easily generated "handshake" signals for interface purposes.

A logic low applied to the $\overline{\text{CHIP SELECT}}$ input (minimum six microseconds) causes the controller to read the 8 DATA IN lines and determine whether a control word or ASCII data word is present, as determined by the logic state of the most significant bit (D_7). If the controller detects a logic high at D_7, the state of D_6-D_0 will define the data entry mode and appropriate display length.

The 8 bit control data word format is outlined in Figure 2. For the control word (D_7 high), bits D_5 and D_4 define the selected data entry mode (Left entry, Right entry, etc.) and bits D_3 to D_0 define display length. Bit D_6 is ignored.

Control word inputs are first checked to verify that the control word is valid. If the word is valid, the present state — next state table shown in Figure 3 is utilized to determine whether or not to clear the display. RAM entry can be used as a powerful editing tool or can be used to preload the cursor. With other transitions, the internal memory is cleared. The CONTROL WORD $1XXX11XX_2$ is used by the controller to initiate the DATA OUT function.

DATA ENTRY CONTROL WORD: $D_7\ D_6\ D_5\ D_4\ D_3\ D_2\ D_1\ D_0$

1	–	X	X	Y	Y	Y	Y

X X	DATA ENTRY MODES
0 0	RAM DATA ENTRY
0 1	LEFT DATA ENTRY
1 0	RIGHT DATA ENTRY
1 1	BLOCK DATA ENTRY

Y Y Y Y	DISPLAY LENGTH	
0 0 1 1	16 DIGITS	HDSP-8716
0 1 0 1	24 DIGITS	HDSP-8724
0 1 1 1	32 DIGITS	HDSP-8732
1 0 0 1	40 DIGITS	HDSP-8740

DATA OUT CONTROL WORD: $D_7\ D_6\ D_5\ D_4\ D_3\ D_2\ D_1\ D_0$

1	–	–	–	1	1	–	–

DATA OUT

Figure 2. Control Word Format for the HDSP-8716/-8724/-8732/-8740 Alphanumeric Display System.

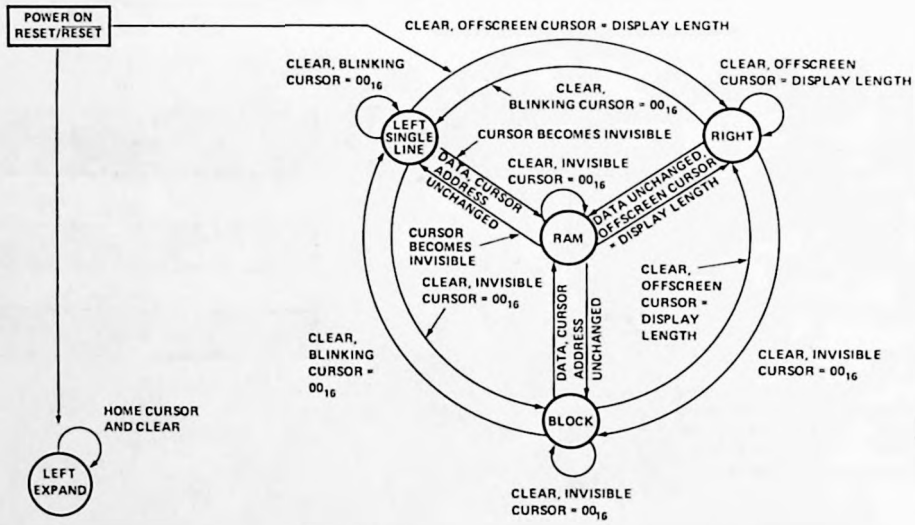


Figure 3. Present State-Next State Diagram for the HDSP-8716/-8724/-8732/-8740 Alphanumeric Display System.

DATA WORD: $D_7\ D_6\ D_5\ D_4\ D_3\ D_2\ D_1\ D_0$

ASCII ASSIGNMENT: 0 X X X X X X X

BS	0 0 0 1 0 0 0	BACKSPACE	RIGHT
LF	0 0 0 1 0 1 0	CLEAR (NEW LINE*)	RIGHT
HT	0 0 0 1 0 0 1	FORWARDSPACE	RIGHT
CR	0 0 0 1 1 0 1	CARRIAGE RETURN	LEFT, SINGLE
US	0 0 1 1 1 1 1	INSERT CHARACTER	LEFT, SINGLE
DEL	1 1 1 1 1 1 1	DELETE CHARACTER	LEFT, SINGLE
VT	0 0 0 1 0 1 1	CURSOR DOWN	LEFT, EXPAND*
FF	0 0 0 1 1 0 0	HOME & CLEAR	LEFT, EXPAND*
RS	0 0 1 1 1 1 0	CURSOR UP	LEFT, EXPAND*

OTHERWISE, THE 7 BIT ASCII CODE

Figure 4. Display Commands for the HDSP-8716/-8724/-8732/-8740 Alphanumeric Display System.

If D_7 is a logic low when the DATA IN lines are read, the controller will interpret D_6-D_0 as standard ASCII data to be stored, decoded, and displayed. The system accepts the standard 7-bit ASCII code. However, the HDSP-87XX system displays only the 64 character subset (20_{16} (space) to $5F_{16}$ (↑)) and ignores all ASCII characters outside this subset with the exception of those characters defined as display commands. These display commands are shown in Figure 4. The displayed character set for the HDSP-87XX system is shown in Figure 5.

Regardless of whether a control word or ASCII data word is presented by the user, a READY signal is generated by the controller after the input word is processed. This READY signal goes low for 35μs and upon a positive transition, a new $\overline{\text{CHIP SELECT}}$ may be accepted by the controller. Data Entry Timing is shown in Figure 6.

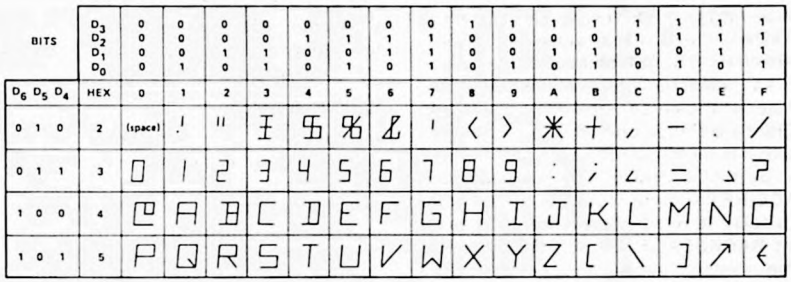
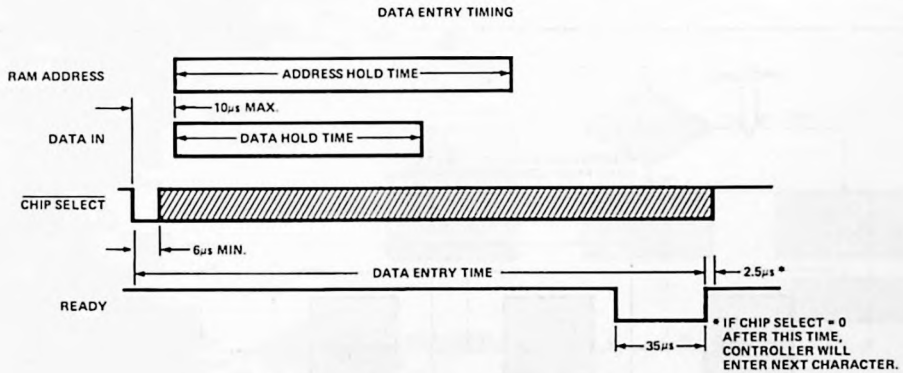


Figure 5. Display Font for the HDSP-8716/-8724/-8732/-8740 Alphanumeric Display System.



MAXIMUM DATA ENTRY TIMES OVER OPERATING TEMPERATURE RANGE

DATA ENTRY MODE		FUNCTION									
	DATA HOLD TIME*	DATA ENTRY	BS	HT	LF	CR	US	INSERT	DEL	VT	FF	RS
LEFT, SINGLE	25μs	250μs	215μs	235μs	505μs	220μs	200μs	665μs	645μs			
LEFT, EXPANDED	25μs	345μs	265μs	265μs	265μs	245μs	245μs	705μs	630μs	250μs	530μs	245μs
RIGHT	25μs	480μs	480μs		485μs							
RAM	25μs 145μs**	220μs										
BLOCK	25μs	130μs (165μs FOLLOWING RIGHTMOST CHARACTER)										
CONTROL	25μs	545μs										
DATA OUT	25μs	280μs + 36nμs, WHERE n = CONFIGURED DISPLAY LENGTH										

*MINIMUM TIME THAT DATA INPUTS MUST REMAIN VALID AFTER CHIP SELECT GOES LOW.
**MINIMUM TIME THAT RAM ADDRESS INPUTS MUST REMAIN VALID AFTER CHIP SELECT GOES LOW.

Figure 6. Data Entry Timing and Data Entry Times for the HDSP-8716/-8724/-8732/-8740 Alphanumeric Display System.

Left Entry Mode

With Left entry, characters are entered in typewriter fashion, i.e., to the right of all previous characters. Left entry uses a blinking cursor to indicate the location where the next character is to be entered. CLEAR loads the display with spaces and resets the cursor to the leftmost display location. BACKSPACE and FORWARDSPACE move the cursor without changing the character string. Thus, the user can backspace to the character to be edited, enter a character and then forwardspace the cursor. CARRIAGE RETURN resets the cursor to the leftmost display location leaving the display unchanged. The DELETE function deletes the displayed character at the cursor location and then shifts the character string following the cursor one location to the left to fill the void of the deleted character. The INSERT CHARACTER sets a flag inside the system that causes subsequent ASCII characters to be inserted to the left of the character at the cursor location. As new characters are entered, the cursor, the character at the cursor, and all characters to the right of the cursor are shifted one location to the right. The INSERT function is terminated by a second INSERT CHARACTER, or by BACKSPACE, FORWARDSPACE, CLEAR, CARRIAGE RETURN, or DELETE. In Left entry mode, after the display is filled, the system ignores all characters except BACKSPACE, CARRIAGE RETURN, and CLEAR. The system allows the cursor to be positioned only in the region between the leftmost display character and immediately to the right (offscreen) of the rightmost display character.

Expanded Left entry is selected by grounding the $\overline{\text{EXPAND}}$ input prior to $\overline{\text{RESET}}$. Expanded Left entry mode allows several HDSP-87XX systems to be connected into a multiple line panel. Expanded Left entry uses the $\overline{\text{ERI}}$ input, $\overline{\text{ELI}}$ input, $\overline{\text{LEFT}}$ input, and $\overline{\text{ACTIVE}}$ output to provide a handshake between each system as shown in Figure 7. With the proper connections, the cursor can be moved in a circular fashion from the end of the last line to the beginning of the first line, or such that it shifts offscreen and is lost until the next CLEAR/HOME display command. Expanded Left entry adds three display commands: CURSOR UP moves the cursor to the same location in the preceeding line; CURSOR DOWN moves the cursor to the same location in the following line; CLEAR/HOME loads all displays with spaces and resets the cursor to the leftmost display location in the first line. The CLEAR command in Left entry mode is replaced by the LINE FEED function. LINE FEED moves the cursor to the leftmost display location in the following line leaving the current line unchanged.

Right Entry Mode

In Right entry mode, characters are entered at the right hand side of the display and shifted to the left as new characters are entered. In this mode, the system stores 48 ASCII characters, although only the last characters entered are displayed. CLEAR loads the display with spaces. BACKSPACE shifts the display one location to the right, deleting the last character entered and displaying the next character in the 48 character buffer. Right entry mode is a simple means to implement the walking or "Times-Square" display. In this mode, the cursor is located immediately to the right (offscreen) of the rightmost displayed character.

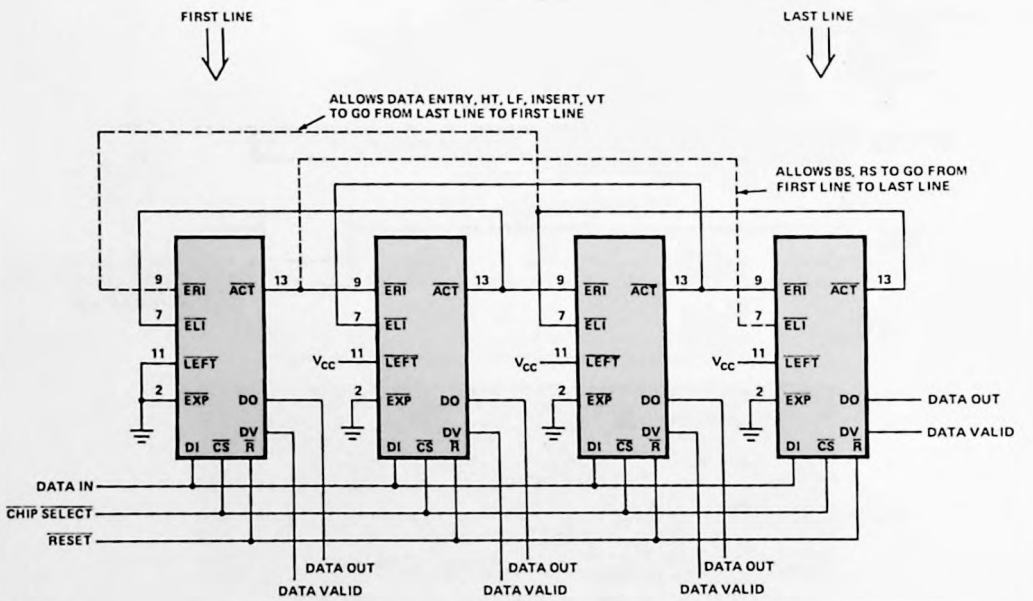


Figure 7. External Connections for Expanded Left Entry Mode for the HDSP-8716/-8724/-8732/-8740 Alphanumeric Display System.

Block Entry Mode

Block entry allows the fastest data entry rate of all four modes. In this mode, characters are loaded from left to right as with Left entry. However, with Block entry, after the display is completely loaded, the next ASCII character is loaded in the leftmost display location, replacing the previous displayed character. While Block entry has a non-visible cursor, the cursor is always loaded with the address of the next character to be entered. The display can be cleared and the cursor reset to the leftmost display location by loading in a new BLOCK control word.

RAM Entry Mode

In RAM entry, ASCII characters are loaded at the address specified by the six bit RAM address. Regardless of display length, address 00 is the leftmost display character. Out of range RAM addresses are ignored. While RAM entry has a non-visible cursor, the cursor is always preloaded with the address to the right of the last character entered. This allows the cursor to be preloaded with an address prior to going into any other entry mode. The display can be cleared by loading in a new RAM control word.

Power-On Reset/$\overline{\text{Reset}}$

When power is first applied to the system, the system clears the display and tests the state of the DATA INPUT, D_7. If $D_7 > 2.0V$, the system loads the control word on the DATA INPUTS into the system. If $D_7 \leq 0.8V$ or the system sees an invalid control word, the system initializes as Left entry for a 40 character display with a flashing cursor in the leftmost location. During $\overline{\text{RESET}}$, the system also tests the state of the $\overline{\text{EXPAND}}$ input. If $\overline{\text{EXPAND}}$ is low, the system initializes in expanded left entry mode. A flow chart that describes the $\overline{\text{RESET}}$ function is shown in Figure 8. For POWER-ON RESET to function properly, the

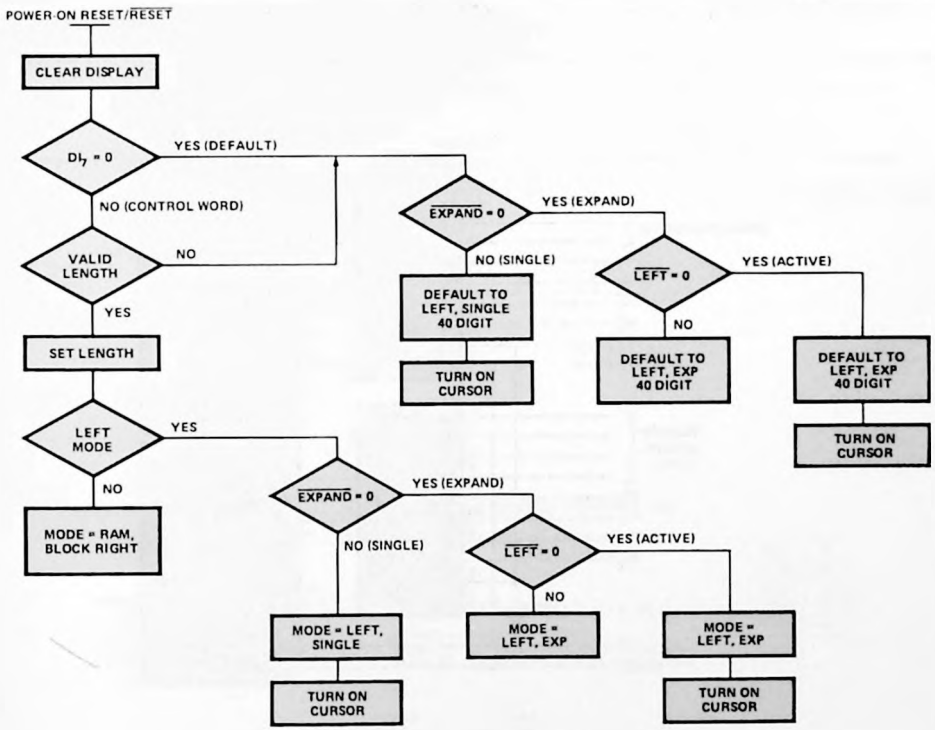


Figure 8. Reset Sequence for the HDSP-8716/-8724/-8732/-8740 Alphanumeric Display System.

power supply must turn on at a rate > 100 V/s. In addition, the system can be reset by pulling the $\overline{\text{RESET}}$ input low for a minimum of 50 milliseconds. POWER-ON RESET/$\overline{\text{RESET}}$ timing is shown in Figure 9.

If some entry mode or display length is desired other than 40 character Left entry, it is necessary to either load the appropriate control word or provide a control word during POWER-ON RESET/$\overline{\text{RESET}}$. The circuit shown in Figure 10 can be used to load any desired preprogrammed control word into the HDSP-87XX Series Display Controller during POWER-ON RESET/$\overline{\text{RESET}}$.

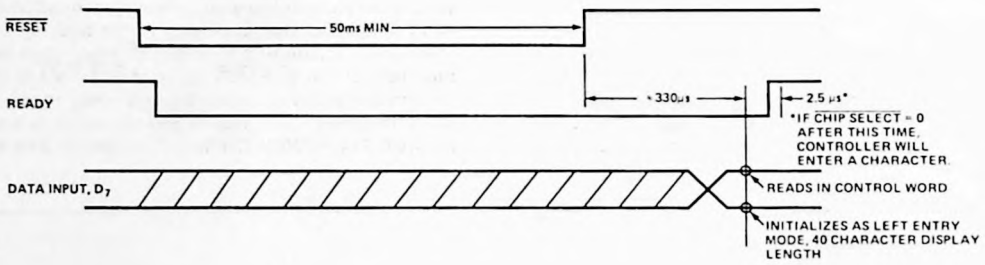
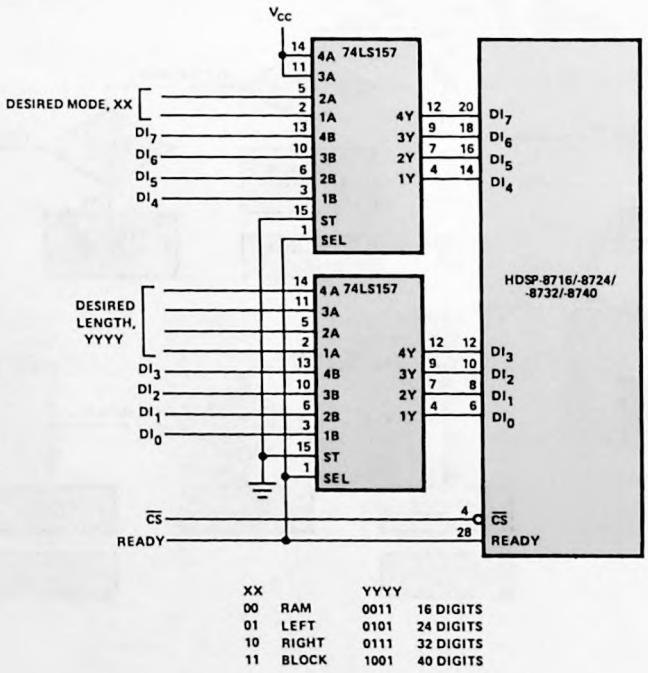


Figure 9. POWER-ON RESET/$\overline{\text{RESET}}$ Timing for the HDSP-8716/-8724/-8732/-8740 Alphanumeric Display System.



XX		YYYY	
00	RAM	0011	16 DIGITS
01	LEFT	0101	24 DIGITS
10	RIGHT	0111	32 DIGITS
11	BLOCK	1001	40 DIGITS

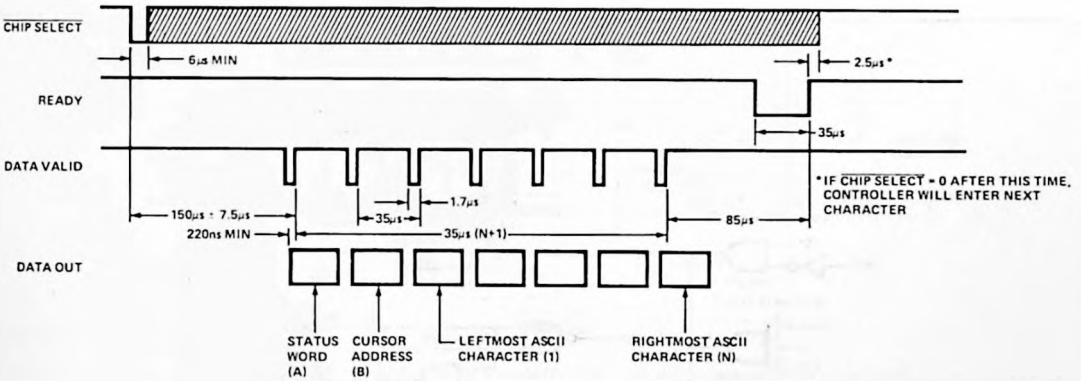
Figure 10. External Circuitry to Load a Control Word into the HDSP-8716/-8724/-8732/-8740 Alphanumeric Display System Upon POWER-ON RESET/$\overline{\text{RESET}}$.

Data Out

Data stored in the HDSP-87XX system is available to the user upon command. Data Out is initiated by the control word $1XXX11XX_2$. Following this control word, the system outputs a STATUS WORD, CURSOR ADDRESS, and a string of ASCII data characters. The STATUS WORD specifies the data entry mode and the display length of the system. The STATUS WORD is the same format as a valid control word with D_7 and D_6 deleted. The CURSOR ADDRESS specifies the location of the cursor within the display. The CURSOR ADDRESS of the leftmost display location is address 00. In Expanded Left entry mode, a CURSOR ADDRESS of 63_{10} ($3F_{16}$) is used to indicate a non-active line. The system outputs the same number of ASCII data characters as the display length specified by the control word. The first ASCII data character is always the leftmost display character. The positive edge of the DATA VALID output can be used to load the DATA OUTPUT words into the user's system. The DATA OUT timing for the HDSP-87XX systems is summarized in Figure 11.

Luminous Intensity Modulation

Pulse width modulation of display luminous intensity can be provided by connecting the $\overline{\text{REFRESH}}$ output of the system to the input of a monostable multivibrator. The output of the monostable multivibrator should then be connected to the $\overline{\text{BLANK}}$ input of the system. Modulation of display luminous intensity is then achieved by varying the delay of the monostable multivibrator with a potentiometer or photoresistor. $\overline{\text{REFRESH}}$ is repeated at a rate of 10ms divided by the configured display length. For example, an HDSP-8732 system, when configured for a 32 character display length, would pulse the $\overline{\text{REFRESH}}$ output every 312.5μs. The circuit shown in Figure 12 may be utilized to provide manual control of display luminous intensity. Automatic control may be achieved by substituting an appropriate value photoconductor for potentiometer R_1. If luminous intensity modulation is not desired, $\overline{\text{BLANK}}$ should be left open.



STATUS WORD FORMAT (A)

$D_5\ D_4\ D_3\ D_2\ D_1\ D_0$

0 0	YYYY	RAM ENTRY
0 1		LEFT ENTRY
1 0		RIGHT ENTRY
1 1		BLOCK ENTRY

YYYY = DISPLAY LENGTH

CURSOR ADDRESS FORMAT (B)

CURSOR ADDRESS = NO. OF CHARACTERS FROM THE LEFT

HDSP	N
-8716	16
-8724	24
-8732	32
-8740	40

DATA WORD FORMAT (1 – N)

LOWEST 6 BITS OF ASCII CODE
WORD (1) = LEFTMOST DISPLAY CHARACTER
WORD (N) = RIGHTMOST DISPLAY CHARACTER

Figure 11. Data Out Timing and Format for the HDSP-8716/-8724/-8732/-8740 Alphanumeric Display System.

Microprocessor Interface

Interfacing the HDSP-87XX Series Display System to microprocessor systems depends on the needs of the particular application. Figure 13 shows a latched interface between the host microprocessor and the HDSP-87XX system. The latch provides temporary storage to avoid making the host microprocessor wait for the system to accept data. Data from the host microprocessor system is loaded into the 74LS273 octal register on the positive transition of the clock input (pin 11). At the same time, the $\overline{\text{CHIP SELECT}}$ input is forced low. The $\overline{\text{CHIP SELECT}}$ input stays low until READY goes low. The host microprocessor should avoid loading new data into the 74LS273 as long as BUSY is high. The latched interface can be implemented with an octal register and $\overline{\text{SR}}$ flip-flop if the HDSP-87XX system is operated in Left, Right, or Block entry. RAM entry requires an additional register for the RAM address inputs. Additional flexibility can be achieved by using a peripheral interface adapter (PIA) to interface the HDSP-87XX system to the host microprocessor system. The PIA provides a data entry handshake between the host microprocessor system and the HDSP-87XX system and allows the host microprocessor system to read the Data Output port of the HDSP-87XX system.

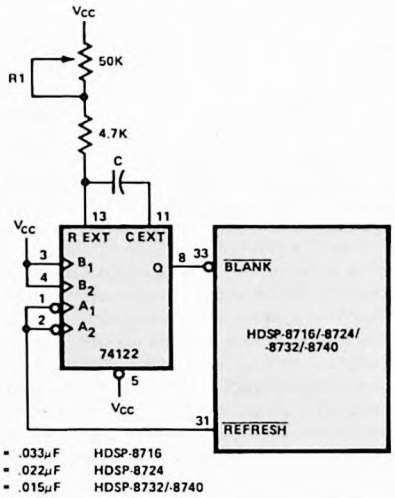
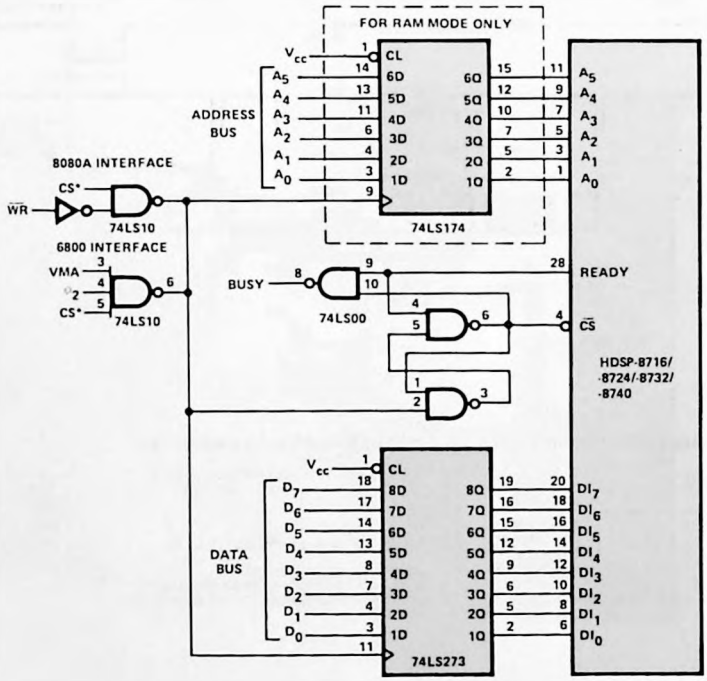


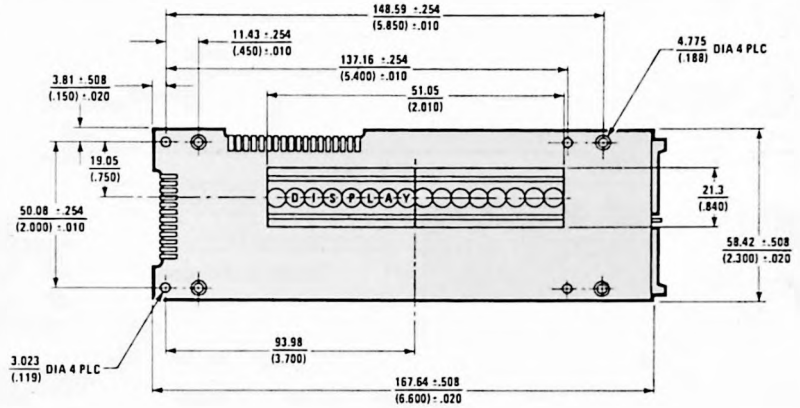
Figure 12. External Circuitry to Vary the Luminous Intensity of the HDSP-8716/-8724/-8732/-8740 Alphanumeric Display System.



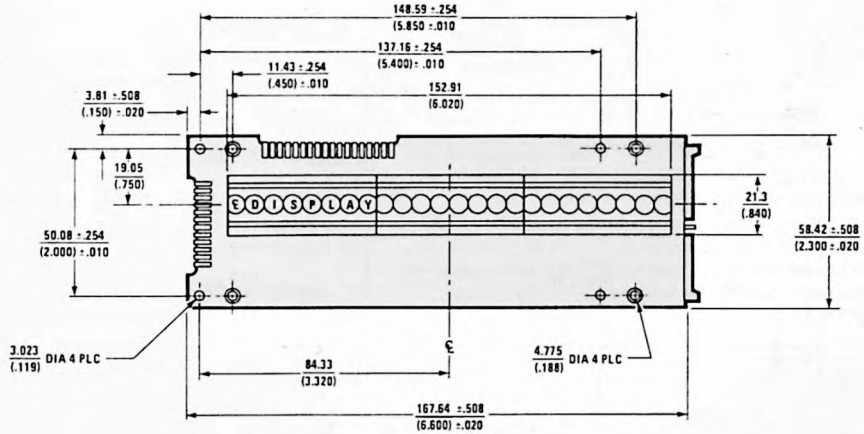
*CS IS A LOGICAL COMBINATION OF HIGH ORDER ADDRESS BITS THAT DISTINGUISH THE ADDRESS OF THE HDSP-8716/-8724/-8732/-8740 FROM THE REST OF THE MICROPROCESSOR SYSTEM.

Figure 13. Latched Interface to the HDSP-87XX Series Alphanumeric Display System.

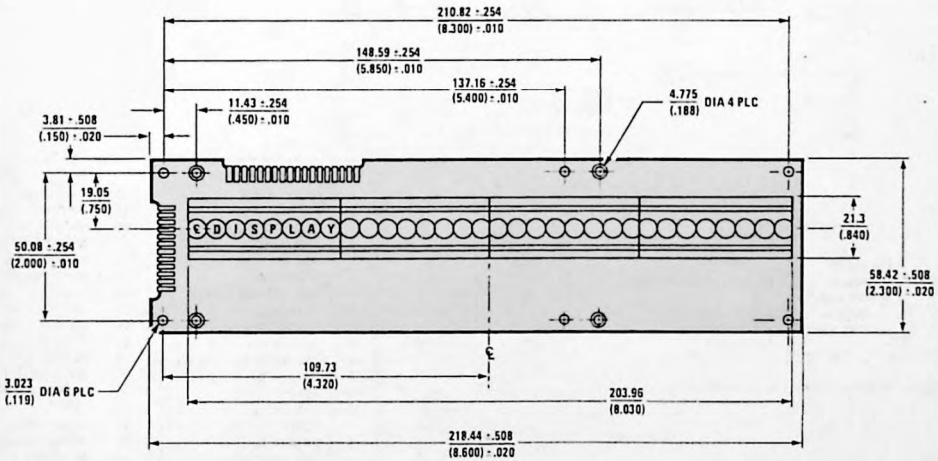
Package Dimensions



HDSP-8716

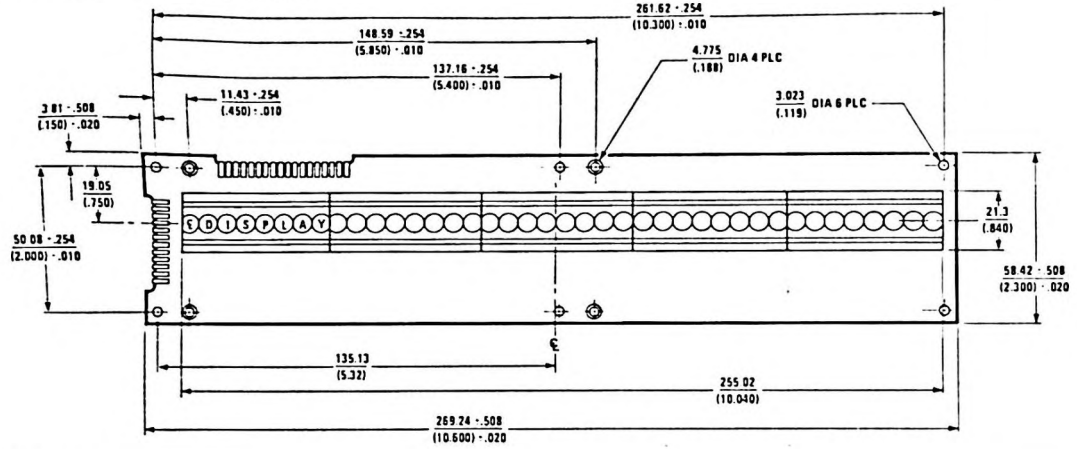


HDSP-8724

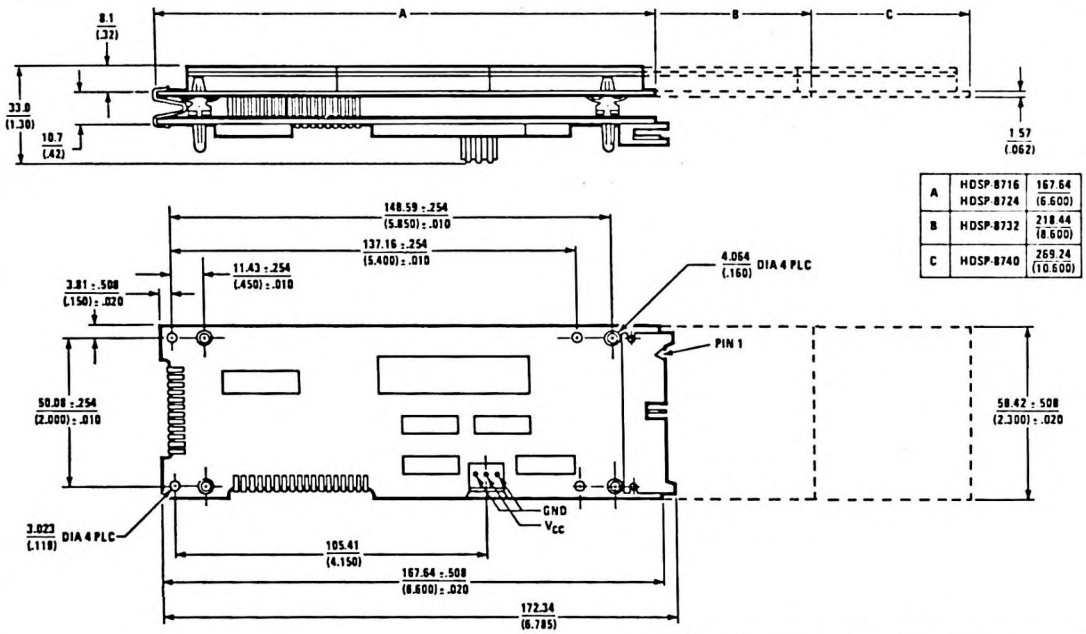


HDSP-8732

Package Dimensions



HDSP-8740

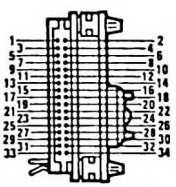


A	HDSP-8716 HDSP-8724	167.64 (6.600)
B	HDSP-8732	218.44 (8.600)
C	HDSP-8740	269.24 (10.600)

CONNECTORS

FUNCTION	TYPE OF CONNECTOR	SUGGESTED MANUFACTURER
CONTROL/DATA ENTRY	34 PIN RIBBON CABLE	3M P/N 3414-X000 SERIES
POWER[1]	3 PIN WITH LOCKING RAMP	MOLEX P/N 09-50-3031 WITH 08-50-0106 TERMINALS

NOTES: (1) POWER LEADS SHOULD BE 18 20 GAUGE STRANDED WIRE.



PIN	DESCRIPTION
1	RAM ADDRESS, A_8
2	$\overline{\text{EXPAND}}$
3	RAM ADDRESS, A_1
4	$\overline{\text{CHIP SELECT}}$
5	RAM ADDRESS, A_2
6	DATA IN, D_8
7	RAM ADDRESS, A_3 (ELI)
8	DATA IN, D_1
9	RAM ADDRESS, A_4 (ERI)
10	DATA IN, D_2
11	RAM ADDRESS, A_5 (LEFT)
12	DATA IN, D_3
13	$\overline{\text{ACTIVE}}$
14	DATA IN, D_4
15	$\overline{\text{RESET}}$
16	DATA IN, D_5
17	NO CONNECTION

PIN	DESCRIPTION
18	DATA IN, D_6
19	NO CONNECTION
20	DATA IN, D_7
21	NO CONNECTION
22	DATA OUT, DO_8
23	DATA OUT, DO_1
24	DATA OUT, DO_2
25	DATA OUT, DO_3
26	DATA OUT, DO_4
27	DATA OUT, DO_5
28	READY
29	DATA VALID
30	400 kHz CLOCK OUT
31	$\overline{\text{REFRESH}}$
32	NO CONNECTION
33	$\overline{\text{DISPLAY BLANK}}$
34	NO CONNECTION

HDSP-8716/-8724/-8732/-8740

HEWLETT PACKARD

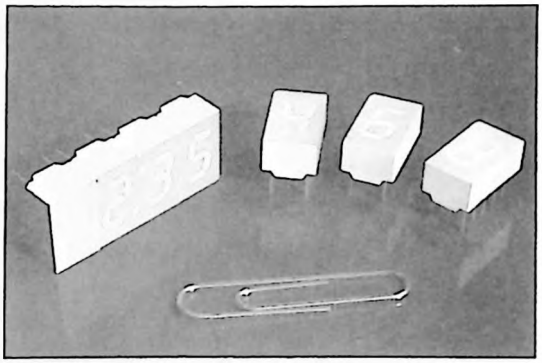
7.6 mm (.3 inch) MICRO BRIGHT 7 SEGMENT DISPLAYS

RED	HDSP-7300
HIGH EFFICIENCY RED	HDSP-7500
YELLOW	HDSP-7400
HIGH PERFORMANCE GREEN	HDSP-7800

TECHNICAL DATA JANUARY 1984

Features

- HIGH BRIGHTNESS
  Package Optimized for High Ambient Conditions
- COMPACT PACKAGE
  0.300 x 0.500 inches
- CHOICE OF FOUR COLORS:
  Red, High Efficiency Red, Yellow,
  High Performance Green
- EXCELLENT CHARACTER APPEARANCE:
  Evenly Lighted Segments
  Mitered Segments
  Wide Viewing Angle
  Grey Package Provides Optimum On-Off Contrast
- EASY MOUNTING ON PC BOARDS OR SOCKETS
  5.08 mm (0.2 inch) DIP Leads on 2.54 mm
  (0.1 inch) Centers
- AVAILABLE WITH COLON FOR CLOCK DISPLAY
- COMMON ANODE OR COMMON CATHODE
  Right Hand Decimal Point
  Overflow ± Character
- CATEGORIZED FOR LUMINOUS INTENSITY;
  YELLOW AND GREEN ALSO CATEGORIZED FOR COLOR
  Use of Like Category Yields a Uniform Display



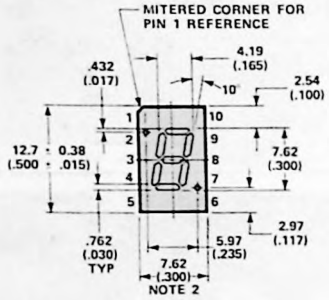
Description

The HDSP-7300/-7500/-7400/-7800 Series are 7.6 mm (0.3 inch) character LED seven segment displays in a compact package. Designed for viewing distances up to 3 metres (10 feet), these displays are ideal for high ambient applications where space is at a premium. Typical applications include instruments, aircraft and marine equipment, point-of-sale terminals, clocks, and appliances.

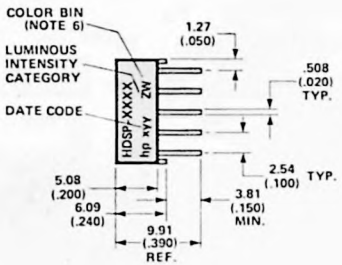
Devices

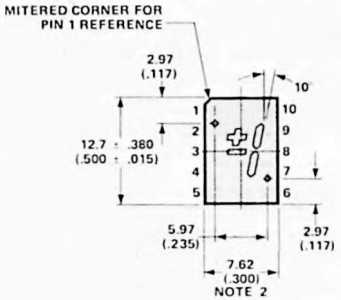
Part Number	Color	Description	Package Drawing
HDSP-7301	Red	Common Anode Right Hand Decimal	A
HDSP-7311	Bright Red	Common Anode Right Hand Decimal	A
HDSP-7302	Red	Common Anode Right Hand Decimal, Colon	B
HDSP-7303	Red	Common Cathode Right Hand Decimal	C
HDSP-7313	Bright Red	Common Cathode Right Hand Decimal	C
HDSP-7304	Red	Common Cathode Right Hand Decimal, Colon	D
HDSP-7307	Red	Overflow ±1 Common Anode	E
HDSP-7317	Bright Red	Overflow ±1 Common Anode	E
HDSP-7308	Red	Overflow ±1 Common Cathode	F
HDSP-7318	Bright Red	Overflow ±1 Common Cathode	F
HDSP-7501	HER	Common Anode Right Hand Decimal	A
HDSP-7502		Common Anode Right Hand Decimal, Colon	B
HDSP-7503		Common Cathode Right Hand Decimal	C
HDSP-7504		Common Cathode Right Hand Decimal, Colon	D
HDSP-7507		Overflow ±1 Common Anode	E
HDSP-7508		Overflow ±1 Common Cathode	F
HDSP-7401	Yellow	Common Anode Right Hand Decimal	A
HDSP-7402		Common Anode Right Hand Decimal, Colon	B
HDSP-7403		Common Cathode Right Hand Decimal	C
HDSP-7404		Common Cathode Right Hand Decimal, Colon	D
HDSP-7407		Overflow ±1 Common Anode	E
HDSP-7408		Overflow ±1 Common Cathode	F
HDSP-7801	Green	Common Anode Right Hand Decimal	A
HDSP-7802		Common Anode Right Hand Decimal, Colon	B
HDSP-7803		Common Cathode Right Hand Decimal	C
HDSP-7804		Common Cathode Right Hand Decimal, Colon	D
HDSP-7807		Overflow ±1 Common Anode	E
HDSP-7808		Overflow ±1 Common Cathode	F

Package Dimensions

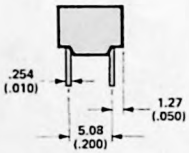


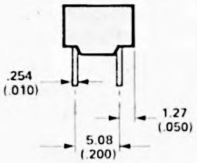
A, B, C, D





E, F

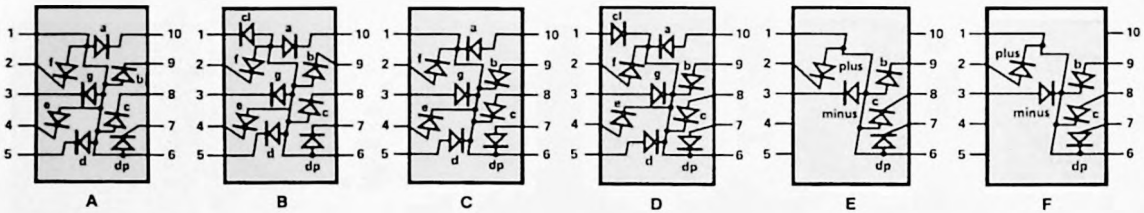




Notes:
1. All dimensions in millimetres (inches).
2. Maximum.
3. All untoleranced dimensions are for reference only.
4. Redundant anodes.
5. Redundant cathodes.
6. For HDSP-7400/-7800 series product only.

	FUNCTION					
PIN	A	B	C	D	E	F
1	ANODE[4]	CATHODE COLON	CATHODE[5]	ANODE COLON	ANODE[4]	CATHODE[5]
2	CATHODE f	CATHODE f	ANODE f	ANODE f	CATHODE PLUS	ANODE PLUS
3	CATHODE g	CATHODE g	ANODE g	ANODE g	CATHODE MINUS	ANODE MINUS
4	CATHODE e	CATHODE e	ANODE e	ANODE e	NC	NC
5	CATHODE d	CATHODE d	ANODE d	ANODE d	NC	NC
6	ANODE[4]	ANODE	CATHODE[5]	CATHODE	ANODE[4]	CATHODE[5]
7	CATHODE DP	CATHODE DP	ANODE DP	ANODE DP	CATHODE DP	ANODE DP
8	CATHODE c	CATHODE c	ANODE c	ANODE c	CATHODE c	ANODE c
9	CATHODE b	CATHODE b	ANODE b	ANODE b	CATHODE b	ANODE b
10	CATHODE a	CATHODE a	ANODE a	ANODE a	NC	NC

Internal Circuit Diagram



Absolute Maximum Ratings

	HDSP-7300/ -7310 Series	HDSP-7500 Series	HDSP-7400 Series	HDSP-7800 Series
Average Power Dissipation per Segment or D.P.	73 mW	105 mW	81 mW	105 mW
Operating Temperature Range	-40°C to +85°C			
Storage Temperature Range	-40°C to +85°C			
Peak Forward Current per Segment or D.P.[7]	150 mA	90 mA	60 mA	90 mA
DC Forward Current per Segment or D.P.[8]	25 mA	30 mA	20 mA	30 mA
Reverse Voltage per Segment or D.P.	3 V	3 V	3 V	3 V
Lead Soldering Temperature 1.59 mm (1/16 inch) below seating plane	260°C for 3 sec.			

7. See Figures 1, 6, 7, and 8 to establish pulsed operating conditions. (Figure 1, HDSP-7300 Series; Figure 6, HDSP-7500 Series; Figure 7, HDSP-7400 Series; Figure 8, HDSP-7800 Series)
8. See Figures 2, 9, 10, and 11 to derate maximum DC current. (Figure 2, HDSP-7300 Series; Figure 9, HDSP-7500 Series; Figure 10, HDSP-7400 Series; Figure 11, HDSP-7800 Series)

Electrical/Optical Characteristics at $T_A = 25°C$

STANDARD RED HDSP-7300 SERIES

Description	Device HDSP-	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity/Segment[9] (Digit Average)	7300	I_V	10 mA DC		450		μcd
			20 mA DC	450	1000		
	7310		10 mA DC		610		
			20 mA DC	610	1355		
Peak Wavelength		λ_{PEAK}			655		nm
Dominant Wavelength[10]		λ_d			640		nm
Forward Voltage, any Segment or D.P.		V_F	$I_F = 20$ mA		1.6	2.0	V
Reverse Voltage, any Segment or D.P.[12]		V_R	$I_R = 100$ μA	3.0	12.0		V
Temperature Coefficient of Forward Voltage		$\Delta V_F/°C$			-2.0		mV/°C
Thermal Resistance LED Junction-to-Pin		$R\theta_{J-PIN}$			200		°C/W/ Seg

HIGH EFFICIENCY RED HDSP-7500 SERIES

Description	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity/Segment[9] (Digit Average)	I_V	5 mA D.C.	275	660		μcd
		20 mA D.C.		3630		
		60 mA Pk: 1 of 6 Duty Factor		2120		
Peak Wavelength	λ_{PEAK}			635		nm
Dominant Wavelength[10]	λ_d			626		nm
Forward Voltage/Segment or D.P.	V_F	$I_F = 5$ mA		1.7		V
		$I_F = 20$ mA		2.0	2.5	
		$I_F = 60$ mA		2.8		
Reverse Voltage/Segment or D.P.[12]	V_R	$I_R = 100$ μA	3.0	30.0		V
Temperature Coefficient of V_F/Segment or D.P.	$\Delta V_F/°C$			—2.0		mV/°C
Thermal Resistance LED Junction-to-Pin	$R\theta_{J-PIN}$			200		°C/W/ Seg

YELLOW HDSP-7400 SERIES

Description	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity/Segment[9] (Digit Average)	I_V	5 mA D.C.	225	480		μcd
		20 mA D.C.		2740		
		60 mA Pk: 1 of 6 Duty Factor		1700		
Peak Wavelength	λ_{PEAK}			583		nm
Dominant Wavelength[10,11]	λ_d		581.5	586	592.5	nm
Forward Voltage/Segment or D.P.	V_F	$I_F = 5$ mA		1.8		V
		$I_F = 20$ mA		2.2	2.5	
		$I_F = 60$ mA		3.1		
Reverse Voltage/Segment or D.P.[12]	V_R	$I_R = 100$ μA	3.0	50.0		V
Temperature Coefficient of V_F/Segment or D.P.	$\Delta V_F/°C$			—2.0		mV/°C
Thermal Resistance LED Junction-to-Pin	$R\theta_{J-PIN}$			200		°C/W/ Seg

9. The digits are categorized for luminous intensity with the intensity category designated by a letter on the right hand side of the package. The luminous intensity minimum and categories are determined by computing the numerical average of the individual segment intensities, decimal point not included.
10. The dominant wavelength is derived from the C.I.E. Chromaticity diagram and is that single wavelength which defines the color of the device.
11. The HDSP-7400/-7800 series are categorized as to dominant wavelength with the category designated by a number adjacent to the intensity category letter.
12. Typical specification for reference only. Do not exceed absolute maximum ratings.

HIGH PERFORMANCE GREEN HDSP-7800 SERIES

Description	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity/Segment[9] (Digit Average)	I_V	5 mA D.C.		480		μcd
		10 mA D.C.	570	1300		
		60 mA Pk: 1 of 6 Duty Factor		1700		
Peak Wavelength	λ_{PEAK}			566		nm
Dominant Wavelength[10, 11] (Digit Average)	λ_d			571	577	nm
Forward Voltage/Segment or D.P.	V_F	I_F = 10 mA		2.1	2.5	V
Reverse Voltage/Segment or D.P.[12]	V_R	I_R = 100 μA	3.0	50.0		V
Thermal Resistance LED Junction-to-Pin	$R\theta_{J\text{-}PIN}$			200		°C/W/ Seg

HDSP-7300 SERIES

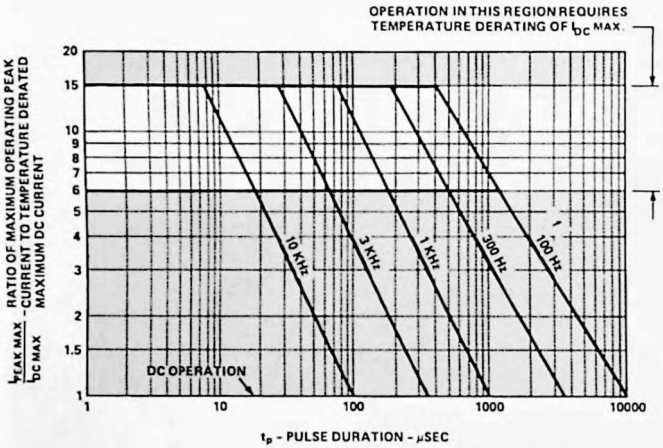


Figure 1. Maximum Tolerable Peak Current vs. Pulse Duration

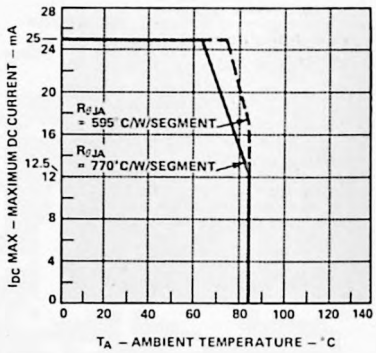


Figure 2. Maximum Allowable DC Current Dissipation per Segment as a Function of Ambient Temperature

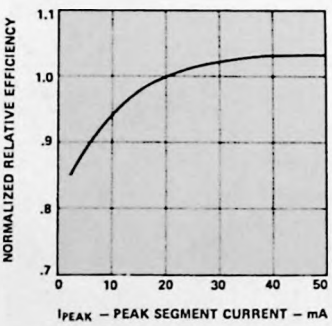


Figure 3. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current per Segment

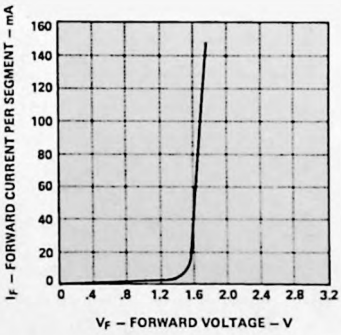


Figure 4. Forward Current vs. Forward Voltage

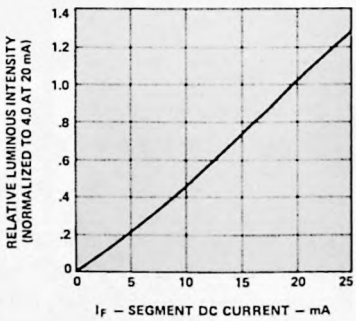


Figure 5. Relative Luminous Intensity vs. DC Forward Current

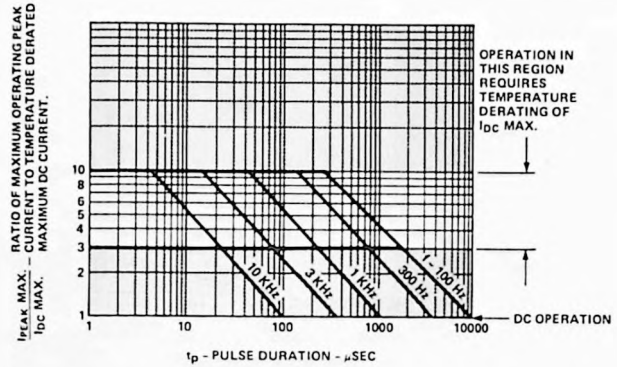


Figure 6. Maximum Tolerable Peak Current vs. Pulse Duration — HDSP-7500 Series

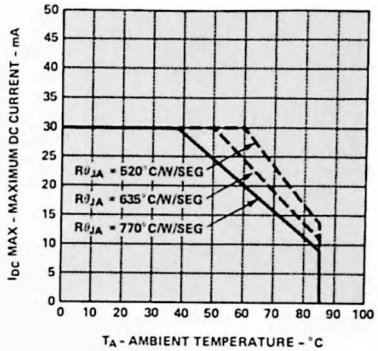


Figure 9. Maximum Allowable DC Current and DC Power Dissipation per Segment as a Function of Ambient Temperature — HDSP-7500 Series

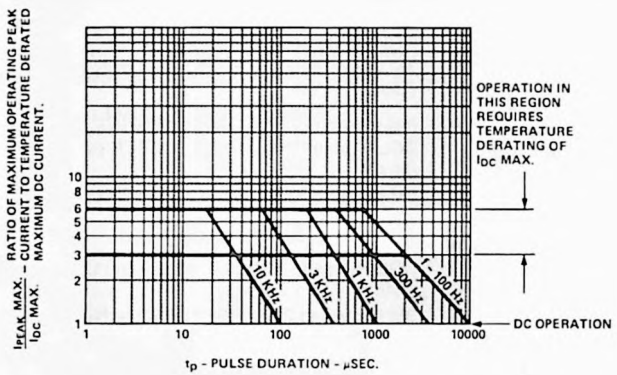


Figure 7. Maximum Tolerable Peak Current vs. Pulse Duration — HDSP-7400 Series

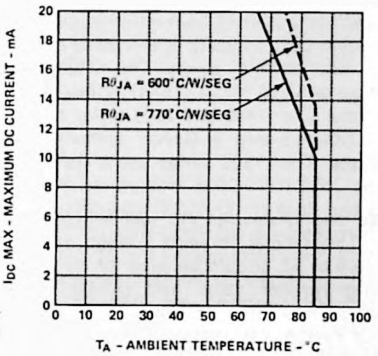


Figure 10. Maximum Allowable DC Current and DC Power Dissipation per Segment as a Function of Ambient Temperature — HDSP-7800 Series

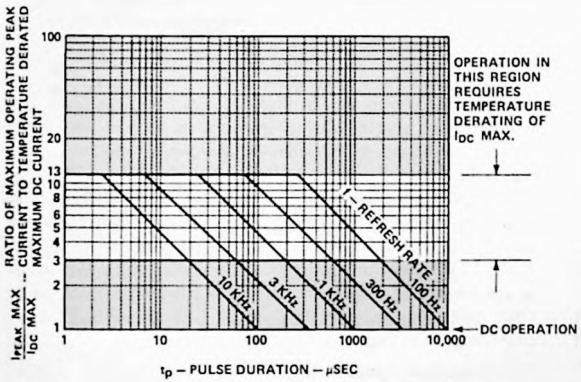


Figure 8. Allowed Peak Current vs. Pulse Duration — HDSP-7800 Series

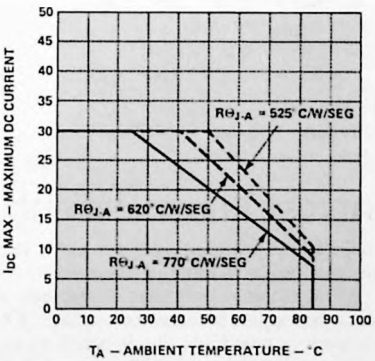


Figure 11. Maximum Allowable DC Current per Segment vs. Ambient Temperature — HDSP-7400 Series

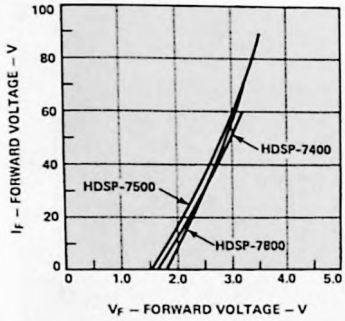


Figure 12. Relative Luminous Efficiency (Luminous Intensity per Unit Current) vs. Peak Segment Current

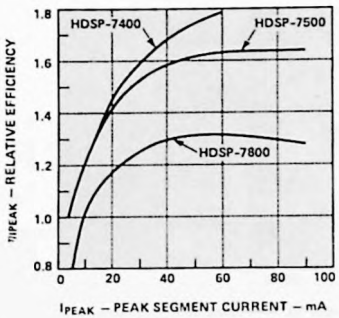


Figure 13. Forward Current vs. Forward Voltage Characteristics

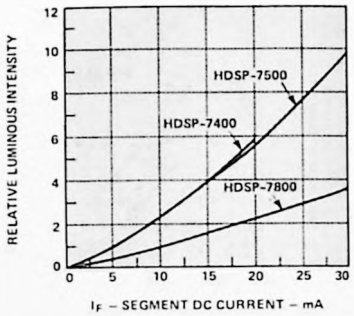


Figure 14. Relative Luminous Intensity vs. DC Forward Current

Electrical

The HDSP-7300/-7400/-7500/-7800 series of display devices are composed of light emitting diodes, with the light from each LED optically stretched to form individual segments and decimal points. The -7300 series uses a p-n junction diffused into a GaAsP epitaxial layer on a GaAs substrate. The -7400 and-7500 series have their p-n junctions diffused into a GaAsP epitaxial layer on a GaP substrate. The -7800 series use a GaP epitaxial layer on GaP.

These display devices are well suited for strobed operation. The typical forward voltage values, scaled from Figure 4 or 13, should be used for calculating the current limiting resistor value and typical power dissipation. Expected maximum V_F values, for the purpose of driver circuit design and maximum power dissipation, may be calculated using the following V_F MAX models:

HDSP-7300 Series:

V_F MAX = 1.85 V + I_{PEAK} (7Ω)
For: $I_{PEAK} \geq 5$ mA

HDSP-7400/-7500 Series:

V_F MAX = 1.75 V + I_{PEAK} (38Ω)
For: $I_{PEAK} \geq 20$ mA
V_F MAX = 1.6 V + I_{DC} (45Ω)
For: 5 mA ≤ I_{DC} ≤ 20 mA

HDSP-7800 Series:

V_F MAX = 2.0 V + I_{PEAK} (50Ω)
For: $I_{PEAK} \geq 5$ mA

Contrast Enhancement

The objective of contrast enhancement is to provide good display readability in the end use ambient light. The concept is to employ both luminance and chrominance contrast techniques to enhance readability by having the OFF-segments blend into the display background and the ON-segments stand out vividly against this same background. Therefore, these display devices are assembled with a gray package and matching encapsulating epoxy in the segments.

Contrast enhancement may be achieved by using one of the following suggested filters:

HDSP-7300: Panelgraphic RUBY RED 60
SGL Homalite H100-1605 RED
3M Louvered Filter R6610 RED or N0210 GRAY

HDSP-7400: Panelgraphic YELLOW 27 or GRAY 10
SGL Homalite H100-1720 AMBER or -1266 GRAY
3M Louvered Filter A5910 AMBER or N0210 GRAY

HDSP-7500: Panelgraphic SCARLET RED 65 or GRAY 10
SGL Homalite H100-1670 RED or -1266 GRAY
3M Louvered Filter R6310 RED or N0210 GRAY

HDSP-7800: Panelgraphic GREEN 48
SGL Homalite H100-1440 GREEN
3M Louvered Filter G5610 GREEN or N0210 GRAY

Mechanical

To optimize device optical performance, specially developed plastics are used which restrict the solvents that may be used for cleaning. It is recommended that only mixtures of Freon (F113) and alcohol be used for vapor cleaning processes. with an immersion time in the vapors of less than two (2) minutes maximum. Some suggested vapor cleaning solvents are Freon TE, Genesolve DI-15 or DE-15, Arklone A or K. A 60°C (140°F) water cleaning process may also be used, which includes a neutralizer rinse (3% ammonia solution or equivalent), a surfactant rinse (1% detergent solution or equivalent), a hot water rinse and a thorough air dry. Room temperature cleaning may be accomplished with Freon T-E35 or T-P35, Ethanol, Isopropanol or water with a mild detergent.

Such cleaning agents from the ketone family (acetone, methyl ethyl ketone, etc.) and from the chlorinated hydrocarbon family (methylene chloride, trichloroethylene, carbon tetrachloride, etc.) are not recommended for cleaning LED parts. All of these various solvents attack or dissolve the encapsulating epoxies used to form the packages of plastic LED devices.

HEWLETT PACKARD

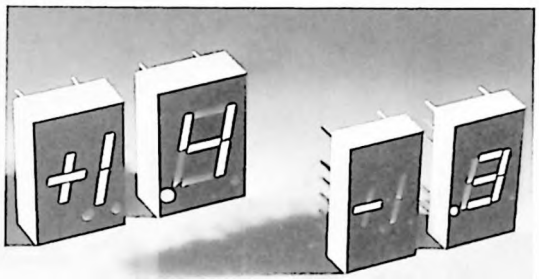
7.6/10.9mm (0.3/0.43 INCH) RED SEVEN SEGMENT DISPLAYS

5082-7730 SERIES
5082-7740
5082-7750 SERIES
5082-7760

TECHNICAL DATA JANUARY 1984

Features

- EXCELLENT CHARACTER APPEARANCE
  - Continuous Uniform Segments
  - Wide Viewing Angle
  - High Contrast
- IC COMPATIBLE
  - 1.6V dc per Segment
- STANDARD 0.3" DIP LEAD CONFIGURATION
  - PC Board or Standard Socket Mountable
- CATEGORIZED FOR LUMINOUS INTENSITY
  - Assures Uniformity of Light Output from Unit to Unit within a Single Category
- MECHANICALLY RUGGED



Description

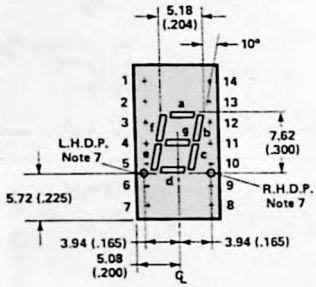
The 5082-7730/7740 series and 5082-7750/7760 series displays are 7.62/10.92 mm (0.3/0.43 in) high red LED displays. The 7730/7740 series devices are designed for viewing distances of up to three meters and the 7750/7760 series devices are designed for viewing distances of up to six meters. These displays are designed for use in instruments, point of sale terminals, clocks and appliances. These devices use LED die made with GaAsP on a GaAs substrate.

Devices

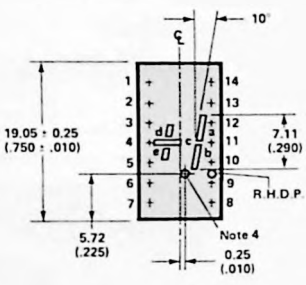
Part No. 5082-	Description	Package Drawing
7730	7.6 mm Common Anode Left Hand Decimal	A
7731	7.6 mm Common Anode Right Hand Decimal	B
7736	7.6 mm Universal Overflow ±1 Right Hand Decimal	C
7740	7.6 mm Common Cathode Right Hand Decimal	D
7750	10.9 mm Common Anode Left Hand Decimal	E
7751	10.9 mm Common Anode Right Hand Decimal	F
7756	10.9 mm Universal Overflow ±1 Right Hand Decimal	G
7760	10.9 mm Common Cathode Right Hand Decimal	H

Note: Universal pinout brings the anode and cathode of each segment's LED out to separate pins. See internal diagram C, G.

Package Dimensions 5082-7730/-7731/-7736/-7740

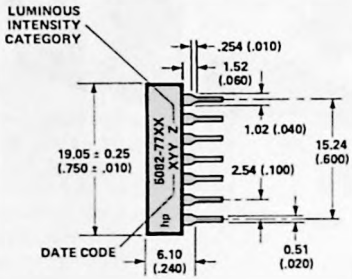


A,B,D

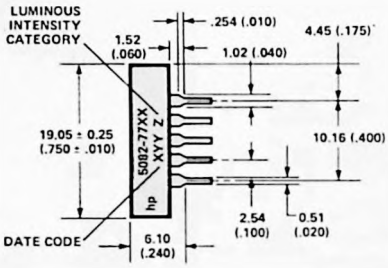


C

PIN	FUNCTION A -7730	B -7731	C -7736	D -7740
1	CATHODE-a	CATHODE-a	ANODE-d	NO PIN
2	CATHODE-f	CATHODE-f	NO PIN	CATHODE [6]
3	ANODE[3]	ANODE[3]	CATHODE-d	ANODE-f
4	NO PIN	NO PIN	CATHODE-c	ANODE-g
5	NO PIN	NO PIN	CATHODE-e	ANODE-e
6	CATHODE-dp	NO CONN.[5]	ANODE-e	ANODE-d
7	CATHODE-e	CATHODE-e	ANODE-c	NO PIN
8	CATHODE-d	CATHODE-d	ANODE-dp	NO PIN
9	NO CONN.[5]	CATHODE-dp	NO PIN	CATHODE [6]
10	CATHODE-c	CATHODE-c	CATHODE-dp	ANODE-dp
11	CATHODE-g	CATHODE-g	CATHODE-b	ANODE-c
12	NO PIN	NO PIN	CATHODE-a	ANODE-b
13	CATHODE-b	CATHODE-b	ANODE-a	ANODE-a
14	ANODE[3]	ANODE[3]	ANODE-b	NO PIN

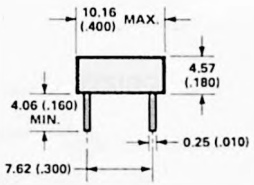


A,B,C



D

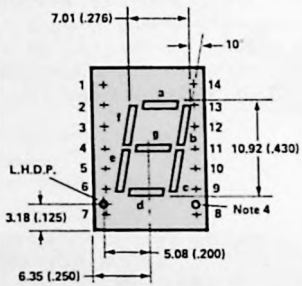
SIDE



A,B,C,D

END

5082-7750/-7751/-7756/-7760



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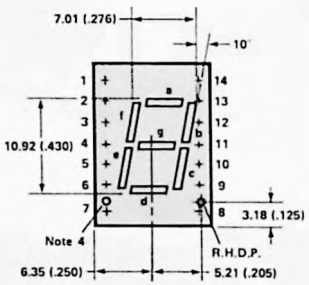
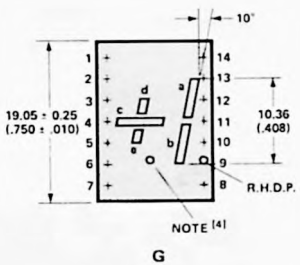


F,H

FRONT VIEW



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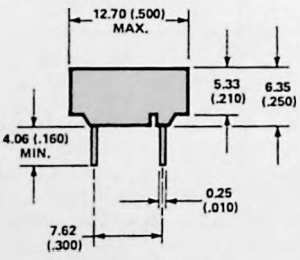
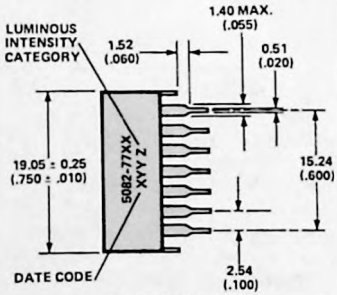


END VIEW



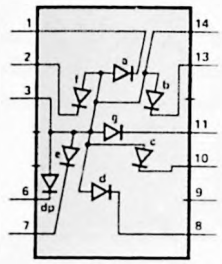
SIDE VIEW

PIN	FUNCTION E -7750	F -7751	G -7756	H -7760
1	CATHODE-a	CATHODE-a	CATHODE-d	ANODE-a
2	CATHODE f	CATHODE-f	ANODE-d	ANODE-f
3	ANODE[3]	ANODE[3]	NO PIN	CATHODE[6]
4	NO PIN	NO PIN	CATHODE-c	NO PIN
5	NO PIN	NO PIN	CATHODE-e	NO PIN
6	CATHODE-dp	NO CONN.[5]	ANODE-e	NO CONN.[5]
7	CATHODE-e	CATHODE-e	ANODE-c	ANODE-e
8	CATHODE-d	CATHODE-d	ANODE-dp	ANODE-d
9	NO CONN.[5]	CATHODE-dp	CATHODE-dp	ANODE-dp
10	CATHODE-c	CATHODE-c	CATHODE-b	ANODE-c
11	CATHODE-g	CATHODE-g	CATHODE-a	ANODE-g
12	NO PIN	NO PIN	NO PIN	NO PIN
13	CATHODE-b	CATHODE-b	ANODE-a	ANODE-b
14	ANODE[3]	ANODE[3]	ANODE-b	CATHODE[6]

NOTES:

1. Dimensions in millimeters and (inches).
2. All untoleranced dimensions are for reference only
3. Redundant anodes.
4. Unused dp position.
5. See Internal Circuit Diagram.
6. Redundant cathode.
7. See part number table for L.H.D.P. and R.H.D.P. designation.

Internal Circuit Diagram



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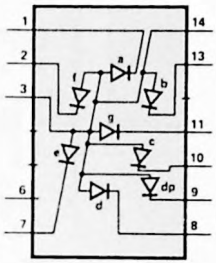

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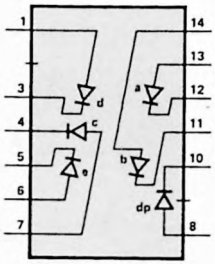

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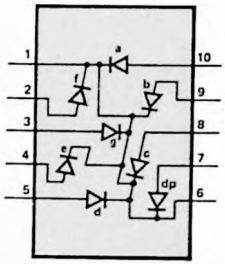

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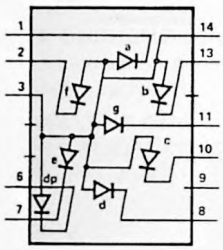

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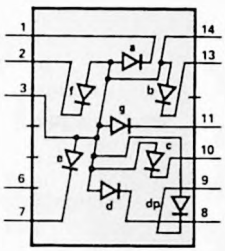

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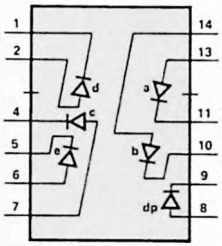

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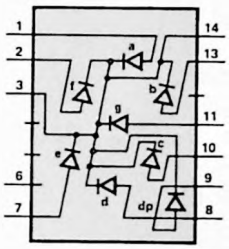


H

Absolute Maximum Ratings

Average Power Dissipation Per Segment or D.P.[1] (T_A=50°C) 65mW
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -40°C to +85°C
Peak Forward Current Per Segment or D.P.[3] (T_A=50°C) 150mA
Average Forward Current Per Segment or D.P.[1,2] (T_A=50°C) 25mA
Reverse Voltage Per Segment or D.P. 3.0V
Lead Soldering Temperature ..... 260°C for 3 Sec
[1.59mm (1/16 inch) below seating plane[4]]

Notes: 1. See power derating curve (Fig.2). 2. Derate DC current from 50°C at 0.43mA/°C per segment. 3. See Fig. 1 to establish pulsed operating conditions. 4. Clean only in water, isopropanol, ethanol, Freon TF or TE (or equivalent) and Genesolv DI-15 or DE-15 (or equivalent).

Electrical/Optical Characteristics at T_A=25°C

Description	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment [2] (Digit Average)	I_V	I_{PEAK} = 100mA 10% Duty Cycle		610		µcd
		I_F = 20mA	240	700		
Peak Wavelength	λ_{PEAK}			655		nm
Dominant Wavelength [2]	λ_d			640		nm
Forward Voltage, any Segment or D.P.[4]	V_F	I_F = 20mA		1.6	2.0	V
Reverse Voltage, any Segment or D.P.[4] [5]	V_R	I_R = 100 µA	3.0	20.0		V
Rise and Fall Time [3]	t_r, t_f			10		ns
Temperature Coefficient of Forward Voltage	ΔV_F/°C			−2.0		mV/°C
Thermal Resistance LED Junction-to-Pin	$R\theta_{J-PIN}$			282		°C/W/ Seg

Notes:
1. The digits are categorized for luminous intensity with the intensity category designated by a letter located on the right hand side of the package.
2. The dominant wavelength, λ_d, is derived from the CIE Chromaticity Diagram and is that single wavelength which defines the color of the device.
3. Time for a 10% - 90% change of light intensity for step change in current.
4. Quality level for electrical characteristics is 1000 parts per million.
5. Typical specification for reference only. Do not exceed absolute maximum ratings.

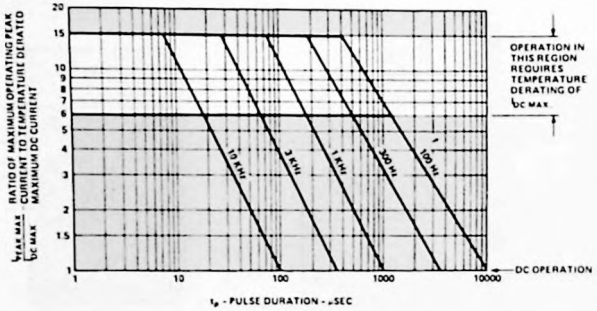


Figure 1. Maximum Tolerable Peak Current vs. Pulse Duration.

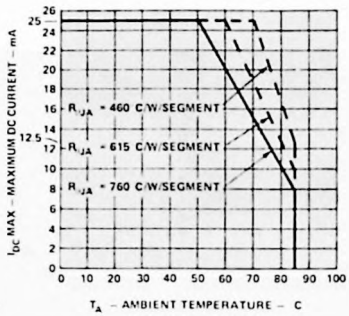


Figure 2. Maximum Allowable DC Current Dissipation per Segment as a Function of Ambient Temperature.

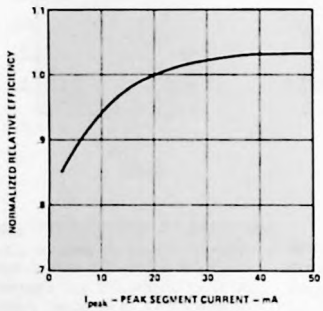


Figure 3. Relative Efficiency (Luminous Intensity per Unit Current) versus Peak Current per Segment.

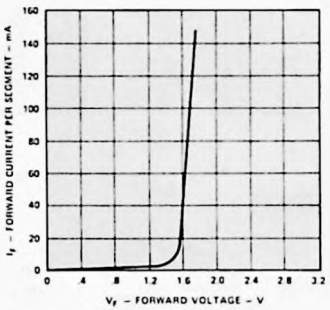


Figure 4. Forward Current vs. Forward Voltage.

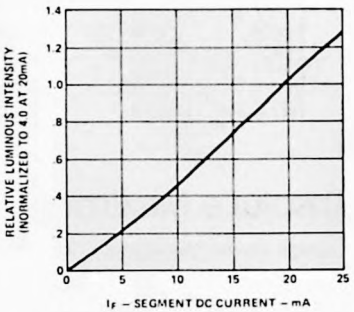


Figure 5. Relative Luminous Intensity vs. DC Forward Current

For a Detailed Explanation on the Use of Data Sheet Information and Recommended Soldering Procedures, See Application Note 1005.

ELECTRICAL 5082-77XX

The 5082-77XX series of display devices are composed of eight light emitting diodes, with the light from each LED optically stretched to form individual segments and a decimal point. The LEDs have the P-N junction diffused into a GaAsP epitaxial layer on a GaAs substrate.

These display devices are designed for strobed operation at high peak currents. The typical forward voltage values, scaled from Figure 4, should be used for calculating the current limiting resistor values and typical power dissipation. Expected maximum V_F values for the purpose of driver circuit design may be calculated using the following V_F model:

$V_F = 1.55V + I_{PEAK}\ (7\Omega)$
For $5mA \leq I_{PEAK} \leq 150mA$

CONTRAST ENHANCEMENT

The 5082-77XX series display may be effectively filtered using one of the following filter products: Homalite H100-1605: H 100-1804 (purple); Panelgraphic Ruby Red 60: Dark Red 63: Purple 90; Plexiglas 2423; 3M Brand Light Control Film for daylight viewing.

HEWLETT PACKARD

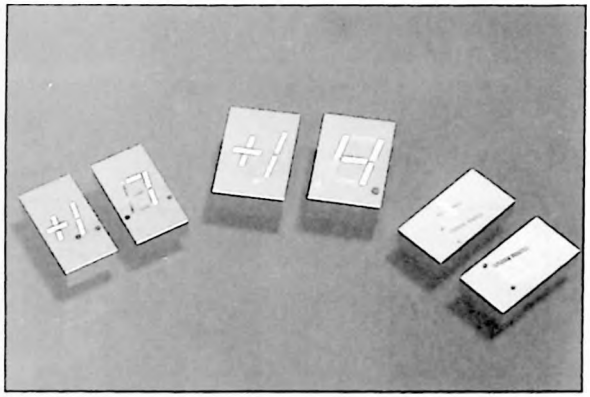
7.6/10.9 mm (0.3/0.43 INCH) SEVEN SEGMENT DISPLAYS

HIGH EFFICIENCY RED • 5082-7610/-7650 SERIES
YELLOW • 5082-7620/-7660 SERIES
HIGH PERFORMANCE GREEN • HDSP-3600/-4600 SERIES

TECHNICAL DATA JANUARY 1984

Features

- COMPACT SIZE
- CHOICE OF 3 BRIGHT COLORS
  - High Efficiency Red
  - Yellow
  - High Performance Green
- LOW CURRENT OPERATION
  - As Low as 3mA per Segment
  - Designed for Multiplex Operation
- EXCELLENT CHARACTER APPEARANCE
  - Evenly Lighted Segments
  - Wide Viewing Angle
  - Body Color Improves "Off" Segment Contrast
- EASY MOUNTING ON PC BOARD OR SOCKETS
  - Industry Standard 7.62mm (0.3 in.) DIP Leads on 2.54mm (0.1 in.) Centers
- CATEGORIZED FOR LUMINOUS INTENSITY; YELLOW CATEGORIZED FOR COLOR
  - Use of Like Categories Yields a Uniform Display
- IC COMPATIBLE
- MECHANICALLY RUGGED



Description

The -7610/-7620/-3600 and -7650/-7660/-4600 series are 7.62/1092 mm (0.3/0.43 in.) high efficiency red, yellow, and green displays. The -7610/-7620/-3600 series displays are designed for viewing distances of up to three metres and the -7650/-7660 -4600 series displays are designed for viewing distances of up to six metres. These displays are designed for use in instruments, point of sale terminals, clocks and appliances.

Devices

Part Number	Color	Description	Package Drawing
5082-7610	High Efficiency Red	7.6 mm Common Anode Left Hand Decimal	A
5082-7611		7.6 mm Common Anode Right Hand Decimal	B
5082-7613		7.6 mm Common Cathode Right Hand Decimal	C
5082-7616		7.6 mm Universal Overflow ±1 Right Hand Decimal	D
5082-7620	Yellow	7.6 mm Common Anode Left Hand Decimal	A
5082-7621		7.6 mm Common Anode Right Hand Decimal	B
5082-7623		7.6 mm Common Cathode Right Hand Decimal	C
5082-7626		7.6 mm Universal Overflow ±1 Right Hand Decimal	D
HDSP-3600	High Performance Green	7.6 mm Common Anode Left Hand Decimal	A
HDSP-3601		7.6 mm Common Anode Right Hand Decimal	B
HDSP-3603		7.6 mm Common Cathode Right Hand Decimal	C
HDSP-3606		7.6 mm Universal Overflow ±1 Right Hand Decimal	D

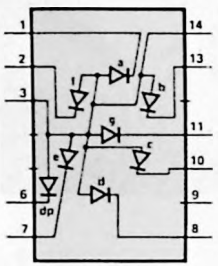
NOTE: Universal pinout brings the anode and cathode of each segment's LED out to separate pins. See internal diagram D.

Devices

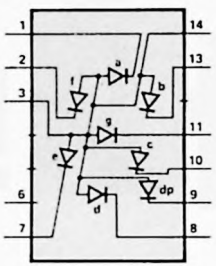
Part Number	Color	Description	Package Drawing
5082-7650	High Efficiency Red	10.9 mm Common Anode Left Hand Decimal	E
5082-7651		10.9 mm Common Anode Right Hand Decimal	F
5082-7653		10.9 mm Common Cathode Right Hand Decimal	G
5082-7656		10.9 mm Universal Overflow ±1 Right Hand Decimal	H
5082-7660	Yellow	10.9 mm Common Anode Left Hand Decimal	E
5082-7661		10.9 mm Common Anode Right Hand Decimal	F
5082-7663		10.9 mm Common Cathode Right Hand Decimal	G
5082-7666		10.9 mm Universal Overflow ±1 Right Hand Decimal	H
HDSP-3600	High Performance Green	10.9 mm Common Anode Left Hand Decimal	E
HDSP-3601		10.9 mm Common Anode Right Hand Decimal	F
HDSP-3603		10.9 mm Common Cathode Right Hand Decimal	G
HDSP-3606		10.9 mm Universal Overflow ±1 Right Hand Decimal	H

NOTE: Universal pinout brings the anode and the cathode of each segment's LED out to separate pins, see internal diagram H.

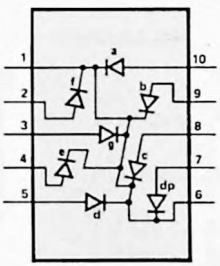
Internal Circuit Diagram



A



B



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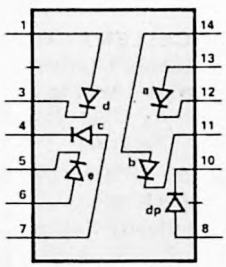

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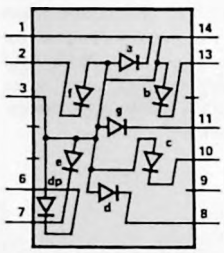

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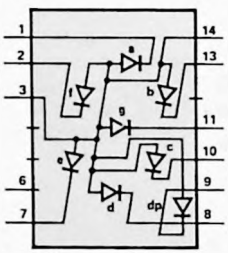

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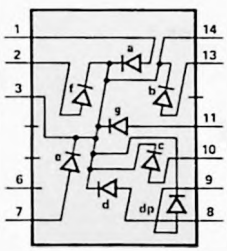

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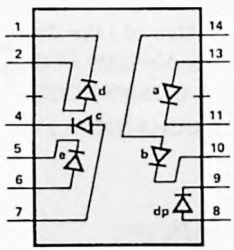


H

Absolute Maximum Ratings

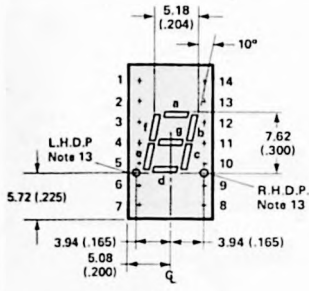
	-7610/-7650 Series	-7620/-7660 Series	-3600/-4600 Series
Average Power Dissipation per Segment or DP	105 mW[1]	81 mW[2]	105 mW[3]
Operating Temperature Range	−40° C to +85° C	−40° C to +85° C	−40° C to +85° C
Storage Temperature Range	−40° C to +85° C	−40° C to +85° C	−40° C to +85° C
Peak Forward Current per Segment or DP	90 mA[4]	60 mA[5]	90 mA[6]
DC Forward Current per Segment or DP	30 mA[1]	20 mA[2]	30 mA[3]
Reverse Voltage per Segment or DP	3.0 V	3.0 V	3.0 V
Lead Soldering Temperature 1.59 mm (1/16 in.) below seating plane	260° C for 3 sec.	260° C for 3 sec.	260° C for 3 sec.

1.59 mm (1/16 inch) below seating plane

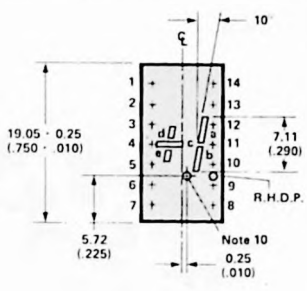
Notes:

1. See power derating curve (Figure 4).
2. See power derating curve (Figure 5).
3. See power derating curve (Figure 6).
4. See Figure 1 to establish pulsed operating conditions.
5. See Figure 2 to establish pulsed operating conditions.
6. See Figure 3 to establish pulsed operating conditions.

Package Dimensions (5082-7610/-7620)

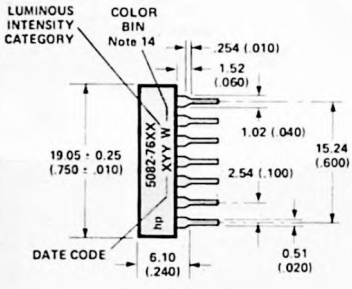


A,B,C

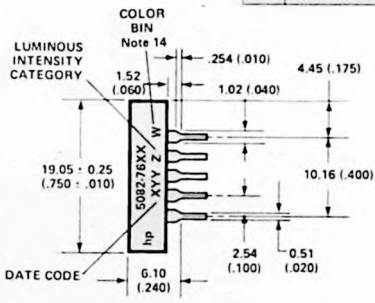


D

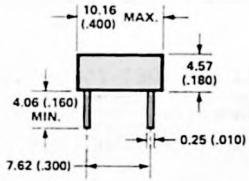
PIN	FUNCTION A -7610/-7620/-3600	B -7611/-7621/-3601	C -7613/-7623/-3603	D -7616/-7626/-3606
1	CATHODE-a	CATHODE-a	NO PIN	ANODE-d
2	CATHODE-f	CATHODE-f	CATHODE[12]	NO PIN
3	ANODE[9]	ANODE[9]	ANODE-f	CATHODE-d
4	NO PIN	NO PIN	ANODE-g	CATHODE-c
5	NO PIN	NO PIN	ANODE-e	CATHODE-e
6	CATHODE-dp	NO CONN.[11]	ANODE-d	ANODE-e
7	CATHODE-e	CATHODE-e	NO PIN	ANODE-c
8	CATHODE-d	CATHODE-d	NO PIN	ANODE-dp
9	NO CONN.[11]	CATHODE-dp	CATHODE[12]	NO PIN
10	CATHODE-c	CATHODE-c	ANODE-dp	CATHODE-dp
11	CATHODE-g	CATHODE-g	ANODE-c	CATHODE-b
12	NO PIN	NO PIN	ANODE-b	CATHODE-a
13	CATHODE-b	CATHODE-b	ANODE-a	ANODE-a
14	ANODE[9]	ANODE[9]	NO PIN	ANODE-b



A,B,D
SIDE

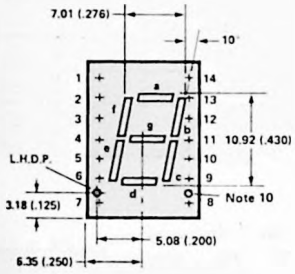


C
SIDE



A,B,C,D
END

(5082-7650/-7660)



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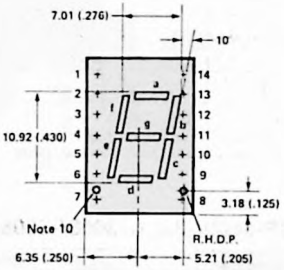
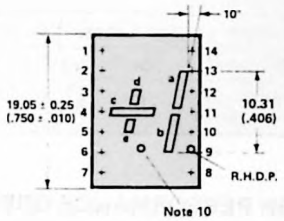


F,G
FRONT VIEW



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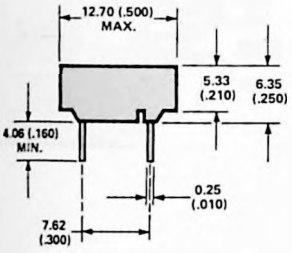
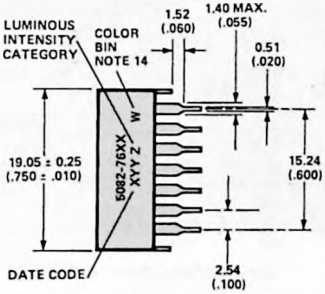


END VIEW



SIDE VIEW

PIN	FUNCTION E -7650/-7660/-4600	F -7651/-7661/-4601	G -7653/-7663/-4603	H -7656/-7666/-4606
1	CATHODE-a	CATHODE-a	ANODE-a	CATHODE-d
2	CATHODE-f	CATHODE-f	ANODE-f	ANODE-d
3	ANODE[9]	ANODE[9]	CATHODE[10]	NO PIN
4	NO PIN	NO PIN	NO PIN	CATHODE-c
5	NO PIN	NO PIN	NO PIN	CATHODE-e
6	CATHODE-dp	NO CONN.[11]	NO CONN.[11]	ANODE-e
7	CATHODE-e	CATHODE-e	ANODE-e	ANODE-c
8	CATHODE-d	CATHODE-d	ANODE-d	ANODE-dp
9	NO CONN.[11]	CATHODE-dp	ANODE-dp	CATHODE-dp
10	CATHODE-c	CATHODE-c	ANODE-c	CATHODE-b
11	CATHODE-g	CATHODE-g	ANODE-g	CATHODE-a
12	NO PIN	NO PIN	NO PIN	NO PIN
13	CATHODE-b	CATHODE-b	ANODE-b	ANODE-a
14	ANODE[9]	ANODE[9]	CATHODE[10]	ANODE-b

NOTES:
7. Dimensions in millimetres and (inches).
8. All untoleranced dimensions are for reference only.
9. Redundant anodes.
10. Unused dp position.
11. See Internal Circuit Diagram.
12. Redundant cathode.
13. See part number table for L.H.D.P. and R.H.D.P. designation.
14. For yellow and green devices only.

Electrical/Optical Characteristics at T_A=25°C

HIGH EFFICIENCY RED 5082-7610/-7611/-7613/-7616/-7650/-7651/-7653/-7656

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment[15]	I_v	5mA D.C.	200	550		µcd
		20mA D.C.		3025		µcd
(Digit Average)		60mA Pk: 1 of 6 Duty Factor		1765		µcd
Peak Wavelength	λ_{PEAK}			635		nm
Dominant Wavelength[16]	λ_d			626		nm
Forward Voltage/Segment or D.P.[18]	V_F	I_F = 5mA		1.7		V
		I_F = 20mA		2.0	2.5	
		I_F = 60mA		2.8		
Reverse Voltage/Segment or D.P.[18, 19]	V_R	I_R = 100 µA	3.0	30.0		V
Temperature Coefficient of V_F/Segment or D.P.	ΔV_F/°C			−2.0		mV/°C
Thermal Resistance LED Junction-to-Pin	$R\theta_{J-PIN}$			282		°C/W/ Seg

YELLOW 5082-7620/-7621/-7623/-7626/-7660/-7661/-7663/-7666

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment[15]	I_v	5mA D.C.	160	400		µcd
		20mA D.C.		2280		µcd
(Digit Average)		60mA Pk: 1 of 6 Duty Factor		1440		µcd
Peak Wavelength	λ_{PEAK}			583		nm
Dominant Wavelength[16, 17]	λ_d		581.5	586	592.5	nm
Forward Voltage/Segment or D.P.[18]	V_f	I_f = 5mA		1.8		V
		I_f = 20mA		2.2	2.5	
		I_f = 60mA		3.1		
Reverse Voltage Segment or D.P.[18, 19]	V_R	I_R = 100 µA	3.0	50.0		V
Temperature Coefficient of V_f/Segment or D.P.	V_f/°C			−2.0		mV/°C
Thermal Resistance LED Junction-to-Pin	$R\theta_{J-PIN}$			282		°C/W/ Seg

HIGH PERFORMANCE GREEN HDSP-3600/-3601/-3603/-3606/-4600/-4601/-4603/-4606

Parameter	Device HDSP-	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/ Segment[15] (Digit Average)	3600 Series	I_V	10 mA DC	400	1100		µcd
			60 mA Pk 1:6 Duty Factor		1440		
	4600 Series		10 mA DC	460	1300		µcd
			60 mA Pk 1:6 Duty Factor		1700		

HIGH PERFORMANCE GREEN HDSP-3600/-3601/-3603/-3606/-4600/-4601/-4603/-4606 (continued)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Peak Wavelength	λ_{PEAK}			566		nm
Dominant Wavelength[16, 17] (Digit Average)	λ_d			571	577	nm
Forward Voltage/Seg. or D.P.[18]	V_F	$I_F = 10$ mA		2.1	2.5	V
Reverse Voltage/Seg. or D.P.[18, 19]	V_R	$I_R = 100\ \mu A$	3.0	50.0		V
Thermal Resistance LED Junction-to-pin	$R\theta_{J-PIN}$			285		°C/W/Seg

NOTES:
15. The digits are categorized for luminous intensity with the intensity category designated by a letter located on the right hand side of the package.
16. The dominant wavelength, λ_d, is derived from the C.I.E. Chromaticity Diagram and is that single wavelength which defines the color of the device.
17. The displays are categorized as to dominant wavelength with the category designated by a number adjacent to the intensity category letter.
18. Quality level for electrical characteristics is 1000 parts per million.
19. Typical specification is for reference only. Do not exceed absolute maximum ratings.

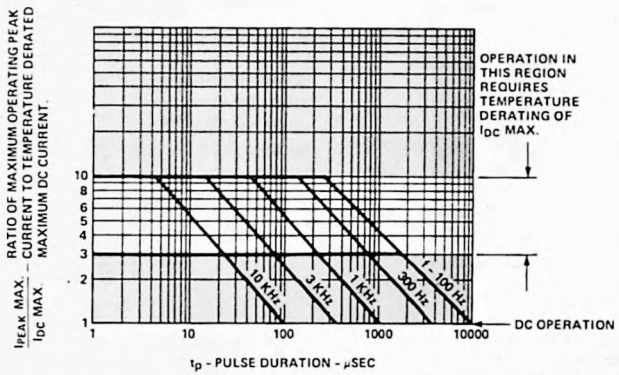


Figure 1. Maximum Tolerable Peak Current vs. Pulse Duration — 5082-7610/-7650 Series

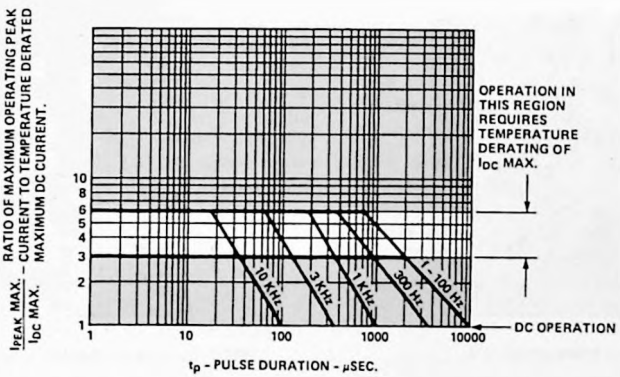


Figure 2. Maximum Tolerable Peak Current vs. Pulse Duration — 5082-7620/-7660 Series

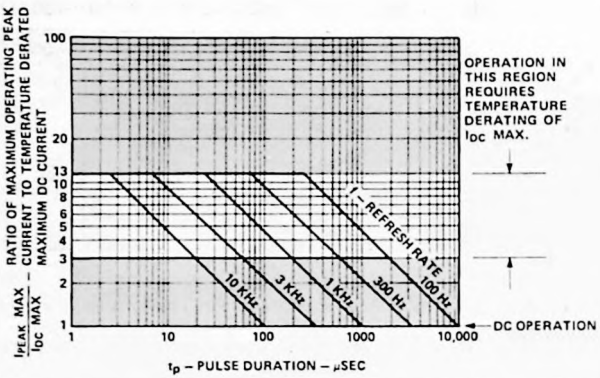


Figure 3. Allowed Peak Current vs. Pulse Duration — HDSP-3600/-4600 Series

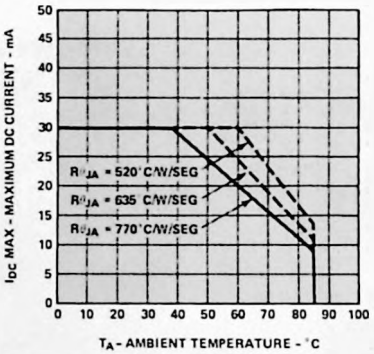


Figure 4. Maximum Allowable DC Current and DC Power Dissipation per Segment as a Function of Ambient Temperature — 5082-7610/-7650 Series

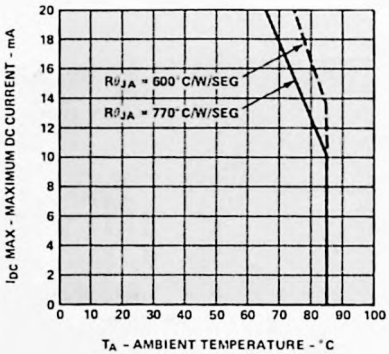


Figure 5. Maximum Allowable DC Current and DC Power Dissipation per Segment as a Function of Ambient Temperature — 5082-7620/-7660 Series

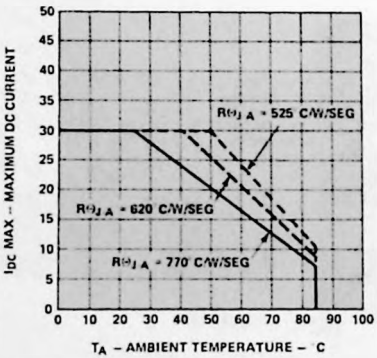


Figure 6. Maximum Allowable DC Current per Segment vs. Ambient Temperature — HDSP-3600/-4600 Series

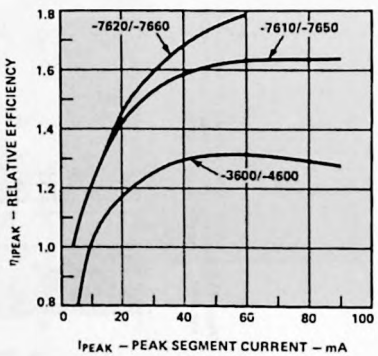


Figure 7. Relative Luminous Efficiency (Luminous Intensity per Unit Current) vs. Peak Segment Current

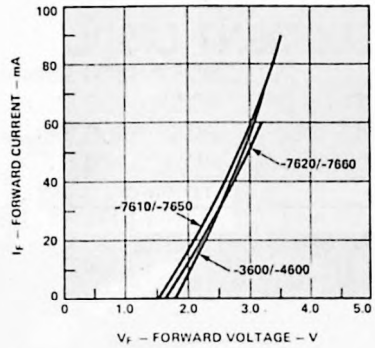


Figure 8. Forward Current vs. Forward Voltage Characteristics

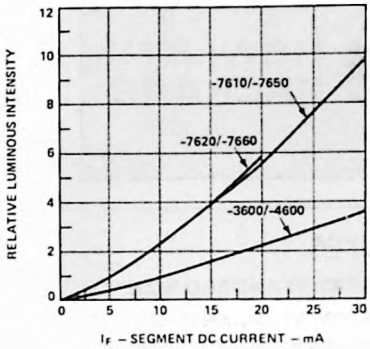


Figure 9. Relative Luminous Intensity vs. DC Forward Current

Electrical

These display devices are composed of light emitting diodes, with the light from each LED optically stretched to form individual segments and decimal points.

These display devices are well suited for strobed operation. The typical forward voltage values, scaled from Figure 8, should be used for calculating the current limiting resistor value and typical power dissipation. Expected maximum V_F values, for the purpose of driver circuit design and maximum power dissipation, may be calculated using the following V_F MAX models:

5082-7610/-7620/-7650/-7660 Series:

V_F MAX = 1.75 V + I_{PEAK} (38Ω)

For: $I_{PEAK} \geq 20$ mA

V_FMAX = 1.6 V + I_{DC} (45Ω)

For: 5 mA ≤ I_{DC} ≤ 20 mA

HDSP-3600/-4600 Series:

V_F MAX = 2.0 V + I_{PEAK} (50Ω)

For: $I_{PEAK} \geq 5$ mA

Contrast Enhancement

The objective of contrast enhancement is to provide good display readability in the end use ambient light. The concept is to employ both luminance and chrominance contrast techniques to enhance readability by having the OFF-segments blend into the display background and the ON-segments stand out vividly against this same background. Therefore, these display devices are assembled with a gray package and matching encapsulating epoxy in the segments.

Contrast enhancement may be achieved by using one of the following suggested filters:

5082-7610/ -7650	Panelgraphic SCARLET RED 65 or GRAY 10 SGL Homalite H100-1670 RED or -1266 GRAY 3M Louvered Filter R6310 RED or N0210 GRAY
5082-7620/ -7660	Panelgraphic YELLOW 27 or GRAY 10 SGL Homalite H100-1720 AMBER or -1266 GRAY 3M Louvered Filter A5910 AMBER or N0210 GRAY
HDSP-3600/ -4600	Panelgraphic GREEN 48 SGL Homalite H100-1440 GREEN 3M Louvered Filter G5610 GREEN or N0210 GRAY

Mechanical

To optimize device optical performance, specially developed plastics are used which restrict the solvents that may be used for cleaning. It is recommended that only mixtures of Freon (F113) and alcohol be used for vapor cleaning processes. with an immersion time in the vapors of less than two (2) minutes maximum. Some suggested vapor cleaning solvents are Freon TE, Genesolve DI-15 or DE-15, Arklone A or K. A 60°C (140°F) water cleaning process may also be used, which includes a neutralizer rinse (3% ammonia solution or equivalent), a surfactant rinse (1% detergent solution or equivalent), a hot water rinse and a thorough air dry. Room temperature cleaning may be accomplished with Freon T-E35 or T-P35, Ethanol, Isopropanol or water with a mild detergent.

Such cleaning agents from the ketone family (acetone, methyl ethyl ketone, etc.) and from the chlorinated hydrocarbon family (methylene chloride, trichloroethylene, carbon tetrachloride, etc.) are not recommended for cleaning LED parts. All of these various solvents attack or dissolve the encapsulating epoxies used to form the packages of plastic LED devices.

HEWLETT PACKARD

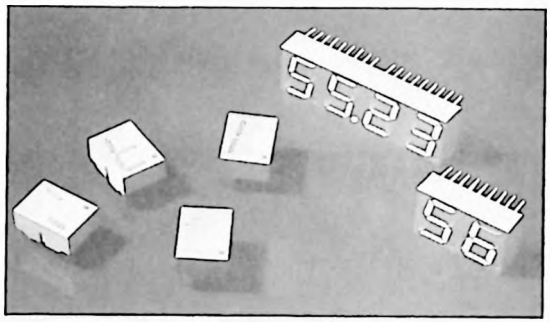
14.2mm (.56 INCH) SEVEN SEGMENT DISPLAYS

RED HDSP-5300 SERIES
HIGH EFFICIENCY RED HDSP-5500 SERIES
HIGH PERFORMANCE GREEN HDSP-5600 SERIES
YELLOW HDSP-5700 SERIES

TECHNICAL DATA JANUARY 1984

Features

- **INDUSTRY STANDARD SIZE**
- **INDUSTRY STANDARD PINOUT**
  15.24mm (.6 inch) DIP Leads on 2.54mm (.1 inch) Centers
- **CHOICE OF FOUR COLORS**
  Red **Yellow**
  High-Efficiency Red **High Performance Green**
- **EXCELLENT CHARACTER APPEARANCE**
  Evenly Lighted Segments
  Mitered Corners on Segments
  Gray Package Gives Optimum Contrast
- **COMMON ANODE OR COMMON CATHODE**
  Right Hand Decimal Point
  Overflow ±1 Character
- **CATEGORIZED FOR LUMINOUS INTENSITY; YELLOW AND GREEN CATEGORIZED FOR COLOR**
  Use of Like Categories Yields a Uniform Display



Description

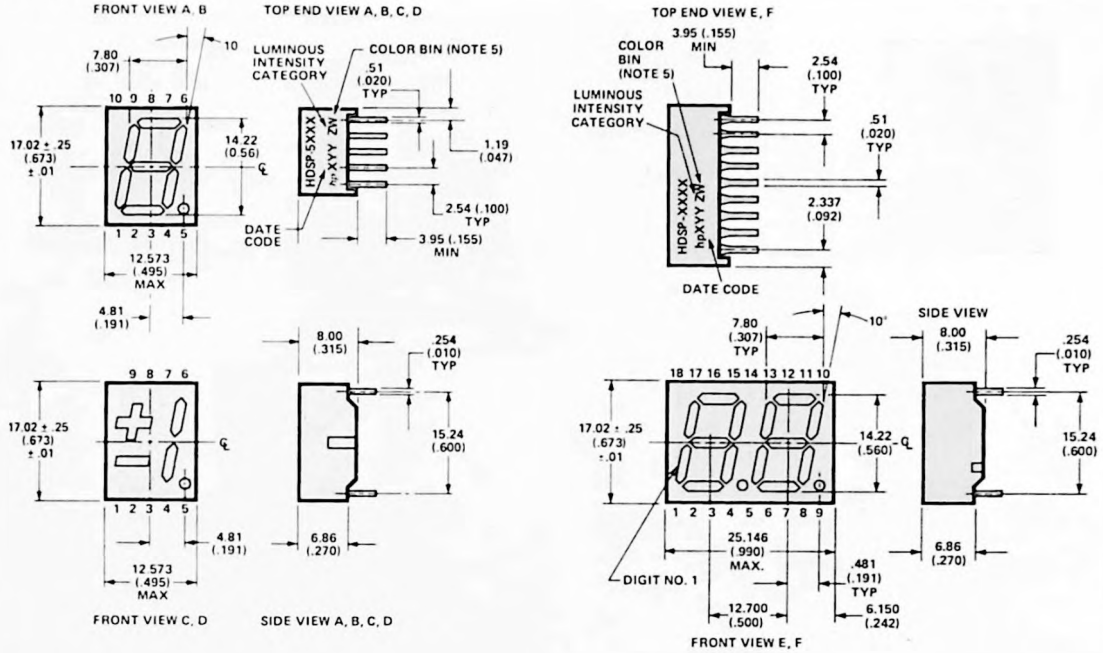
The HDSP-5300/-5500/-5600/-5700 Series are large 14.22 mm (.56 inch) LED seven segment displays. Designed for viewing distances up to 7 metres (23 feet), these displays provide excellent readability in bright ambients.

These devices utilize an industry standard size package and pin function configuration. Both the numeric and ±1 overflow devices feature a right hand decimal point and are available as either common anode or common cathode.

Devices

Part No. HDSP-	Color	Description	Package Drawing
5301	Red	Common Anode Right Hand Decimal	A
5303		Common Cathode Right Hand Decimal	B
5307		Overflow ± Common Anode	C
5308		Overflow ± Common Cathode	D
5321		Two Digit Common Anode Right Hand Decimal	E
5323		Two Digit Common Cathode Right Hand Decimal	F
5501	High Efficiency Red	Common Anode Right Hand Decimal	A
5503		Common Cathode Right Hand Decimal	B
5507		Overflow ± Common Anode	C
5508		Overflow ± Common Cathode	D
5521		Two Digit Common Anode Right Hand Decimal	E
5523		Two Digit Common Cathode Right Hand Decimal	F
5601	High Performance Green	Common Anode Right Hand Decimal	A
5603		Common Cathode Right Hand Decimal	B
5607		Overflow ± Common Anode	C
5608		Overflow ± Common Cathode	D
5621		Two Digit Common Anode Right Hand Decimal	E
5623		Two Digit Common Cathode Right Hand Decimal	F
5701	Yellow	Common Anode Right Hand Decimal	A
5703		Common Cathode Right Hand Decimal	B
5707		Overflow ± Common Anode	C
5708		Overflow ± Common Cathode	D
5721		Two Digit Common Anode Right Hand Decimal	E
5723		Two Digit Common Cathode Right Hand Decimal	F

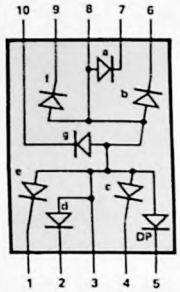
Package Dimensions



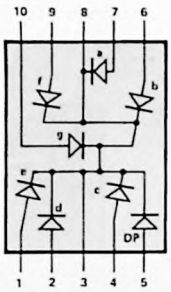
PIN	FUNCTION					
	A	B	C	D	E	F
1	CATHODE e	ANODE e	CATHODE c	ANODE c	E CATHODE NO. 1	E ANODE NO. 1
2	CATHODE d	ANODE d	ANODE c, d	CATHODE c, d	D CATHODE NO. 1	D ANODE NO. 1
3	ANODE[3]	CATHODE[4]	CATHODE b	ANODE b	C CATHODE NO. 1	C ANODE NO. 1
4	CATHODE c	ANODE c	ANODE a, b, DP	CATHODE a, b, DP	DP CATHODE NO. 1	DP ANODE NO. 1
5	CATHODE DP	ANODE DP	CATHODE DP	ANODE DP	E CATHODE NO. 2	E ANODE NO. 2
6	CATHODE b	ANODE b	CATHODE a	ANODE a	D CATHODE NO. 2	D ANODE NO. 2
7	CATHODE a	ANODE a	ANODE a, b, DP	CATHODE a, b, DP	G CATHODE NO. 2	G ANODE NO. 2
8	ANODE[3]	CATHODE[4]	ANODE c, d	CATHODE c, d	C CATHODE NO. 2	C ANODE NO. 2
9	CATHODE f	ANODE f	CATHODE d	ANODE d	DP CATHODE NO. 2	DP ANODE NO. 2
10	CATHODE g	ANODE g	NO PIN	NO PIN	B CATHODE NO. 2	B ANODE NO. 2
11					A CATHODE NO. 2	A ANODE NO. 2
12					F CATHODE NO. 2	F ANODE NO. 2
13					DIGIT NO. 2 ANODE	DIGIT NO. 2 CATHODE
14					DIGIT NO. 1 ANODE	DIGIT NO. 1 CATHODE
15					B CATHODE NO. 1	B ANODE NO. 1
16					A CATHODE NO. 1	A ANODE NO. 1
17					G CATHODE NO. 1	G ANODE NO. 1
18					F CATHODE NO. 1	F ANODE NO. 1

Notes:
1. All dimensions in millimetres (inches).
2. All untoleranced dimensions are for reference only.
3. Redundant anodes.
4. Redundant cathodes.
5. For HDSP-5600/-5700 series product only.

Internal Circuit Diagram



A



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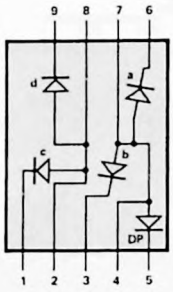

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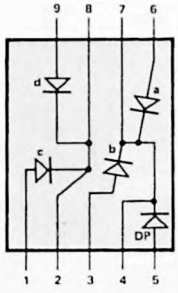

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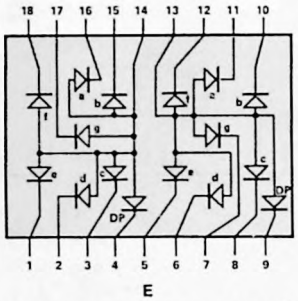

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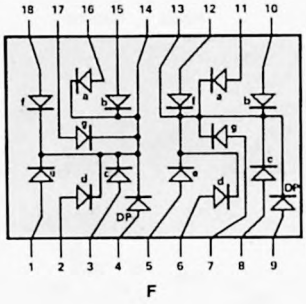


F

Absolute Maximum Ratings

	-5300 Series	-5500/-5600 Series	-5700 Series
Average Power per Segment or DP	60 mW	105 mW	80 mW
Peak Forward Current per Segment or DP	150 mA[6] (Pulse Width ≤ .2 ms)	90 mA [7] (Pulse Width ≤ 1 ms)	60 mA[8] (Pulse Width ≤ 1 ms)
DC Forward Current per Segment[9] or DP	25 mA	30 mA	20 mA
Operating Temperature Range	-40° C to +85° C	-40° C to +85° C	-40° C to +85° C
Storage Temperature Range	-40° C to +85° C	-40° C to +85° C	-40° C to +85° C
Reverse Voltage per Segment or DP	3.0V	3.0V	3.0V
Lead Solder Temperature	260° C for 3 sec. (1.59 mm [1/16 in.] below seating plane)	260° C for 3 sec.	260° C for 3 sec.

Notes:

6. See Figure 1 to establish pulsed operating conditions.
7. See Figure 6 to establish pulsed operating conditions. HDSP-5500. See Figure 7 to establish pulsed operating conditions. HDSP-5600.
8. See Figure 8 to establish pulsed operating conditions.
9. Derate Maximum DC current: See Figure 2 for -5300 Series. See Figure 9 for -5500 Series. See Figure 10 for -5600 Series. See Figure 11 for -5700 Series.

Electrical/Optical Characteristics at $T_A = 25°C$

RED HDSP-5300 Series

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment[10] (Digit Average)	I_V	$I_F = 20$ mA	400	1200		μcd
		100 mA Peak: 1 of 5 Duty Factor		1300		
Peak Wavelength	λ_{PEAK}			655		nm
Dominant Wavelength[11]	λ_d			640		nm
Forward Voltage/Segment or DP[12]	V_F	$I_F = 20$ mA		1.6	2.0	V
Reverse Voltage/Segment or DP[12] [17]	V_R	$I_R = 100$ μA	3	12		V
Thermal Resistance LED Junction-to-Pin	$R\theta_{J-PIN}$			345		°C/W/ Seg.

Notes:

10. The digits are categorized for luminous intensity with category designated by a letter located on the right hand side of the package. The luminous intensity minimum and categories are determined by computing the numerical average of the individual segment intensities, decimal point not included.
11. The dominant wavelength, λ_d, is derived from the C.I.E. Chromaticity Diagram and is that single wavelength which defines the color of the device.
12. Quality level for Electrical Characteristics is 1000 parts per million.

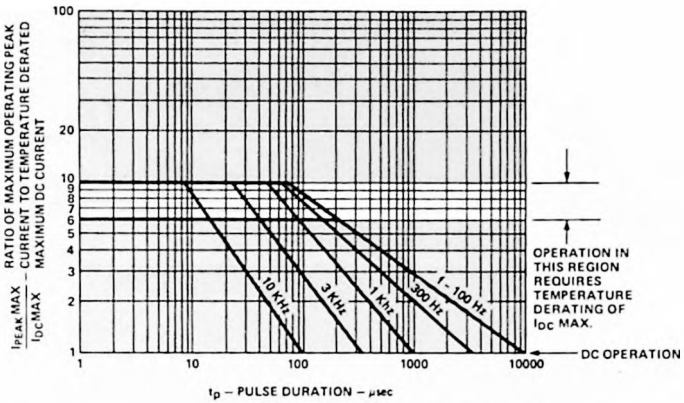


Figure 1. Maximum Tolerable Peak Current vs. Pulse Duration.

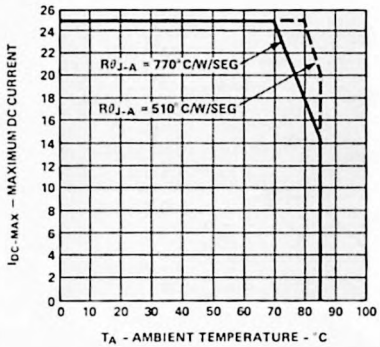


Figure 2. Maximum Allowable Average Forward Current Per Segment vs. Ambient Temperature. Deratings Based on Maximum Allowed Thermal Resistance Values, LED Junction to Ambient on a per Segment Basis. T_J MAX = 105°C.

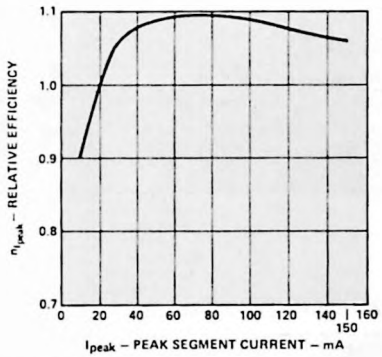


Figure 3. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Segment Current.

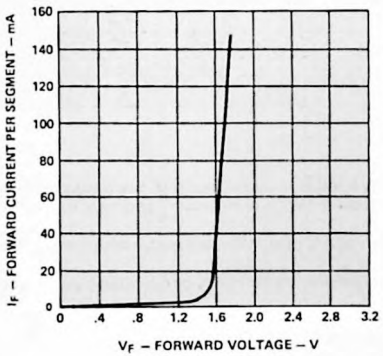


Figure 4. Forward Current vs. Forward Voltage.

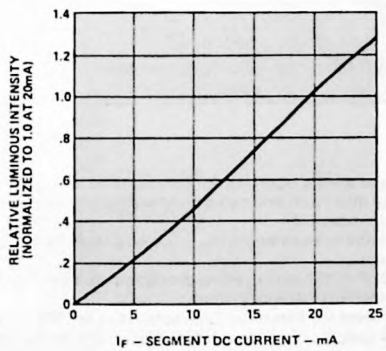


Figure 5. Relative Luminous Intensity vs. D.C. Forward Current.

For a Detailed Explanation of the Use of Data Sheet Information and Recommended Soldering Procedures, See Application Note 1005.

HIGH EFFICIENCY RED HDSP-5500 SERIES

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment[13] (Digit Average)	I_V	10 mA DC	600	2500		μcd
		60 mA Peak: 1 of 6 Duty Factor		3300		
Peak Wavelength	λ_{PEAK}			635		nm
Dominant Wavelength[14]	λ_d			626		nm
Forward Voltage/Segment or DP[16]	V_F	I_F = 20 mA		2.1	2.5	V
Reverse Voltage/Segment or DP[16]	V_R	I_R = 100 μA	3	30		V
Thermal Resistance LED Junction-to-Pin	$R\theta_{J-PIN}$			345		°C/W/ Seg.

HIGH PERFORMANCE GREEN HDSP-5600 SERIES

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment[13] (Digit Average)	I_V	10 mA DC	600	1500		μcd
		60 mA Peak: 1 of 6 Duty Factor		1920		
Peak Wavelength	λ_{PEAK}			566		nm
Dominant Wavelength[14, 15]	λ_d			571	577	nm
Forward Voltage/Segment or DP[16]	V_F	I_F = 10 mA		2.1	2.5	V
Reverse Voltage/Segment or DP[16,17]	V_R	I_R = 100 μA	3	50		V
Thermal Resistance LED Junction-to-Pin	$R\theta_{J-PIN}$			345		°C/W/ Seg.

YELLOW HDSP-5700 SERIES

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment[13] (Digit Average)	I_V	10 mA DC	600	1800		μcd
		60 mA Peak: 1 of 6 Duty Factor		2750		
Peak Wavelength	λ_{PEAK}			583		nm
Dominant Wavelength[14, 15]	λ_d		581.5	586	592.5	nm
Forward Voltage/Segment or DP[16]	V_F	I_F = 20 mA		2.2	2.5	V
Reverse Voltage/Segment or DP[16,17]	V_R	I_R = 100 μA	3	40		V
Thermal Resistance LED Junction-to-Pin	$R\theta_{J-PIN}$			345		°C/W/ Seg.

Notes:

13. The digits are categorized for luminous intensity with category designated by a letter located on top of the package. The luminous intensity minimum and categories are determined by computing the numerical average of the individual segment intensities, decimal point not included.
14. The dominant wavelength, λ_d, is derived from the C.I.E. Chromaticity Diagram and is that single wavelength which defines the color of the device.
15. The HDSP-5700 series yellow displays are categorized as to dominant wavelength with the category designated by a number adjacent to the intensity category letter.
16. Quality level for Electrical Characteristics is 1000 parts per million.
17. Typical specification for reference only. Do not exceed absolute maximum ratings.

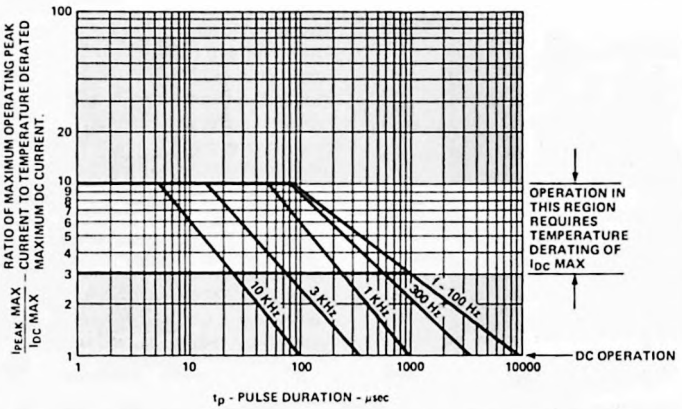


Figure 6. Maximum Tolerable Peak Current vs. Pulse Duration — HDSP-5500 Series.

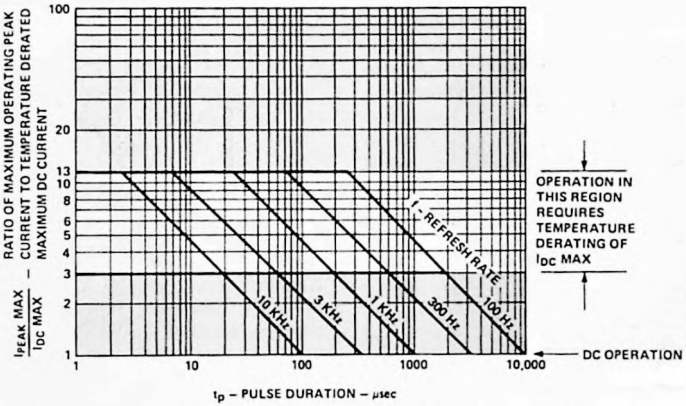


Figure 7. Maximum Tolerable Peak Current vs. Pulse Duration — HDSP-5600 Series.

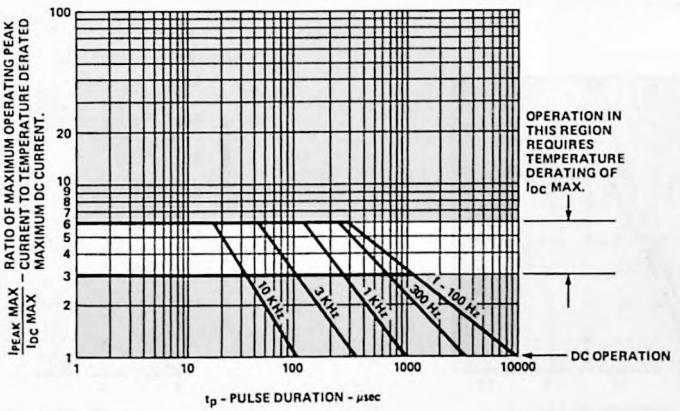


Figure 8. Maximum Tolerable Peak Current vs. Pulse Duration — HDSP-5700 Series.

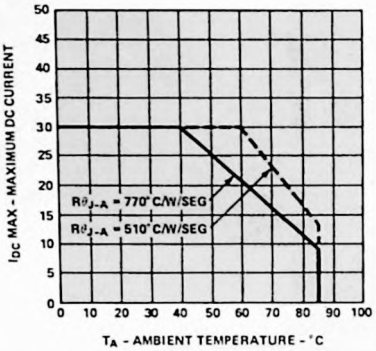


Figure 9. Maximum Allowable Average Current per Segment vs. Ambient Temperature. Derating Based on Maximum Allowed Thermal Resistance Values. LED Junction to Ambient on a per Segment Basis. T_J LED MAX = 105°C — HDSP-5500 Series.

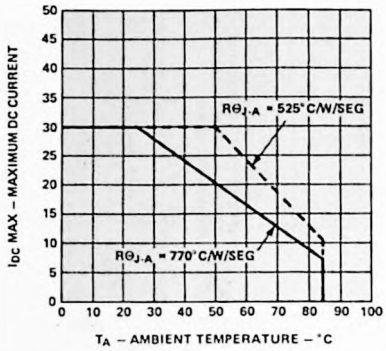


Figure 10. Maximum Allowable Average Current per Segment vs. Ambient Temperature. Derating Based on Maximum Allowed Thermal Resistance Values, LED Junction to Ambient on a per Segment Basis. T_J LED MAX = 105°C. — HDSP-5600 Series.

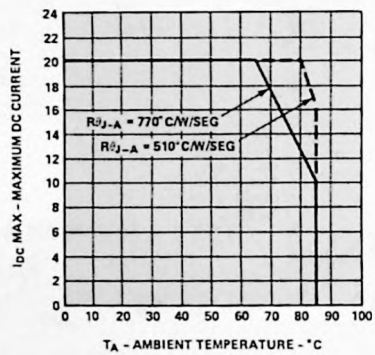


Figure 11. Maximum Allowable Average Current per Segment vs. Ambient Temperature. Derating Based on Maximum Allowed Thermal Resistance Values, LED Junction to Ambient on a per Segment Basis. T_J LED MAX = 105°C — HDSP-5700 Series.

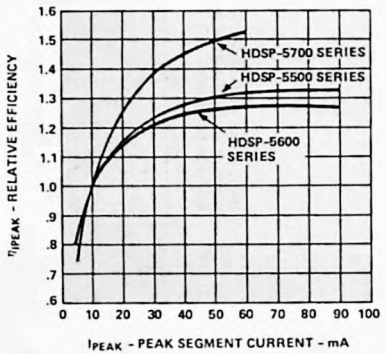


Figure 12. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Segment Current.

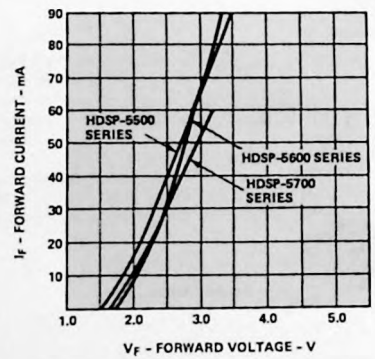


Figure 13. Forward Current vs. Forward Voltage Characteristics.

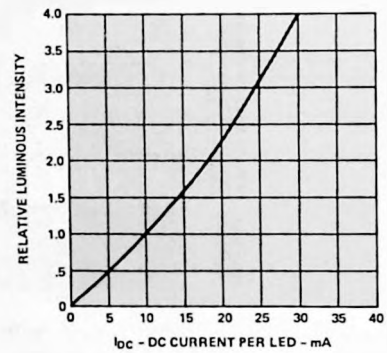


Figure 14. Relative Luminous Intensity vs. DC Forward Current. HDSP-5500/-5600/-5700

Electrical

The HDSP-5300/-5500/-5600/-5700 series of display devices are composed of light emitting diodes, with the light from each LED optically stretched to form individual segments and decimal points. The -5300 series uses a p-n junction diffused into a GaAsP epitaxial layer on a GaAs substrate. The -5500 and -5700 series have their p-n junctions diffused into a GaAsP epitaxial layer on a GaP substrate. The -5600 series use a GaP epitaxial layer on GaP.

These display devices are designed for strobed operation. The typical forward voltage values, scaled from Figure 4 or 13, should be used for calculating the current limiting resistor value and typical power dissipation. Expected maximum V_F values, for the purpose of driver circuit design and maximum power dissipation, may be calculated using the following V_F MAX models:

HDSP-5300 Series:

V_F MAX = 1.55V + I_{PEAK} (7Ω)

For: $I_{PEAK} \geq 5$ mA

HDSP-5500/-5700 Series:

V_F MAX = 1.75V + I_{PEAK} (38Ω)

For: $I_{PEAK} \geq 20$ mA

V_F MAX = 1.5V + I_{DC} (45Ω)

For: 5 mA ≤ I_{DC} ≤ 20 mA

HDSP-5600 Series:

V_F MAX = 2.0V + I_{PEAK} (50Ω)

For: $I_{PEAK} \geq 5$ mA

Contrast Enhancement

The objective of contrast enhancement is to provide good display readability in the end use ambient light. The concept is to employ both luminance and chrominance contrast techniques to enhance readibility by having the OFF-segments blend into the display background and the ON-segments stand out vividly against this same background. Therefore, these display devices are assembled with a gray package and matching encapsulating epoxy in the segments.

Contrast enhancement may be achieved by using one of the following suggested filters:

HDSP-5300: Panelgraphic RUBY RED 60
SGL Homalite H100-1605 RED
3M Louvered Filter R6610 RED or N0210 GRAY

HDSP-5500: Panelgrahpic SCARLET RED 65 or GRAY 10
SGL Homalite H100-1670 RED or -1266 GRAY
3M Louvered Filter R6310 RED or N0210 GRAY

HDSP-5600: Panelgraphic GREEN 48
SGL Homalite H100-1440 GREEN
3M Louvered Filter G5610 GREEN or N0210 GRAY

HDSP-5700: Panelgraphic YELLOW 27 or GRAY 10
SGL Homalite H100-1720 AMBER or -1266 GRAY
3M Louvered Filter A5910 AMBER or N0210 GRAY

Mechanical

To optimize device optical performance, specially developed plastics are used which restrict the solvents that may be used for cleaning. It is recommended that only mixtures of Freon (F113) and alcohol be used for vapor cleaning processes, with an immersion time in the vapors of less than two (2) minutes maximum. Some suggested vapor cleaning solvents are Freon TE, Genesolve DI-15 or DE-15. Arklone A or K. A 60°C (140°F) water cleaning process may also be used, which includes a neutralizer rinse (3% ammonia solution or equivalent), a surfactant rinse (1% detergent solution or equivalent), a hot water rinse and a thorough air dry. Room temperature cleaning may be accomplished with Freon T-E35 or T-P35, Ethanol, Isopropanol or water with a mild detergent.

Such cleaning agents from the ketone family (acetone, methyl ethyl ketone, etc.) and from the chlorinated hydrocarbon family (methylene chloride, trichloroethylene, carbon tetrachloride, etc.) are not recommended for cleaning LED parts. All of these various solvents attack or dissolve the encapsulating epoxies used to form the packages of plastic LED devices.

HEWLETT PACKARD

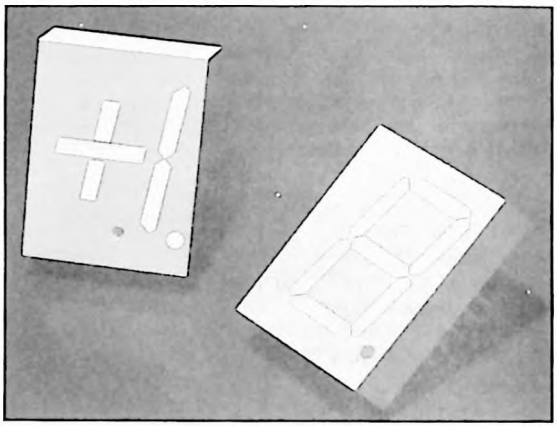
LARGE 20 mm (0.8") SEVEN SEGMENT DISPLAYS

RED HDSP-3400 Series
HIGH EFFICIENCY RED HDSP-3900 Series
YELLOW HDSP-4200 Series
HIGH PERFORMANCE GREEN HDSP-8600 Series

TECHNICAL DATA JANUARY 1984

Features

- **20 mm (0.8") DIGIT HEIGHT**
  Viewable Up to 10 Metres (33 Feet)
- **CHOICE OF FOUR COLORS**
  Red Yellow
  High Efficiency Red Green
- **EXCELLENT CHARACTER APPEARANCE**
  Evenly Lighted Segments
  Wide Viewing Angle
  Mitered Corners on Segments
  Grey Package Provides Optimum Contrast
- **CATEGORIZED FOR LUMINOUS INTENSITY; YELLOW AND GREEN CATEGORIZED FOR COLOR**
  Use of Like Categories Yields a Uniform Display
- **IC COMPATIBLE**
- **MECHANICALLY RUGGED**



Description

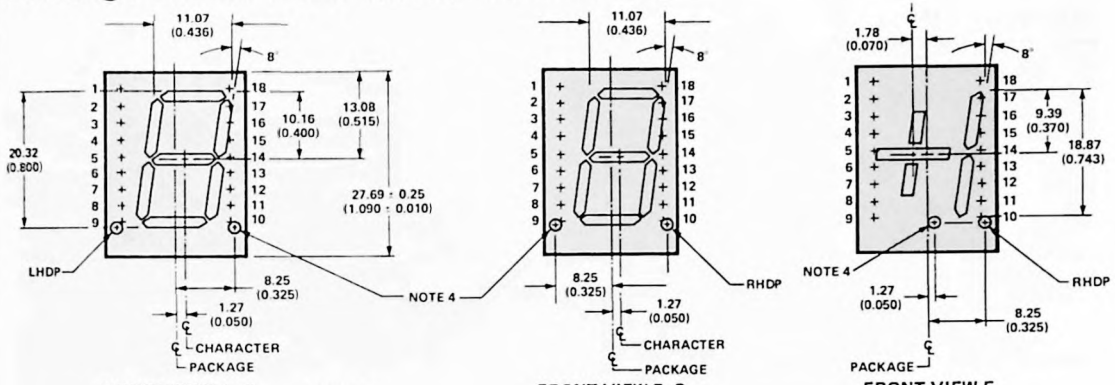
The HDSP-3400/-3900/-4200/-8600 Series are very large 20 mm (0.8 in.) LED seven segment displays. Designed for viewing distances up to 10 metres (33 feet), these single digit displays provide excellent readability.

These devices utilize a standard 15.24 mm (0.6 in.) dual in line package configuration that permits mounting on PC boards or in standard IC sockets. Requiring a low forward voltage, these displays are inherently IC compatible, allowing for easy integration into electronic instrumentation, point-of-sale terminals, TVs, weighing scales, and digital clocks.

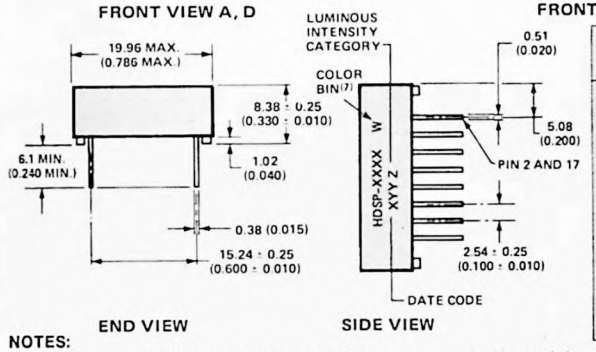
Devices

Part Number	Color	Description	Package Drawing
HDSP-3400	Red	Common Anode Left Hand Decimal	A
HDSP-3401		Common Anode Right Hand Decimal	B
HDSP-3403		Common Cathode Right Hand Decimal	C
HDSP-3405		Common Cathode Left Hand Decimal	D
HDSP-3406		Universal Overflow ±1 Right Hand Decimal	E
HDSP-3900	High Efficiency Red	Common Anode Left Hand Decimal	A
HDSP-3901		Common Anode Right Hand Decimal	B
HDSP-3903		Common Cathode Right Hand Decimal	C
HDSP-3905		Common Cathode Left Hand Decimal	D
HDSP-3906		Universal Overflow ±1 Right Hand Decimal	E
HDSP-4200	Yellow	Common Anode Left Hand Decimal	A
HDSP-4201		Common Anode Right Hand Decimal	B
HDSP-4203		Common Cathode Right Hand Decimal	C
HDSP-4205		Common Cathode Left Hand Decimal	D
HDSP-4206		Universal Overflow ±1 Right Hand Decimal	E
HDSP-8600	High Performance Green	Common Anode Left Hand Decimal	A
HDSP-8601		Common Anode Right Hand Decimal	B
HDSP-8603		Common Cathode Right Hand Decimal	C
HDSP-8605		Common Cathode Left Hand Decimal	D
HDSP-8606		Universal Overflow ±1	E

Package Dimensions (3900/4200 Series)



FRONT VIEW A, D — FRONT VIEW B, C — FRONT VIEW E

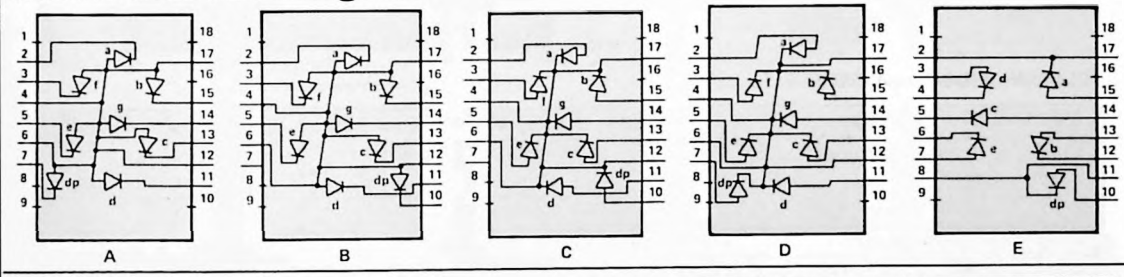


END VIEW — SIDE VIEW

Pin	Function A 3400/3900/4200/8600	B 3401/3901/4201/8601	C 3403/3903/4203/8603	D 3405/3905/4205/8605	E 3406/3906/4206/8606
1	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN
2	CATHODE a	CATHODE a	ANODE a	ANODE a	CATHODE a
3	CATHODE f	CATHODE f	ANODE f	ANODE f	ANODE d
4	ANODE[3]	ANODE[3]	CATHODE[4]	CATHODE[4]	CATHODE d
5	CATHODE e	CATHODE e	ANODE e	ANODE e	CATHODE c
6	ANODE[2]	ANODE[3]	CATHODE[4]	CATHODE[4]	CATHODE e
7	CATHODE dp	NO. CONNEC.	NO CONNEC	ANODE dp	ANODE e
8	NO PIN	NO PIN	NO PIN	NO PIN	CATHODE dp
9	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN
10	NO PIN	CATHODE dp	ANODE dp	NO PIN	ANODE dp
11	CATHODE d	CATHODE d	ANODE d	ANODE d	CATHODE dp
12	ANODE[3]	ANODE[3]	CATHODE[4]	CATHODE[4]	CATHODE b
13	CATHODE c	CATHODE c	ANODE c	ANODE c	ANODE b
14	CATHODE g	CATHODE g	ANODE g	ANODE g	ANODE c
15	CATHODE b	CATHODE b	ANODE b	ANODE b	ANODE a
16	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN
17	ANODE[3]	ANODE[3]	CATHODE[4]	CATHODE[4]	CATHODE a
18	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN

NOTES:
1. Dimensions in millimeters and (inches).
2. All untoleranced dimensions are for reference only.
3. Redundant anodes.
4. Unused dp position.
5. See Internal Circuit Diagram.
6. Redundant Cathodes.
7. For HDSP-4200/-8600 Series product only.
8. See part number table for LHDP and RHDP designation.

Internal Circuit Diagram



A B C D E

Absolute Maximum Ratings

	-3400 Series	-3900/-4200 Series	-8600 Series
Average Power per Segment or DP (T_A = 25° C)[9]	120 mW	105 mW	105 mW
Operating Temperature Range	−40° C to +85° C	−40° C to +85° C	−40° C to +85° C
Storage Temperature Range	−40° C to +85° C	−40° C to +85° C	−40° C to +85° C
Peak Forward Current per Segment or DP (T_A = 25° C, Pulse Width = 1.2 ms)[10]	200 mA	135 mA	90 mA
DC Forward Current per Segment or DP (T_A = 25° C)[9]	50 mA	40 mA	30 mA
Reverse Voltage per Segment or DP	3.0 V	3.0 V	3.0 V
Lead Soldering Temperature (1.6 mm [1/6 in.] Below Seating Plane)	260° C for 3 sec.	260° C for 3 sec.	260° C for 3 sec.

Notes:
9. See Power Derating Curves (see Figure 2 for -3400 Series, Figure 7 for -3900/-4200 Series, and Figure 12 for -8600 Series).
10. See appropriate curves to establish pulsed operating conditions (see Figure 1 for -3400 Series, Figure 6 for -3900/-4200 Series, Figure 11 for -8600 Series).

Electrical/Optical Characteristics at $T_A = 25°C$

RED HDSP-3400 SERIES

Description	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment (Digit Average)[11, 12]	I_V	$I_F = 20$ mA	500	1200		μcd
Peak Wavelength	λ_{PEAK}			655		nm
Dominant Wavelength[13]	λ_d			640		nm
Forward Voltage, any Segment or DP[15]	V_F	$I_F = 20$ mA		1.6	2.0	V
Reverse Voltage, any Segment or DP[14, 15]	V_R	$I_R = 100\ \mu A$	3.0	20.0		V
Temperature Coefficient of Forward Voltage	$\Delta V_F/°C$	$I_F = 20$ mA		−1.5		mV/°C
Thermal Resistance LED Junction-to-Pin	$R\theta_{J-PIN}$			375		°C/W/ Seg

HIGH EFFICIENCY RED HDSP-3900 SERIES

Description	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment (Digit Average)[11, 12]	I_V	100 mA Pk; 1 of 5 Duty Factor	2200	7000		μcd
		20 mA DC		4800		
Peak Wavelength	λ_{PEAK}			635		nm
Dominant Wavelength[13] (Digit Average)	λ_d			626		nm
Forward Voltage, any Segment or DP[15]	V_F	$I_F = 100$ mA		2.6	3.5	V
Reverse Voltage, any Segment or DP[15, 16]	V_R	$I_R = 100\ \mu A$	3.0	25.0		V
Temperature Coefficient of Forward Voltage	$\Delta V_F/°C$	$I_F = 100$ mA		−1.1		mV/°C
Thermal Resistance LED Junction-to-Pin	$R\theta_{J-PIN}$			375		°C/W/ Seg

YELLOW HDSP-4200 SERIES

Description	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment (Digit Average)[11, 12]	I_V	100 mA Pk; 1 of 5 Duty Factor	2200	7000		μcd
		20 mA DC		3400		
Peak Wavelength	λ_{PEAK}			583		nm
Dominant Wavelength[13, 14] (Digit Average)	λ_d		581.5	586	592.5	nm
Forward Voltage, any Segment or DP[15]	V_F	$I_F = 100$ mA		2.6	3.5	V
Reverse Voltage, any Segment or DP[15, 16]	V_R	$I_R = 100\ \mu A$	3.0	25.0		V
Temperature Coefficient of Forward Voltage	$\Delta V_F/°C$	$I_F = 100$ mA		−1.1		mV/°C
Thermal Resistance LED Junction-to-Pin	$R\theta_{J-PIN}$			375		°C/W/ Seg

HIGH PERFORMANCE GREEN HDSP-8600 SERIES

Description	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment (Digit Average)[11, 12]	I_V	60 mA Pk; 1 of 5 Duty Factor		1960		μcd
		10 mA DC	700	1500		
Peak Wavelength	λ_{PEAK}			566		nm
Dominant Wavelength[13, 14] (Digit Average)	λ_d			571	577	nm
Forward Voltage, any Segment or DP[15]	V_F	I_F = 10 mA		2.1	2.5	V
Reverse Voltage, any Segment or DP[15, 16]	V_R	I_R = 100 μA	3.0	50.0		V
Thermal Resistance LED Junction-to-Pin	$R\theta_{J-PIN}$			375		°C/W/ Seg

Notes:
11. Case temperature of the device immediately prior to the intensity measurement is 25° C.
12. The digits are categorized for luminous intensity with the intensity category designated by a letter on the side of the package.
13. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and is that single wavelength which defines the color of the device.
14. The yellow and green displays are categorized as to dominant wavelength with the category designated by a number adjacent to the intensity category letter.
15. Quality level for electrical characteristics is 1000 parts per million.
16. Typical specification for reference only. Do not exceed absolute maximum ratings.

HDSP-3400 SERIES

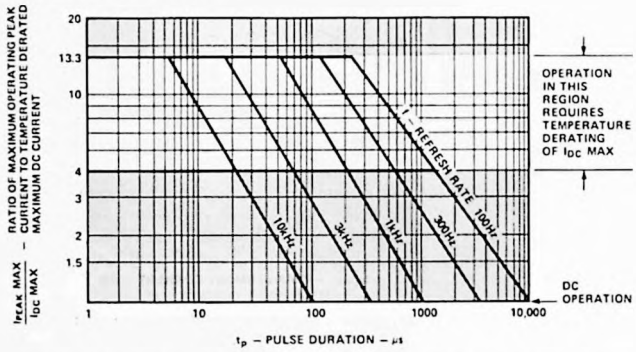


Figure 1. Maximum Allowable Peak Current vs. Pulse Duration

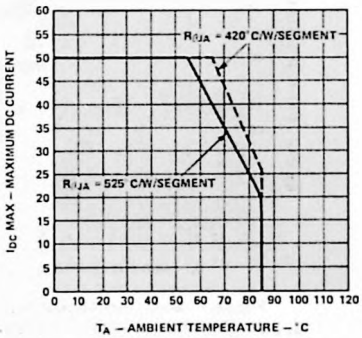


Figure 2. Maximum Allowable DC Current per Segment vs. Ambient Temperature

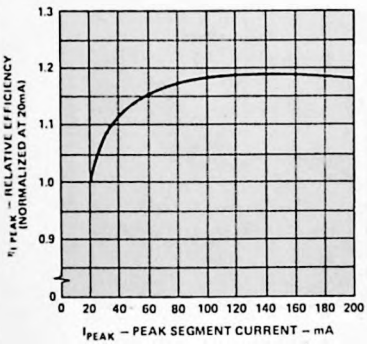


Figure 3. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Segment Current

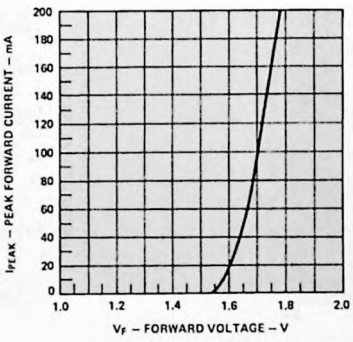


Figure 4. Peak Forward Segment Current vs. Peak Forward Voltage

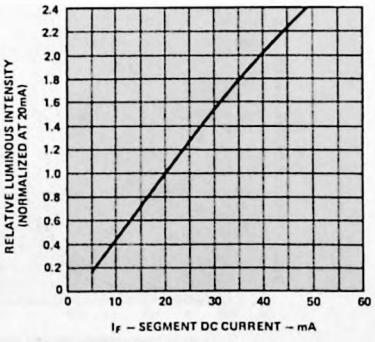


Figure 5. Relative Luminous Intensity vs. DC Forward Current

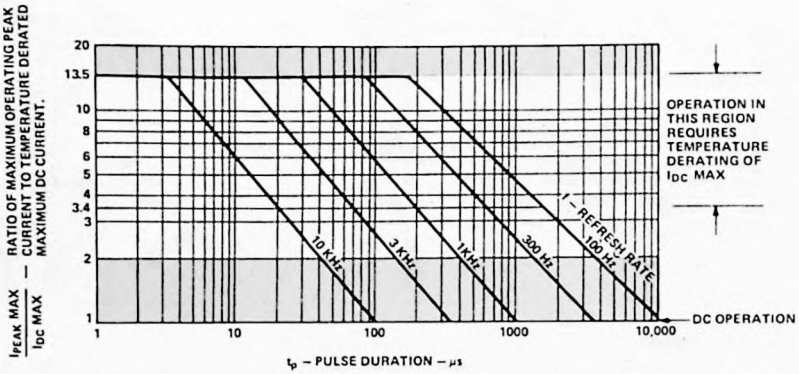


Figure 6. Maximum Allowed Peak Current vs. Pulse Duration

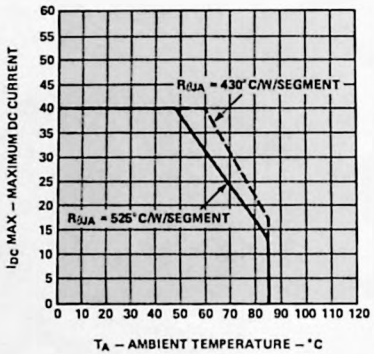


Figure 7. Maximum Allowable DC Current per Segment vs. Ambient Temperature

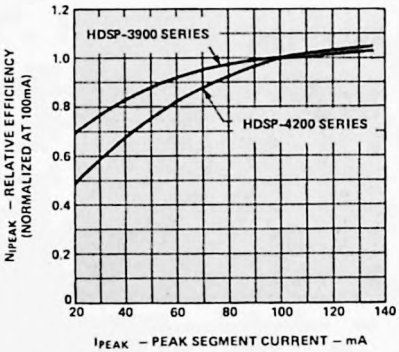


Figure 8. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Segment Current

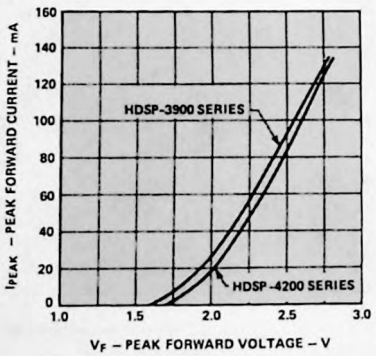


Figure 9. Peak Forward Segment Current vs. Peak Forward Voltage

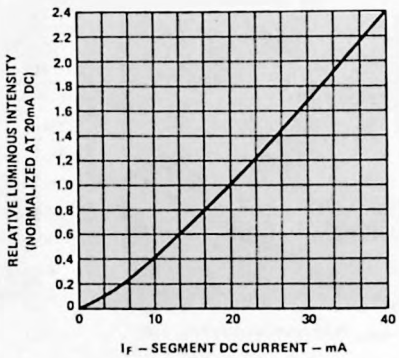


Figure 10. Relative Luminous Intensity vs. DC Forward Current

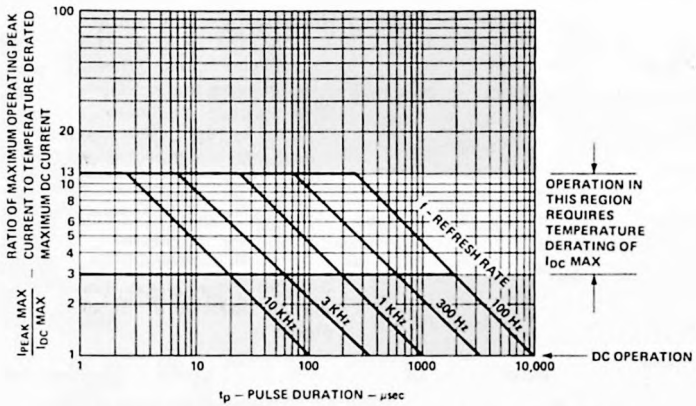


Figure 11. Maximum Allowed Peak Current vs. Pulse Duration

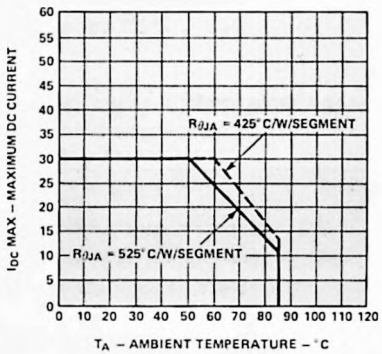


Figure 12. Maximum Allowable DC Current per Segment vs. Ambient Temperature

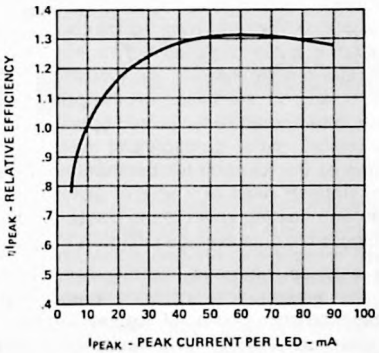


Figure 13. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Segment Current

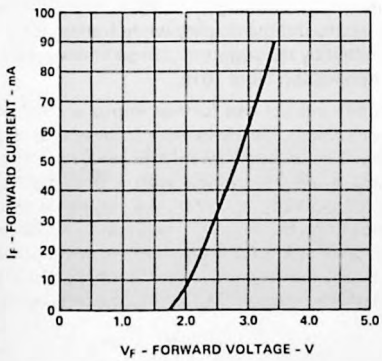


Figure 14. Peak Forward Segment Current vs. Peak Forward Voltage

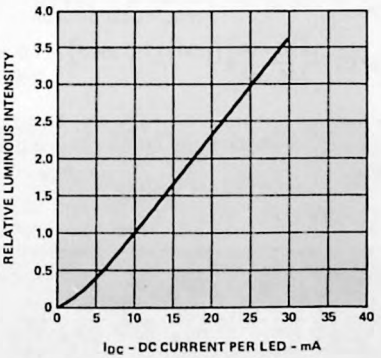


Figure 15. Relative Luminous Intensity vs. DC Forward Current

Electrical

These display devices are composed of eight light emitting diodes, with light from each LED optically stretched to form individual segments and a decimal point.

These display devices are designed for strobed operation. The typical forward voltage values, scaled from Figure 4, 9, or 14 should be used for calculating the current limiting resistor value and typical power dissipation. Expected maximum V_F values, for the purpose of driver circuit design and maximum power dissipation, may be calculated using the following V_F MAX models:

HDSP-3400 Series	V_F MAX = 1.55 V + I_{PEAK} (7Ω) For: $I_{PEAK} \geq 5$ mA
HDSP-3900/-4200 Series	V_F MAX = 2.15 V + I_{PEAK} (13.5Ω) For: $I_F \geq 30$ mA
	V_F MAX = 1.9 V + I_{DC} (21.8Ω) For: 10 mA ≤ I_F ≤ 30 mA
HDSP-8600 Series	V_F MAX = 2.0 V + I_{PEAK} (50Ω) For: $I_{PEAK} \geq 5$ mA

Temperature derated strobed operating conditions are obtained from Figures 1, 6, or 11 and 2, 7, or 12. Figures 1, 6, and 11 relate pulse duration (t_p), refresh rate (f), and the ratio of maximum peak current to maximum dc current (I_{PEAK} MAX/I_{DC} MAX). Figures 2, 7, and 12 present the maximum allowed dc current vs. ambient temperature. Figures 1, 6, and 11 are based on the principle that the peak junction temperature for pulsed operation at a specified peak current, pulse duration and refresh rate should be the same as the junction temperature at maximum DC operation. Refresh rates of 1 kHz or faster minimize the pulsed junction heating effect of the device resulting in the maximum possible time average luminous intensity.

The time average luminous intensity can be calculated knowing the average forward current and relative efficiency characteristic, η_{IPEAK}, of Figures 3, 8, or 13. Time average luminous intensity for a device case temperature of 25°C, I_V (25°C), is calculated as follows:

$$I_V\ (25°C) = \left[\frac{I_{AVG}}{I_{AVG}\ \text{Test Condition}}\right]\left[\eta_{IPEAK}\right]\left[I_V\ \text{DATA SHEET}\right]$$

Example: For HDSP-4200 series

η_{IPEAK} = 1.00 at I_{PEAK} = 100 mA. For DF = 1/5:

$$I_V\ (25°C) = \left[\frac{20\ mA}{20\ mA}\right]\left[1.00\right]\left[7.0\ mcd\right] = 7.0\ mcd/segment$$

The time average luminous intensity may be adjusted for operating junction temperature by the following exponential equation:

$$I_V\ (T_J) = I_V\ (25°C)\ e^{|k(T_J + 25°C)|}$$

where $T_J = T_A + P_D \cdot R\theta_{J-A}$

Device	K
-3400	-0.0188/°C
-3900	-0.0131/°C
-4200	-0.0112/°C
-8600	-0.0044/°C

Mechanical

These devices are constructed utilizing a lead frame in a standard DIP package. The LED dice are attached directly to the lead frame. Therefore, the cathode leads are the direct thermal and mechanical stress paths to the LED dice. The absolute maximum allowed junction temperature, T_J MAX, is 105°C. The maximum power ratings have been established so that the worst case V_F device does not exceed this limit.

Worst case thermal resistance pin-to-ambient is 400°C/W/Seg when these devices are soldered into minimum trace width PC boards. When installed in a PC board that provides $R\theta_{PIN-A}$ less than 400°C/W/Seg these displays may be operated at higher average currents as shown in Figure 2.

Optical

The radiation pattern for these devices is approximately Lambertian. The luminous sterance may be calculated using one of the two following formulas.

$$L_V\ (cd/m^2) = \frac{I_V\ (cd)}{A\ (m^2)}$$

$$L_V\ (\text{footlamberts}) = \frac{\pi I_V\ (cd)}{A\ (ft^2)}$$

Area/Seg. mm^2	Area/Seg. $in.^2$
14.9	0.0231

Contrast Enhancement

The objective of contrast enhancement is to optimize display readability. Adequate contrast enhancement can be achieved in indoor applications through luminous contrast techniques. Luminous contrast is the observed brightness of the illuminated segment compared to the brightness of the surround. Appropriate wavelength filters maximize luminous contrast by reducing the amount of light reflected from the area around the display while transmitting most of the light emitted by the segment. These filters are described further in Application Note 1015.

Chrominance contrast can further improve display readability. Chrominance contrast refers to the color difference between the illuminated segment and the surrounding area. These displays are assembled with a gray package and untinted encapsulating epoxy in the segments to improve chrominance contrast of the ON segments. Additional contrast enhancement in bright ambients may be achieved by using a neutral density gray filter such as Panelgraphic Chromafilter Gray 10, or 3M Light Control Film (louvered film).

HEWLETT PACKARD

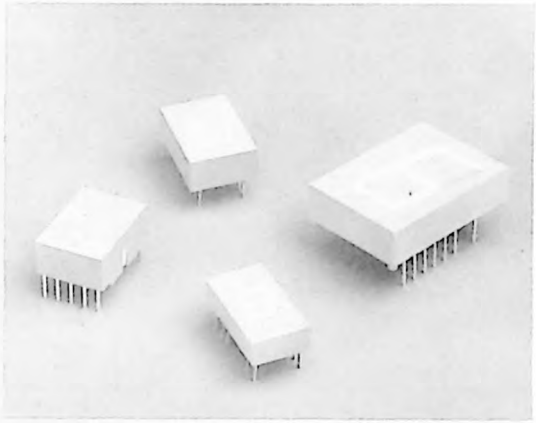
SEVEN SEGMENT DISPLAYS FOR HIGH LIGHT AMBIENT CONDITIONS

HIGH EFFICIENCY RED HDSP-3530/-3730/-5530/-3900 SERIES
YELLOW HDSP-4030/-4130/-5730/-4200 SERIES

TECHNICAL DATA JANUARY 1984

Features

- HIGH LIGHT OUTPUT
  Typical Intensities of up to 7.0 mcd/seg at 100 mA pk 1 of 5 duty factor.
- CAPABLE OF HIGH CURRENT DRIVE
  Excellent for Long Digit String Multiplexing
- FOUR CHARACTER SIZES
  7.6 mm, 10.9 mm, 14.2 mm, and 20.3 mm
- CHOICE OF TWO COLORS
  High Efficiency Red
  Yellow
- EXCELLENT CHARACTER APPEARANCE
  Evenly Lighted Segments
  Wide Viewing Angle
  Grey Body for Optimum Contrast
- CATEGORIZED FOR LUMINOUS INTENSITY; YELLOW CATEGORIZED FOR COLOR
  Use of Like Categories Yields a Uniform Display
- IC COMPATIBLE
- MECHANICALLY RUGGED



Description

The HDSP-3530/-3730/-5530/-3900 and HDSP-4030/-4130/-5730/-4200 are 7.6 mm, 10.9 mm/14.2 mm/20.3 mm high efficiency red and yellow displays designed for use in high light ambient condition. The four sizes of displays allow for viewing distances at 3, 6, 7, and 10 meters. These seven segment displays utilize large junction high efficiency LED chips made from GaAsP on a transparent GaP substrate. Due to the large junction area, these displays can be driven at high peak current levels needed for high ambient conditions or many character multiplexed operation.

These displays have industry standard packages, and pin configurations and ±1 overflow display are available in all four sizes. These numeric displays are ideal for applications such as Automotive and Avionic Instrumentation, Point of Sale Terminals, and Gas Pump.

Devices

Part No. HDSP-	Color	Description	Package Drawing
3530	High Efficiency Red	7.6 mm Common Anode Left Hand Decimal	A
3531		7.6 mm Common Anode Right Hand Decimal	B
3533		7.6 mm Common Cathode Right Hand Decimal	C
3536		7.6 mm Universal Overflow ±1 Right Hand Decimal	D
4030	Yellow	7.6 mm Common Anode Left Hand Decimal	A
4031		7.6 mm Common Anode Right Hand Decimal	B
4033		7.6 mm Common Cathode Right Hand Decimal	C
4036		7.6 mm Universal Overflow ±1 Right Hand Decimal	D

Note: Universal pinout brings the anode and cathode of each segment's LED out to separate pins. See internal diagrams D and H.

Devices

Part No. HDSP	Color	Description	Package Drawing
3730	High Efficiency Red	10.9 mm Common Anode Left Hand Decimal	E
3731		10.9 mm Common Anode Right Hand Decimal	F
3733		10.9 mm Common Cathode Right Hand Decimal	G
3736		10.9 mm Universal Overflow ±1 Right Hand Dec.	H
4130	Yellow	10.9 mm Common Anode Left Hand Decimal	E
4131		10.9 mm Common Anode Right Hand Decimal	F
4133		10.9 mm Common Cathode Right Hand Decimal	G
4136		10.9 mm Universal Overflow ±1 Right Hand Dec.	H
5531	High Efficiency Red	14.2 mm Common Anode Right Hand Decimal	I
5533		14.2 mm Common Cathode Right Hand Decimal	J
5537		14.2 mm Overflow ±1 Common Anode	K
5538		14.2 mm Overflow ±1 Common Cathode	L
5731	Yellow	14.2 mm Common Anode Right Hand Decimal	I
5733		14.2 mm Common Cathode Right Hand Decimal	J
5737		14.2 mm Overflow ±1 Common Anode	K
5738		14.2 mm Overflow ±1 Common Cathode	L
3900	High Efficiency Red	20.3 mm Common Anode Left Hand Decimal	M
3901		20.3 mm Common Anode Right Hand Decimal	N
3903		20.3 mm Common Cathode Right Hand Decimal	O
3905		20.3 mm Common Cathode Left Hand Decimal	P
3906		20.3 mm Universal Overflow ±1 Right Hand Decimal	Q
4200	Yellow	20.3 mm Common Anode Left Hand Decimal	M
4201		20.3 mm Common Anode Right Hand Decimal	N
4203		20.3 mm Common Cathode Right Hand Decimal	O
4205		20.3 mm Common Cathode Left Hand Decimal	P
4206		20.3 mm Universal Overflow ±1 Right Hand Decimal	Q

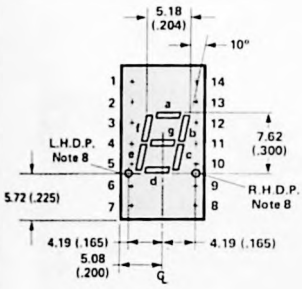
Note: Universal pinout brings the anode and cathode of each segment's LED out to separate pins. See internal diagram Q.

Absolute Maximum Ratings (All Products)

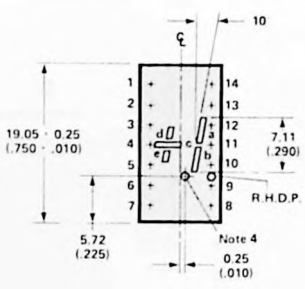
Average Power per Segment or DP (T_A = 25°C)	105 mW
Peak Forward Current per Segment or DP (T_A = 25°C)[1]	135 mA (Pulse Width = 0.16 ms)
DC Forward Current per Segment[2] or DP (T_A = 25°C)	40 mA
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-40°C to +85°C
Reverse Voltage per Segment or DP	3.0V
Lead Solder Temperature (1.59 mm [1/16 inch] below seating plane)	260°C for 3 sec.

Notes:
1. See Figure 1 to establish pulsed operating conditions.
2. Derate maximum DC current above T_A = 25°C at .50 mA/°C per segment, see Figure 2.

Package Dimensions (HDSP-3530/4030 Series)

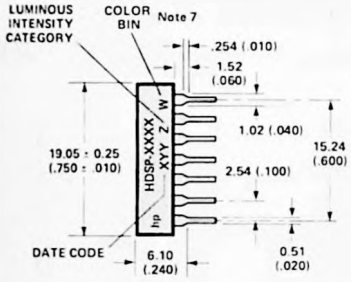


A,B,C

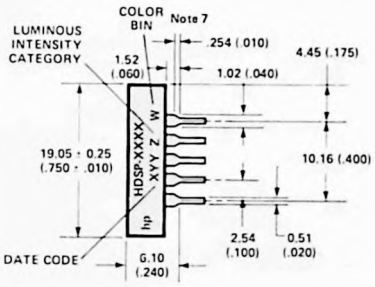


D

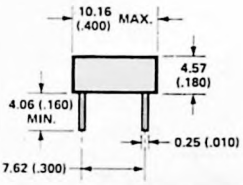
PIN	FUNCTION A -3530/-4030	B -3531/-4031	C -3533/-4033	D -3536/-4036
1	CATHODE-a	CATHODE-a	NO PIN	ANODE-d
2	CATHODE-f	CATHODE-f	CATHODE [6]	NO PIN
3	ANODE[3]	ANODE[3]	ANODE-f	CATHODE-d
4	NO PIN	NO PIN	ANODE-g	CATHODE-c
5	NO PIN	NO PIN	ANODE-e	CATHODE-e
6	CATHODE-dp	NO CONN.[5]	ANODE-d	ANODE-e
7	CATHODE-e	CATHODE-e	NO PIN	ANODE-c
8	CATHODE-d	CATHODE-d	NO PIN	ANODE-dp
9	NO CONN.[5]	CATHODE-dp	CATHODE[6]	NO PIN
10	CATHODE-c	CATHODE-c	ANODE-dp	CATHODE-dp
11	CATHODE-g	CATHODE-g	ANODE-c	CATHODE-b
12	NO PIN	NO PIN	ANODE-b	CATHODE-a
13	CATHODE-b	CATHODE-b	ANODE-a	ANODE-a
14	ANODE[3]	ANODE[3]	NO PIN	ANODE-b



A,B,D
SIDE

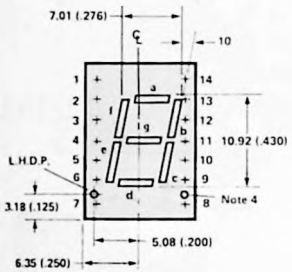


C
SIDE

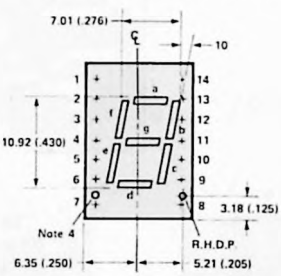


A,B,C,D
END

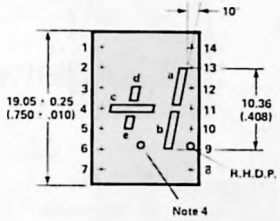
Package Dimensions (HDSP-3730/4130 Series)



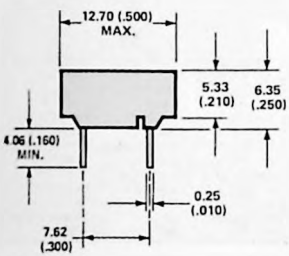
E



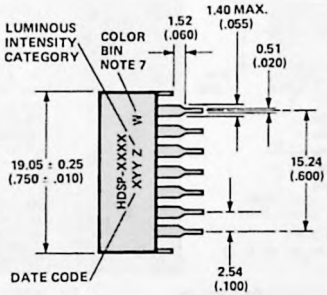
F,G
FRONT VIEW



H



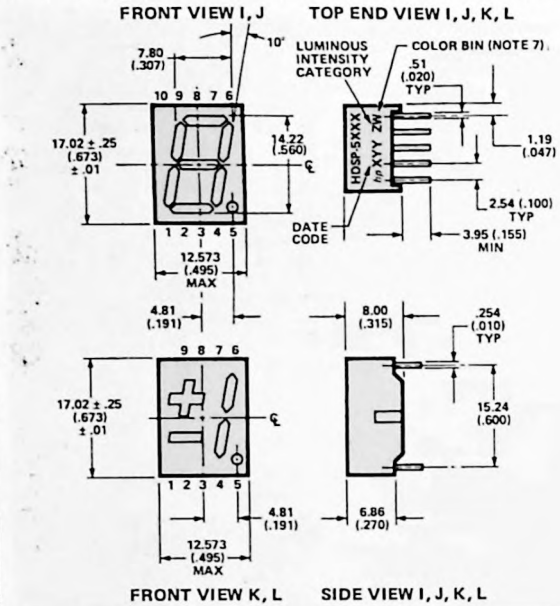
END VIEW



SIDE VIEW

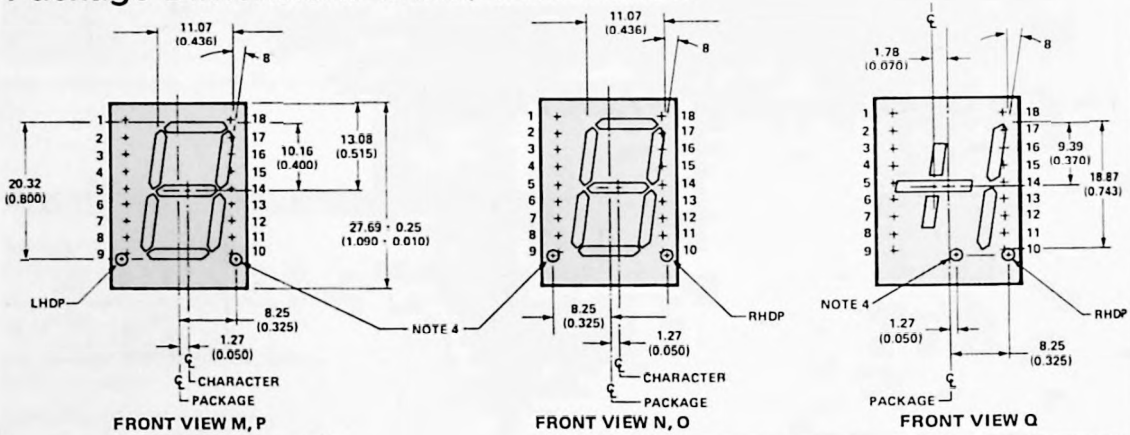
PIN	FUNCTION E -3730/-4130	F -3731/-4131	G -3733/-4133	H -3736/-4136
1	CATHODE-a	CATHODE a	ANODE-a	CATHODE-d
2	CATHODE f	CATHODE-f	ANODE-f	ANODE d
3	ANODE[3]	ANODE[3]	CATHODE[6]	NO PIN
4	NO PIN	NO PIN	NO PIN	CATHODE-c
5	NO PIN	NO PIN	NO PIN	CATHODE-e
6	CATHODE-dp	NO CONN.[5]	NO CONN.[5]	ANODE-e
7	CATHODE-e	CATHODE-e	ANODE-e	ANODE-c
8	CATHODE d	CATHODE-d	ANODE-d	ANODE dp
9	NO CONN.[5]	CATHODE-dp	ANODE dp	CATHODE dp
10	CATHODE-c	CATHODE c	ANODE-c	CATHODE b
11	CATHODE g	CATHODE-g	ANODE-g	CATHODE a
12	NO PIN	NO PIN	NO PIN	NO PIN
13	CATHODE b	CATHODE-b	ANODE-b	ANODE-a
14	ANODE[3]	ANODE[3]	CATHODE[6]	ANODE b

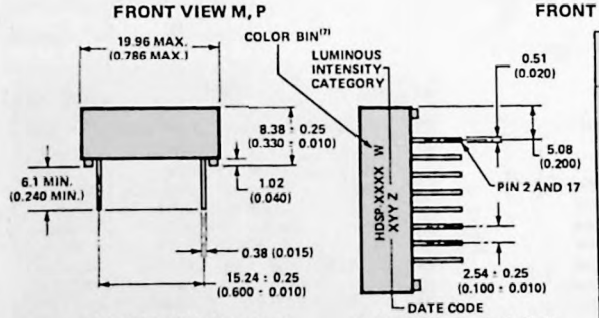
Package Dimensions (5530/5730 Series)



PIN	FUNCTION			
	I 5531	J 5533	K 5537	L 5538
1	CATHODE e	ANODE e	CATHODE c	ANODE c
2	CATHODE d	ANODE d	ANODE c, d	CATHODE c, d
3	ANODE[3]	CATHODE[6]	CATHODE b	ANODE b
4	CATHODE c	ANODE c	ANODE a, b DP	CATHODE a, b, DP
5	CATHODE DP	ANODE DP	CATHODE DP	ANODE DP
6	CATHODE b	ANODE b	CATHODE a	ANODE a
7	CATHODE a	ANODE a	ANODE a, b, DP	CATHODE a, b, DP
8	ANODE[3]	CATHODE[6]	ANODE c, d	CATHODE c, d
9	CATHODE f	ANODE f	CATHODE d	ANODE d
10	CATHODE g	ANODE g	NO PIN[5]	NO PIN[5]

Package Dimensions (3900/4200 Series)



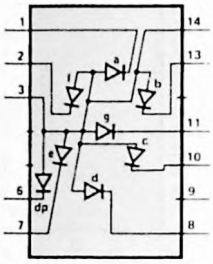


Pin	Function				
	M 3900/4200	N 3901/4201	O 3903/4203	P 3905/4205	Q 3906/4206
1	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN
2	CATHODE a	CATHODE a	ANODE a	ANODE a	CATHODE a
3	CATHODE f	CATHODE f	ANODE f	ANODE f	ANODE d
4	ANODE[3]	ANODE[3]	CATHODE[4]	CATHODE[4]	CATHODE d
5	CATHODE e	CATHODE e	ANODE e	ANODE e	CATHODE c
6	ANODE[3]	ANODE[3]	CATHODE[4]	CATHODE[4]	CATHODE e
7	CATHODE dp	NO CONNEC	NO CONNEC	ANODE dp	ANODE e
8	NO PIN	NO PIN	NO PIN	NO PIN	CATHODE dp
9	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN
10	NO PIN	CATHODE dp	ANODE dp	NO PIN	ANODE dp
11	CATHODE d	CATHODE d	ANODE d	ANODE d	CATHODE dp
12	ANODE[3]	ANODE[3]	CATHODE[4]	CATHODE[4]	CATHODE b
13	CATHODE c	CATHODE c	ANODE c	ANODE c	ANODE b
14	CATHODE g	CATHODE g	ANODE g	ANODE g	ANODE c
15	CATHODE b	CATHODE b	ANODE b	ANODE b	ANODE a
16	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN
17	ANODE[3]	ANODE[3]	CATHODE[4]	CATHODE[4]	CATHODE a
18	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN

NOTES:

1. Dimensions in millimeters and (inches).
2. All untoleranced dimensions are for reference only.
3. Redundant anodes.
4. Unused dp position.
5. See Internal Circuit Diagram.
6. Redundant Cathodes.
7. For HDSP-4030/-4130/-5730/-4200 Series product only.
8. See part number table for LHDP and RHDP designation.

Internal Circuit Diagram (HDSP-3530/4030 Series)



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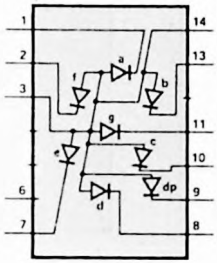
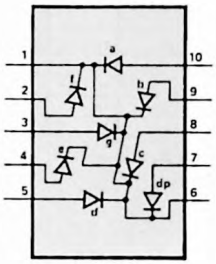


B



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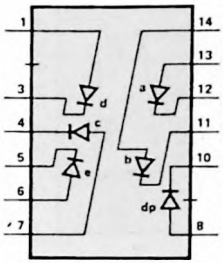
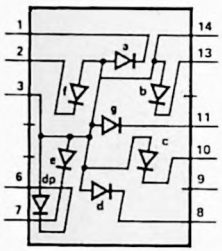


D

Internal Circuit Diagram (HDSP-3730/4130 Series)



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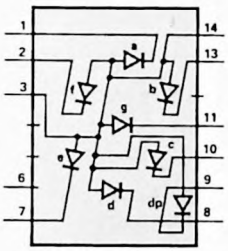

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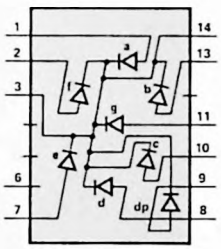

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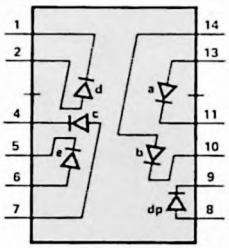
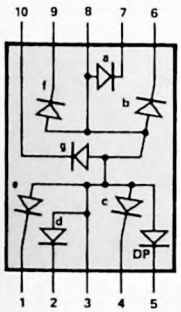


H

Internal Circuit Diagram (HDSP-5530/5730 Series)



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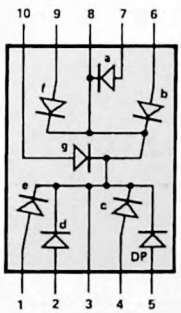

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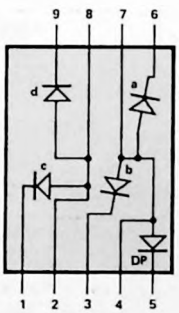
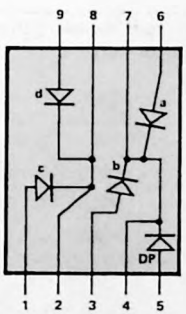
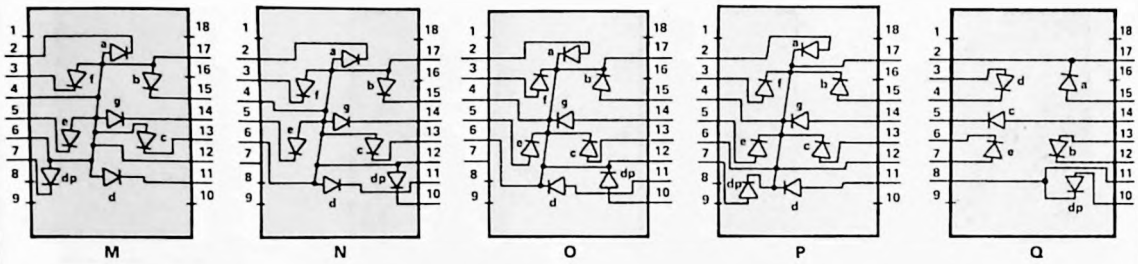


K



L

Internal Circuit Diagram (HDSP-3900/4200 Series)



Electrical/Optical Characteristics at $T_A = 25°C$

Parameter	Symbol	Device HDSP-	Test Condition	Min	Typ	Max	Units
Luminous Intensity/ Segment[9,10] (Digit Average)	I_V	3530 3730 5530 3900	100 mA Pk; 1 of 5 Duty Factor	1500 1500 2200 2200	4500 5000 7000 7000		µcd
		3530 3730 5530 3900	20 mA DC		3100 3500 4800 4800		µcd
		4030 4130 5730 4200	100 mA Pk; 1 of 5 Duty Factor	1500 1500 2200 2200	4500 5000 7000 7000		µcd
		4030 4130 5730 4200	20 mA DC		2200 2500 3400 3400		µcd
Peak Wavelength	λ_{PEAK}	3530/3730/ 5530/3900			635		nm
		4030/4130/ 5730/4200			583		nm
Dominant Wavelength[11,12] (Digit Average)	λ_d	3530/3730/ 5530/3900			626		
		4030/4130/ 5730/4200		581.5	586	592.5	nm
Forward Voltage/Segment or D.P.[13]	V_F	All Devices	I_F = 100 mA		2.6	3.5	V
Reverse Voltage/Segment or D.P.[13,14]	V_R	All Devices	I_R = 100 µA	3.0	25.0		V
Temp. Coeff. of V_F/Seg or D.P.	ΔV_F/°C	All Devices	I_F = 100 mA		-1.1		mV/°C
Thermal Resistance LED Junction-to-pin	$R\theta_{J-PIN}$	3530/4030/ 3730/4130			282		°C/W/Seg
		5530/5730			345		°C/W/Seg
		3900/4200			375		°C/W/Seg

Notes:

9. Case temperature of the device immediately prior to the intensity measurement is 25°C.
10. The digits are categorized for luminous intensity with the intensity category designated by a letter on the side of the package.
11. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and is that single wavelength which defines the color of the device.
12. The yellow displays are categorized as to dominant wavelength with the category designated by a number adjacent to the intensity category letter.
13. Quality level for electrical characteristics is 1000 parts per million.
14. Typical specification for reference only. Do not exceed absolute maximum ratings.

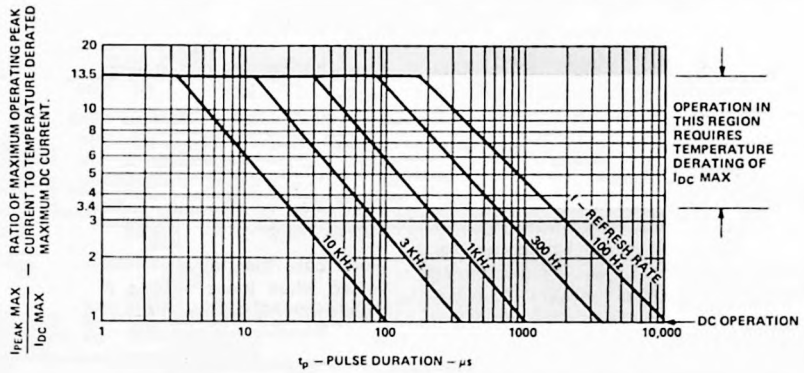


Figure 1. Maximum Allowed Peak Current vs. Pulse Duration

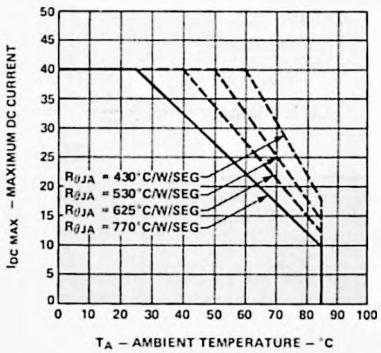


Figure 2. Maximum Allowable DC Current per Segment vs. Ambient Temperature

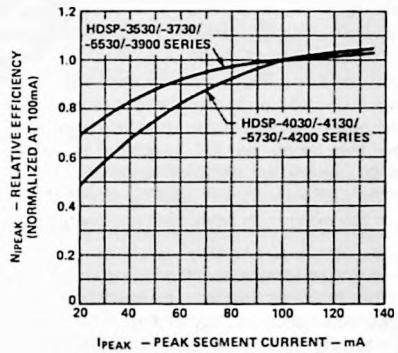


Figure 3. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Segment Current

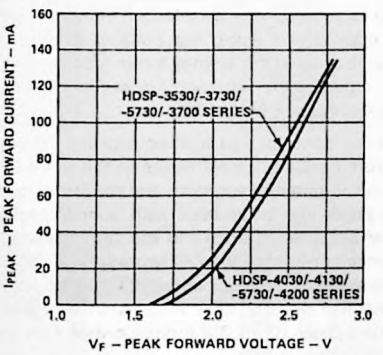


Figure 4. Peak Forward Segment Current vs. Peak Forward Voltage

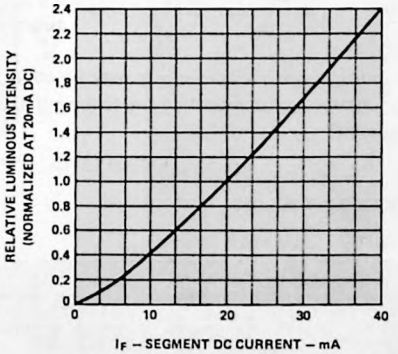


Figure 5. Relative Luminous Intensity vs. DC Forward Current

Electrical

These display devices are composed of eight light emitting diodes, with light from each LED optically stretched to form individual segments and a decimal point.

The devices utilize LED chips which are made from GaAsP on a transparent GaP substrate.

These display devices are designed for strobed operation. The typical forward voltage values, scaled from Figure 4 should be used for calculating the current limiting resistor value and typical power dissipation. Expected maximum V_F values, for the purpose of driver circuit design and maximum power dissipation, may be calculated using the following V_F MAX models:

V_F MAX = 2.15V + I_{PEAK} (13.5Ω)
For: $I_F \geq 30$ mA

V_F MAX = 1.9V + I_{DC} (21.8Ω)
For: 10 mA ≤ I_F ≤ 30 mA

Temperature derated strobed operating conditions are obtained from Figures 1 and 2. Figure 1 relates pulse duration (t_p), refresh rate (f), and the ratio of maximum peak current to maximum dc current (I_{PEAK} MAX/I_{DC} MAX). Figure 2 presents the maximum allowed dc current vs. ambient temperature. Figure 1 is based on the principle that the peak junction temperature for pulsed operation at a specified peak current, pulse duration and refresh rate should be the same as the junction temperature at maximum DC operation. Refresh rates of 1 kHz or faster minimize the pulsed junction heating effect of the device resulting in the maximum possible time average luminous intensity.

The time average luminous intensity can be calculated knowing the average forward current and relative efficiency characteristic, ηI_{PEAK}, of Figure 3. Time average luminous intensity for a device case temperature of 25° C, I_V (25° C), is calculated as follows:

$$I_V\,(25°\,C) = \left[\frac{I_{AVG}}{20\text{ mA}}\right]\left[\eta_{IPEAK}\right]\left[I_V \text{ DATA SHEET}\right]$$

Example: For HDSP-4030 series

η_{IPEAK} = 1.00 at I_{PEAK} = 100 mA. For DF = 1/5:

$$I_V\,(25°\,C) = \left[\frac{20\text{ mA}}{20\text{ mA}}\right][1.00][4.5\text{ mcd}] = 4.5\text{ mcd/segment}$$

The time average luminous intensity may be adjusted for operating junction temperature by the following exponential equation:

$$I_V\,(T_J) = I_V\,(25°\,C)\; e^{[k(T_J + 25°\,C)]}$$

where $T_J = T_A + P_D \cdot R\theta_{J-A}$

DEVICE	K
-3530/-3730/-5530/-3900	-0.0131/° C
-4030/-4130/-5730/-4200	-0.0112/° C

Mechanical

These devices are constructed utilizing a lead frame in a standard DIP package. The LED dice are attached directly to the lead frame. Therefore, the cathode leads are the direct thermal and mechanical stress paths to the LED dice. The absolute maximum allowed junction temperature, T_J MAX, is 105° C. The maximum power ratings have been established so that the worst case V_F device does not exceed this limit.

Worst case thermal resistance pin-to-ambient is 400° C/W/Seg when these devices are soldered into minimum trace width PC boards. When installed in a PC board that provides $R\theta_{PIN-A}$ less than 400° C/W/Seg these displays may be operated at higher average currents as shown in Figure 2.

Optical

The radiation pattern for these devices is approximately Lambertian. The luminous sterance may be calculated using one of the two following formulas.

$$L_V(\text{cd/m}^2) = \frac{I_V(\text{cd})}{A(\text{m}^2)}$$

$$L_V(\text{footlamberts}) = \frac{\pi I_V(\text{cd})}{A(\text{ft}^2)}$$

DEVICE	AREA/SEG. mm^2	AREA/SEG. $IN.^2$
-3530/-4030	2.5	.0039
-3730/-4130	4.4	.0068
-5530/-5730	8.8	.0137
-3900/-4200	14.9	.0231

Contrast Enhancement

The objective of contrast enhancement is to optimize display readability. Adequate contrast enhancement can be achieved in indoor applications through luminous contrast techniques. Luminous contrast is the observed brightness of the illuminated segment compared to the brightness of the surround. Appropriate wavelength filters maximize luminous contrast by reducing the amount of light reflected from the area around the display while transmitting most of the light emitted by the segment. These filters are described further in Application Note 1015.

Chrominance contrast can further improve display readability. Chrominance contrast refers to the color difference between the illuminated segment and the surrounding area. These displays are assembled with a gray package and untinted encapsulating epoxy in the segments to improve chrominance contrast of the ON segments. Additional contrast enhancement in bright ambients may be achieved by using a neutral density gray filter such as Panelgraphic Chromafilter Gray 10, or 3M Light Control Film (louvered film).

HEWLETT PACKARD

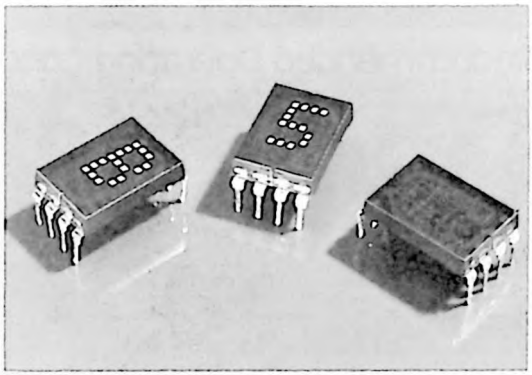
HEXADECIMAL AND NUMERIC INDICATORS

5082-7300
5082-7302
5082-7304
5082-7340

TECHNICAL DATA JANUARY 1984

Features

- NUMERIC 5082-7300/-7302
  - 0-9, Test State, Minus Sign, Blank States
  - Decimal Point
    - 7300 Right Hand D.P.
    - 7302 Left Hand D.P.
- HEXADECIMAL 5082-7340
  - 0-9, A-F, Base 16 Operation
  - Blanking Control, Conserves Power
  - No Decimal Point
- DTL/TTL COMPATIBLE
- INCLUDES DECODER/DRIVER WITH 5 BIT MEMORY
  - 8421 Positive Logic Input
- 4 x 7 DOT MATRIX ARRAY
  - Shaped Character, Excellent Readibility
- STANDARD .600 INCH x .400 INCH DUAL-IN-LINE PACKAGE INCLUDING CONTRAST FILTER
- CATEGORIZED FOR LUMINOUS INTENSITY
  - Assures Uniformity of Light Output from Unit to Unit within a Single Category



Description

The HP 5082-7300 series solid state numeric and hexadecimal indicators with on-board decoder/driver and memory provide a reliable, low-cost method for displaying digital information.

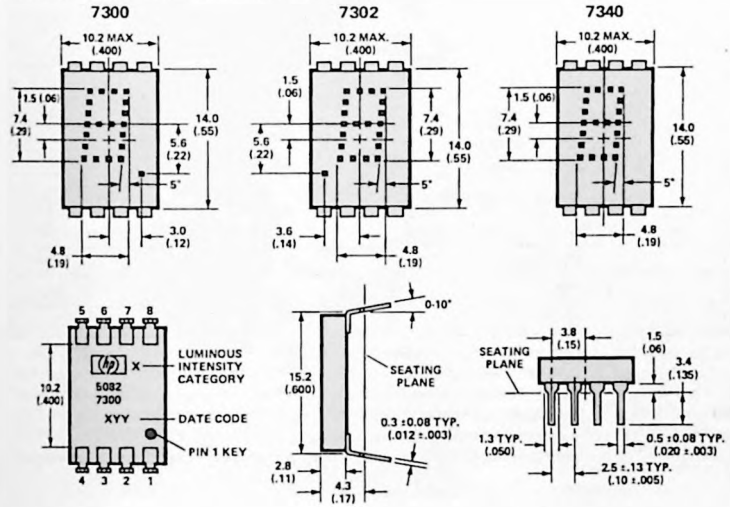
The 5082-7300 numeric indicator decodes positive 8421 BCD logic inputs into characters 0-9, a "-" sign, a test pattern, and four blanks in the invalid BCD states, The unit employs a right-hand decimal point. Typical applications include point-of-sale terminals, instrumentation, and computer systems.

The 5082-7302 is the same as the 5082-7300, except that the decimal point is located on the left-hand side of the digit.

The 5082-7340 hexadecimal indicator decodes positive 8421 logic inputs into 16 states, 0-9 and A-F. In place of the decimal point an input is provided for blanking the display (all LED's off), without losing the contents of the memory. Applications include terminals and computer systems using the base-16 character set.

The 5082-7304 is a (± 1.) overrange character, including decimal point, used in instrumentation applications.

Package Dimensions



PIN	FUNCTION	
	5082-7300 and 7302 Numeric	5082-7340 Hexadecimal
1	Input 2	Input 2
2	Input 4	Input 4
3	Input 8	Input 8
4	Decimal point	Blanking control
5	Latch enable	Latch enable
6	Ground	Ground
7	V_{cc}	V_{cc}
8	Input 1	Input 1

NOTES:
1. Dimensions in millimetres and (inches).
2. Unless otherwise specified, the tolerance on all dimensions is ±.38mm (±.015")
3. Digit center line is ±.25mm (±.01") from package center line.

Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Unit
Storage temperature, ambient	T_S	−40	+100	°C
Operating temperature, case [1,2]	T_C	−20	+85	°C
Supply voltage [3]	V_{CC}	−0.5	+7.0	V
Voltage applied to input logic, dp and enable pins	V_I, V_{DP}, V_E	−0.5	+7.0	V
Voltage applied to blanking input [7]	V_B	−0.5	V_{CC}	V
Maximum solder temperature at 1.59mm (.062 inch) below seating plane; t ⩽ 5 seconds			230	°C

Recommended Operating Conditions

Description	Symbol	Min.	Nom.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Operating temperature, case	T_C	-20		+85	°C
Enable Pulse Width	t_W	120			nsec
Time data must be held before positive transition of enable line	t_{SETUP}	50			nsec
Time data must be held after positive transition of enable line	t_{HOLD}	50			nsec
Enable pulse rise time	t_{TLH}			200	nsec

Electrical/Optical Characteristics (T_C = -20° C to +85° C, unless otherwise specified).

Description	Symbol	Test Conditions	Min.	Typ.[4]	Max.	Unit
Supply Current	I_{CC}	V_{CC}=5.5V (Numeral		112	170	mA
Power dissipation	P_T	5 and dp lighted)		560	935	mW
Luminous intensity per LED (Digit average) [5,6]	I_v	V_{CC}=5.0V, T_C=25° C	32	70		μcd
Logic low-level input voltage	V_{IL}	V_{CC}=4.5V			0.8	V
Logic high-level input voltage	V_{IH}		2.0			V
Enable low-voltage; data being entered	V_{EL}				0.8	V
Enable high-voltage; data not being entered	V_{EH}		2.0			V
Blanking low-voltage; display not blanked [7]	V_{BL}				0.8	V
Blanking high-voltage; display blanked [7]	V_{BH}		3.5			V
Blanking low-level input current [7]	I_{BL}	V_{CC}=5.5V, V_{BL}=0.8V			20	μA
Blanking high-level input current [7]	I_{BH}	V_{CC}=5.5V, V_{BH}=4.5V			2.0	mA
Logic low-level input current	I_{IL}	V_{CC}=5.5V, V_{IL}=0.4V			−1.6	mA
Logic high-level input current	I_{IH}	V_{CC}=5.5V, V_{IH}=2.4V			+250	μA
Enable low-level input current	I_{EL}	V_{CC}=5.5V, V_{EL}=0.4V			−1.6	mA
Enable high-level input current	I_{EH}	V_{CC}=5.5V, V_{EH}=2.4V			+250	μA
Peak wavelength	λ_{PEAK}	T_C=25° C		655		nm
Dominant Wavelength [8]	λ_d	T_C=25° C		640		nm
Weight				0.8		gm

Notes: 1. Nominal thermal resistance of a display mounted in a socket which is soldered into a printed circuit board: θ_{JA}=50° C/W; θ_{JC}=15° C/W; 2. θ_{CA} of a mounted display should not exceed 35° C/W for operation up to T_C = +85° C. 3. Voltage values are with respect to device ground, pin 6. 4. All typical values at V_{CC}=5.0 Volts, T_C=25° C. 5. These displays are categorized for luminous intensity with the intensity category designated by a letter located on the back of the display contiguous with the Hewlett-Packard logo marking. 6. The luminous intensity at a specific case temperature, $I_v(T_C)$ may be calculated from this relationship: $I_v(T_C)=I_v\ (25°C)\ e^{[-.0188/°C\ (T_C-25°C)]}$ 7. Applies only to 7340. 8. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.

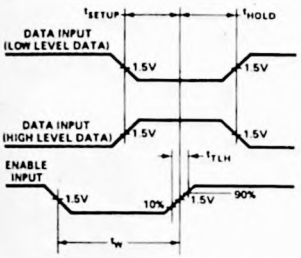


Figure 1. Timing Diagram of 5082-7300 Series Logic.

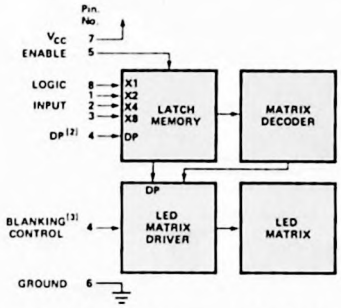


Figure 2. Block Diagram of 5082-7300 Series Logic.

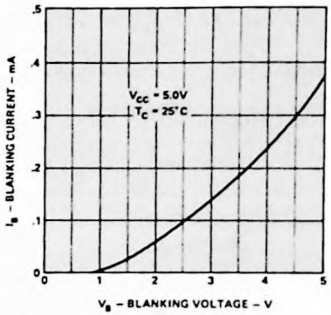


Figure 3. Typical Blanking Control Current vs. Voltage for 5082-7340.

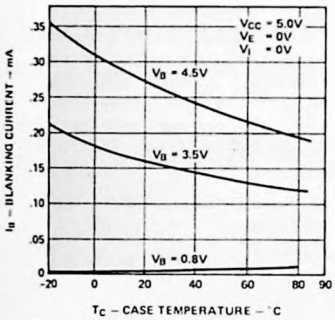


Figure 4. Typical Blanking Control Input Current vs. Temperature 5082-7340.

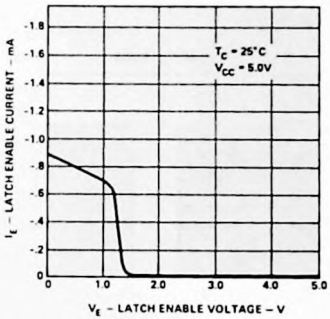


Figure 5. Typical Latch Enable Input Current vs. Voltage for the 5082-7300 Series Devices.

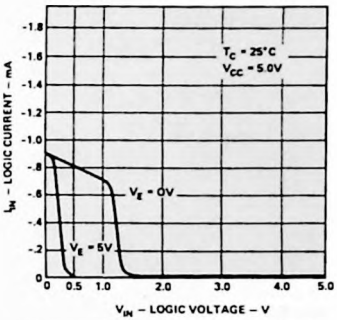


Figure 6. Typical Logic and Decimal Point Input Current vs. Voltage for the 5082-7300 Series Devices. Decimal Point Applies to 5082-7300 and -7302 Only.

TRUTH TABLE					
BCD DATA[1]				5082-7300/7302	5082-7340
X_8	X_4	X_2	X_1		
L	L	L	L	0	0
L	L	L	H	1	1
L	L	H	L	2	2
L	L	H	H	3	3
L	H	L	L	4	4
L	H	L	H	5	5
L	H	H	L	6	6
L	H	H	H	7	7
H	L	L	L	8	8
H	L	L	H	9	9
H	L	H	L	8	A
H	L	H	H	(BLANK)	B
H	H	L	L	(BLANK)	C
H	H	L	H	----	D
H	H	H	L	(BLANK)	E
H	H	H	H	(BLANK)	F
DECIMAL PT.[2]		ON			V_{DP} = L
		OFF			V_{DP} = H
ENABLE[1]		LOAD DATA			V_E = L
		LATCH DATA			V_E = H
BLANKING[3]		DISPLAY ON			V_B = L
		DISPLAY OFF			V_B = H

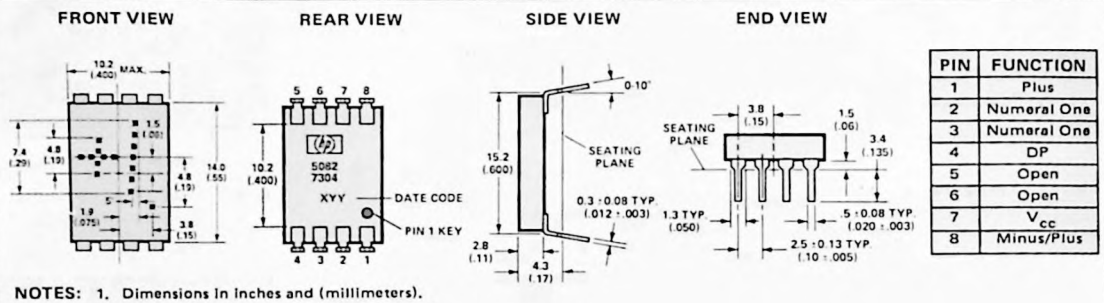
Notes:

1. H = Logic High; L = Logic Low. With the enable input at logic high changes in BCD input logic levels or D.P. input have no effect upon display memory, displayed character, or D.P.
2. The decimal point input, DP, pertains only to the 5082-7300 and 5082-7302 displays.
3. The blanking control input, B, pertains only to the 5082-7340 hexadecimal display. Blanking input has no effect upon display memory.

Solid State Over Range Character

For display applications requiring a ±, 1, or decimal point designation, the 5082-7304 over range character is available. This display module comes in the same package as the 5082-7300 series numeric indicator and is completely compatible with it.

Package Dimensions



PIN	FUNCTION
1	Plus
2	Numeral One
3	Numeral One
4	DP
5	Open
6	Open
7	V_{cc}
8	Minus/Plus

NOTES: 1. Dimensions in inches and (millimeters).
2. Unless otherwise specified, the tolerance on all dimensions is ±.015 inches. (± .38mm)

5082–7304

TRUTH TABLE FOR 5082-7304

CHARACTER	PIN			
	1	2,3	4	8
+	H	X	X	H
–	L	X	X	H
1	X	H	X	X
Decimal Point	X	X	H	X
Blank	L	L	L	L

NOTES: L: Line switching transistor in Fig. 7 cutoff.
H: Line switching transistor in Fig. 7 saturated.
X: 'don't care'

TYPICAL DRIVING CIRCUIT FOR 5082-7304.

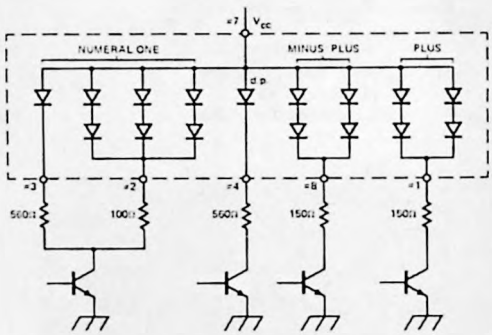


Figure 7.

Absolute Maximum Ratings

DESCRIPTION	SYMBOL	MIN	MAX	UNIT
Storage temperature, ambient	T_s	-40	+100	°C
Operating temperature, case	T_C	-20	+85	°C
Forward current, each LED	I_F		10	mA
Reverse voltage, each LED	V_R		4	V

RECOMMENDED OPERATING CONDITIONS

	SYMBOL	MIN	NOM	MAX	UNIT
LED supply voltage	V_{cc}	4.5	5.0	5.5	V
Forward current, each LED	I_F		5.0	10	mA

NOTE:
LED current must be externally limited. Refer to figure 7 for recommended resistor values.

Electrical/Optical Characteristics (T_C = -20°C TO +85°C, UNLESS OTHERWISE SPECIFIED)

DESCRIPTION	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Forward Voltage per LED	V_F	I_F = 10 mA		1.6	2.0	V
Power dissipation	P_T	I_F = 10 mA all diodes lit		250	320	mW
Luminous Intensity per LED (digit average)	I_v	I_F = 6 mA T_C = 25°C	32	70		µcd
Peak wavelength	λ_{peak}	T_C = 25°C		655		nm
Dominant Wavelength	λ_d	T_C = 25°C		640		nm
Weight				0.8		gm

HEWLETT PACKARD

HEXADECIMAL AND NUMERIC DISPLAYS FOR INDUSTRIAL APPLICATIONS

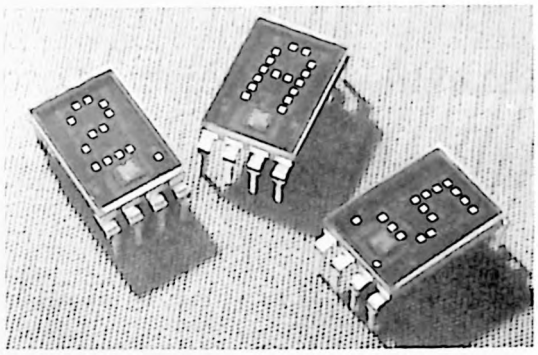
5082-7356
5082-7357
5082-7358
5082-7359

TECHNICAL DATA JANUARY 1984

SOLID STATE DISPLAYS

Features

- CERAMIC/GLASS PACKAGE
- ADDED RELIABILITY
- NUMERIC 5082-7356/-7357
  0-9, Test State, Minus Sign, Blank States
  Decimal Point
  7356 Right Hand D.P.
  7357 Left Hand D.P.
- HEXADECIMAL 5082-7359
  0-9, A-F, Base 16 Operation
  Blanking Control, Conserves Power
  No Decimal Point
- TTL COMPATIBLE
- INCLUDES DECODER/DRIVER WITH 5 BIT MEMORY
  8421 Positive Logic Input and Decimal Point
- 4 x 7 DOT MATRIX ARRAY
  Shaped Character, Excellent Readability
- STANDARD DUAL-IN-LINE PACKAGE
  15.2mm x 10.2mm (.6 inch x .4 inch)
- CATEGORIZED FOR LUMINOUS INTENSITY
  Assures Uniformity of Light Output from Unit to Unit within a Single Category



Description

The HP 5082-7350 series solid state numeric and hexadecimal indicators with on-board decoder/driver and memory provide 7.4mm (0.29 inch) displays for use in adverse industrial environments.

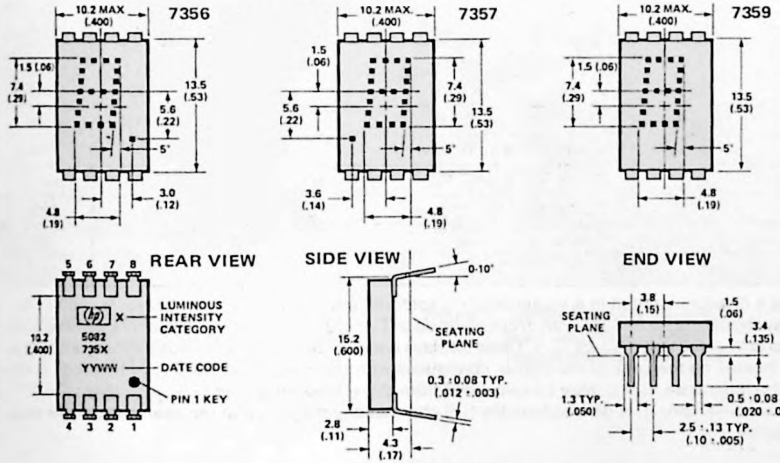
The 5082-7356 numeric indicator decodes positive 8421 BCD logic inputs into characters 0-9, a " −" sign, a test pattern, and four blanks in the invalid BCD states. The unit employs a right-hand decimal point. Typical applications include control systems, instrumentation, communication systems and transportation equipment.

The 5082-7357 is the same as the 5082-7356 except that the decimal point is located on the left-hand side of the digit.

The 5082-7359 hexadecimal indicator decodes positive 8421 logic inputs into 16 states, 0-9 and A-F. In place of the decimal point an input is provided for blanking the display (all LED's off), without losing the contents of the memory. Applications include terminals and computer systems using the base-16 character set.

The 5082-7358 is a "±1." overrange display, including a right hand decimal point.

Package Dimensions



PIN	FUNCTION	
	5082-7356 AND 7357 NUMERIC	5082-7359 HEXA-DECIMAL
1	Input 2	Input 2
2	Input 4	Input 4
3	Input 8	Input 8
4	Decimal point	Blanking control
5	Latch enable	Latch enable
6	Ground	Ground
7	V_{CC}	V_{CC}
8	Input 1	Input 1

NOTES:
1. Dimensions in millimetres and (inches).
2. Unless otherwise specified, the tolerance on all dimensions is ±.38mm (±.015")
3. Digit center line is ±.25mm (±.01") from package center line.

Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Unit
Storage temperature, ambient	T_S	−65	+125	°C
Operating temperature, ambient [1,2]	T_A	−55	+100	°C
Supply voltage [3]	V_{CC}	−0.5	+7.0	V
Voltage applied to input logic, dp and enable pins	V_I,V_{DP},V_E	−0.5	+7.0	V
Voltage applied to blanking input [7]	V_B	−0.5	V_{CC}	V
Maximum solder temperature at 1.59mm (.062 inch) below seating plane; t ≤ 5 seconds			260	°C

Recommended Operating Conditions

Description	Symbol	Min.	Nom.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Operating temperature, ambient	T_A	-20		+70	°C
Enable Pulse Width	t_W	100			nsec
Time data must be held before positive transition of enable line	t_{SETUP}	50			nsec
Time data must be held after positive transition of enable line	t_{HOLD}	50			nsec
Enable pulse rise time	t_{TLH}			200	nsec

Electrical/Optical Characteristics (T_A = -20° C to +70° C, Unless Otherwise Specified)

Description	Symbol	Test Conditions	Min.	Typ.[4]	Max.	Unit
Supply Current	I_{CC}	V_{CC}=5.5V (Numeral		112	170	mA
Power dissipation	P_T	5 and dp lighted)		560	935	mW
Luminous intensity per LED (Digit average) [5,6]	I_v	V_{CC}=5.0V, T_A=25° C	40	85		µcd
Logic low-level input voltage	V_{IL}	V_{CC}=4.5V			0.8	V
Logic high-level input voltage	V_{IH}		2.0			V
Enable low-voltage; data being entered	V_{EL}				0.8	V
Enable high-voltage; data not being entered	V_{EH}		2.0			V
Blanking low-voltage; display not blanked [7]	V_{BL}				0.8	V
Blanking high-voltage; display blanked [7]	V_{BH}		3.5			V
Blanking low-level input current [7]	I_{BL}	V_{CC}=5.5V, V_{BL}=0.8V			50	µA
Blanking high-level input current [7]	I_{BH}	V_{CC}=5.5V, V_{BH}=4.5V			1.0	mA
Logic low-level input current	I_{IL}	V_{CC}=5.5V, V_{IL}=0.4V			−1.6	mA
Logic high-level input current	I_{IH}	V_{CC}=5.5V, V_{IH}=2.4V			+100	µA
Enable low-level input current	I_{EL}	V_{CC}=5.5V, V_{EL}=0.4V			−1.6	mA
Enable high-level input current	I_{EH}	V_{CC}=5.5V, V_{EH}=2.4V			+130	µA
Peak wavelength	λ_{PEAK}	T_A=25° C		655		nm
Dominant Wavelength [8]	λ_d	T_A=25° C		640		nm
Weight				1.0		gm

Notes: 1. Nominal thermal resistance of a display mounted in a socket which is soldered into a printed circuit board: Θ_{JA}=50° C/W; Θ_{JC}=15° C/W; 2. Θ_{CA} of a mounted display should not exceed 35° C/W for operation up to T_A=+100° C. 3. Voltage values are with respect to device ground, pin 6. 4. All typical values at V_{CC}=5.0 Volts, T_A=25° C. 5. These displays are categorized for luminous intensity with the intensity category designated by a letter located on the back of the display contiguous with the Hewlett-Packard logo marking. 6. The luminous intensity at a specific ambient temperature, $I_V(T_A)$, may be calculated from this relationship: $I_V(T_A)=I_{V(25°C)}(.985)^{[T_A-25°C]}$ 7. Applies only to 7359. 8. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.

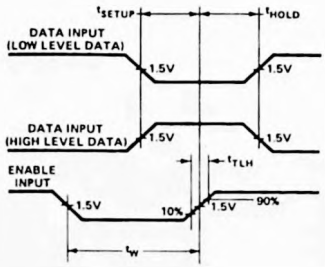


Figure 1. Timing Diagram of 5082-7350 Series Logic.

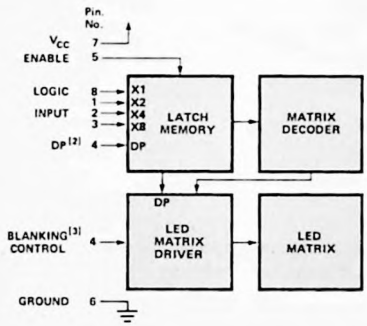


Figure 2. Block Diagram of 5082-7350 Series Logic.

TRUTH TABLE					
BCD DATA[1]				5082-7356/7357	5082-7359
X_8	X_4	X_2	X_1		
L	L	L	L	0	0
L	L	L	H	1	1
L	L	H	L	2	2
L	L	H	H	3	3
L	H	L	L	4	4
L	H	L	H	5	5
L	H	H	L	6	6
L	H	H	H	7	7
H	L	L	L	8	8
H	L	L	H	9	9
H	L	H	L	A	A
H	L	H	H	(BLANK)	B
H	H	L	L	(BLANK)	C
H	H	L	H	—	D
H	H	H	L	(BLANK)	E
H	H	H	H	(BLANK)	F
DECIMAL PT.[2]			ON		V_{DP} = L
			OFF		V_{DP} = H
ENABLE[1]			LOAD DATA		V_E = L
			LATCH DATA		V_E = H
BLANKING[3]			DISPLAY-ON		V_B = L
			DISPLAY-OFF		V_B = H

Notes:
1. H = Logic High; L = Logic Low. With the enable input at logic high changes in BCD input logic levels or D.P. input have no effect upon display memory, displayed character, or D.P.
2. The decimal point input, DP, pertains only to the 5082-7356 and 5082-7357 displays.
3. The blanking control input, B, pertains only to the 5082-7359 hexadecimal display. Blanking input has no effect upon display memory.

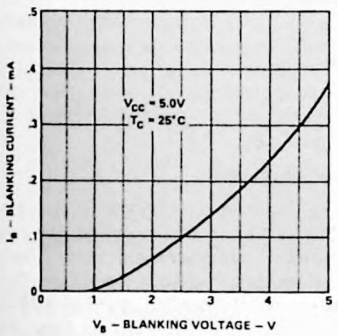


Figure 3. Typical Blanking Control Current vs. Voltage for 5082-7359.

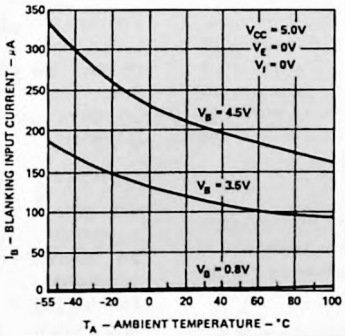


Figure 4. Typical Blanking Control Input Current vs. Ambient Temperature for 5082-7359.

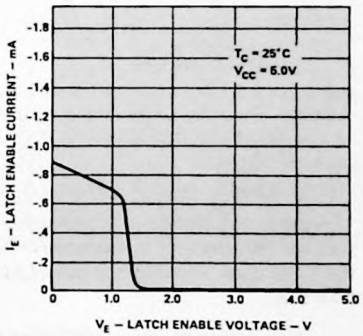


Figure 5. Typical Latch Enable Input Current vs. Voltage.

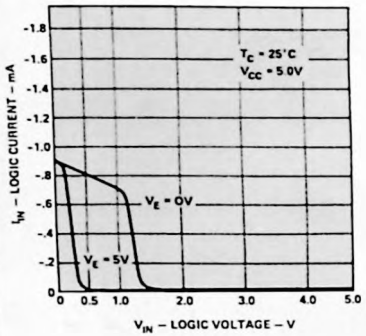


Figure 6. Typical Logic and Decimal Point Input Current vs. Voltage.

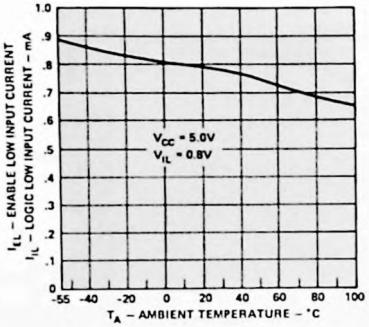


Figure 7. Typical Logic and Enable Low Input Current vs. Ambient Temperature.

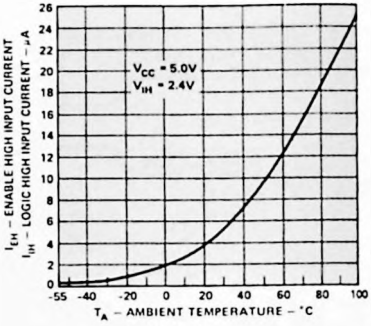


Figure 8. Typical Logic and Enable High Input Current vs. Ambient Temperature.

Operational Considerations

ELECTRICAL

The 5082-7350 series devices use a modified 4 x 7 dot matrix of light emitting diodes (LED's) to display decimal/hexadecimal numeric information. The LED's are driven by constant current drivers. BCD information is accepted by the display memory when the enable line is at logic low and the data is latched when the enable is at logic high. To avoid the latching of erroneous information, the enable pulse rise time should not exceed 200 nanoseconds. Using the enable pulse width and data setup and hold times listed in the Recommended Operating Conditions allows data to be clocked into an array of displays at a 6.7MHz rate.

The blanking control input on the 5082-7395 display blanks (turns off) the displayed hexadecimal information without disturbing the contents of display memory. The display is blanked at a minimum threshold level of 3.5 volts. This may be easily achieved by using an open collector TTL gate and a pull-up resistor. For example, (1/6) 7416 hexinverter buffer/driver and a 120 ohm pull-up resistor will provide sufficient drive to blank eight displays. The size of the blanking pull-up resistor may be calculated from the following formula, where N is the number of digits:

$$R_{blank} = (V_{CC} - 3.5V)/[N\ (1.0mA)]$$

The decimal point input is active low true and this data is latched into the display memory in the same fashion as is the BCD data. The decimal point LED is driven by the on-board IC.

MECHANICAL

These displays are designed for use in adverse industrial environments.

These displays may be mounted by soldering directly to a printed circuit board or inserted into a socket. The lead-to-lead pin spacing is 2.54mm (0.100 inch) and the lead row spacing is 15.24mm (0.600 inch). These displays may be end stacked with 2.54mm (0.100 inch) spacing between outside pins of adjacent displays. Sockets such as Augat 324-AG2D (3 digits) or Augat 508-AG8D (one digit, right angle mounting) may be used.

The primary thermal path for power dissipation is through the device leads. Therefore, to insure reliable operation up to an ambient temperature of +100° C, it is important to maintain a case-to-ambient thermal resistance of less than 35° C/watt as measured on top of display pin 3.

Post solder cleaning may be accomplished using water, Freon/alcohol mixtures formulated for vapor cleaning processing (up to 2 minutes in vapors at boiling) or Freon/alcohol mixtures formulated for room temperature cleaning. Suggested solvents: Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15.

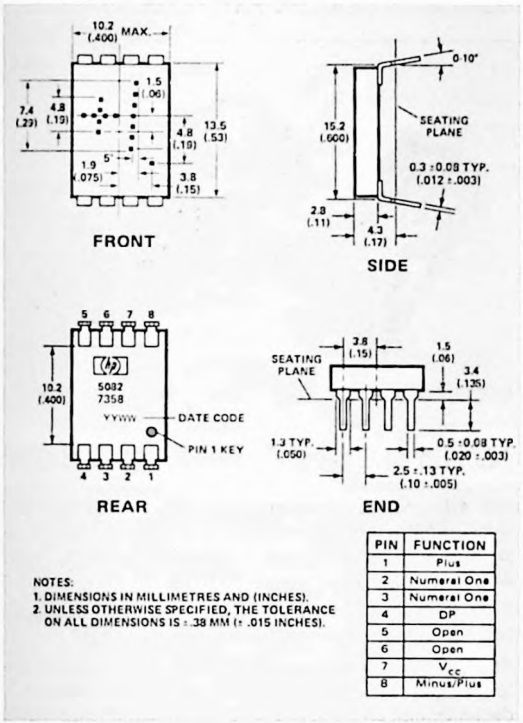
CONTRAST ENHANCEMENT

The 5082-7350 displays have been designed to provide the maximum posible ON/OFF contrast when placed behind an appropriate contrast enhancement filter. Some suggested filters are Panelgraphic Ruby Red 60 and Dark Red 63, SGL Homalite H100-1605, 3M Light Control Film and Polaroid HRCP Red Circular Polarizing Filter. For further information see Hewlett-Packard Application Note 964.

Solid State Over Range Character

For display applications requiring a ±, 1, or decimal point designation, the 5082-7358 over range character is available. This display module comes in the same package as the 5082-7350 series numeric indicator and is completely compatible with it.

Package Dimensions



PIN	FUNCTION
1	Plus
2	Numeral One
3	Numeral One
4	DP
5	Open
6	Open
7	V_{CC}
8	Minus/Plus

NOTES:
1. DIMENSIONS IN MILLIMETRES AND (INCHES).
2. UNLESS OTHERWISE SPECIFIED, THE TOLERANCE ON ALL DIMENSIONS IS ±.38 MM (± .015 INCHES).

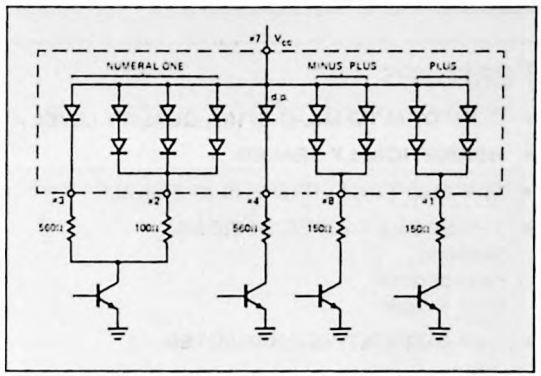


Figure 9. Typical Driving Circuit.

TRUTH TABLE

CHARACTER	PIN			
	1	2,3	4	8
+	H	X	X	H
−	L	X	X	H
1	X	H	X	X
Decimal Point	X	X	H	X
Blank	L	L	L	L

NOTES: L: Line switching transistor in Figure 9 cutoff.
H: Line switching transistor in Figure 9 saturated.
X: 'Don't care'

Electrical/Optical Characteristics

5082-7358 (T_A = -20°C to 70°C, Unless Otherwise Specified)

DESCRIPTION	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Forward Voltage per LED	V_F	I_F = 10 mA		1.6	2.0	V
Power dissipation	P_T	I_F = 10 mA all diodes lit		280	320	mW
Luminous Intensity per LED (digit average)	I_v	I_F = 6 mA T_C = 25°C	40	85		µcd
Peak wavelength	λ_{peak}	T_C = 25°C		655		nm
Dominant Wavelength	λ_d	T_C = 25°C		640		nm
Weight				1.0		gm

Recommended Operating Conditions

	SYMBOL	MIN	NOM	MAX	UNIT
LED supply voltage	V_{CC}	4.5	5.0	5.5	V
Forward current, each LED	I_F		5.0	10	mA

NOTE:
LED current must be externally limited. Refer to Figure 9 for recommended resistor values.

Absolute Maximum Ratings

DESCRIPTION	SYMBOL	MIN.	MAX.	UNIT
Storage temperature, ambient	T_S	-65	+125	°C
Operating temperature, ambient	T_A	-55	+100	°C
Forward current, each LED	I_F		10	mA
Reverse voltage, each LED	V_R		4	V

HEWLETT PACKARD

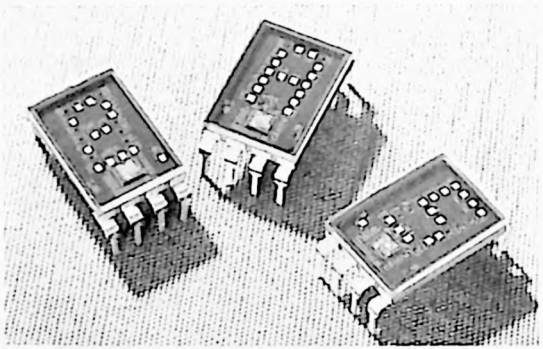
HERMETIC, HEXADECIMAL AND NUMERIC DISPLAYS FOR HIGH RELIABILITY APPLICATIONS

4N51 (5082-7391)/4N51TXV/4N51TXVB
4N52 (5082-7392)/4N52TXV/4N52TXVB
4N53 (5082-7393)/4N53TXV/4N53TXVB
4N54 (5082-7395)/4N54TXV/4N54TXVB

TECHNICAL DATA JANUARY 1984

Features

- CONFORM TO MIL-D-87157, QUALITY LEVEL A
- HERMETICALLY SEALED
- TXV AND TXVB VERSIONS AVAILABLE
- THREE CHARACTER OPTIONS
  Numeric
  Hexadecimal
  Over Range
- 4 x 7 DOT MATRIX CHARACTER
- PERFORMANCE GUARANTEED OVER TEMPERATURE
- HIGH TEMPERATURE STABILIZED
- GOLD PLATED LEADS
- MEMORY LATCH/DECODER/DRIVER
  TTL Compatible
- CATEGORIZED FOR LUMINOUS INTENSITY



Description

The 4N51-4N54 series solid state numeric and hexadecimal indicators with on-board decoder/driver and memory are hermetically sealed 7.4mm (0.29 inch) displays for use in military and aerospace applications.

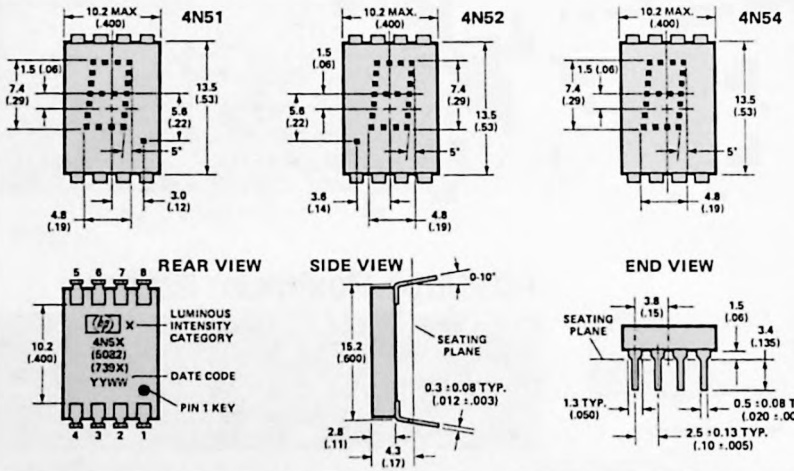
The 4N51 numeric indicator decodes positive 8421 BCD logic inputs into characters 0-9, a "—" sign, a test pattern, and four blanks in the invalid BCD states. The unit employs a right-hand decimal point.

The 4N52 is the same as the 4N51 except that the decimal point is located on the left-hand side of the digit.

The 4N54 hexadecimal indicator decodes positive 8421 logic inputs into 16 states, 0-9 and A-F. In place of the decimal point an input is provided for blanking the display (all LED's off), without losing the contents of the memory.

The 4N53 is a "±1." overrange display, including a right-hand decimal point.

Package Dimensions*



PIN	FUNCTION	
	4N51 4N52 NUMERIC	4N54 HEXA-DECIMAL
1	Input 2	Input 2
2	Input 4	Input 4
3	Input 8	Input 8
4	Decimal point	Blanking control
5	Latch enable	Latch enable
6	Ground	Ground
7	V_{CC}	V_{CC}
8	Input 1	Input 1

NOTES:
1. Dimensions in millimetres and (inches).
2. Unless otherwise specified, the tolerance on all dimensions is ±.38mm (±.015").
3. Digit center line is ±.25mm (±.01") from package center line.
4. Lead material is gold plated copper alloy.

*JEDEC Registered Data.

Absolute Maximum Ratings*

Description	Symbol	Min.	Max.	Unit
Storage temperature, ambient	T_S	−65	+125	°C
Operating temperature, ambient [1,2]	T_A	−55	+100	°C
Supply voltage [3]	V_{CC}	−0.5	+7.0	V
Voltage applied to input logic, dp and enable pins	V_I, V_{DP}, V_E	−0.5	V_{CC}	V
Voltage applied to blanking input [7]	V_B	−0.5	V_{CC}	V
Maximum solder temperature at 1.59mm (.062 inch) below seating plane; t ≤ 5 seconds			260	°C

Recommended Operating Conditions*

Description	Symbol	Min.	Nom.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Operating temperature, ambient [1,2]	T_A	−55		+100	°C
Enable Pulse Width	t_W	100			nsec
Time data must be held before positive transition of enable line	t_{SETUP}	50			nsec
Time data must be held after positive transition of enable line	t_{HOLD}	50			nsec
Enable pulse rise time	t_{TLH}			200	nsec

Electrical/Optical Characteristics* (T_A = −55°C to +100°C, unless otherwise specified)

Description	Symbol	Test Conditions	Min.	Typ. [4]	Max.	Unit
Supply Current	I_{CC}	V_{CC}=5.5V (Numeral		112	170	mA
Power dissipation	P_T	5 and dp lighted)		560	935	mW
Luminous intensity per LED (Digit average) [5,6]	I_v	V_{CC}=5.0V, T_A=25°C	40	85		μcd
Logic low-level input voltage	V_{IL}	V_{CC}=4.5V			0.8	V
Logic high-level input voltage	V_{IH}		2.0			V
Enable low-voltage; data being entered	V_{EL}				0.8	V
Enable high-voltage; data not being entered	V_{EH}		2.0			V
Blanking low-voltage; display not blanked [7]	V_{BL}				0.8	V
Blanking high-voltage; display blanked [7]	V_{BH}		3.5			V
Blanking low-level input current [7]	I_{BL}	V_{CC}=5.5V, V_{BL}=0.8V			50	μA
Blanking high-level input current [7]	I_{BH}	V_{CC}=5.5V, V_{BH}=4.5V			1.0	mA
Logic low-level input current	I_{IL}	V_{CC}=5.5V, V_{IL}=0.4V			−1.6	mA
Logic high-level input current	I_{IH}	V_{CC}=5.5V, V_{IH}=2.4V			+100	μA
Enable low-level input current	I_{EL}	V_{CC}=5.5V, V_{EL}=0.4V			−1.6	mA
Enable high-level input current	I_{EH}	V_{CC}=5.5V, V_{EH}=2.4V			+130	μA
Peak wavelength	λ_{PEAK}	T_A=25°C		655		nm
Dominant Wavelength [8]	λ_d	T_A=25°C		640		nm
Weight**				1.0		gm
Leak Rate					$5x10^{-8}$	cc/sec

Notes: 1. Nominal thermal resistance of a display mounted in a socket which is soldered into a printed circuit board: θ_{JA}=50°C/W; θ_{JC}=15°C/W. 2. θ_{CA} of a mounted display should not exceed 35°C/W for operation up to T_A=+100°C. 3. Voltage values are with respect to device ground, pin 6. 4. All typical values at V_{CC}=5.0 Volts, T_A=25°C. 5. These displays are categorized for luminous intensity with the intensity category designated by a letter located on the back of the display contiguous with the Hewlett-Packard logo marking. 6. The luminous intensity at a specific ambient temperature, $I_V(T_A)$, may be calculated from this relationship: $I_V(T_A)=I_{V(25°C)}(.985)^{[T_A-25°C]}$ 7. Applies only to 4N54. 8. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.

*JEDEC Registered Data. **Non Registered Data.

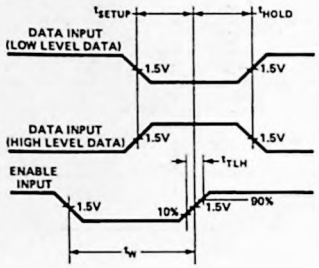


Figure 1. Timing Diagram of 4N51-4N54 Series Logic.

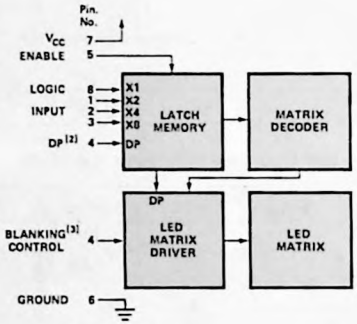


Figure 2. Block Diagram of 4N51-4N54 Series Logic.

TRUTH TABLE					
BCD DATA[1]				4N51 AND 4N52	4N54
X_8	X_4	X_2	X_1		
L	L	L	L	0	0
L	L	L	H	1	1
L	L	H	L	2	2
L	L	H	H	3	3
L	H	L	L	4	4
L	H	L	H	5	5
L	H	H	L	6	6
L	H	H	H	7	7
H	L	L	L	8	8
H	L	L	H	9	9
H	L	H	L	-	A
H	L	H	H	(BLANK)	B
H	H	L	L	(BLANK)	C
H	H	L	H	-	D
H	H	H	L	(BLANK)	E
H	H	H	H	(BLANK)	F
DECIMAL PT.[2]			ON		V_{DP} = L
			OFF		V_{DP} = H
ENABLE[1]			LOAD DATA		V_E = L
			LATCH DATA		V_E = H
BLANKING[3]			DISPLAY-ON		V_B = L
			DISPLAY-OFF		V_B = H

Notes:

1. H = Logic High; L = Logic Low. With the enable input at logic high changes in BCD input logic levels or D.P. input have no effect upon display memory, displayed character, or D.P.
2. The decimal point input, DP, pertains only to the 4N51 and 4N52 displays.
3. The blanking control input, B, pertains only to the 4N54 hexadecimal display. Blanking input has no effect upon display memory.

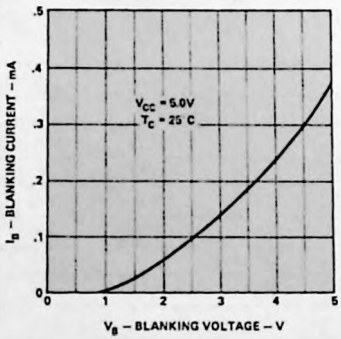


Figure 3. Typical Blanking Control Current vs. Voltage for 4N54.

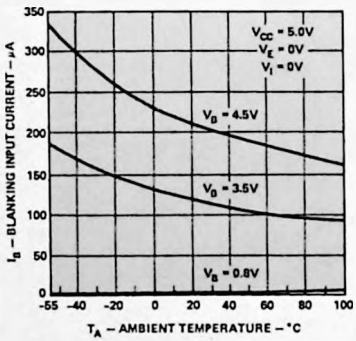


Figure 4. Typical Blanking Control Input Current vs. Ambient Temperature for 4N54.

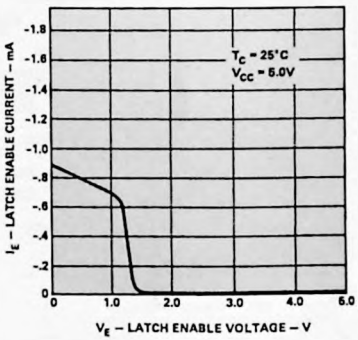


Figure 5. Typical Latch Enable Input Current vs. Voltage.

*JEDEC Registered Data.

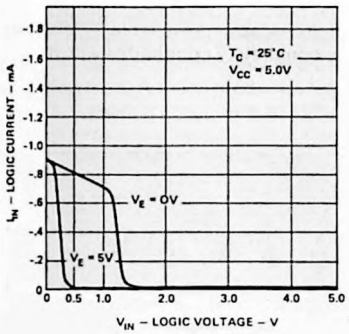


Figure 6. Typical Logic and Decimal Point Input Current vs. Voltage.

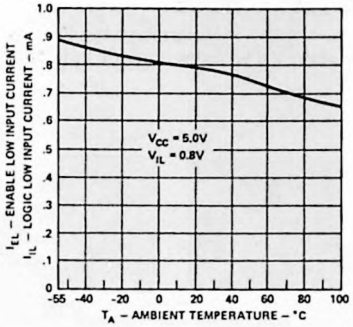


Figure 7. Typical Logic and Enable Low Input Current vs. Ambient Temperature.

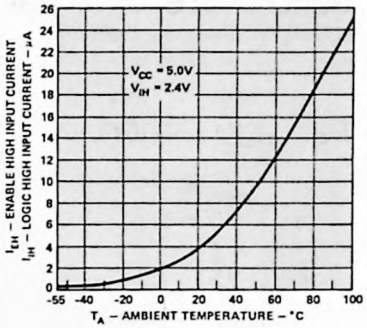


Figure 8. Typical Logic and Enable High Input Current vs. Ambient Temperature.

Operational Considerations

ELECTRICAL

The 4N51-4N54 series devices use a modified 4 x 7 dot matrix of light emitting diodes (LED's) to display decimal/hexadecimal numeric information. The LED's are driven by constant current drivers. BCD information is accepted by the display memory when the enable line is at logic low and the data is latched when the enable is at logic high. To avoid the latching of erroneous information, the enable pulse rise time should not exceed 200 nanoseconds. Using the enable pulse width and data setup and hold times listed in the Recommended Operating Conditions allows data to be clocked into an array of displays at a 6.7MHz rate.

The blanking control input on the 4N54 display blanks (turns off) the displayed hexadecimal information without disturbing the contents of display memory. The display is blanked at a minimum threshold level of 3.5 volts. This may be easily achieved by using an open collector TTL gate and a pull-up resistor. For example, (1/6) 7416 hexinverter buffer/driver and a 120 ohm pull-up resistor will provide sufficient drive to blank eight displays. The size of the blanking pull-up resistor may be calculated from the following formula, where N is the number of digits:

$$R_{blank} = (V_{CC} - 3.5V)/[N\ (1.0mA)]$$

The decimal point input is active low true and this data is latched into the display memory in the same fashion as the BCD data. The decimal point LED is driven by the on-board IC.

MECHANICAL

4N51-4N54 series displays are hermetically tested for use in environments which require a high reliability device. These displays are designed and tested to meet a helium leak rate of 5 x 10^{-8} CC/SEC and a standard dye penetrant gross leak test.

These displays may be mounted by soldering directly to a printed circuit board or inserted into a socket. The lead-to-lead pin spacing is 2.54mm (0.100 inch) and the lead row spacing is 15.24mm (0.600 inch). These displays may be end stacked with 2.54mm (0.100 inch) spacing between outside pins of adjacent displays. Sockets such as Augat 324-AG2D (3 digits) or Augat 508-AG8D (one digit, right angle mounting) may be used.

The primary thermal path for power dissipation is through the device leads. Therefore, to insure reliable operation up to an ambient temperature of +100° C, it is important to maintain a case-to-ambient thermal resistance of less than 35° C/watt as measured on top of display pin 3.

Post solder cleaning may be accomplished using water, Freon/alcohol mixtures formulated for vapor cleaning processing (up to 2 minutes in vapors at boiling) or Freon/alcohol mixtures formulated for room temperature cleaning. Suggested solvents: Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15.

PRECONDITIONING

4N51-4N54 series displays are 100% preconditioned by 24 hour storage at 125° C.

CONTRAST ENHANCEMENT

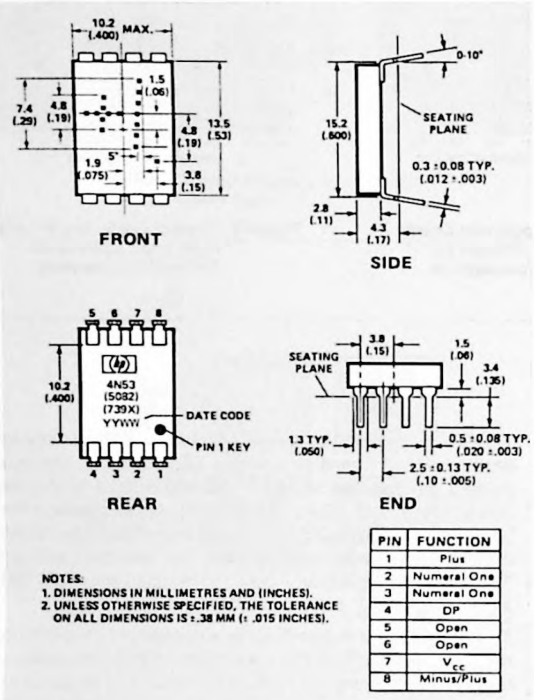
The 4N51-4N54 displays have been designed to provide the maximum posible ON/OFF contrast when placed behind an appropriate contrast enhancement filter. Some suggested filters are Panelgraphic Ruby Red 60 and Dark Red 63, SGL Homalite H100-1605, 3M Light Control Film and Polaroid HRCP Red Circular Polarizing Filter. For further information see Hewlett-Packard Application Note 964.

*JEDEC Registered Data.

Solid State Over Range Character

For display applications requiring a +, 1, or decimal point designation, the 4N53 over range character is available. This display module comes in the same package as the 4N51-4N54 series numeric indicator and is completely compatible with it.

Package Dimensions*



PIN	FUNCTION
1	Plus
2	Numeral One
3	Numeral One
4	DP
5	Open
6	Open
7	V_{cc}
8	Minus/Plus

NOTES:
1. DIMENSIONS IN MILLIMETRES AND (INCHES).
2. UNLESS OTHERWISE SPECIFIED, THE TOLERANCE ON ALL DIMENSIONS IS ±.38 MM (± .015 INCHES).

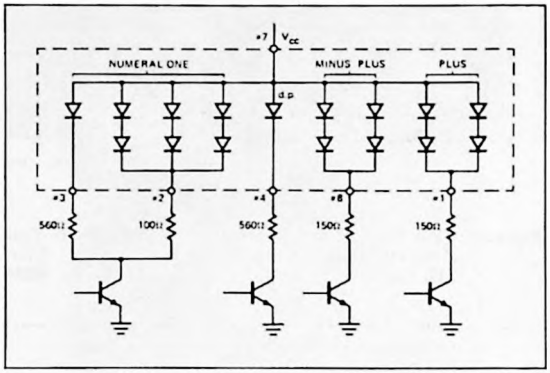


Figure 9. Typical Driving Circuit.

TRUTH TABLE

CHARACTER	PIN			
	1	2,3	4	8
+	H	X	X	H
–	L	X	X	H
1	X	H	X	X
Decimal Point	X	X	H	X
Blank	L	L	L	L

NOTES: L: Line switching transistor in Figure 9 cutoff.
H: Line switching transistor in Figure 9 saturated.
X: 'Don't care'

Electrical/Optical Characteristics*

4N53 (T_A = –55°C to +100°C, Unless Otherwise Specified)

DESCRIPTION	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Forward Voltage per LED	V_F	I_F = 10 mA		1.6	2.0	V
Power dissipation	P_T	I_F = 10 mA all diodes lit		280	320	mW
Luminous Intensity per LED (digit average)	I_v	I_F = 6 mA T_C = 25°C	40	85		µcd
Peak wavelength	λ_{peak}	T_C = 25°C		655		nm
Dominant Wavelength	λ_d	T_C = 25°C		640		nm
Weight**				1.0		gm

Recommended Operating Conditions*

	SYMBOL	MIN	NOM	MAX	UNIT
LED supply voltage	V_{CC}	4.5	5.0	5.5	V
Forward current, each LED	I_F		5.0	10	mA

NOTE:
LED current must be externally limited. Refer to Figure 9 for recommended resistor values.

*JEDEC Registered Data. **Non Registered Data.

Absolute Maximum Ratings*

DESCRIPTION	SYMBOL	MIN.	MAX.	UNIT
Storage temperature, ambient	T_S	–65	+125	°C
Operating temperature, ambient	T_A	–55	+100	°C
Forward current, each LED	I_F		10	mA
Reverse voltage, each LED	V_R		4	V

High Reliability Testing

Two standard reliability testing programs are available. The TXVB program is in conformance with Quality Level A of MIL-D-87157 for hermetically sealed displays with 100% screening tests. A TXVB product is tested to Tables I, II, IIIa, and IVa. A second program is an HP modification to the full conformance program and offers the 100% screening portion of Level A, Table I, and Group A, Table II.

PART MARKING SYSTEM

Standard Product	With Table I and II	With Tables I, II, IIIa and IVa
PREFERRED PART NUMBER SYSTEM		
4N51	4N51TXV	4N51TXVB
4N52	4N52TXV	4N52TXVB
4N54	4N54TXV	4N54TXVB
4N53	4N53TXV	4N53TXVB
ALTERNATE PART NUMBER SYSTEM		
5082-7391	TXV-7391	TXVB-7391
5082-7392	TXV-7392	TXVB-7392
5082-7395	TXV-7395	TXVB-7395
5082-7393	TXV-7393	TXVB-7393

100% Screening

TABLE I.
QUALITY LEVEL A OF MIL-D-87157

Test Screen	MIL-STD-750 Method	Conditions
1. Precap Visual	—	HP Procedure 5956-7572-52
2. High Temperature Storage	1032	T_A = 125°C, Time = 24 hours
3. Temperature Cycling	1051	Condition B, 10 Cycles, 15 Min. Dwell
4. Constant Acceleration	2006	10,000 G's at Y_1 orientation
5. Fine Leak	1071	Condition H
6. Gross Leak	1071	Condition C
7. Interim Electrical/Optical Tests[2]	—	I_V, I_{CC}, I_{BL}, I_{BH}, I_{EL}, I_{EH}, I_{IL}, and I_{IH} and visual function. T_A = 25°C
8. Burn-In[1, 3]	1015	Condition B at V_{CC} = 5V and cycle through logic at 1 character per second. T_A = 100°C, t = 160 hours
9. Final Electrical Test[2]	—	Same as Step 7
10. Delta Determinations	—	ΔI_V = -20%, ΔI_{CC} = ± 10 mA, ΔI_{IH} = ±10μA and ΔI_{EH} = ±13 μA
11. External Visual[1]	2009	

Notes:
1. MIL-STD-883 Test Method applies.
2. Limits and conditions are per the electrical/optical characteristics.
3. Burn-in for the over range shall use Condition B at a nominal I_F = 8 mA with '+1' illuminated for t = 160 hours.

TABLE II
GROUP A ELECTRICAL TESTS — MIL-D-87157

Test	Parameters	LTPD
Subgroup 1 DC Electrical Tests at 25°C[1]	I_V, I_{CC}, I_{BL}, I_{BH}, I_{EL}, I_{EH}, I_{IL}, and I_{IH} and visual function, T_A = 25°C	5
Subgroup 2 DC Electrical Tests at High Temperature[1]	Same as Subgroup 1, except delete I_V and visual function. T_A = +100°C	7
Subgroup 3 DC Electrical Tests at Low Temperature[1]	Same as Subgroup 1, except delete I_V and visual function. T_A = -55°C	7
Subgroup 4, 5, and 6 not tested		
Subgroup 7 Optical and Functional Tests at 25°C	Satisfied by Subgroup 1	5
Subgroup 8 External Visual		7

1. Limits and conditions are per the electrical/optical characteristics.

TABLE IIIa
GROUP B, CLASS A AND B OF MIL-D-87157

Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1			
Resistance to Solvents	1022		4 Devices/ 0 Failures
Internal Visual and Mechanical[3]	2014		1 Device/ 0 Failures
Subgroup 2[1,2]			
Solderability	2026	T_A = 260° C for 5 seconds	LTPD = 15
Subgroup 3			
Thermal Shock (Temp. Cycle)	1051	Condition B, 10 Cycles, 15 Min. Dwell	LTPD = 15
Moisture Resistance	1021		
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C	
Electrical/Optical Endpoints[4]	—	I_V, I_{CC}, I_{BL}, I_{BH}, I_{EL}, I_{EH}, I_{IL}, I_{IH} and visual function. T_A = 25° C	
Subgroup 4			
Operating Life Test (340 hrs.)[5]	1027	T_A = +100° C at V_{CC} = 5.0V and cycling through logic at 1 character per second.	LTPD = 10
Electrical/Optical Endpoints[4]	—	Same as Subgroup 3.	
Subgroup 5			
Non-operating (Storage) Life Test (340 hrs.)	1032	T_A = +125° C	LTPD = 10
Electrical/Optical Endpoints[4]	—	Same as Subgroup 3	

1. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
2. The LTPD applies to the number of leads inspected except in no case shall less than 3 displays be used to provide the number of leads required.
3. MIL-STD-883 methods apply.
4. Limits and conditions are per the electrical/optical characteristics.
5. Burn-in for the over range shall use Condition B at a nominal I_F = 8 mA with '+1' illuminated for t = 160 hours.

TABLE IVa
GROUP C, CLASS A AND B OF MIL-D-87157

Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1			
Physical Dimensions	2066		2 Devices/ 0 Failures
Subgroup 2[2,7]			LTPD = 15
Lead Integrity	2004	Condition B2	
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C	
Subgroup 3			LTPD = 15
Shock	2016	1500G, Time = 0.5 ms, 5 blows in each orientation X_1, Y_1, Y_2	
Vibration, Variable Frequency	2056		
Constant Acceleration	2006	10,000G at Y_1 orientation	
External Visual[4]	1010 or 1011		
Electrical/Optical Endpoints[8]	—	I_V, I_{CC}, I_{BL}, I_{BH}, I_{EL}, I_{EH}, I_{IL}, I_{IH} and visual Function, $T_A = 25°C$	
Subgroup 4[1,3]			LTPD = 15
Salt Atmosphere	1041		
External Visual[4]	1010 or 1011		
Subgroup 5			
Bond Strength[5]	2037	Condition A	LTPD = 20 (C = 0)
Subgroup 6			$\lambda = 10$
Operating Life Test[6]	1026	$T_A = +100°C$	
Electrical/Optical Endpoints[8]	—	Same as Subgroup 3	

1. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
2. The LTPD applies to the number of leads inspected except in no case shall less than three displays be used to provide the number of leads required.
3. Solderability samples shall not be used.
4. Visual requirements shall be as specified in MIL-STD-883, Methods 1010 or 1011.
5. Displays may be selected prior to seal.
6. If a given inspection lot undergoing Group B inspection has been selected to satisfy Group C inspection requirements, the 340 hour life tests may be continued on test to 1000 hours in order to satisfy the Group C Life Test requirements. In such cases, either the 340 hour endpoint measurements shall be made a basis for Group B lot acceptance or the 1000 hour endpoint measurement shall be used as the basis for both Group B and Group C acceptance.
7. MIL-STD-883 test method applies.
8. Limits and conditions are per the electrical/optical characteristics.

HEWLETT PACKARD

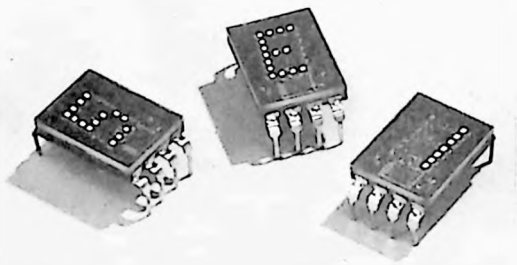
HEXADECIMAL AND NUMERIC DISPLAYS FOR INDUSTRIAL APPLICATIONS

HIGH EFFICIENCY RED	
Low Power	HDSP-0760/0761/0762/0763
High Brightness	HDSP-0770/0771/0772/0763
YELLOW	HDSP-0860/0861/0862/0863
GREEN	HDSP-0960/0961/0962/0963

TECHNICAL DATA JANUARY 1984

Features

- **THREE COLORS**
  High-Efficiency Red
  Yellow
  High Performance Green
- **THREE CHARACTER OPTIONS**
  Numeric
  Hexadecimal
  Over Range
- **TWO HIGH-EFFICIENCY RED OPTIONS**
  Low Power
  High Brightness
- **PERFORMANCE GUARANTEED OVER TEMPERATURE**
- **MEMORY LATCH/DECODER/DRIVER**
  TTL Compatible
- **4x7 DOT MATRIX CHARACTER**
- **CATEGORIZED FOR LUMINOUS INTENSITY**
  YELLOW AND GREEN CATEGORIZED FOR COLOR
  Use of Like Categories Yields a Uniform Display



Description

These solid state display devices are designed and tested for use in adverse industrial environments. The character height is 7.4mm (0.29 inch). The numeric and hexadecimal devices incorporate an on-board IC that contains the data memory, decoder and display driver functions.

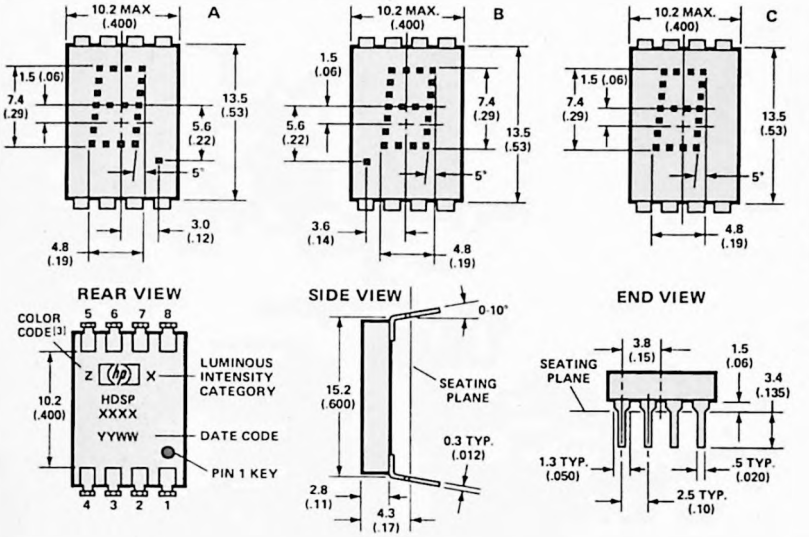
The numeric devices decode positive BCD logic into characters "0-9", a "—" sign, decimal point, and a test pattern. The hexadecimal devices decode positive BCD logic into 16 characters, "0-9, A-F". An input is provided on the hexadecimal devices to blank the display (all LED's off) without losing the contents of the memory.

The over range device displays "±1" and right hand decimal point and is typically driven via external switching transistors.

Devices

Part Number HDSP-	Color	Description	Front View
0760	High-Efficiency Red Low Power	Numeric, Right Hand DP	A
0761		Numeric, Left Hand DP	B
0762		Hexadecimal	C
0763		Over Range ±1	D
0770	High-Efficiency Red High Brightness	Numeric, Right Hand DP	A
0771		Numeric, Left Hand DP	B
0772		Hexadecimal	C
0763		Over Range ±1	D
0860	Yellow	Numeric, Right Hand DP	A
0861		Numeric, Left Hand DP	B
0862		Hexadecimal	C
0863		Over Range ±1	D
0960	Green	Numeric, Right Hand DP	A
0961		Numeric, Left Hand DP	B
0962		Hexadecimal	C
0963		Over Range ±1	D

Package Dimensions



PIN	FUNCTION	
	NUMERIC	HEXA-DECIMAL
1	Input 2	Input 2
2	Input 4	Input 4
3	Input 8	Input 8
4	Decimal point	Blanking control
5	Latch enable	Latch enable
6	Ground	Ground
7	V_{CC}	V_{CC}
8	Input 1	Input 1

NOTES:
1. Dimensions in millimetres and (inches).
2. Vertical digit center line is ± .51mm (± .02") from vertical package center line.
3. HDSP-0860 and HDSP-0960 Series.

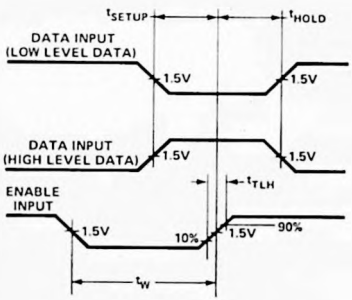


Figure 1. Timing Diagram

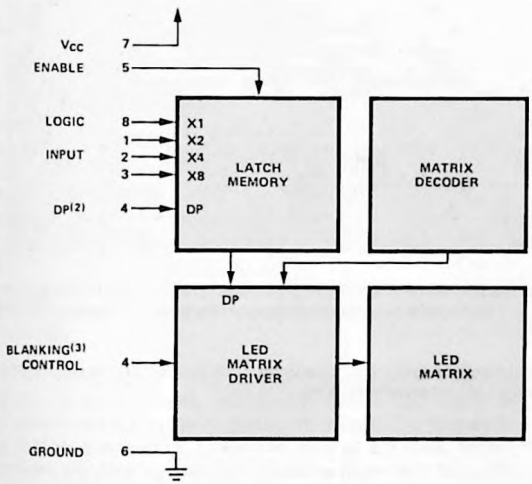


Figure 2. Logic Block Diagram

TRUTH TABLE						
BCD DATA[1]					NUMERIC	HEXA-DECIMAL
X_8	X_4	X_2	X_1			
L	L	L	L		0	0
L	L	L	H		1	1
L	L	H	L		2	2
L	L	H	H		3	3
L	H	L	L		4	4
L	H	L	H		5	5
L	H	H	L		6	6
L	H	H	H		7	7
H	L	L	L		8	8
H	L	L	H		9	9
H	L	H	L		A	A
H	L	H	H		(BLANK)	B
H	H	L	L		(BLANK)	C
H	H	L	H		-	D
H	H	H	L		(BLANK)	E
H	H	H	H		(BLANK)	F
DECIMAL PT [2]				ON		V_{DP} = L
				OFF		V_{DP} = H
ENABLE[1]				LOAD DATA		V_E = L
				LATCH DATA		V_E = H
BLANKING[3]				DISPLAY ON		V_B = L
				DISPLAY OFF		V_B = H

Notes:
1. H = Logic High; L = Logic Low. With the enable input at logic high changes in BCD input logic levels have no effect upon display memory, displayed character, or DP.
2. The decimal point input, DP, pertains only to the numeric displays.
3. The blanking control input, B, pertains only to the hexadecimal displays. Blanking input has no effect upon display memory.

Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Unit
Storage temperature, ambient	T_S	−65	+100	°C
Operating temperature, ambient [1]	T_A	−55	+70	°C
Supply voltage [2]	V_{CC}	−0.5	+7.0	V
Voltage applied to input logic, dp and enable pins	V_I, V_{DP}, V_E	−0.5	V_{CC}	V
Voltage applied to blanking input [2]	V_B	−0.5	V_{CC}	V
Maximum solder temperature at 1.59mm (.062 inch) below seating plane; t ≤ 5 seconds			260	°C

Recommended Operating Conditions

Description	Symbol	Min.	Nom.	Max.	Unit
Supply Voltage [2]	V_{CC}	4.5	5.0	5.5	V
Operating temperature, ambient [1]	T_A	-55		+70	°C
Enable Pulse Width	t_W	100			nsec
Time data must be held before positive transition of enable line	t_{SETUP}	50			nsec
Time data must be held after positive transition of enable line	t_{HOLD}	50			nsec
Enable pulse rise time	t_{TLH}			1.0	msec

Optical Characteristics at T_A = 25°C, V_{CC} = 5.0V

Device	Description	Symbol	Min.	Typ.	Max.	Unit
HDSP-0760 Series	Luminous Intensity per LED (Digit Average) [3,4]	I_V	65	140		μcd
	Peak Wavelength	λ_{PEAK}		635		nm
	Dominant Wavelength [5]	λ_d		626		nm
HDSP-0770 Series	Luminous Intensity per LED (Digit Average) [3,4]	I_V	260	620		μcd
	Peak Wavelength	λ_{PEAK}		635		nm
	Dominant Wavelength [5]	λ_d		626		nm
HDSP-0860 Series	Luminous Intensity per LED (Digit Average) [3,4]	I_V	215	490		μcd
	Peak Wavelength	λ_{PEAK}		583		nm
	Dominant Wavelength [5,6]	λ_d		585		nm
HDSP-0960 Series	Luminous Intensity per LED (Digit Average) [3,4]	I_V	298	1100		μcd
	Peak Wavelength	λ_{PEAK}		568		nm
	Dominant Wavelength [5,6]	λ_d		574		nm

Notes:
1. The nominal thermal resistance of a display mounted in a socket that is soldered onto a printed circuit board is $R\theta_{JA}$ = 50° C/W/device. The device package thermal resistance is $R\theta_{J-PIN}$ = 15° C/W/device. The thermal resistance device pin-to-ambient through the PC board should not exceed 35° C/W/device for operation at T_A = +70° C.
2. Voltage values are with respect to device ground, pin 6.
3. These displays are categorized for luminous intensity with the intensity category designated by a letter code located on the back of the display package. Case temperature of the device immediately prior to the light measurement is equal to 25° C.

Electrical Characteristics; T_A = 0°C to +70°C

Description		Symbol	Test Conditions	Min.	Typ.[7]	Max.	Unit
Supply Current	HDSP-0760 Series	I_{CC}	V_{CC} = 5.5V (Numeral 5 and DP Illuminated)		78	105	mA
	HDSP-0770 Series HDSP-0860 Series HDSP-0960 Series				120	175	
Power Dissipation	HDSP-0760 Series	P_T	V_{CC} = 5.5V (Numeral 5 and DP Illuminated)		390	573	mW
	HDSP-0770 Series HDSP-0860 Series HDSP-0960 Series				690	963	
Logic, Enable and Blanking Low-Level Input Voltage		V_{IL}	V_{CC} = 4.5V			0.8	V
Logic, Enable and Blanking High-Level Input Voltage		V_{IH}		2.0			V
Logic and Enable Low-Level Input Current		I_{IL}	V_{CC} = 5.5V			-1.6	mA
Blanking Low-Level Input Current		I_{BL}	V_{IL} = 0.4V			-10	μA
Logic, Enable and Blanking High-Level Input Current		I_{IH}	V_{CC} = 5.5V V_{IH} = 2.4V			+40	μA
Weight					1.0		gm
Leak Rate						$5x10^{-8}$	cc/sec

Notes:

4. The luminous intensity at a specific operating ambient temperature, $I_V(T_A)$ may be approximated from the following expotential equation: $I_V(T_A = I_V(25°C)\, e^{K(T_A - 25°C)}$.

Device	K
HDSP-0760 Series HDSP-0770 Series	-0.0131/°C
HDSP-0860 Series	-0.0112/°C
HDSP-0960 Series	-0.0104/°C

5. The dominant wavelength, λ_d, is derived from the CIE Chromaticity Diagram and is that single wavelength which defines the color of the device.
6. The HDSP-0860 and HDSP-0960 series devices are categorized as to dominant wavelength with the category designated by a number on the back side of the display package.
7. All typical values at V_{CC} = 5.0V and T_A = 25°C.

Operational Considerations

ELECTRICAL

These devices use a modified 4 x 7 dot matrix of light emitting diode to display decimal/hexadecimal numeric information. The high efficiency red and yellow LED's are GaAsP epitaxial layer on a GaP transparent substrate. The green LED's are GaP epitaxial layer on a GaP transparent substrate. The LED's are driven by constant current drivers, BCD information is accepted by the display memory when the enable line is at logic low and the data is latched when the enable is at logic high. Using the enable pulse width and data setup and hold times listed in the Recommended Operating Conditions allows data to be clocked into an array of displays at a 6.7 MHz rate.

The decimal point input is active low true and this data is latched into the display memory in the same fashion as the BCD data. The decimal point LED is driven by the on-board IC.

The blanking control input on the hexadecimal displays blanks (turns off) the displayed information without disturbing the contents of display memory. The display is blanked at a minimum threshold level of 2.0 volts. When blanked, the display standby power is nominally 250 mW at T_A = 25°C.

MECHANICAL

The primary thermal path for power dissipation is through the device leads. Therefore, to insure reliable operation up to an ambient temperature of +70°C, it is important to maintain a case-to-ambient thermal resistance of less than 35°C watt/device as measured on top of display pin 3.

Post solder cleaning may be accomplished using water, Freon/alcohol mixtures formulated for vapor cleaning processing (up to 2 minutes in vapors at boiling) or Freon/alcohol mixutres formulated for room temperature cleaning. Suggested solvents: Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15.

CONTRAST ENHANCEMENT

These display devices are designed to provide an optimum ON/OFF contrast when placed behind an appropriate contrast enhancement filter. The following filters are suggested:

HIGH EFFICIENCY RED

Panelgraphic Ruby Red 60
Chequers Red 112
3M Light Control Film

YELLOW

Panelgraphic Yellow 27
Chequers Amber 107
3M Light Control Film

GREEN

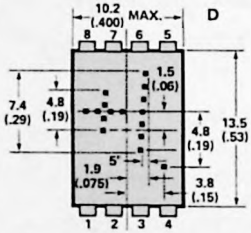
Panelgraphic Green 48
Chequers Green 107
3M Light Control Film

For many applications a neutral density gray filter in either plastic, circular polarizer or optically coated glass will provide the needed contrast enhancement. Suggested plastic neutral density gray filters are Panelgraphic Gray 10, Chequers Gray 105, or Polaroid HNCP37. The optically coated glass/circular polarized HNCP10 filter by Polaroid provides superior contrast enhancement for very bright ambients.

Over Range Character

The over range devices display "±1" and decimal point. The character height and package configuration are the same as the numeric and hexadecimal devices. Character selection is obtained via external switching transistors and current limiting resistors.

Package Dimensions



FRONT VIEW

Pin	Function
1	Plus
2	Numeral One
3	Numeral One
4	DP.
5	Open
6	Open
7	Vcc
8	Minus/Plus

Note:
1. Dimensions in millimetres and (inches).

Character	Pin			
	1	2,3	4	8
+	1	X	X	1
—	0	X	X	1
1	X	1	X	X
Decimal Point	X	X	1	X
Blank	0	0	0	0

Notes:
0: Line switching transistor in Figure 7 cutoff.
1: Line switching transistor in Figure 7 saturated.
X: 'don't care'

Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Unit
Storage Temperature, Ambient	T_S	-65	+100	°C
Operating Temperature Ambient	T_A	-55	+70	°C
Forward Current, Each LED	I_F		10	mA
Reverse Voltage, Each LED	V_R		5	V

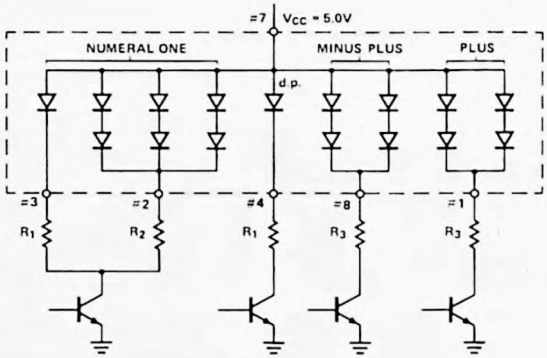


Figure 3. Typical Driving Circuit

Recommended Operating Conditions V_{CC} = 5.0V

Device		Forward Current Per LED, mA	Resistor Value		
			R_1	R_2	R_3
HDSP-0763	Low Power	2.3	1300	200	300
	High Brightness	8	360	47	68
HDSP-0863		8	360	36	56
HDSP-0963		8	360	30	43

Luminous Intensity Per LED

(Digit Average)[3,4] at T_A = 25°C

Device	Test Conditions	Min.	Typ.	Units
HDSP-0763	I_F = 2.3 mA	65	140	µcd
	I_F = 8 mA		620	µcd
HDSP-0863	I_F = 8 mA	215	490	µcd
HDSP-0963	I_F = 8 mA	298	1100	µcd

Electrical Characteristics; T_A = 0°C to +70°C

Device	Description	Symbol	Test Condition	Min.	Typ.	Max.	Units
HDSP-0763	Power Dissipation (all LED's Illuminated)	P_T	I_F = 2.8 mA		72		mW
			I_F = 8 mA		224	282	
	Forward Voltage per LED	V_F	I_F = 2.8 mA		1.6		V
			I_F = 8 mA		1.75	2.2	
HDSP-0863	Power Dissipation (all LED's Illuminated)	P_T	I_F = 8 mA		237	282	mW
	Forward Voltage per LED	V_F			1.90	2.2	V
HDSP-0963	Power Dissipation (all LED's Illuminated)	P_T	I_F = 8 mA		243	282	mW
	Forward Voltage per LED	V_F			1.85	2.2	V

HEWLETT PACKARD

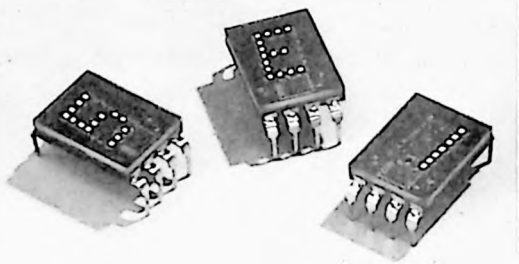
HERMETIC, HEXADECIMAL AND NUMERIC DISPLAYS FOR MILITARY APPLICATIONS

HIGH EFFICIENCY RED	
Low Power	HDSP-078X/078XTXV/078XTXVB
High Brightness	HDSP-079X/079XTXV/079XTXVB
YELLOW	HDSP-088X/088XTXV/088XTXVB

TECHNICAL DATA JANUARY 1984

Features

- CONFORM TO MIL-D-87157, QUALITY LEVEL A
- HERMETICALLY SEALED
- TXV AND TXVB VERSIONS AVAILABLE
- THREE CHARACTER OPTIONS
  Numeric
  Hexadecimal
  Over Range
- 4 x 7 DOT MATRIX CHARACTER
- HIGH EFFICIENCY RED AND YELLOW
- TWO HIGH EFFICIENCY RED OPTIONS
  Low Power
  High Brightness
- PERFORMANCE GUARANTEED OVER TEMPERATURE
- HIGH TEMPERATURE STABILIZED
- GOLD PLATED LEADS
- MEMORY LATCH/DECODER/DRIVER
  TTL Compatible
- CATEGORIZED FOR LUMINOUS INTENSITY



Description

These displays are hermetic, solid state numeric and hexadecimal indicators with on-board decoder/drivers and memory. They are designed and tested for use in military and aero-space applications. The character height is 7.4 mm (0.29 inch). The TXVB versions of these products conform to Quality Level A of MIL-D-87157, the general specification for light emitting diode displays.

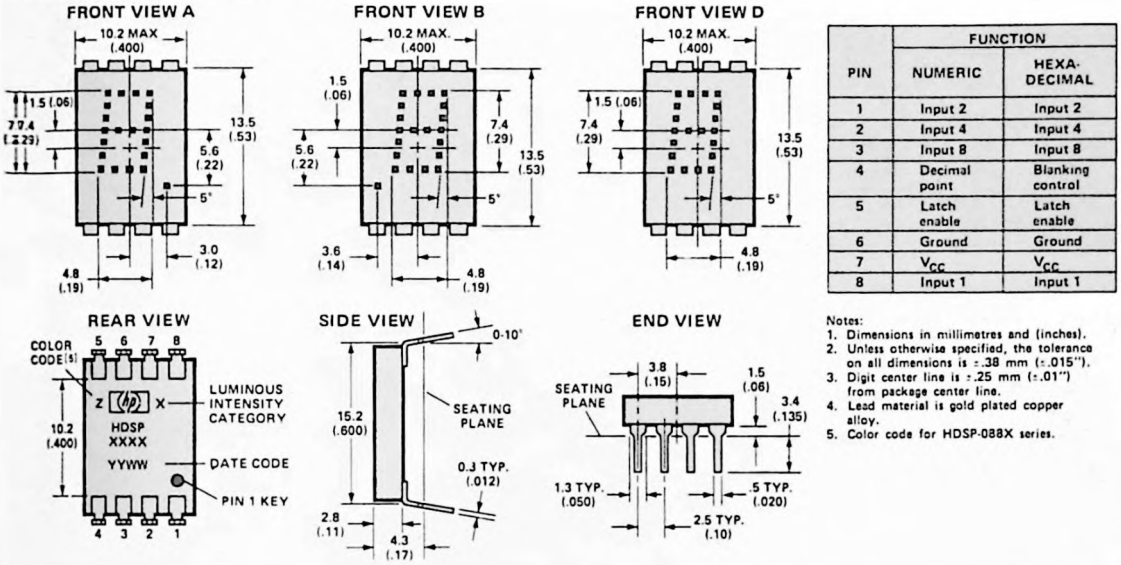
The numeric devices decode positive BCD logic into characters "0-9", a "—" sign, decimal point, and a test pattern. The hexadecimal devices decode positive BCD logic into 16 characters, "0-9, A-F". An input is provided on the hexadecimal devices to blank the display (all LEDs off) without losing the contents of the memory.

The over range device displays "±1" and right hand decimal point and is typically driven via external switching transistors.

Devices

Part Number HDSP-	Color	Description	Front View
0781/0781TXV/0781TXVB	High-Efficiency Red Low Power	Numeric, Right Hand DP	A
0782/0782TXV/0782TXVB		Numeric, Left Hand DP	B
0783/0783TXV/0783TXVB		Over Range ±1	C
0784/0784TXV/0784TXVB		Hexadecimal	D
0791/0791TXV/0791TXVB	High-Efficiency Red High Brightness	Numeric, Right Hand DP	A
0792/0792TXV/0792TXVB		Numeric, Left Hand DP	B
0783/0783TXV/0783TXVB		Over Range ±1	C
0794/0794TXV/0794TXVB		Hexadecimal	D
0881/0881TXV/0881TXVB	Yellow	Numeric, Right Hand DP	A
0882/0882TXV/0882TXVB		Numeric, Left Hand DP	B
0883/0883TXV/0883TXVB		Over Range ±1	C
0884/0884TXV/0884TXVB		Hexadecimal	D

Package Dimensions



PIN	FUNCTION	
	NUMERIC	HEXA-DECIMAL
1	Input 2	Input 2
2	Input 4	Input 4
3	Input 8	Input 8
4	Decimal point	Blanking control
5	Latch enable	Latch enable
6	Ground	Ground
7	V_{CC}	V_{CC}
8	Input 1	Input 1

Notes:
1. Dimensions in millimetres and (inches).
2. Unless otherwise specified, the tolerance on all dimensions is ±.38 mm (±.015").
3. Digit center line is ±.25 mm (±.01") from package center line.
4. Lead material is gold plated copper alloy.
5. Color code for HDSP-088X series.

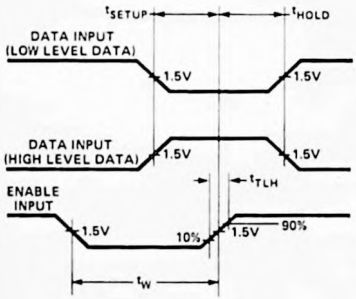


Figure 1. Timing Diagram

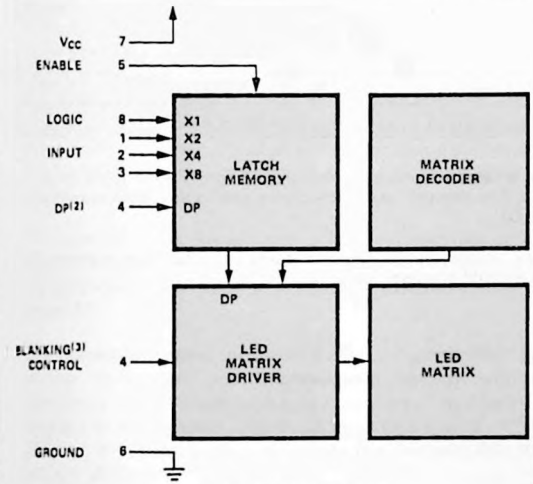


Figure 2. Logic Block Diagram

TRUTH TABLE						
BCD DATA[1]				NUMERIC	HEXA-DECIMAL	
X_8	X_4	X_2	X_1			
L	L	L	L	0	0	
L	L	L	H	1	1	
L	L	H	L	2	2	
L	L	H	H	3	3	
L	H	L	L	4	4	
L	H	L	H	5	5	
L	H	H	L	6	6	
L	H	H	H	7	7	
H	L	L	L	8	8	
H	L	L	H	9	9	
H	L	H	L	(BLANK)	A	
H	L	H	H	(BLANK)	B	
H	H	L	L	(BLANK)	C	
H	H	L	H	(BLANK)	D	
H	H	H	L	(BLANK)	E	
H	H	H	H	(BLANK)	F	
DECIMAL PT [2]				ON		V_{DP} = L
				OFF		V_{DP} = H
ENABLE[1]				LOAD DATA		V_E = L
				LATCH DATA		V_E = H
BLANKING[3]				DISPLAY ON		V_B = L
				DISPLAY OFF		V_B = H

Notes:
1. H = Logic High; L = Logic Low. With the enable input at logic high changes in BCD input logic levels have no effect upon display memory, displayed character, or DP.
2. The decimal point input, DP, pertains only to the numeric displays.
3. The blanking control input, B, pertains only to the hexadecimal displays. Blanking input has no effect upon display memory.

Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Unit
Storage temperature, ambient	T_S	−65	+125	°C
Operating temperature, ambient [1]	T_A	−55	+100	°C
Supply voltage [2]	V_{CC}	−0.5	+7.0	V
Voltage applied to input logic, dp and enable pins	V_I, V_{DP}, V_E	−0.5	V_{CC}	V
Voltage applied to blanking input [2]	V_B	−0.5	V_{CC}	V
Maximum solder temperature at 1.59mm (.062 inch) below seating plane; t ≤ 5 seconds			260	°C

Recommended Operating Conditions

Description	Symbol	Min.	Nom.	Max.	Unit
Supply Voltage [2]	V_{CC}	4.5	5.0	5.5	V
Operating temperature, ambient [1]	T_A	-55		+100	°C
Enable Pulse Width	t_W	100			nsec
Time data must be held before positive transition of enable line	t_{SETUP}	50			nsec
Time data must be held after positive transition of enable line	t_{HOLD}	50			nsec
Enable pulse rise time	t_{ILH}			1.0	msec

Optical Characteristics at $T_A = 25°C$, $V_{CC} = 5.0V$

Device	Description	Symbol	Min.	Typ.	Max.	Unit
HDSP-078X Series	Luminous Intensity per LED (Digit Average) [3,4]	I_V	65	140		μcd
	Peak Wavelength	λ_{PEAK}		635		nm
	Dominant Wavelength [5]	λ_d		626		nm
HDSP-079X Series	Luminous Intensity per LED (Digit Average) [3,4]	I_V	260	620		μcd
	Peak Wavelength	λ_{PEAK}		635		nm
	Dominant Wavelength [5]	λ_d		626		nm
HDSP-088X Series	Luminous Intensity per LED (Digit Average) [3,4]	I_V	215	490		μcd
	Peak Wavelength	λ_{PEAK}		583		nm
	Dominant Wavelength [5,6]	λ_d		585		nm

Notes:

1. The nominal thermal resistance of a display mounted in a socket that is soldered onto a printed circuit board is $R\theta_{JA} = 50°C/W$/device. The device package thermal resistance is $R\theta_{J\text{-}PIN} = 15°C/W$/device. The thermal resistance device pin-to-ambient through the PC board should not exceed 35° C/W/device for operation at $T_A = +100°C$.
2. Voltage values are with respect to device ground, pin 6.
3. These displays are categorized for luminous intensity with the intensity category designated by a letter code located on the back of the display package. Case temperature of the device immediately prior to the light measurement is equal to 25° C.

Electrical Characteristics; (T_A = -55° C to +100° C, unless otherwise specified)

Description		Symbol	Test Conditions	Min.	Typ.[7]	Max.	Unit
Supply Current	HDSP-078X Series	I_{CC}	V_{CC} = 5.5 V (Numeral 5 and DP Illuminated)		78	105	mA
	HDSP-079X Series HDSP-088X Series				120	175	
Power Dissipation	HDSP-078X Series	P_T	V_{CC} = 5.5 V (Numeral 5 and DP Illuminated)		390	573	mW
	HDSP-079X Series HDSP-088X Series				690	963	
Logic, Enable and Blanking Low-Level Input Voltage		V_{IL}	V_{CC} = 4.5 V			0.8	V
Logic, Enable High-Level Input Voltage		V_{IH}		2.0			V
Blanking High Voltage; Display Blanked		V_{BH}		2.3			V
Logic and Enable Low-Level Input Current		I_{IL}	V_{CC} = 5.5 V			-1.6	mA
Blanking Low-Level Input Current		I_{BL}	V_{IL} = 0.4 V			-10	μA
Logic, Enable and Blanking High-Level Input Current		I_{IH}	V_{CC} = 5.5 V V_{IH} = 2.4 V			+40	μA
Weight					1.0		gm
Leak Rate						5×10^{-8}	cc/sec.

Notes:

4. The luminous intensity at a specific operating ambient temperature, $I_V(T_A)$ may be approximated from the following expotential equation: $I_V(T_A) = I_V(25°C) \cdot e^{K(T_A - 25°C)}$

Device	K
HDSP-078X Series HDSP-079X Series	-0.0131/° C
HDSP-088X Series	-0.0112/° C

5. The dominant wavelength, λ_d, is derived from the CIE Chromaticity Diagram and is that single wavelength which defines the color of the device.
6. The HDSP-088X series devices are categorized as to dominant wavelength with the category designated by a number on the back side of the display package.
7. All typical values at V_{CC} = 5.0V and T_A = 25° C.

Operational Considerations

ELECTRICAL

These devices use a modified 4 x 7 dot matrix of light emitting diodes to display decimal/hexadecimal numeric information. The high efficiency red and yellow LEDs are GaAsP epitaxial layer on a GaP transparent substrate. The LEDs are driven by constant current drivers, BCD information is accepted by the display memory when the enable line is at logic low and the data is latched when the enable is at logic high. Using the enable pulse width and data setup and hold times listed in the Recommended Operating Conditions allows data to be clocked into an array of displays at a 6.7 MHz rate.

The decimal point input is active low true and this data is latched into the display memory in the same fashion as the BCD data. The decimal point LED is driven by the on-board IC.

The blanking control input on the hexadecimal displays blanks (turns off) the displayed information without disturbing the contents of display memory. The display is blanked at a minimum threshold level of 2.0 volts. When blanked, the display standby power is nominally 250 mW at T_A = 25° C.

MECHANICAL

These displays are hermetically sealed for use in environments that require a high reliability device. These displays are designed and tested to meet a helium leak rate of 5 x 10^{-8} cc/sec.

These displays may be mounted by soldering directly to a printed circuit board or inserted into a socket. The lead-to-lead pin spacing is 2.54 mm (0.100 inch) and the lead row spacing is 15.24 mm (0.600 inch). These displays may be end stacked with 2.54 mm (0.100 inch) spacing between outside pins of adjacent displays. Sockets such as Augat 324-AG2D (3 digits) or Augat 508-AG8D (one digit, right angle mounting) may be used.

The primary thermal path for power dissipation is through the device leads. Therefore, to insure reliable operation up to an ambient temperature of +70° C, it is important to maintain a base-to-ambient thermal resistance of less than 35° C watt/device as measured on top of display pin 3.

Post solder cleaning may be accomplished using water, Freon/alcohol mixtures formulated for vapor cleaning processing (up to 2 minutes in vapors at boiling) or

Freon/alcohol mixtures formulated for room temperature cleaning. Suggested solvents: Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15.

PRECONDITIONING

These displays are 100% preconditioned by 24 hour storage at 125°C.

CONTRAST ENHANCEMENT

These display devices are designed to provide an optimum ON/OFF contrast when placed behind an appropriate contrast enhancement filter. The following filters are suggested:

HIGH EFFICIENCY RED

Panelgraphic Scarlet Red 65
SGL Homalite H100-1670
3M Louvered Filter R6310

YELLOW

Panelgraphic Yellow 27
SGL Homalite H100-1720
3M Louvered Filter A5910

For many applications a neutral density gray filter in either plastic, circular polarizer or optically coated glass will provide the needed contrast enhancement. Suggested plastic neutral density gray filters are Panelgraphic Gray 10, SGL Homalite H100-1266 or 3M N0220. The optically coated glass/circular polarized SUNGARD filter by Optical Coating Laboratory, Inc., or the HNCP10 filter by Polaroid, provides superior contrast enhancement for very bright ambients.

Over Range Character

The over range devices display "±1" and decimal point. The character height and package configuration are the same as the numeric and hexadecimal devices. Character selection is obtained via external switching transistors and current limiting resistors.

Character	Pin			
	1	2,3	4	8
+	1	X	X	1
—	0	X	X	1
1	X	1	X	X
Decimal Point	X	X	1	X
Blank	0	0	0	0

Notes:
0: Line switching transistor in Figure 7 cutoff.
1: Line switching transistor in Figure 7 saturated.
X: 'don't care'

Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Unit
Storage Temperature, Ambient	T_S	-65	+125	°C
Operating Temperature Ambient	T_A	-55	+100	°C
Forward Current, Each LED	I_F		10	mA
Reverse Voltage, Each LED	V_R		5	V

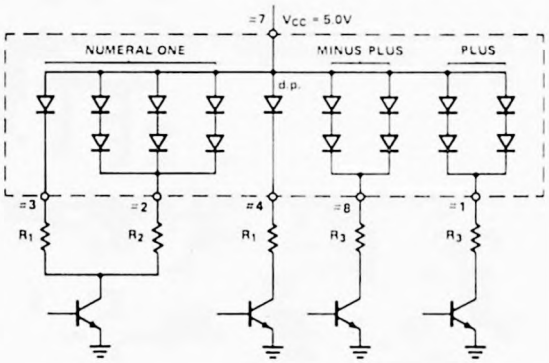


Figure 3. Typical Driving Circuit

Recommended Operating Conditions V_{CC} = 5.0V

Device		Forward Current Per LED, mA	Resistor Value		
			R_1	R_2	R_3
HDSP-0783	Low Power	2.3	1300	200	300
	High Brightness	8	360	47	68
HDSP-0883		8	360	36	56

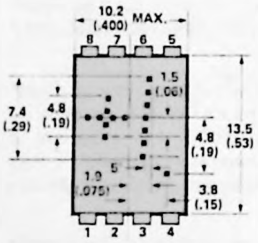
Luminous Intensity Per LED

(Digit Average) at T_A = 25°C

Device	Test Conditions	Min.	Typ.	Units
HDSP-0783	I_F = 2.3 mA	65	140	µcd
	I_F = 8 mA		620	µcd
HDSP-0883	I_F = 8 mA	215	490	µcd

Package Dimensions

FRONT VIEW C



Pin	Function
1	Plus
2	Numeral One
3	Numeral One
4	DP
5	Open
6	Open
7	Vcc
8	Minus/Plus

Note:
1. Dimensions in millimetres and (inches).

Electrical Characteristics; (T_A = −55° C to +100° C, unless otherwise specified)

Device	Description	Symbol	Test Condition	Min.	Typ.	Max.	Units
HDSP-0783	Power Dissipation (all LEDs Illuminated)	P_T	I_F = 2.8 mA		72		mW
			I_F = 8 mA		224	282	
	Forward Voltage per LED	V_F	I_F = 2.8 mA		1.6		V
			I_F = 8 mA		1.75	2.2	
HDSP-0883	Power Dissipation (all LEDs Illuminated)	P_T	I_F = 8 mA		237	282	mW
	Forward Voltage per LED	V_F			1.90	2.2	V

High Reliability Testing

Two standard reliability testing programs are available. The TXVB program is in conformance with Quality Level A of MIL-D-87157 for hermetically sealed displays with 100% screening tests. A TXVB product is tested to Tables I, II, IIIa, and IVa. A second program is an HP modification to the full conformance program and offers the 100% screening portion of Level A, Table I, and Group A, Table II.

PART MARKING SYSTEM

Standard Product	With Table I and II	With Tables I, II, IIIa and IVa
HDSP-078X	HDSP-078XTXV	HDSP-078XTXVB
HDSP-079X	HDSP-079XTXV	HDSP-079XTXVB
HDSP-088X	HDSP-088XTXV	HDSP-088XTXVB

100% Screening

TABLE I.
QUALITY LEVEL A OF MIL-D-87157

Test Screen	MIL-STD-750 Method	Conditions
1. Precap Visual	—	HP Procedure 5956-7572-52
2. High Temperature Storage	1032	T_A = 125° C, Time = 24 hours
3. Temperature Cycling	1051	Condition B, 10 Cycles, 15 Min. Dwell
4. Constant Acceleration	2006	10,000 G at Y_1 orientation
5. Fine Leak	1071	Condition H
6. Gross Leak	1071	Condition C
7. Interim Electrical/Optical Tests[2]	—	I_V, I_{CC}, I_{BL}, I_{BH}, I_{EL}, I_{EH}, I_{IL}, and I_{IH} and visual function. T_A = 25° C
8. Burn-In[1, 3]	1015	Condition B at V_{CC} = 5V and cycle through logic at 1 character per second. T_A = 100° C, t = 160 hours
9. Final Electrical Test[2]	—	Same as Step 7
10. Delta Determinations	—	ΔI_V = -20%, ΔI_{CC} = ± 10 mA, ΔI_{IH} = ±10μA and ΔI_{EH} = ±13 μA
11. External Visual[1]	2009	

Notes:
1. MIL-STD-883 Test Method applies.
2. Limits and conditions are per the electrical/optical characteristics.
3. Burn-in for the over range display shall use Condition B at a nominal I_F = 8 mA with '+1' illuminated for t = 160 hours.

TABLE II
GROUP A ELECTRICAL TESTS — MIL-D-87157

Test	Parameters	LTPD
Subgroup 1 DC Electrical Tests at 25°C[1]	Iv, I_{CC}, I_{BL}, I_{BH}, I_{EL}, I_{EH}, I_{IL}, and I_{IH} and visual function, T_A = 25°C	5
Subgroup 2 DC Electrical Tests at High Temperature[1]	Same as Subgroup 1, except delete Iv and visual function. T_A = +100°C	7
Subgroup 3 DC Electrical Tests at Low Temperature[1]	Same as Subgroup 1, except delete Iv and visual function. T_A = -55°C	7
Subgroup 4, 5, and 6 not tested		
Subgroup 7 Optical and Functional Tests at 25°C	Satisfied by Subgroup 1	5
Subgroup 8 External Visual		7

1. Limits and conditions are per the electrical/optical characteristics.

TABLE IIIa
GROUP B, CLASS A AND B OF MIL-D-87157

Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1 Resistance to Solvents	1022		4 Devices/ 0 Failures
Internal Visual and Mechanical[3]	2014		1 Device/ 0 Failures
Subgroup 2[1,2] Solderability	2026	T_A = 260°C for 5 seconds	LTPD = 15
Subgroup 3 Thermal Shock (Temp. Cycle)	1051	Condition B, 10 Cycles, 15 Min. Dwell	LTPD = 15
Moisture Resistance	1021		
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C	
Electrical/Optical Endpoints[4]	—	Iv, I_{CC}, I_{BL}, I_{BH}, I_{EL}, I_{EH}, I_{IL}, I_{IH} and visual function. T_A = 25°C	
Subgroup 4 Operating Life Test (340 hrs.)[5]	1027	T_A = +100°C at V_{CC} = 5.0V and cycling through logic at 1 character per second.	LTPD = 10
Electrical/Optical Endpoints[4]	—	Same as Subgroup 3.	
Subgroup 5 Non-operating (Storage) Life Test (340 hrs.)	1032	T_A = +125°C	LTPD = 10
Electrical/Optical Endpoints[4]	—	Same as Subgroup 3	

1. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
2. The LTPD applies to the number of leads inspected except in no case shall less than 3 displays be used to provide the number of leads required.
3. MIL-STD-883 methods apply.
4. Limits and conditions are per the electrical/optical characteristics.
5. Burn-in for the over range display shall use Condition B at a nominal $I_F \pm 8$ mA with '+' illuminated for t = 160 hours.

TABLE IVa
GROUP C, CLASS A AND B OF MIL-D-87157

Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1			
Physical Dimensions	2066		2 Devices/ 0 Failures
Subgroup 2[2,7]			LTPD = 15
Lead Integrity	2004	Condition B2	
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C	
Subgroup 3			
Shock	2016	1500G, Time = 0.5 ms, 5 blows in each orientation X_1, Y_1, Y_2	LTPD = 15
Vibration, Variable Frequency	2056		
Constant Acceleration	2006	10,000G at Y_1 orientation	
External Visual[4]	1010 or 1011		
Electrical/Optical Endpoints[8]	—	I_V, I_{CC}, I_{BL}, I_{BH}, I_{EL}, I_{EH}, I_{IL}, I_{IH} and visual Function, T_A = 25°C	
Subgroup 4[1,3]			
Salt Atmosphere	1041		LTPD = 15
External Visual[4]	1010 or 1011		
Subgroup 5			
Bond Strength[5]	2037	Condition A	LTPD = 20 (C = 0)
Subgroup 6			λ = 10
Operating Life Test[6]	1026	T_A = +100°C	
Electrical/Optical Endpoints[8]	—	Same as Subgroup 3	

1. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
2. The LTPD applies to the number of leads inspected except in no case shall less than three displays be used to provide the number of leads required.
3. Solderability samples shall not be used.
4. Visual requirements shall be as specified in MIL-STD-883, Methods 1010 or 1011.
5. Displays may be selected prior to seal.
6. If a given inspection lot undergoing Group B inspection has been selected to satisfy Group C inspection requirements, the 340 hour life tests may be continued on test to 1000 hours in order to satisfy the Group C Life Test requirements. In such cases, either the 340 hour endpoint measurements shall be made a basis for Group B lot acceptance or the 1000 hour endpoint measurement shall be used as the basis for both Group B and Group C acceptance.
7. MIL-STD-883 test method applies.
8. Limits and conditions are per the electrical/optical characteristics.

HEWLETT PACKARD

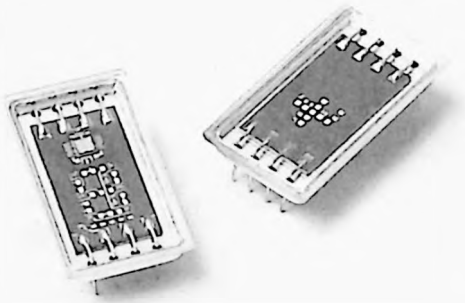
SOLID STATE NUMERIC INDICATOR

5082-7010
5082-7011

TECHNICAL DATA JANUARY 1984

Features

- RUGGED, SHOCK RESISTANT
- INCLUDES DECODER/DRIVER BCD Inputs
- TTL/DTL COMPATIBLE
- CONTROLLABLE LIGHT OUTPUT
- 5 x 7 LED MATRIX CHARACTER



Description

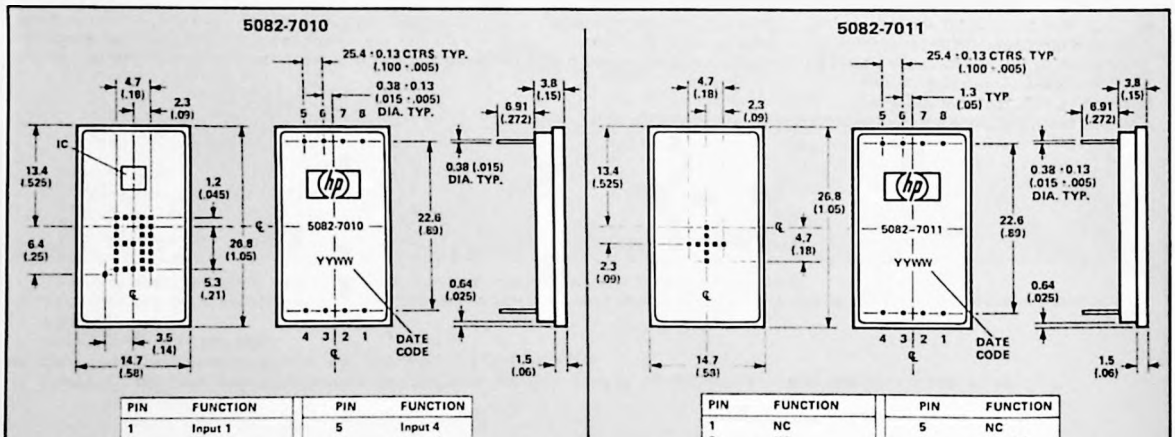
The HP 5082-7010 solid state numeric indicator with built-in decoder/driver provides an excellent 6.8mm (0.27 in.) display for use in military or adverse industrial environments. Typical applications include ground, airborne and shipboard equipment, fire control systems, medical instruments, and space flight systems.

The 5082-7010 is a modified 5x7 matrix display that indicates the numerals 0-9 when presented with a BCD code. The BCD code is negative logic with blanks displayed for invalid codes. A left-hand decimal point is included which must be externally current limited.

The 5082-7011 is a companion plus/minus sign in the same type package. Plus/minus indications require only that voltage be applied to two input pins.

Both displays allow luminous intensity to be varied by changing the DC drive voltage or by pulse duration modulation of the LED voltage.

Package Dimensions



PIN	FUNCTION	PIN	FUNCTION
1	Input 1	5	Input 4
2	V_{DP}	6	Ground
3	V_{LED}	7	V_{CC}
4	Input 8	8	Input 2

PIN	FUNCTION	PIN	FUNCTION
1	NC	5	NC
2	NC	6	Ground
3	Plus	7	Minus/Plus
4	NC	8	NC

Notes:
1. Unless otherwise specified, the tolerance on all dimensions is ±0.38 mm. (±0.015 inches).
2. All dimensions in millimetres and (inches).
3. The package and mounting pins are tin plated Kovar.

Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Unit
Storage Temperature, Ambient	T_S	−65	+100	°C
Operating Temperature, Case	T_C	−55	+95	°C
Logic Supply Voltage to Ground	V_{CC}	−0.5	+7.0	V
Logic Input Voltage	V_I	−0.5	+5.5	V
LED Supply Voltage to Ground	V_{LED} [1]	−0.5	+5.5	V
Decimal Point Current	I_{DP}		−10	mA

Note: 1. Above T_C = 65°C derate V_{LED} per derating curve in Figure 10.

Recommended Operating Conditions

Description	Symbol	Min.	Nom.	Max.	Unit
Logic Supply Voltage	V_{CC}	4.5	5.0	5.5	V
LED Supply Voltage, Display Off	V_{LED}	−0.5	0	+1.0	V
LED Supply Voltage, Display On	V_{LED}	3.0	4.2	5.5	V
Decimal Point Current	I_{DP} [2]	0	−5.0	−10.0	mA
Logic Input Voltage, "H" State	V_{IH}	2.0		5.5	V
Logic Input Voltage, "L" State	V_{IL}	0		0.8	V

Note: 2. Decimal point current must be externally current limited. See application information.

Electrical/Optical Characteristics

Case Temperature, T_C = 0°C to 70°C, unless otherwise specified

Description	Symbol	Test Conditions		Min.	Typ. [4]	Max.	Unit
Logic Supply Current	I_{CC}	V_{CC} = 5.5V			45	75	mA
LED Supply Current	I_{LED} [3] [5]	V_{CC}	V_{LED}				mA
		5.5V	5.5V		255	350	
		5.5V	4.2V		170	235	
		5.5V	3.5V		125		
Logic Input Current, "H" State (ea. input)	I_{IH}	V_{CC} = 5.5V V_{IH} = 2.4V				100	µA
Logic Input Current, "L" State (ea. input)	I_{IL}	V_{CC} = 5.5V V_{IL} = 0.4V				−1.6	mA
Decimal Point Voltage Drop	V_{LED} − V_{DP}	I_{DP} = −10mA			1.6	2.0	V
Power Dissipation	P_T [3] [5]	V_{CC}	V_{LED}				W
		5.5V	5.5V		1.7	2.3	
		5.5V	4.2V		1.0	1.4	
		5.5V	3.5V		0.7		
Luminous Intensity per LED (digit avg.)	I_V	V_{LED}	T_C				µcd
		5.5V	25°C	60	115		
		4.2V	25°C	40	80		
		3.5V	25°C		50		
Peak Wavelength	λ_{peak}				655		nm
Spectral Halfwidth	$\Delta\lambda_{1/2}$				30		nm
Weight					4.9		gram

Notes: 3. With numeral 8 displayed.
4. All typical values at T_C = 25°C.
5. T_C = 0°C to 65°C for V_{LED} = 5.5V.

Truth Table

Character	Logic X8	X4	X2	X1	
0	H	H	H	H	0
1	H	H	H	L	1
2	H	H	L	H	2
3	H	H	L	L	3
4	H	L	H	H	4
5	H	L	H	L	5
6	H	L	L	H	6
7	H	L	L	L	7
8	L	H	H	H	8
9	L	H	H	L	9
Blank	L	H	L	H	
Blank	L	H	L	L	
Blank	L	L	H	H	
Blank	L	L	H	L	
Blank	L	L	L	H	
Blank	L	L	L	L	

V_{IL} = 0.0 to 0.8V
V_{IH} = 2.0 to 5.5V

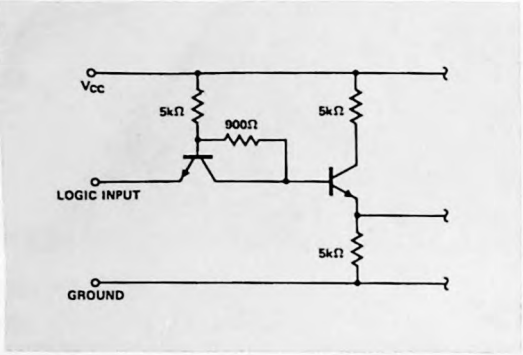


Figure 1. Equivalent input circuit of the 5082-7010 decoder. Note: Display metal case is isolated from ground pin #6.

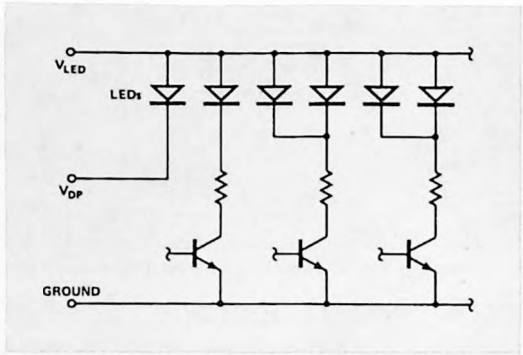


Figure 2. Equivalent circuit of the 5082-7010 as seen from LED and decimal point drive lines.

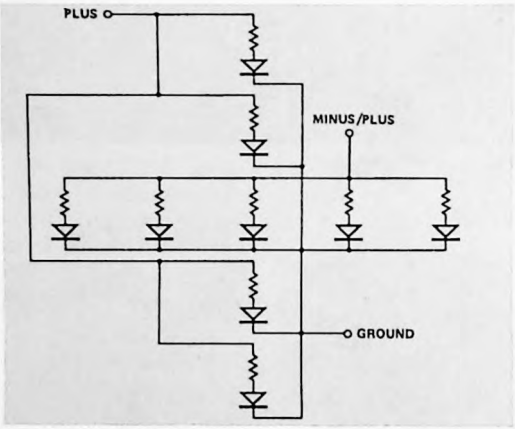


Figure 3. Equivalent circuit of 5082-7011 plus/minus sign. All resistors 345Ω typical. Note: Display metal case is isolated from ground pin #6.

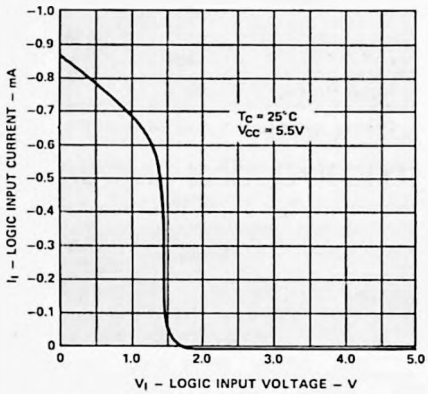


Figure 4. Input current as a function of input voltage, each input.

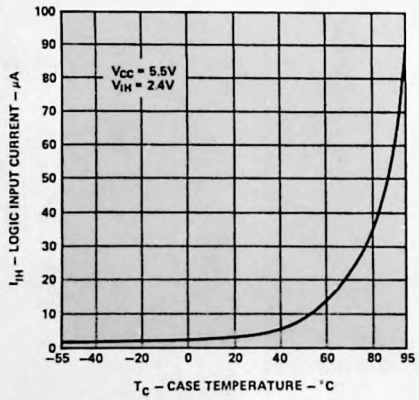


Figure 5. Logic "H" input current as a function of case temperature, each input.

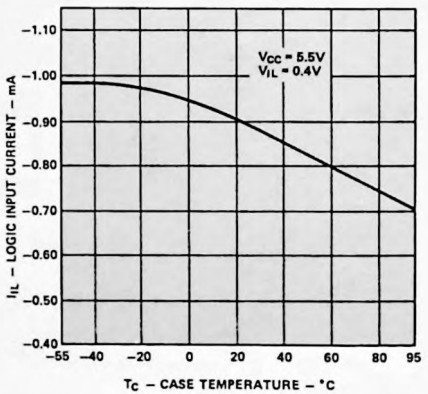


Figure 6. Logic "L" input current as a function of case temperature, each input.

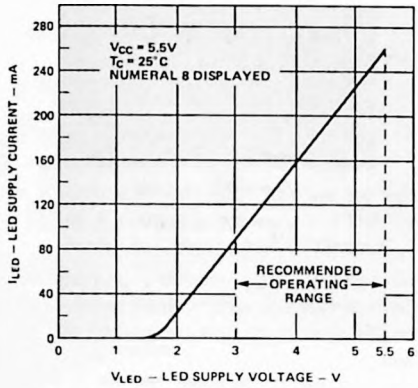


Figure 7. LED supply current as a function of LED supply voltage.

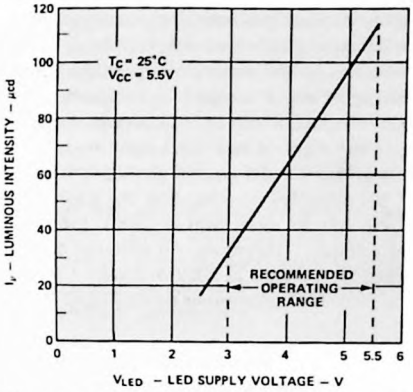


Figure 8. Luminous intensity per LED (digit average) as a function of LED supply voltage.

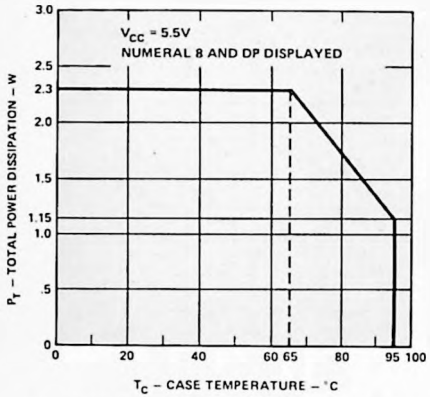


Figure 9. Maximum power derating as a function of case temperature.

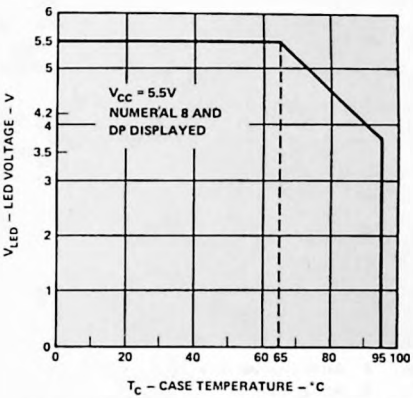


Figure 10. LED voltage derating as a function of case temperature.

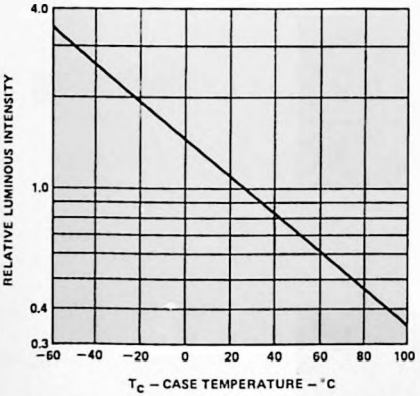


Figure 11. Relative luminous intensity as a function of case temperature at fixed current level.

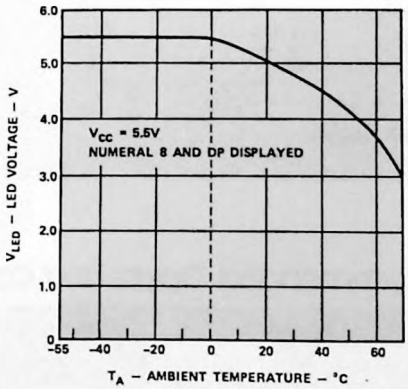


Figure 12. LED voltage derating as a function of ambient temperature, display soldered into P.C. board without heat sink.

Solid State Plus/Minus Sign

For display applications requiring ± designation, the 5082-7011 solid state plus/minus sign is available. This display module comes in the same package as the 5082-7010 numeric indicator and is completely compatible with it. Plus or minus information can be indicated by supplying voltage to one (minus sign) or two (plus sign) input leads. A third lead is provided for the ground connection. Luminous intensity is controlled by changing the LED drive voltage. Each LED has its own built-in 345Ω (nominal) current limiting resistor. Therefore, no external current limiting is required for voltages at 5.5V or lower. Like the numeric indicator, the -7011 plus/minus sign is TTL/DTL compatible.

Truth Table

CHARACTER	PIN	
	3	7
+	H	H
–	L	H
Blank	L	L

V_L = –0.5 to 1.0V

V_H = 3.0 to 5.5V

Electrical/Optical Characteristics

Case Temperature, T_C = 0°C to 70°C, unless otherwise specified

Description	Symbol	Test Conditions	Min.	Typ.[1]	Max.	Unit
LED Supply Current	I_{LED}	V_{LED} = 5.5V		105	150	mA
		V_{LED} = 4.2V		70	100	
Power Dissipation	P_T	V_{LED} = 5.5V		0.6	0.9	W
		V_{LED} = 4.2V		0.3	0.6	
Luminous Intensity per LED (Digit Avg.)	I_V [2]	V_{LED} = 5.5V	60	115		µcd
		V_{LED} = 4.2V	40	80		
		V_{LED} = 3.5V		50		
Peak Wavelength	λ_{peak}			655		nm
Spectral Halfwidth	$\Delta\lambda_{1/2}$			30		nm
Weight				4.9		gram

Notes: 1. All typical values at T_C = 25°C
2. At T_C = 25°C

Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Unit
Storage Temperature, Ambient	T_S	–65	+100	°C
Operating Temperature, Case	T_C	–55	+95	°C
Plus, Plus/Minus Input Potential to Ground	V_{LED}	–0.5	5.5	V

Recommended Operating Conditions

Description	Symbol	Min.	Nom.	Max.	Unit
LED Supply Voltage, Display Off	V_{LED}	–0.5	0	1.0	V
LED Supply Voltage, Display On	V_{LED}	3.0	4.2	5.5	V

Applications

Decimal Point Limiting Resistor

The decimal point of the 5082-7010 display requires an external current limiting resistor, between pin 2 and ground. Recommended resistor value is 220Ω, 1/4 watt.

Mounting

The 5082-7010 and 5082-7011 displays are packaged with two rows of 4 contact pins each in a DIP configuration with a row center line spacing of 0.890 inches.

Normal mounting is directly onto a printed circuit board. If desired, these displays may be socket mounted using contact strip connectors such as Augat's 325-AGI or AMP 583773-1 or 583774-1.

Heat Sink Operation

Optimum display case operating temperature for the 5082-7010 and 7011 displays is T_C=0°C to 70°C as measured on back surface. Maintaining the display case operating temperature within this range may be achieved by mounting the display on an appropriate heat sink or metal core printed circuit board. Thermal conducting compound such as Wakefield 120 or Dow Corning 340 can be used between display and heat sink. See figure 10 for V_{LED} derating vs. display case temperature.

Operation Without Heat Sink

These displays may also be operated without the use of a heat sink. The thermal resistance from case to ambient for these displays when soldered into a printed circuit board is nominally θ_{CA}=30°C/W. See figure 12 for V_{LED} derating vs. ambient temperature.

Cleaning

Post solder cleaning may be accomplished using water, Freon/alcohol mixtures formulated for vapor cleaning processing (up to 2 minutes in vapors at boiling) or Freon/alcohol mixtures formulated for room temperature cleaning. Suggested solvents: Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15.

HEWLETT PACKARD

LEADFRAME MOUNTED SEVEN SEGMENT MONOLITHIC NUMERIC INDICATORS

5082-7400/7430 SERIES

TECHNICAL DATA JANUARY 1984

Features

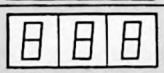
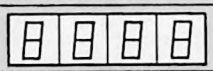
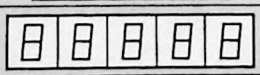
- **COMPACT PACKAGE SIZES**
  .25" Package Width
  .150" and .200" Digit Spacing
- **STROBED OPERATION**
  Minimizes Lead Connections
- **FULLY ENCAPSULATED STANDARD DIP PACKAGES**
  End Stackable
  Integral Red Filter
  Extremely Rugged Construction
- **I.C. COMPATIBLE**
- **CATEGORIZED FOR LUMINOUS INTENSITY**
  Assures uniformity of light output from unit to unit within single category.

Description

The HP 5082-7400/-7430 series are 2.79 mm (.11"), seven segment GaAsP numeric indicators packaged in 2, 3, 4 and 5 digit clusters. An integral magnification technique increases the luminous intensity, thereby making low power consumption possible. Options include either the standard lower right hand decimal point or a centered decimal point.

Applications include hand held calculators, portable instruments and many other products requiring compact, rugged, long lifetime active indicators.

Device Selection Guide

Digits per Cluster	Configuration Device	Inter-Digit Spacing mm (inches)	Part Number Center Decimal Point	Part Number Right Decimal Point
2 (right)		5.08 (.200)		5082-7432
3		5.08 (.200)		5082-7433
4		3.81 (.150)	5082-7404	5082-7414
5		3.81 (.150)	5082-7405	5082-7415

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Peak Forward Current per Segment or dp (Duration < 500 μs) 5082-7432/7433	I_{PEAK}		50	mA
Peak Forward Current per Segment or dp (Duration < 1 msec) 5082-7404/7405/7414/7415	I_{PEAK}		110	mA
Average Current per Segment or dp	I_{AVG}		5	mA
Power Dissipation per Digit [1]	P_D		80	mW
Operating Temperature, Ambient	T_A	-40	75	°C
Storage Temperature	T_S	-40	100	°C
Reverse Voltage	V_R		5	V
Solder Temperature 1/16" below seating plane (t ≤ 3 sec) [2]			230	°C

Notes: 1. Derate linearly @ 1 mW/°C above 25°C ambient.
2. See Mechanical section for recommended flux removal solvents.

Electrical/Optical Characteristics at $T_A = 25°C$

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment or dp [3,4] 5082-7432/7433	I_V	I_{AVG} = 500 μA (I_{PK} = 5 mA duty cycle = 10%)	10	40		μcd
Luminous Intensity/Segment or dp [3,4] (Time Averaged) 5082-7404/7405/7414/7415	I_V	I_{AVG} = 1 mA I_{PK} = 10 mA duty cycle = 10%)	5	20		μcd
Peak Wavelength	λ_{PEAK}			655		nm
Forward Voltage/Segment or dp 5082-7432/-7433	V_F	I_F = 5 mA		1.55	2.0	V
Forward Voltage/Segment or dp 5082-7404/7405/7414/7415	V_F	I_F = 10 mA		1.55	2.0	V
Reverse Voltage/Segment or dp	V_R	I_R = 200 μA	5			V
Rise and Fall Time [5]	t_r, t_f			10		ns

Notes: 3. The digits are categorized for luminous intensity. Intensity categories are designated by a letter located on the back side of the package.
4. Operation at Peak Currents less than 5.0 mA is not recommended.
5. Time for a 10%-90% change of light intensity for step change in current.

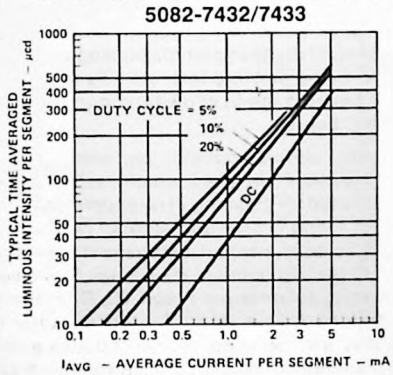


Figure 1. Typical Time Averaged Luminous Intensity per Segment (Digit Average) vs. Current per Segment.

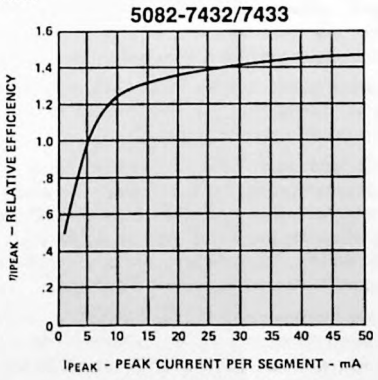


Figure 2. Relative Luminous Efficiency vs. Peak Current per Segment.

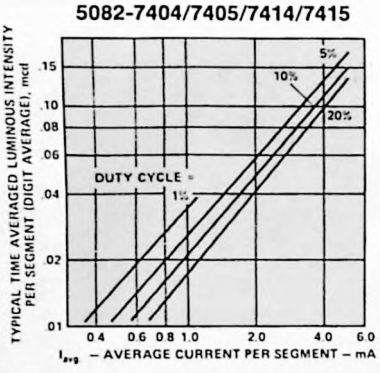


Figure 3. Typical Time Averaged Luminous Intensity per Segment (Digit Average) vs. Average Current per Segment.

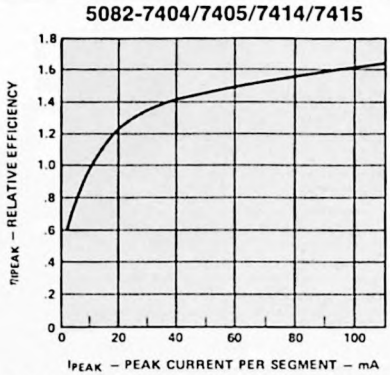


Figure 4. Relative Luminous Efficiency vs. Peak Current per Segment.

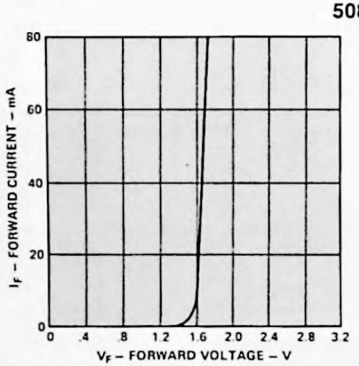


Figure 5. Forward Current vs. Forward Voltage.

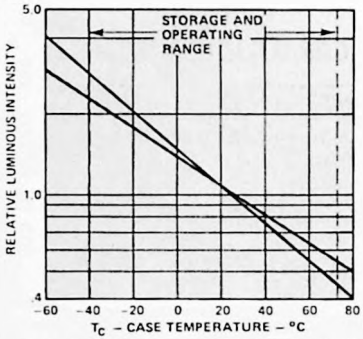


Figure 6. Relative Luminous Intensity vs. Case Temperature at Fixed Current Level.

Electrical/Optical

The 5082-7400/7430 series devices utilize a monolithic GaAsP chip of 8 common cathode segments for each display digit. The segment anodes of each digit are interconnected, forming an 8 by N line array, where N is the number of characters in the display. Each chip is positioned under an integrally molded lens giving a magnified character height of 2.79mm (0.11) inches. Satisfactory viewing will be realized within an angle of ±30° for the 7404/7405/7414/7415 and ±20° for the 7432/7433, measured from the center line of the digit.

The decimal point in the 7432, 7433, 7414, and 7415 displays is located at the lower right of the digit for conventional driving schemes.

The 5082-7404 and 7405 displays contain a centrally located decimal point which is activated in place of a digit. In long registers, this technique of setting off the decimal point significantly improves the display's readability. With respect to timing, the decimal point is treated as a separate character with its own unique time frame.

To improve display contrast, the plastic incorporates a red dye that absorbs strongly at all visible wavelengths except the 655 nm emitted by the LED. In addition, the lead frames are selectively darkened to reduce reflectance. An additional filter, such as Plexiglass 2423, Panelgraphic 60 or 63, and SGL Homalite 100-1605, will further lower the ambient reflectance and improve display contrast.

Mechanical

The 5082-7400/7430 series package is a standard 12 or 14 Pin DIP consisting of a plastic encapsulated lead frame with integral molded lenses. It is designed for plugging into DIP sockets or soldering into PC boards. The lead frame construction allows use of standard DIP insertion tools and techniques. Alignment problems are simplified due to the clustering of digits in a single package. The shoulders of the lead frame pins are intentionally raised above the bottom of the package to allow tilt mounting of up to 20° from the PC board.

To optimize device optical performance, specially developed plastics are used which restrict the solvents that may be used for cleaning. It is recommended that only mixtures of Freon (F113) and alcohol be used for vapor cleaning processes, with an immersion time in the vapors of less than two (2) minutes maximum. Some suggested vapor cleaning solvents are Freon TE, Genesolv DI-15 or DE-15, Arklone A or K. A 60°C (140°C) water cleaning process may also be used, which includes a neutralizer rinse (3% ammonia solution or equivalent), a surfactant rinse (1% detergent solution or equivalent), a hot water rinse and a thorough air dry. Room temperature cleaning may be accomplished with Freon T-E35 or T-P35, Ethanol, Isopropanol or water with a mild detergent.

Package Description 5082-7404, -7405, -7414, -7415

Notes: 6. Dimensions in millimeters and (inches).
7. Tolerances on all dimensions are ±0.038 mm (±.015 in.) unless otherwise noted.

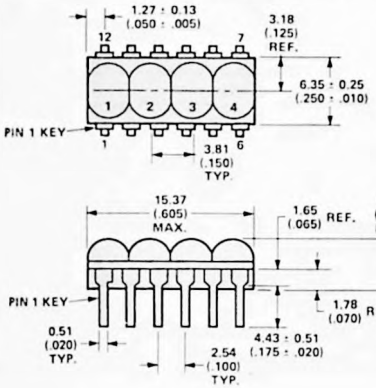


Figure 7. 5082-7404/7414

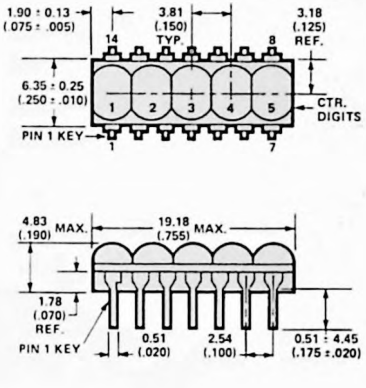


Figure 8. 5082-7405/7415.

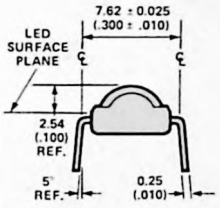
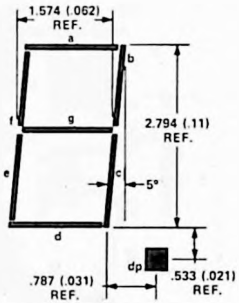


Figure 9. 5082-7404/7405/7414/7415

Magnified Character Font Description

DIMENSIONS IN MILLIMETERS AND (INCHES).



DEVICES

5082-7404
5082-7405
5082-7414
5082-7415

Figure 10. Center and Right Decimal Point Configuration.

Device Pin Description

5082-7404/7414 FUNCTION	5082-7405/7415 FUNCTION
CATHODE 1	CATHODE 1
ANODE e	ANODE e
ANODE c	ANODE c
CATHODE 3	CATHODE 3
ANODE dp	ANODE dp
CATHODE 4	ANODE d
ANODE g	CATHODE 5
ANODE d	ANODE g
ANODE f	CATHODE 4
CATHODE 2	ANODE f
ANODE b	SEE NOTE 8.
ANODE a	ANODE b
–	CATHODE 2
–	ANODE a

Note 8: Leave Pin Unconnected.

Package Description 5082-7432, -7433

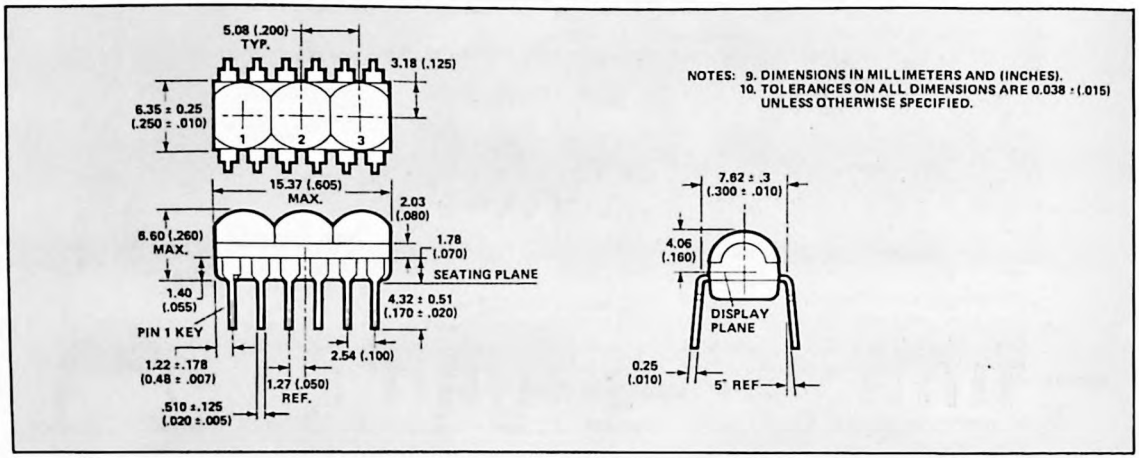


Figure 11.

Magnified Character Font Description

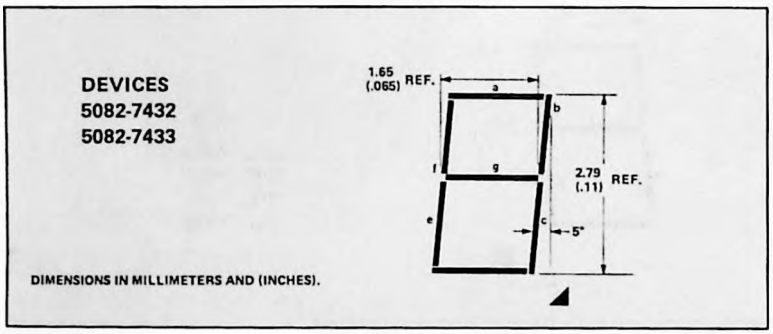


Figure 12.

Device Pin Description

PIN NUMBER	5082-7432 FUNCTION	5082-7433 FUNCTION
1	SEE NOTE 11.	CATHODE 1
2	ANODE e	ANODE e
3	ANODE d	ANODE d
4	CATHODE 2	CATHODE 2
5	ANODE c	ANODE c
6	ANODE dp	ANODE dp
7	CATHODE 3	CATHODE 3
8	ANODE b	ANODE b
9	ANODE g	ANODE g
10	ANODE a	ANODE a
11	ANODE f	ANODE f
12	SEE NOTE 11.	SEE NOTE 11.

NOTE 11. Leave Pin unconnected.

HEWLETT PACKARD

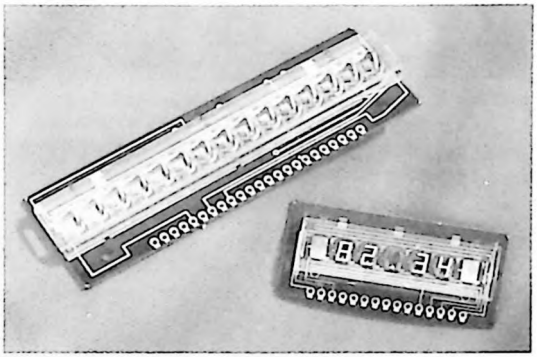
PRINTED CIRCUIT BOARD MOUNTED SEVEN SEGMENT NUMERIC INDICATORS

5082-7200/7440 SERIES

TECHNICAL DATA JANUARY 1984

Features

- MOS COMPATIBLE
- AVAILABLE IN 9 TO 16 DIGIT CONFIGURATIONS
- CHARACTER HEIGHTS OF .105", .115" AND .175"
- LOW POWER
- CATEGORIZED FOR LUMINOUS INTENSITY



Description

The HP-5082-7200/7440 series of displays are seven segment GaAsP Numeric Indicators mounted on printed circuit boards. A plastic lens magnifies the digits and includes an integral protective bezel. Character heights of .105" (2.67 mm), .115" (2.92 mm) and .175" (4.45 mm) are available. For large quantity applications, digit string lengths of 8, 12 and 14 digits are available by special order.

Applications are hand held calculators and portable equipment requiring compact, low power, long life time, active displays.

Device Selection Guide

Part Number	Digits Per PC Board	Decimal Point	Package	Character Height (mm) In.	Inter-Digit Spacing (mm) In.
5082-7441	9	Right Hand	Fig. 9	(2.67) .105"	(5.08) .200"
5082-7446	16	Right Hand	Fig. 11	(2.92) .115"	(3.81) .150"
5082-7285	5	Right Hand	Fig. 14	(4.45) .175"	(5.84) .230"
5082-7295	15	Right Hand	Fig. 13	(4.45) .175"	(5.84) .230"

Maximum Ratings 5082-7441/7446

Parameter	Symbol	Min.	Max.	Units
Peak Forward Current per Segment or dp (Duration < 500μs)	I_{PEAK}		50	mA
Average Current per Segment or dp[1]	I_{AVG}		3	mA
Power Dissipation per Digit [2]	P_D		50	mW
Operating Temperature, Ambient	T_A	-20	+85	°C
Storage Temperature	T_S	-20	+85	°C
Reverse Voltage	V_R		3	V
Solder Temperature at connector edge (t≤3 sec.)[3]			230	°C

NOTES: 1. Derate linearly at 0.1mA/°C above 60°C ambient.
2. Derate linearly at 1.7mW/°C above 60°C ambient.
3. See Mechanical section for recommended soldering techniques and flux removal solvents.

Maximum Ratings 5082-7285/7295

Parameter	Symbol	Min.	Max.	Units
Peak Forward Current per Segment or DP (Duration <35μs)	I_{PEAK}		200	mA
Average Current per Segment or DP [4]	I_{AVG}		7	mA
Power Dissipation per Digit [5]	P_D		125	mW
Operating Temperature, Ambient	T_A	-20	+70	°C
Storage Temperature	T_S	-20	+80	°C
Reverse Voltage	V_R		3	V
Solder Temperature at connector edge (t≤3 sec.) [6]			230	°C

NOTES: 4. Derate linearly at 0.12mA/°C above 25°C ambient.
5. Derate linearly at 2.3mW/°C above 25°C ambient.
6. See Mechanical section for recommended soldering techniques and flux removal solvents.

Electrical/Optical Characteristics at T_A = 25°C 5082-7441/7446

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment or dp[7] 5082-7440	I_V	I_{AVG} = 500μA (I_{PK} = 5mA duty cycle = 10%)	9	40		μcd
5082-7446		5mA Peak 1/16 Duty Cycle	7	35		μcd
Peak Wavelength	λ_{peak}			655		nm
Forward Voltage/Segment or dp	V_F	I_F = 5mA		1.55		V

NOTES: 7. Operation at Peak Currents of less than 3.5mA is not recommended.

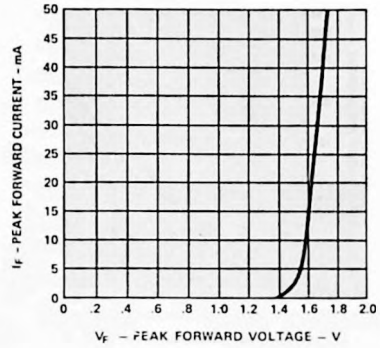


Figure 1. Peak Forward Current vs. Peak Forward Voltage.

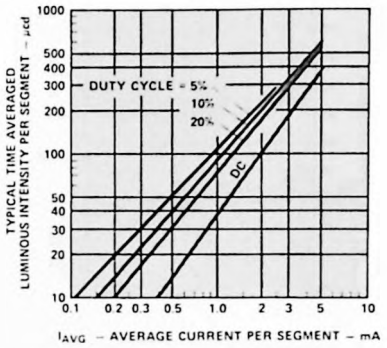


Figure 2. Typical Time Averaged Luminous Intensity per Segment vs. Average Current per Segment.

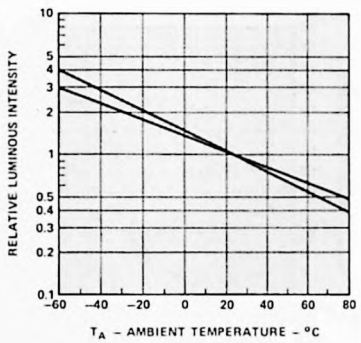


Figure 3. Relative Luminous Intensity vs. Ambient Temperature at Fixed Current Level.

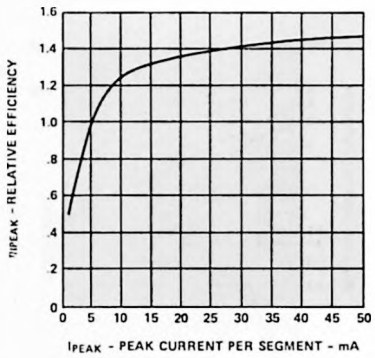


Figure 4. Relative Luminous Efficiency vs. Peak Current per Segment.

Electrical/Optical Characteristics at T_A=25°C 5082-7285/7295

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment or dp (Time Averaged) 15 digit display 5082-7295[8,10]	I_v	$I_{avg.}$ = 2 mA (30 mA Peak 1/15 duty cycle)	30	90		µcd
Luminous Intensity/Segment or dp (Time Averaged) 5 digit display 5082-7285[8,10]	I_v	$I_{avg.}$ = 2 mA (10 mA Peak 1/5 duty cycle)	30	70		µcd
Forward Voltage per Segment or dp 5082-7295 15 digit display	V_F	I_F = 30 mA		1.60	2.3	V
Forward Voltage per Segment or dp 5082-7285 5 digit display	V_F	I_F = 10 mA		1.55	2.0	V
Peak Wavelength	λ_{PEAK}			655		nm
Dominant Wavelength[9]	λ_d			640		nm
Reverse Current per Segment or dp	I_R	V_R = 5V		10		µA
Temperature Coefficient of Forward Voltage	$\Delta V_F/°C$			-2.0		mV/°C

NOTES:
8. The luminous intensity at a specific ambient temperature, $I_V(T_A)$, may be calculated from this relationship: $I_V(T_A) = I_{V(25\ C)}(.985)^{(T_A - 25°C)}$
9. The dominant wavelength λ_d, is derived from the C.I.E. Chromaticity Diagram and represents the single wavelength which defines the color of the device.
10. Operation at peak currents of less than 6.0 mA is not recommended.

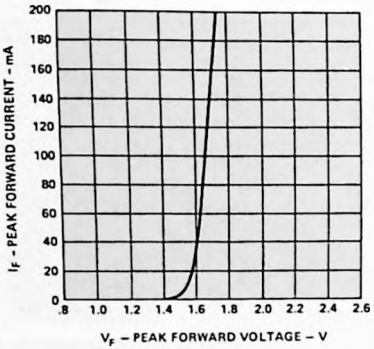


Figure 5. Peak Forward Current vs. Peak Forward Voltage.

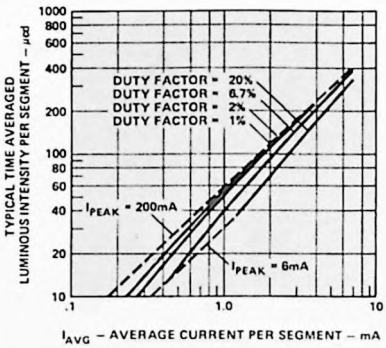


Figure 6. Typical Time Averaged Luminous Intensity per Segment vs. Average Current per Segment.

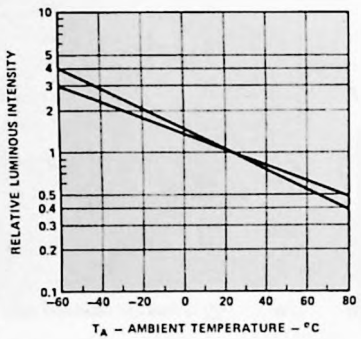


Figure 7. Relative Luminous Intensity vs. Ambient Temperature at Fixed Current Level.

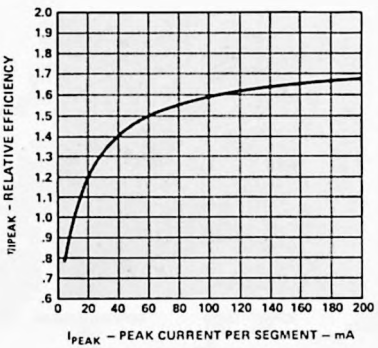


Figure 8. Relative Luminous Efficiency vs. Peak Current per Segment.

Mechanical

These devices are constructed on a standard printed circuit board substrate. A separately molded plastic lens is attached to the PC board over the digits. The lens is an acrylic styrene material that gives good optical lens performance, but is subject to scratching so care should be exercised in handling.

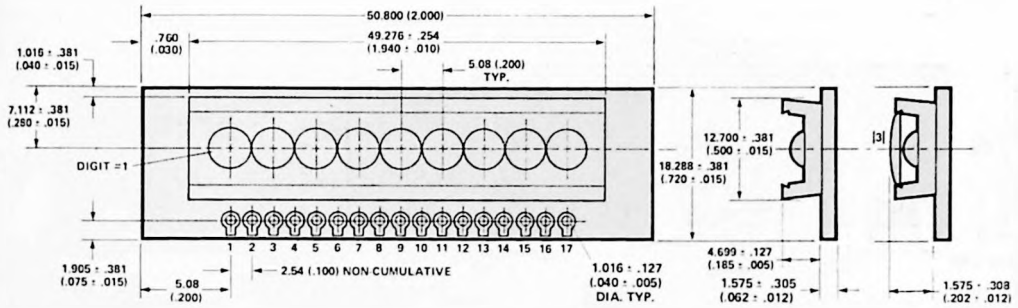
The device may be mounted either by use of pins which may be hand soldered into the plated through holes at the connector edge of the PC board or by insertion into a standard PC board connector. The devices may be hand soldered for up to 3 seconds per tab at a maximum soldering temperature of 230°C. Heat should be applied only to the edge connector tab areas of the PC board. Heating other areas of the board to temperatures in excess of 85°C can result in permanent damage to the display. It is recommended that a non-activated rosin core wire solder or a low temperature deactivating flux and solid wire solder be used in soldering operations.

The PC board is silver plated. To prevent the formation of a tarnish (Ag_2S) which could impair solderability the displays should be stored in the unopened shipping packages until they are used. Further information on the storage, handling, and cleaning of silver plated components is contained in Hewlett-Packard Application Bulletin No. 3.

Electrical/Optical

The HP 5082-7441, -7446, -7285 and 7295 devices utilize a monolithic GaAsP chip containing 7 segments and a decimal point for each display digit. The segments of each digit are interconnected, forming an 8 by N line array, where N is the number of digits in the display. Each chip is positioned under a separate element of a plastic magnifying lens, producing a magnified character. Satisfactory viewing will be realized within an angle of approximately ±20° from the centerline of the digit. A filter, such as plexiglass 2423, Panelgraphic 60 or 63, and Homalite 100-1600, will lower the ambient reflectance and improve display contrast. Digit encoding of these devices is performed by standard 7 segment decoder driver circuits.

Package Dimensions

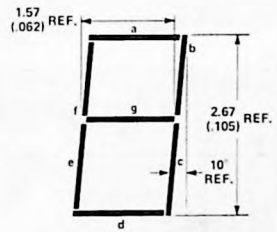


NOTES: 1. Dimensions in millimeters and (inches).
2. Logo and part number are on back of package.
3. Secondary 1.25X magnifier that slides into primary lens and increases character height to 3.33 (.131) available as special product.
4. Tolerances: ±.881 (.015)

Figure 9. 5082-7441

Magnified Character Font Description

5082-7441



Note: All dimensions in millimeters and (inches).

Figure 10.

Device Pin Description

Pin No.	5082-7441 Function	Pin No.	5082-7441 Function
1	Dig. 1 Cathode	10	Seg. d Anode
2	Seg. c Anode	11	Dig. 6 Cathode
3	Dig. 2 Cathode	12	Seg. g Anode
4	d.p. Anode	13	Dig. 7 Cathode
5	Dig. 3 Cathode	14	Seg. b Anode
6	Seg. a Anode	15	Dig. 8 Cathode
7	Dig. 4 Cathode	16	Seg. f Anode
8	Seg. e Anode	17	Dig. 9 Cathode
9	Dig. 5 Cathode		

Package Dimensions

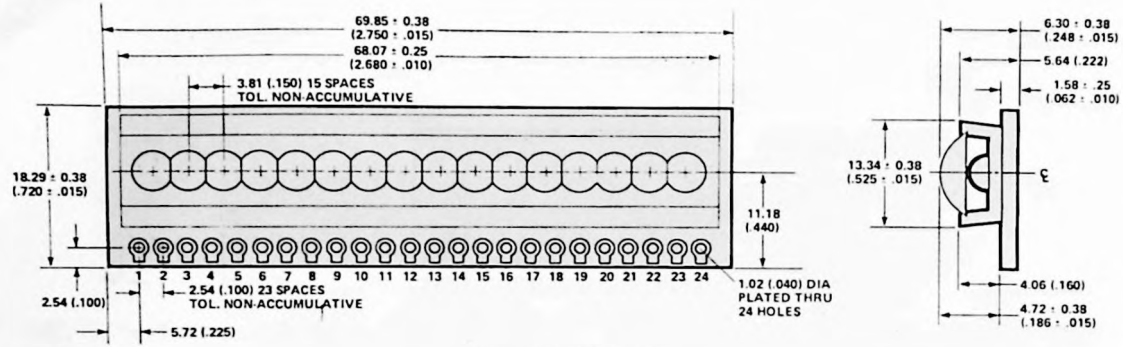
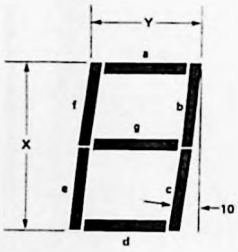


Figure 11. 5082-7446

Magnified Character Font Description



DEVICE	X	Y
5082-7446	2.92 (.115)	1.40 (.055)

NOTES: 1. ALL DIMENSIONS IN MILLIMETRES AND (INCHES).
2. TOLERANCES ON ALL DIMENSIONS ARE ±0.38 (.015) UNLESS OTHERWISE SPECIFIED.

Figure 12.

Device Pin Description

Pin No.	5082-7446 Function
1	Cathode-Digit 1
2	Cathode-Digit 2
3	Cathode-Digit 3
4	Cathode-Digit 4
5	Cathode-Digit 5
6	Anode-Segment e
7	Cathode-Digit 6
8	Anode-Segment d
9	Cathode-Digit 7
10	Anode-Segment a
11	Cathode-Digit 8
12	Anode-Segment DP
13	Cathode-Digit 9
14	Anode-Segment c
15	Cathode-Digit 10
16	Anode-Segment g
17	Cathode-Digit 11
18	Anode-Segment b
19	Cathode-Digit 12
20	Anode-Segment f
21	Cathode-Digit 13
22	Cathode-Digit 14
23	Cathode-Digit 15
24	Cathode-Digit 16

Package Dimensions

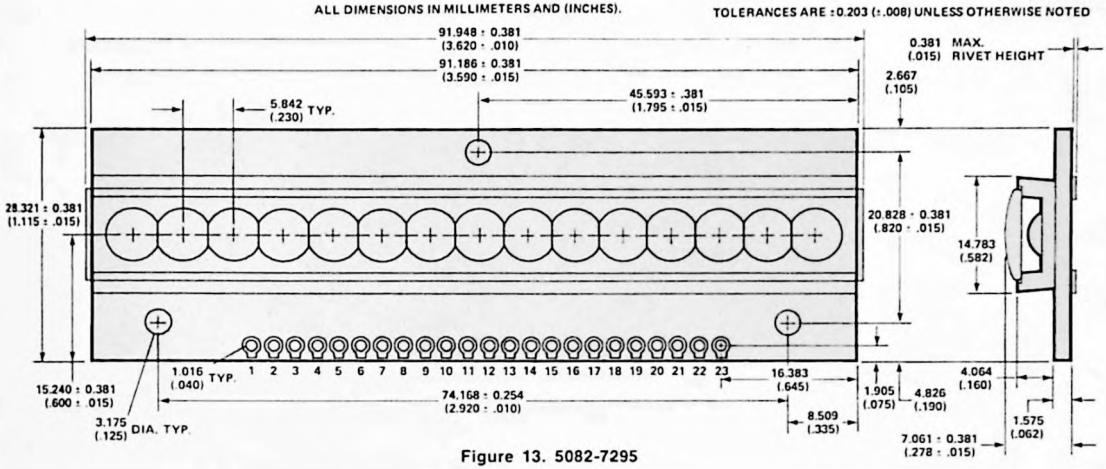


Figure 13. 5082-7295

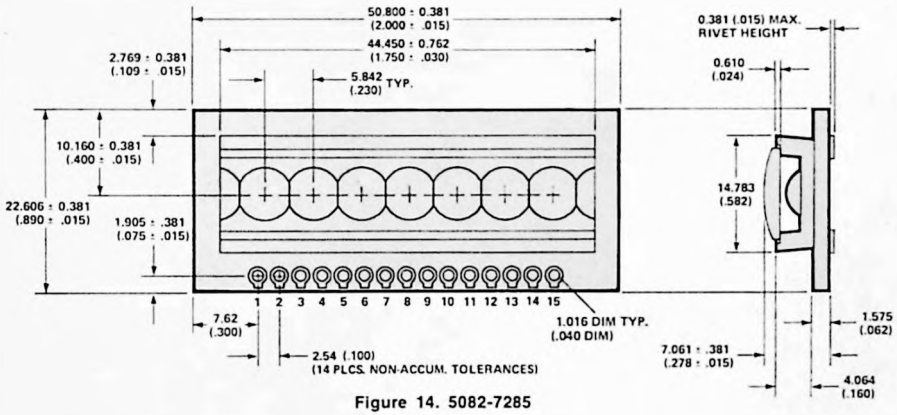


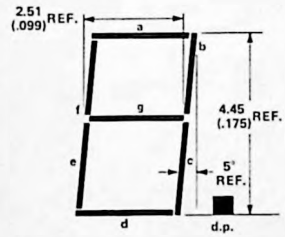
Figure 14. 5082-7285

Magnified Character Font Description

DEVICES

5082-7285

5082-7295



ALL DIMENSIONS IN MILLIMETERS AND (INCHES).

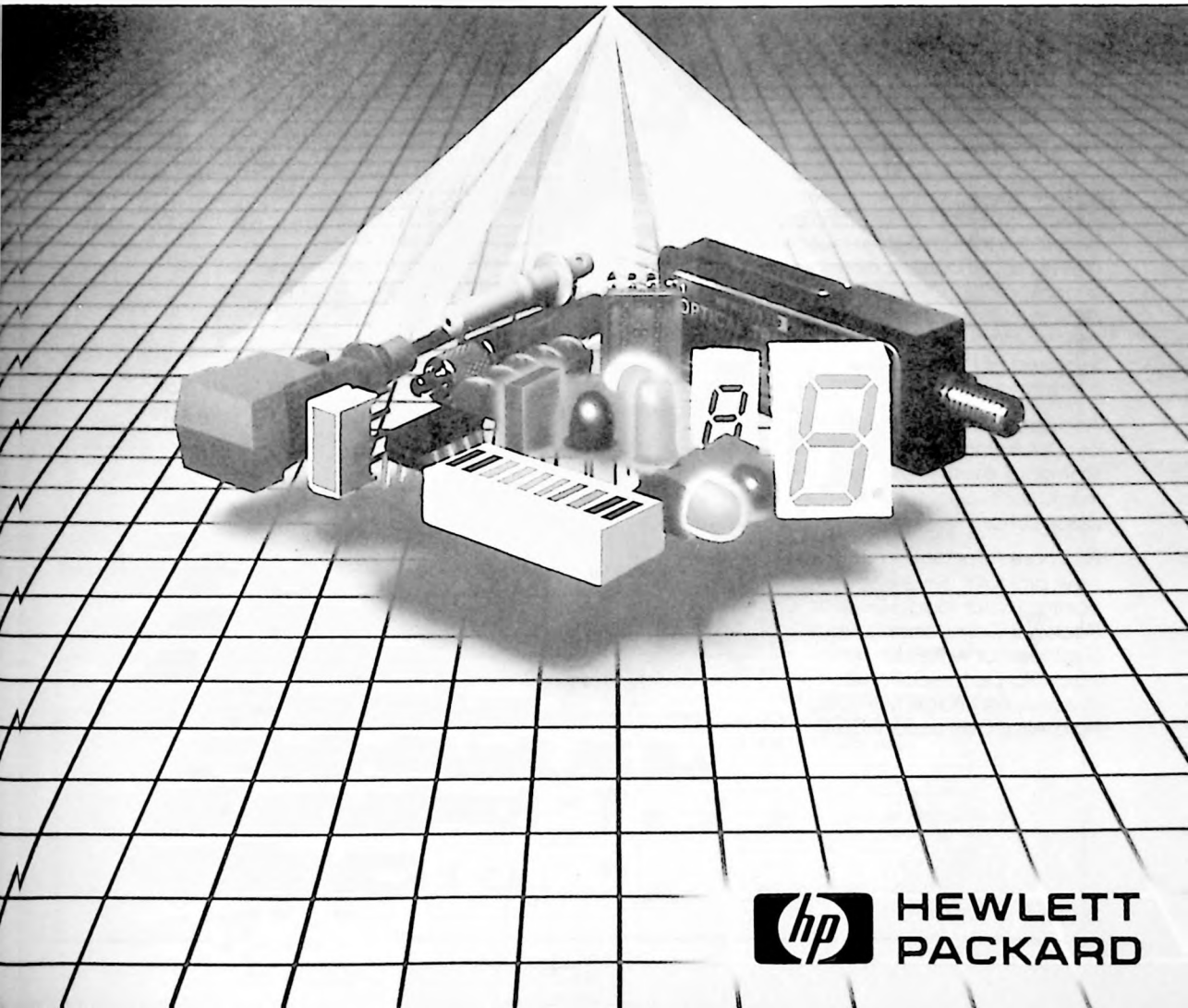
Figure 15.

Device Pin Description

Pin No.	5082-7285 Function	5082-7295 Function
1	Anode Segment b	Cathode Digit 1
2	Anode Segment g	Cathode Digit 2
3	Anode Segment e	Cathode Digit 3
4	Cathode Digit 1	Cathode Digit 4
5	Cathode Digit 2	Anode Segment dp
6	Cathode Digit 3	Cathode Digit 5
7	Cathode Digit 4	Anode Segment c
8	Cathode Digit 5	Cathode Digit 6
9	Cathode Digit 6	Anode Segment e
10	Cathode Digit 7	Cathode Digit 7
11	Anode Segment dp	Anode Segment a
12	Anode Segment d	Cathode Digit 8
13	Anode Segment c	Anode Segment g
14	Anode Segment a	Cathode Digit 9
15	Anode Segment f	Anode Segment d
16		Cathode Digit 10
17		Anode Segment f
18		Cathode Digit 11
19		Anode Segment b
20		Cathode Digit 12
21		Cathode Digit 13
22		Cathode Digit 14
23		Cathode Digit 15

4. Shaft Encoders

- 28 mm Diameter Encoders
- 56 mm Diameter Encoders



HEWLETT PACKARD

Shaft Encoders

As an extension of our emitter/detector systems capability, Hewlett-Packard has developed optical shaft encoding systems. HP's optical encoders are motion sensors that provide a digital link converting mechanical shaft rotation into TTL logic level signals. Encoders are used in a wide variety of closed loop servo applications varying from computer peripherals and professional audio-video systems to automated production equipment. Encoders also find widespread usage in industrial and instrument applications where digital information is needed to monitor rotary motion.

With three easy to assemble components, the HP encoder system takes advantage of a specialized optical design and a custom integrated circuit to deliver superior performance in a compact package. The design also minimizes the mechanical tolerances required of the shaft and mounting surface.

A range of products are available including options for standard shaft sizes and count resolutions ideal for your application.

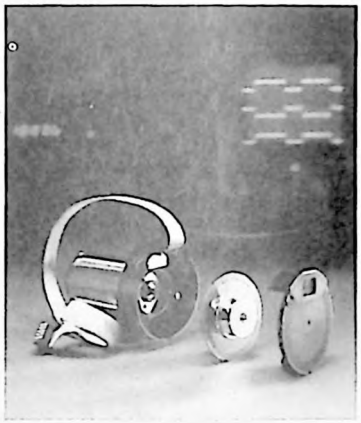
For more information on these new product developments, contact your local Hewlett-Packard Components Field Engineer, or write Hewlett-Packard Optoelectronics Division, 640 Page Mill Road, Palo Alto, California 94304.

HP System Features

- Fully tested, prealigned components
- Quick assembly — No special tools required
- 2 digital outputs in quadrature
- 1 digital index channel
- Fully integrated electronics for high performance and high reliability
- Balanced system compensates for variations in components over time and temperature
- TTL compatible
- 130 KHz minimum frequency response
- -20°C to 85°C operating range
- 0.25 mm (.010 inches) shaft endplay allowance

28 mm Diameter Encoders

- Small Size
- Low Inertia



56 mm Diameter Encoders

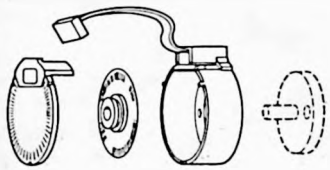
- High Resolution
- Large Shaft Sizes

Optical Shaft Encoders

28 mm Diameter Encoders — HEDS-5000 Series

Package Outline Drawing	Part No.	Channels	Option Code: Resolution	Option Code: Shaft Size	Page No.
	HEDS-5000 OPT □ □□	A, B	□ C 100 CPR D 192 CPR E 200 CPR F 256 CPR G 360 CPR H 400 CPR A 500 CPR I 512 CPR	□□ 01 2 mm 02 3 mm 03 1/8 in. 04 5/32 in. 05 3/16 in. 06 1/4 in. 11 4 mm 14 5 mm	4-4
	HEDS-5010 OPT □ □□	A, B, I			

56 mm Diameter Encoders — HEDS-6000 Series

Package Outline Drawing	Part No.	Channels	Option Code: Resolution	Option Code: Shaft Size	Page No.
	HEDS-6000 OPT □ □□	A, B	□ E 200 CPR H 400 CPR A 500 CPR I 512 CPR B 1000 CPR J 1024 CPR	□□ 05 3/16 in. 06 1/4 in. 07 5/16 in. 08 3/8 in. 09 1/2 in. 10 5/8 in. 11 4 mm 12 6 mm 13 8 mm	4-12
	HEDS-6010 OPT □ □□	A, B, I			

Convenience Assembly Tools for 28 mm Diameter Encoders — Not Required

Package Outline Drawing	Part No.	Description	Page No.
	HEDS-8930	HEDS-5000 Series Tool Kit • Holding Screwdriver • Torque Limiting Screwdriver • HEDS-8920 Hub Puller • HEDS-8922 Gap Setter	4-4
	HEDS-892X	Centering Cones • Aid in High Volume Assembly • Order in Appropriate Shaft Size	

HEWLETT PACKARD

28 mm DIAMETER TWO AND THREE CHANNEL INCREMENTAL OPTICAL ENCODER KIT

HEDS-5000 SERIES

TECHNICAL DATA JANUARY 1984

Features

- SMALL SIZE — 28 mm DIAMETER
- 100-512 CYCLES/REVOLUTION AVAILABLE
- MANY RESOLUTIONS STANDARD
- LOW INERTIA
- QUICK ASSEMBLY
- 0.25 mm (.010 INCHES) END PLAY ALLOWANCE
- TTL COMPATIBLE DIGITAL OUTPUT
- SINGLE 5V SUPPLY
- WIDE TEMPERATURE RANGE
- INDEX PULSE AVAILABLE

Description

The HEDS-5000 series is a high resolution incremental optical encoder kit emphasizing reliability and ease of assembly. The 28 mm diameter package consists of 3 parts: the encoder body, a metal code wheel, and an emitter end plate. An LED source and lens transmit collimated light from the emitter module through a precision metal code wheel and phase plate into a bifurcated detector lens.

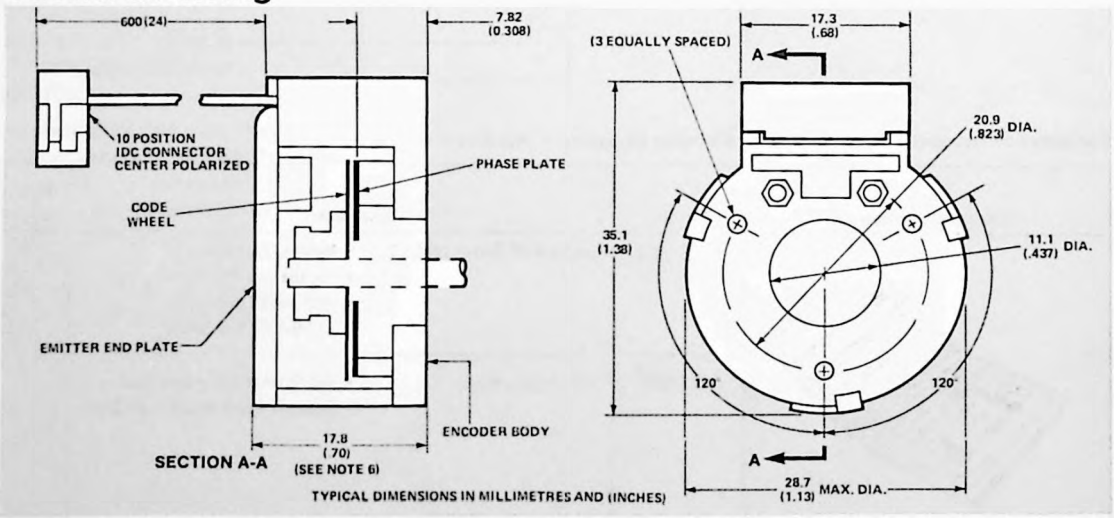
The light is focused onto pairs of closely spaced integrated detectors which output two square wave signals in quadrature and an optional index pulse. Collimated light and a custom photodetector configuration increase long life reliability by reducing sensitivity to shaft end play, shaft eccentricity and LED degradation. The outputs and the 5V supply input of the HEDS-5000 are accessed through a 10 pin connector mounted on a .6 metre ribbon cable.

A standard selection of shaft sizes is available and resolutions between 100 and 512 cycles per revolution are available as options. The part number for the standard 2 channel kit is HEDS-5000, while that for the 3 channel device, with index pulse, is HEDS-5010. See Ordering Information for more details.

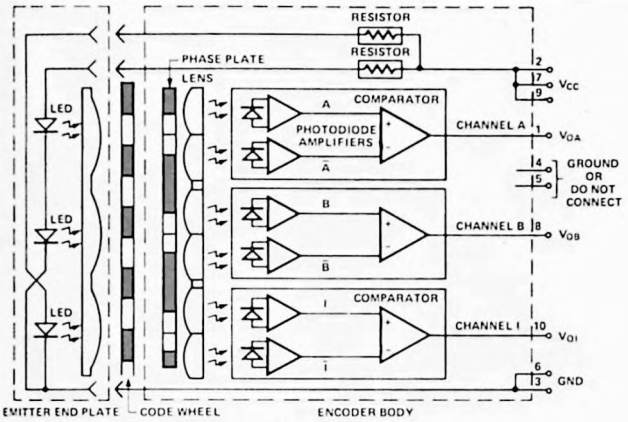
Applications

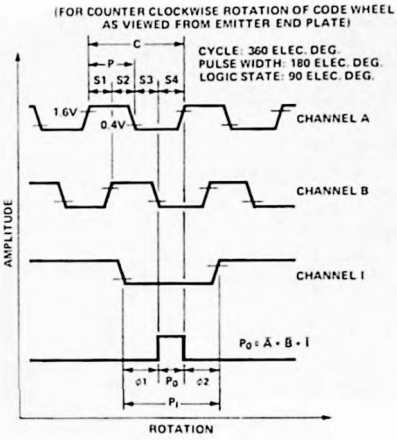
Printers, Plotters, Tape Drives, Positioning Tables, Automatic Handlers, Robots, and any other servo loop where a small high performance encoder is required.

Outline Drawing



Block Diagram and Output Waveforms





Theory of Operation

The incremental shaft encoder operates by translating the rotation of a shaft into interruptions of a light beam which are then output as electrical pulses.

In the HEDS-5XXX the light source is a Light Emitting Diode collimated by a molded lens into a parallel beam of light. The Emitter End Plate contains two or three similar light sources, one for each channel.

The standard Code Wheel is a metal disc which has N equally spaced apertures around its circumference. A matching pattern of apertures is positioned on the stationary phase plate. The light beam is transmitted only when the apertures in the code wheel and the apertures in the phase plate line up; therefore, during a complete shaft revolution, there will be N alternating light and dark periods. A molded lens beneath the phase plate aperture collects the modulated light into a silicon detector.

The Encoder Body contains the phase plate and the detection elements for two or three channels. Each channel consists of an integrated circuit with two photodiodes and amplifiers, a comparator, and output circuitry.

The apertures for the two photodiodes are positioned so that a light period on one detector corresponds to a dark period on the other ("push-pull"). The photodiode signals are amplified and fed to the comparator whose output changes state when the difference of the two photocurrents changes sign. The second channel has a similar configuration but the location of its aperture pair provides an output which is in quadrature to the first channel (phase difference of 90°). Direction of rotation is determined by observing which of the channels is the leading waveform. The outputs are TTL logic level signals.

The optional index channel is similar in optical and electrical configuration to the A and B channels previously described. An index pulse of typically 1 cycle width is generated for each rotation of the code wheel. Using the recommended logic interface, a unique logic state (P_0) can be identified if such accuracy is required.

The three part kit is assembled by attaching the Encoder Body to the mounting surface using three screws. The Code Wheel is set to the correct gap and secured to the shaft. Snapping the cover (Emitter End Plate) on the body completes the assembly. The only adjustment necessary is the encoder centering relative to the shaft. This optimizes quadrature and the optional index pulse outputs.

Index Pulse Considerations

The motion sensing application and encoder interface circuitry will determine the necessary phase relationship of the index pulse to the main data tracks. A unique shaft position can be identified by using the index pulse output only or by logically relating the index pulse to the A and B data channels. The HEDS-5010 allows some adjustment of the index pulse position with respect to the main data channels. The position is easily adjusted during the assembly process as illustrated in the assembly procedures.

Definitions

Electrical degrees:

1 shaft rotation = 360 angular degrees
= N electrical cycles

1 cycle = 360 electrical degrees

Position Error:

The angular difference between the actual shaft position and its position as calculated by counting the encoder's cycles.

Cycle Error:

An indication of cycle uniformity. The difference between an observed shaft angle which gives rise to one electrical cycle, and the nominal angular increment of 1/N of a revolution.

Phase:

The angle between the center of Pulse A and the center of Pulse B.

Index Phase:

For counter clockwise rotation as illustrated above, the Index Phase is defined as:

$$\Phi_1 = \frac{(\phi_1 - \phi_2)}{2}.$$

ϕ_1 is the angle, in electrical degrees between the falling edge of I and falling edge of B. ϕ_2 is the angle, in electrical degrees, between the rising edge of A and the rising edge of I.

Index Phase Error:

The Index Phase Error ($\Delta\Phi_I$) describes the change in the Index Pulse position after assembly with respect to the A and B channels over the recommended operating conditions.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_S	-55	100	°Celsius	
Operating Temperature	T_A	-55	100	°Celsius	See Note 1
Vibration			20	g	See Note 1
Shaft Axial Play			.50 (20)	mm(1inch/1000) TIR	
Shaft Eccentricity Plus Radial Play			.1 (4)	mm(1inch/1000) TIR	Movement should be limited even under shock conditions.
Supply Voltage	V_{CC}	-0.5	7	Volts	
Output Voltage	V_O	-0.5	V_{CC}	Volts	
Output Current per Channel	I_O	-1	5	mA	
Velocity			30,000	R.P.M.	
Acceleration	α		250,000	Rad. Sec^{-2}	

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Notes
Temperature	T	-20	85	°Celsius	Non-condensing atmos.
Supply Voltage	Vcc	4.5	5.5	Volt	Ripple < $100mV_{p-p}$
Code Wheel Gap			1.1 (45)	mm (inch/1000)	Nominal gap = 0.63 mm (.025 in.) when shaft is at minimum gap position.
Shaft Perpendicularity Plus Axial Play			0.25 (10)	mm (inch/1000) TIR	
Shaft Eccentricity Plus Radial Play			0.04 (1.5)	mm (inch/1000) TIR	10 mm (0.4 inch) from mounting surface.
Load Capacitance	C_L		100	pF	

Encoding Characteristics

The specifications below apply within the recommended operating conditions and reflect performance at 500 cycles per revolution (N = 500). Some encoding characteristics improve with decreasing cycles (N). Consult Application Note 1011 or factory for additional details.

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes (See Definitions)
Position Error - Worst Error Full Rotation	$\Delta\Theta$		10	40	Minutes of Arc	1 Cycle = 43.2 Minutes See Figure 5.
Cycle Error - Worst Error Full Rotation	ΔC		3	5.5	Electrical deg.	
Max. Count Frequency	f_{MAX}	130,000	200,000		Hertz	f = Velocity (RPM) x N/60
Pulse Width Error - Worst Error Full Rotation	ΔP		16		Electrical deg.	T = 25° C, f = 8 KHz See Note 2
Phase Sensitivity to Eccentricity			520 (13)		Elec. deg./mm (Elec. deg./mil)	mil = inch/1000
Phase Sensitivity to Axial Play			20 (.5)		Elec. deg./mm (Elec. deg./mil)	mil = inch/1000
Logic State Width Error - Worst Error Full Rotation	ΔS		25		Electrical deg.	T = 25° C, f = 8 KHz See Note 2
Index Pulse Width	P_I		360		Electrical deg.	T = 25° C, f = 8 KHz See Note 3
Index Phase Error	$\Delta\Phi_I$		0	17	Electrical deg.	See Notes 4, 5
Index Pulse Phase Adjustment Range		±70	±130		Electrical deg.	See Note 5

Mechanical Characteristics

Parameter	Symbol	Dimension	Tolerance	Units	Notes
Outline Dimensions		See Mech. Dwg.			
Code Wheel Available to Fit the Following Standard Shaft Diameters		2 4 3 5	+.000 −.015	mm	
		5/32	+.0002 −.0005	inches	
		1/8 3/16 1/4	+.0000 −.0007	inches	
Moment of Inertia	J	0.4 (6 x 10^{-6})		gcm² (oz-in-s²)	
Required Shaft Length		12.8 (.50)	±0.5 (±0.02)	mm (inches)	See Figure 10. Shaft in minimum length position.
Bolt Circle		20.9 (.823)	±0.13 (±.005)	mm (inches)	See Figure 10.
Mounting Screw Size		1.6 x 0.35 x 5 mm DIN 84 or 0-80 x 3/16 Binding Head		mm inches	

Electrical Characteristics When operating within the recommended operating range.

Electrical Characteristics over Recommended Operating Range (Typical at 25° C).

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Current	I_{CC}		21	40	mA	HEDS-5000 (2 Channel)
			36	60		HEDS-5010 (3 Channel)
High Level Output Voltage	V_{OH}	2.4			V	I_{OH} = -40μA Max.
Low Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 3.2 mA
Rise Time	t_r		0.5		μs	C_L = 25 pF, R_L = 11K Pull-up
Fall Time	t_f		0.2			See Note 7
Cable Capacitance	C_{CO}		12		pF/metres	Output Lead to Ground

NOTES:

1. The structural parts of the HEDS-5000 have been tested to 20g and up to 500 Hz. For use outside this range, operation may be limited at low frequencies (high displacement) by cable fatigue and at high frequencies by code wheel resonances. Resonant frequency depends on code wheel material and number of counts per revolution. For temperatures below -20° C the ribbon cable becomes brittle and sensitive to displacements. Maximum operating and storage temperature includes the surface area of the encoder mounting. Consult factory for further information. See Application Note 1011.
2. In a properly assembled lot 99% of the units, when run at 25° C and 8 KHz, should exhibit a pulse width error less than 35 electrical degrees, and a state width error less than 45 electrical degrees. To calculate errors at other speeds and temperatures add the values specified in Figures 1 or 2 to to the typical values specified under encoding characteristics or to the maximum 99% values specified in this note.
3. In a properly assembled lot, 99% of the units when run at 25° C and 8 KHz should exhibit an index pulse width greater than 260 electrical degrees and less than 460 electrical degrees. To calculate index pulse widths at other speeds and temperatures add the values specified in Figures 3 or 4 to the typical 360° pulse width or to the maximum 99% values specified in this note.
4. After adjusting index phase at assembly, the index phase error specification ($\Delta\Phi_I$) indicates the expected shift in index pulse position with respect to channels A and B over the range of recommended operating conditions and up to 50 KHz.
5. When the index pulse is centered on the low-low states of channels A and B as shown on page 2, a unique P_O can be defined once per revolution within the recommended operating conditions and up to 25 KHz. Figure 6 shows how P_O can be derived from A, B, and I outputs. The adjustment range indicates how far from the center of the low-low state that the center of the index pulse may be adjusted.
6. The typical length of an assembled HEDS-5000 encoder is 17.8 (.70 inch). However, it is recommended that room be left to accomodate a length of 21.6 (.85 inch). Future developments may result in an enhanced version of the HEDS-5000 encoder that is slightly longer.
7. The rise time is primarily a fuction of the RC time constant of R_L and C_L. A faster rise time can be achieved with either a lower value of R_L or C_L. Care must be observed not to exceed the recommended value of I_{OL} under worst case conditions.

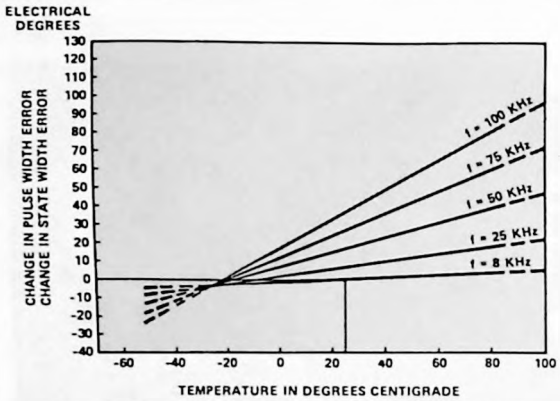


Figure 1. Typical Change in Pulse Width Error or in State Width Error due to Speed and Temperature

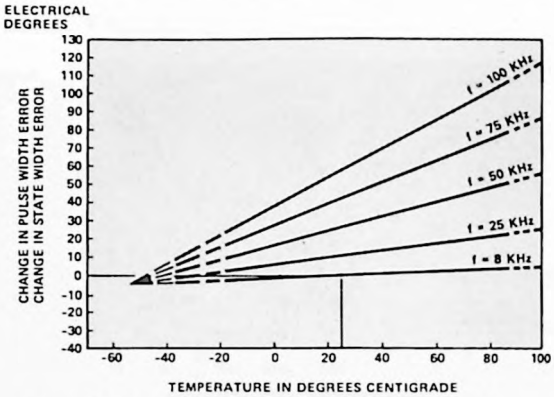


Figure 2. Maximum Change in Pulse Width Error or in State Width Error Due to Speed and Temperature

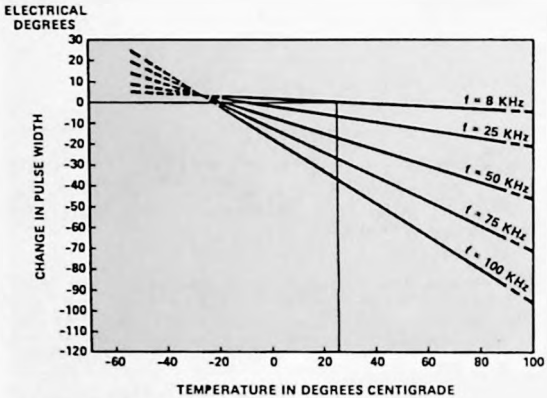


Figure 3. Typical Change in Index Pulse Width Due to Speed and Temperature

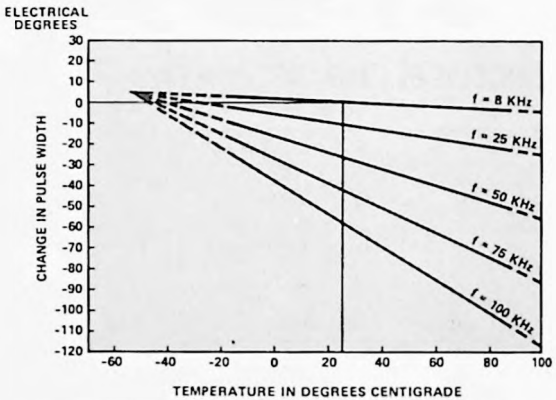


Figure 4. Maximum Change in Index Pulse Width Due to Speed and Temperature

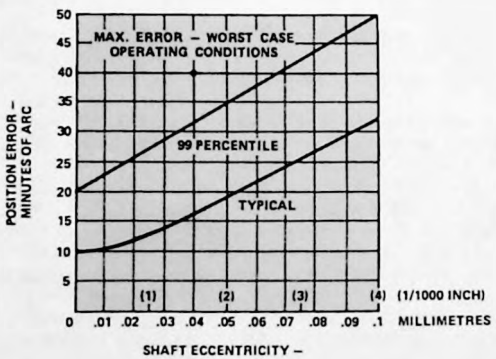
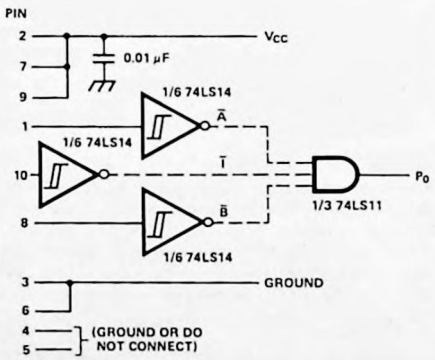
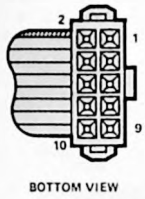


Figure 5. Position Error vs. Shaft Eccentricity



DASHED LINES REPRESENT AN OPTIONAL INDEX SUMMING CIRCUIT. STANDARD 74 SERIES COULD ALSO BE USED TO IMPLEMENT THIS CIRCUIT.

Figure 6. Recommended Interface Circuit



BOTTOM VIEW

PINOUT

PIN #	FUNCTION
1	CHANNEL A
2	V_{CC}
3	GROUND
4	N.C. OR GROUND
5	N.C. OR GROUND
6	GROUND
7	V_{CC}
8	CHANNEL B
9	V_{CC}
10	CHANNEL I

NOTE: REVERSE INSERTION OF THE CONNECTOR WILL PERMANENTLY DAMAGE THE DETECTOR IC.

MATING CONNECTOR
BERG 65-692-001 OR EQUIVALENT

Figure 7. Connector Specifications

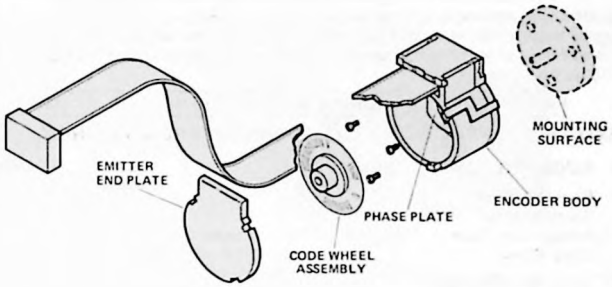


Figure 8. HEDS-5000 Series Encoder Kit

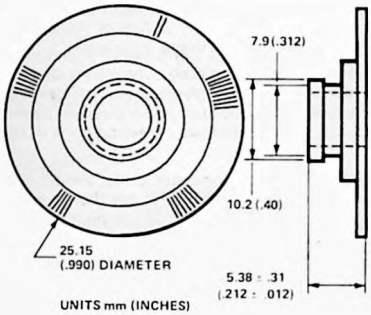


Figure 9. Code Wheel

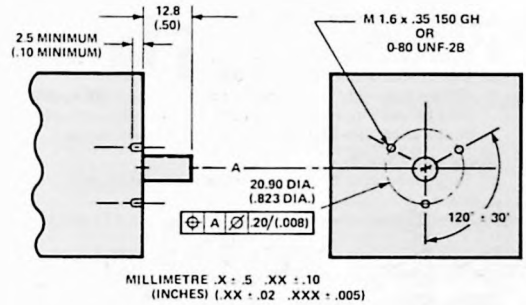


Figure 10. Mounting Requirements

Ordering Information

HEDS-5 ☐☐☐
OPTION* ☐☐

RESOLUTION (CYCLES PER REVOLUTION)

C – 100 CPR	G – 360 CPR
D – 192 CPR	H – 400 CPR
E – 200 CPR	A – 500 CPR
F – 256 CPR	I – 512 CPR

NOTE: OTHER RESOLUTIONS AVAILABLE ON SPECIAL REQUEST.

SHAFT DIAMETER

01 – 2 mm
02 – 3 mm
03 – 1/8 in.
04 – 5/32 in.
05 – 3/16 in.
06 – 1/4 in.
11 – 4 mm
14 – 5 mm
00 – USE WHEN ORDERING ENCODER BODIES

PRODUCT TYPE

0 – 28 mm COMPLETE KIT
1 – 28 mm CODE WHEEL
2 – 28 mm ENCODER BODY
3 – 28 mm EMITTER END PLATE*

OUTPUTS

0 – 2 CHANNEL DIGITAL
1 – 3 CHANNEL DIGITAL

MECHANICAL CONFIGURATION

0 – 0.6 m (24 in.) CABLE

*NO OPTION IS SPECIFIED WHEN ORDERING EMITTER END PLATES ONLY.

Shaft Encoder Kit Assembly **See Application Note 1011 for further discussion.**

The following assembly procedure represents a simple and reliable method for prototype encoder assembly. High volume assembly may suggest modifications to this procedure using custom designed tooling. In certain high volume applications encoder assembly can be accomplished in less than 30 seconds. Consult factory for further details. Note: The code wheel to phase plate gap should be set between 0.015 in. and 0.045 in.

WARNING: THE ADHESIVES USED MAY BE HARMFUL. CONSULT THE MANUFACTURER'S RECOMMENDATIONS.

READ THE INSTRUCTIONS TO THE END BEFORE STARTING ASSEMBLY.

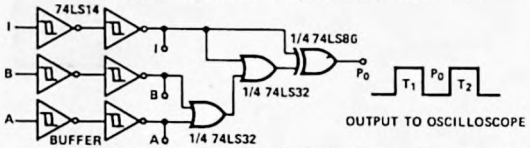
1.0 SUGGESTED MATERIALS

1.1 Encoder Parts
Encoder Body
Emitter End Plate
Code Wheel

1.2 Assembly Materials
RTV — General Electric 162
— Dow Corning 3145
Epoxy—Hysol 1C
Acetone
Mounting Screws (3)
RTV and Epoxy Applicators

1.3 Suggested Assembly Tools
a) Holding Screwdriver.
b) Torque Limiting Screwdriver, 0.36 cm kg (5.0 in. oz.).
c) Depth Micrometer or HEDS-8922 Gap Setter.
d) Oscilloscope or Phase Meter (Described in AN 1011). Either may be used for two channel phase adjustment. An oscilloscope is required for index pulse phase adjustment.

1.4 Suggested Circuits
a) Suggested circuit for index adjustment (HEDS-5010).



For optimal index phase, adjust encoder position to equalize T_1 and T_2 pulse widths.

b) Phase Meter Circuit
Recommended for volume assembly. Please see Application Note 1011 for details.

2.0 SURFACE PREPARATION

THE ELAPSED TIME BETWEEN THIS STEP AND THE COMPLETION OF STEP 8 SHOULD NOT EXCEED 1/2 HOUR.

2.1 Clean and degrease with acetone the mounting surface and shaft making sure to keep the acetone away from the motor bearings.

2.2 Load the syringe with RTV.

2.3 Apply RTV into screw threads on mounting surface. Apply more RTV on the surface by forming a daisy ring pattern connecting the screw holes as shown above.

CAUTION: KEEP RTV AWAY FROM THE SHAFT BEARING.

3.0 ENCODER BODY ATTACHMENT

3.1 Place the encoder body on the mounting surface and slowly rotate the body to spread the adhesive. Align the mounting screw holes with the holes in the body base.

3.2 Place the screws in the holding screwdriver and thread them into the mounting holes. Tighten to approximately 0.36 cm kg (5.0 in. oz.) using a torque limiting screwdriver if available (See notes a and b below). Remove centering cone if used.

Notes:
a) At this torque value, the encoder body should slide on the mounting surface only with considerable thumb pressure.
b) The torque limiting screwdriver should be periodically calibrated for proper torque.

4.0 EPOXY APPLICATION

CAUTION: HANDLE THE CODE WHEEL WITH CARE.

4.1 Collect a small dab of epoxy on an applicator.

4.2 Spread the epoxy inside the lower part of the hub bore.

4.3 Holding the code wheel by its hub, slide it down the shaft just enough to sit it squarely. About 3 mm (1/8").

5.0 CODE WHEEL POSITIONING

5.1 Take up any loose play by lightly pulling down on the shaft's load end.

5.2 Using the gap setter or a depth micrometer, push the code wheel hub down to a depth of 1.65 mm (.065 in.) below the rim of the encoder body. The registration holes in the gap setter will align with the snaps protruding from the encoder body near the cable.

5.3 Check that the gap setter or micrometer is seated squarely on the body rim and maintains contact with the code wheel hub.

5.4 No epoxy should extrude through the shaft hole.

DO NOT TOUCH THE CODE WHEEL AFTER ASSEMBLY.

6.0 EMITTER END PLATE

6.1 Visually check that the wire pins in the encoder body are straight and straighten if necessary.

6.2 Hold the end plate parallel to the encoder body rim. Align the guiding pin on the end plate with the hole in the encoder body and press the end plate straight down until it is locked into place.

6.3 Visually check to see if the end plate is properly seated.

7.0 PHASE ADJUSTMENT

7.1 The following procedure should be followed when phase adjusting channels A and B.

7.2 Connect the encoder cable.

7.3 Run the motor. Phase corresponds to motor direction. See output waveforms and definitions. Using either an oscilloscope or a phase meter, adjust the encoder for minimum phase error by sliding the encoder forward or backward on the mounting surface as shown above. See Application Note 1011 for the phase meter circuit.

7.4 No stress should be applied to the encoder package until the RTV cures. Cure time is 2 hours @ 70° C or 24 hrs. at room temperature.

Note: After mounting, the encoder should be free from mechanical forces that could cause a shift in the encoder's position relative to its mounting surface.

CODE WHEEL REMOVAL

In the event that the code wheel has to be removed after the epoxy has set, use the code wheel extractor as follows:

1 Remove the emitter end plate by prying a screwdriver in the slots provided around the encoder body rim. Avoid bending the wire leads.

2 Turn the screw on the extractor counter-clockwise until the screw tip is no longer visible.

3 Slide the extractor's horseshoe shaped lip all the way into the groove on the code wheel's hub.

4 While holding the extractor body stationary, turn the thumb screw clockwise until the screw tip pushes against the shaft.

5 Applying more turning pressure will pull the hub upwards breaking the epoxy bond.

6 Clean the shaft before reassembly.

8.0 INDEX PULSE ADJUSTMENT (HEDS-5010)

8.1 Some applications require that the index pulse be aligned with the main data channels. The index pulse position and the phase must be adjusted simultaneously. This procedure sets index phase to zero.

8.2 Connect the encoder cable.

8.3 Run the motor. Adjust for minimum phase error using an oscilloscope or phase meter (see 7.3).

8.4 Using an oscilloscope and the circuit shown in 1.4, set the trigger for the falling edge of the I output. Adjust the index pulse so that T_1 and T_2 are equal in width. The physical adjustment is a side to side motion as shown by the arrow.

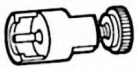
8.5 Recheck the phase adjustment.

8.6 Repeat steps 8.3-8.5 until both phase and index pulse position are as desired.

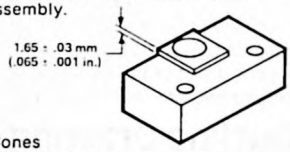
8.7 No stress should be applied to the encoder package until the RTV has cured. Cure time: 2 hours @ 70° C or 24 hrs. at room temperature.

SPECIALITY TOOLS — Available from Hewlett-Packard

a) HEDS-8920 Hub Puller
This tool may be used to remove code wheels from shafts after the epoxy has cured.



b) HEDS-8922 Gap Setter
This tool may be used in place of a depth micrometer as an aid in large volume assembly.



c) HEDS-892X Centering Cones
For easier volume assembly this tool in its appropriate shaft size may be used in step 3.0 to initially center the encoder body with respect to the shaft and aid in locating the mounting screw holes. Depending on the resolution and accuracy required this centering may eliminate the need for phase adjustment steps 7 and 8.

Part Number	Shaft Size
HEDS-8923	2 mm
HEDS-8924	3 mm
HEDS-8925	1/8 in.
HEDS-8926	5/32 in.
HEDS-8927	3/16 in.
HEDS-8928	1/4 in.
HEDS-8929	4 mm
HEDS-8931	5 mm

d) HEDS-8930 HEDS-5000 Tool Kit
1 Holding Screwdriver
1 Torque Limiting Screwdriver, 0.36 cm kg (5.0 in. oz.)
1 HEDS-8920 Hub Puller
1 HEDS-8922 Gap Setter
1 Carrying Case

HEWLETT PACKARD

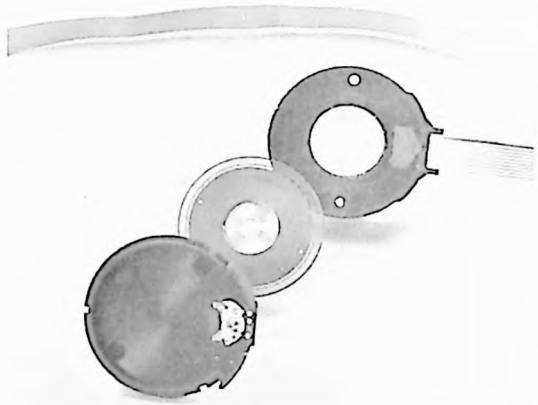
56 mm DIAMETER TWO AND THREE CHANNEL INCREMENTAL OPTICAL ENCODER KIT

HEDS-6000 SERIES

TECHNICAL DATA JANUARY 1984

Features

- 192-1024 CYCLES/REVOLUTION AVAILABLE
- MANY RESOLUTIONS STANDARD
- QUICK ASSEMBLY
- 0.25 mm (.010 INCHES) END PLAY ALLOWANCE
- TTL COMPATIBLE DIGITAL OUTPUT
- SINGLE 5V SUPPLY
- WIDE TEMPERATURE RANGE
- SOLID STATE RELIABILITY
- INDEX PULSE AVAILABLE



Description

The HEDS-6000 series is a high resolution incremental optical encoder kit emphasizing ease of assembly and reliability. The 56 mm diameter package consists of 3 parts: the encoder body, a metal code wheel, and emitter end plate. An LED source and lens transmit collimated light from the emitter module through a precision metal code wheel and phase plate into a bifurcated detector lens.

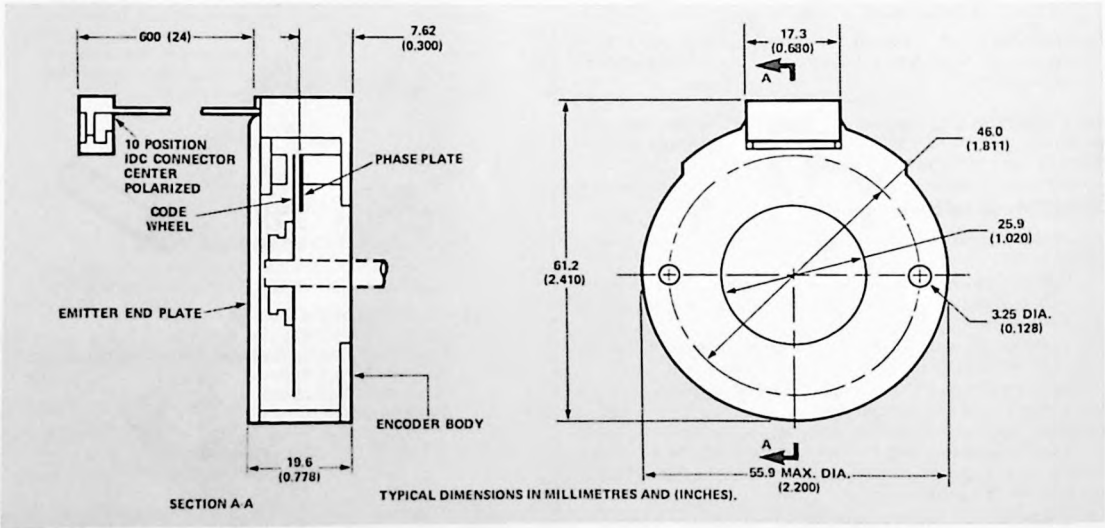
The light is focused onto pairs of closely spaced integrated detectors which output two square wave signals in quadrature and an optional index pulse. Collimated light and a custom photodetector configuration increase long life reliability by reducing sensitivity to shaft end play, shaft eccentricity and LED degradation. The outputs and the 5V supply input of the HEDS-6000 are accessed through a 10 pin connector mounted on a .6 metre ribbon cable.

A standard selection of shaft sizes is available and resolutions between 192 and 1024 cycles per revolution are available as options. The part number for the standard 2 channel bit is HEDS-6000, while that for the 3 channel device, with index pulse, is HEDS-6010. See Ordering Information for more details.

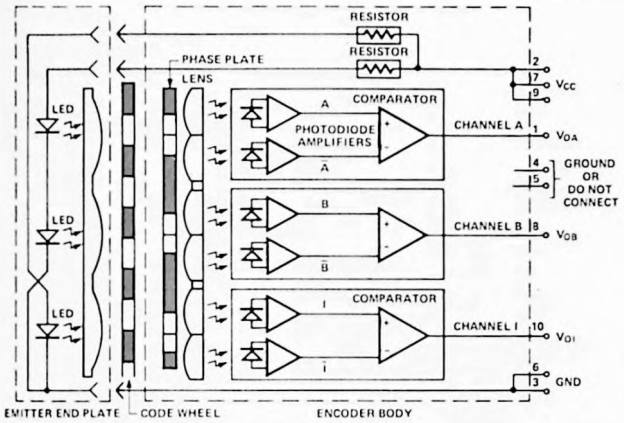
Applications

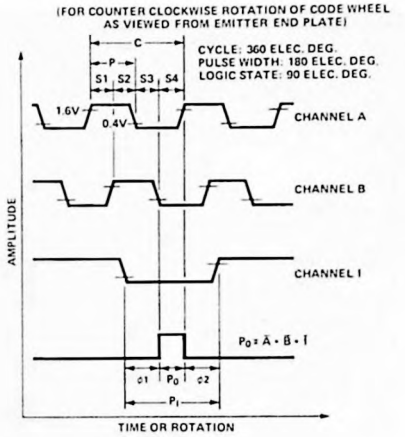
Printers, Plotters, Tape Drives, Positioning Tables, Automatic Handlers, Robots, and any other servo loop where a small high performance encoder is required.

Outline Drawing



Block Diagram and Output Waveforms





Theory of Operation

The incremental shaft encoder operates by translating the rotation of a shaft into interruptions of a light beam which are then output as electrical pulses.

In the HEDS-6XXX the light source is a Light Emitting Diode collimated by a molded lens into a parallel beam of light. The Emitter End Plate contains two or three similar light sources, one for each channel.

The standard Code Wheel is a metal disc which has N equally spaced slits around its circumference. An aperture with a matching pattern is positioned on the stationary phase plate. The light beam is transmitted only when the slits in the code wheel and the aperture line up; therefore, during a complete shaft revolution, there will be N alternating light and dark periods. A molded lens beneath the phase plate aperture collects the modulated light into a silicon detector.

The Encoder Body contains the phase plate and the detection elements for two or three channels. Each channel consists of an integrated circuit with two photodiodes and amplifiers, a comparator, and output circuitry.

The apertures for the two photodiodes are positioned so that a light period on one detector corresponds to a dark period on the other. The photodiode signals are amplified and fed to the comparator whose output changes state when the difference of the two photo currents changes sign ("Push-Pull"). The second channel has a similar configuration but the location of its aperture pair provides an output which is in quadrature to the first channel (phase difference of 90°). Direction of rotation is determined by observing which of the channels is the leading waveform. The outputs are TTL logic level signals.

The optional index channel is similar in optical and electrical configuration to the A,B channels previously described. An index pulse of typically 1 cycle width is generated for each rotation of the code wheel. Using the recommended logic interface, a unique logic state (P_0) can be identified if such accuracy is required.

The three part kit is assembled by attaching the Encoder Body to the mounting surface using two screws. The Code Wheel is set to the correct gap and secured to the shaft. Snapping the cover (Emitter End Plate) on the body completes the assembly. The only adjustment necessary is the encoder centering relative to the shaft, to optimize quadrature and optional index pulse output.

Index Pulse Considerations

The motion sensing application and encoder interface circuitry will determine the need for relating the index pulse to the main data tracks. A unique shaft position is identified by using the index pulse output only or by logically relating the index pulse to the A and B data channels. The HEDS-6010 index pulse can be uniquely related with the A and B data tracks in a variety of ways providing maximum flexibility. Statewidth, pulse width or edge transitions can be used. The index pulse position, with respect to the main data channels, is easily adjusted during the assembly process and is illustrated in the assembly procedures.

Definitions

Electrical degrees:
1 shaft rotation = 360 angular degrees
= N electrical cycles
1 cycle = 360 electrical degrees

Position Error:
The angular difference between the actual shaft position and its position as calculated by counting the encoder's cycles.

Cycle Error:
An indication of cycle uniformity. The difference between an observed shaft angle which gives rise to one electrical cycle, and the nominal angular increment of 1/N of a revolution.

Phase:
The angle between the center of Pulse A and the center of Pulse B.

Index Phase:
For counter clockwise rotation as illustrated above, the Index Phase is defined as:

$$\Phi_I = \frac{(\phi_1 - \phi_2)}{2}.$$

ϕ_1 is the angle, in electrical degrees, between the falling edge of I and falling edge of B. ϕ_2 is the angle, in electrical degrees, between the rising edge of A and the rising edge of I.

Index Phase Error:
The Index Phase Error ($\Delta\Phi_I$) describes the change in the Index Pulse position after assembly with respect to the A and B channels over the recommended operating conditions.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_S	-55	100	°Celsius	
Operating Temperature	T_A	-55	100	°Celsius	See Note 1
Vibration			20	g	See Note 1
Shaft Axial Play			.58 (23)	mm (inch/1000) TIR	
Shaft Eccentricity Plus Radial Play			.25 (10)	mm (inch/1000) TIR	Movement should be limited even under shock conditions.
Supply Voltage	V_{CC}	-0.5	7	Volts	
Output Voltage	V_O	-0.5	V_{CC}	Volts	
Output Current	I_O	-1	5	mA	
Velocity			12,000	R.P.M.	
Acceleration	α		250,000	Rad. Sec^{-2}	

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Notes
Temperature	T	-20	85	°Celsius	Non-condensing atmos.
Supply Voltage	V_{CC}	4.5	5.5	Volt	Ripple < 100mV_{p-p}
Code Wheel Gap			1.1 (45)	mm (inch/1000)	Nominal gap = 0.76 mm (.030 in.) when shaft is at minimum gap position.
Shaft Perpendicularity Plus Axial Play			0.25 (10)	mm (inch/1000) TIR	
Shaft Eccentricity Plus Radial Play			0.04 (1.5)	mm (inch/1000) TIR	10 mm (0.4 inch) from mounting surface.
Load Capacitance	C_L		100	pF	

Encoding Characteristics

The specifications below apply within the recommended operating conditions and reflect performance at 1000 cycles per revolution (N = 1000). Some encoding characteristics improve with decreasing cycles (N). Consult Application Note 1011 or factory for additional details.

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes (See Definitions)
Position Error	$\Delta\Theta$		7	18	Minutes of Arc	1 Cycle = 21.6 Minutes See Figure 5.
Cycle Error	ΔC		3	5.5	Electrical deg.	
Max. Count Frequency	f_{MAX}	130,000	200,000		Hertz	f = Velocity (RPM) x N/60
Pulse Width Error	ΔP		12		Electrical deg.	T = 25° C, f = 8 KHz See Note 2
Phase Sensitivity to Eccentricity			227 (5.8)		Elec. deg./mm (Elec. deg./mil)	mil = inch/1000
Phase Sensitivity to Axial Play			20 (.5)		Elec. deg./mm (Elec. deg./mil)	mil = inch/1000
Logic State Width Error	ΔS		25		Electrical deg.	T = 25° C, f = 8 KHz See Note 2
Index Pulse Width	P_I		360		Electrical deg.	T = 25° C, f = 8 KHz See Note 3
Index Phase Error	$\Delta\Phi_I$		0	17	Electrical deg.	See Notes 4, 5
Index Pulse Adjustment Range			±165		Electrical deg.	

Mechanical Characteristics

Parameter	Symbol	Dimension	Tolerance	Units	Notes
Outline Dimensions		See Mech. Dwg.			
Code Wheel Available to Fit the Following Standard Shaft Diameters		4 6 8	+.000 −.015	mm	
		3/16 3/8 1/4 1/2 5/16 5/8	+.0000 −.0007	inches	
Moment of Inertia	J	7.7 (110 x 10^{-6})		gcm^2 ($oz\text{-}in\text{-}s^2$)	
Required Shaft Length		15.9 (0.625)	±0.6 (±.024)	mm (inches)	See Figure 10. Shaft at minimum length position.
Bolt Circle		46.0 (1.811)	±0.13 (±.005)	mm (inches)	See Figure 10.
Mounting Screw Size		2.5 x 0.45 x 5 OR #2-56 x 3/16 Pan Head		mm inches	

Electrical Characteristics When operating within the recommended operating range.

Electrical Characteristics over Recommended Operating Range (Typical at 25° C).

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Current	I_{CC}		21	40	mA	HEDS-6000 (2 Channel)
			36	60		HEDS-6010 (3 Channel)
High Level Output Voltage	V_{OH}	2.4			V	I_{OH} = -40μA Max.
Low Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 3.2 mA
Rise Time	t_r		0.5		μs	C_L = 25 pF, R_L = 11K Pull-up
Fall Time	t_f		0.2			See Note 6
Cable Capacitance	C_{CO}		12		pF/meter	Output Lead to Ground

NOTES:

1. The structural parts of the HEDS-6000 have been successfully tested to 20g. In a high vibration environment use is limited at low frequencies (high displacement) by cable fatigue and at high frequencies by code wheel resonances. Resonant frequency depends on code wheel material and number of counts per revolution. For temperatures below -20° C the ribbon cable becomes brittle and sensitive to displacements. Maximum operating and storage temperature includes the surface area of the encoder mounting. Consult factory for further information. See Application Note 1011.
2. In a properly assembled lot 99% of the units, when run at 25° C and 8 KHz, should exhibit a pulse width error less than 32 electrical degrees, and a state width error less than 40 electrical degrees. To calculate errors at other speeds and temperatures add the values specified in Figures 1 or 2 to the typical values specified under encoding characteristics or to the maximum 99% values specified in this note.
3. In a properly assembled lot, 99% of the units when run at 25° C and 8 KHz should exhibit an index pulse width greater than 260 electrical degrees and less than 460 electrical degrees. To calculate index pulse widths at other speeds and temperatures add the values specified in Figures 3 or 4 to the typical 360° pulse width or to the maximum 99% values specified in this note.
4. Index phase is adjusted at assembly. Index phase error is the maximum change in index phase expected over the full temperature range and up to 50 KHz, after assembly adjustment of the index pulse position has been made.
5. When the index pulse is centered on the low-low states of channels A and B as shown on page 2, a unique P_O can be defined once per revolution within the recommended operating conditions and up to 25 KHz. Figure 6 shows how P_O can be derived from A, B, and I outputs. The adjustment range indicates how far from the center of the low-low state that the center of the index pulse may be adjusted.
6. The rise time is primarily a function of the RC time constant of R_L and C_L. A faster rise time can be achieved with either a lower value of R_L or C_L. Care must be observed not to exceed the recommended value of I_{OL} under worst case conditions.

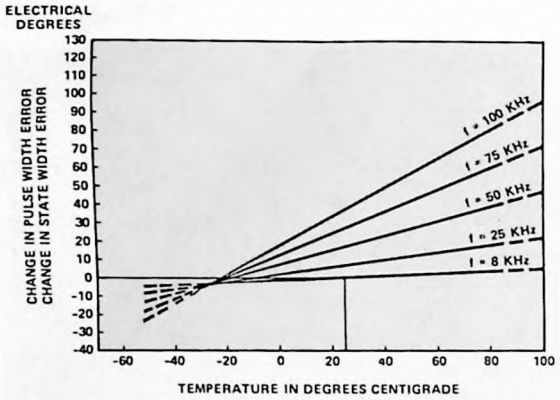


Figure 1. Typical Change in Pulse Width Error or in State Width Error due to Speed and Temperature

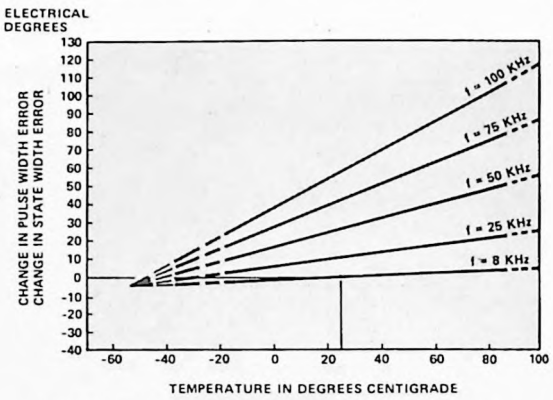


Figure 2. Maximum Change in Pulse Width Error or in State Width Error Due to Speed and Temperature

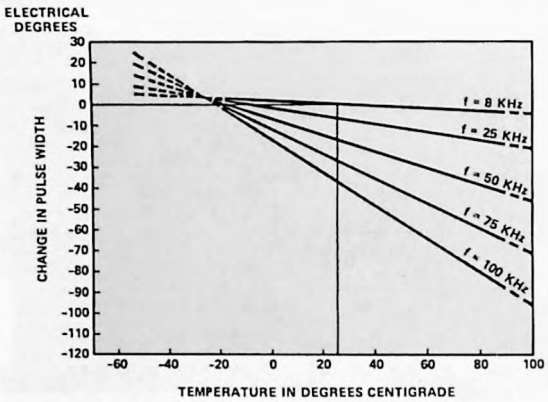


Figure 3. Typical Change in Index Pulse Width Due to Speed and Temperature

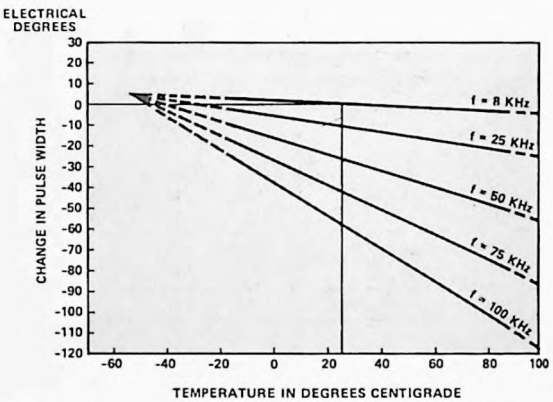


Figure 4. Maximum Change in Index Pulse Width Due to Speed and Temperature

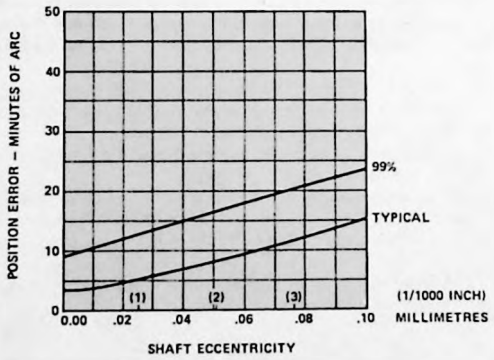
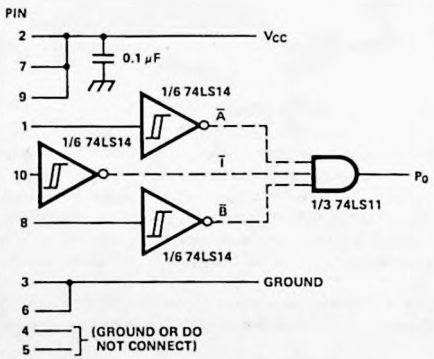
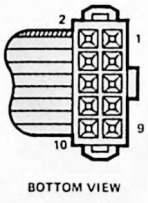


Figure 5. Position Error vs. Shaft Eccentricity



DASHED LINES REPRESENT AN OPTIONAL INDEX SUMMING CIRCUIT. STANDARD 74 SERIES COULD ALSO BE USED TO IMPLEMENT THIS CIRCUIT.

Figure 6. Recommended Interface Circuit



BOTTOM VIEW

PINOUT

PIN #	FUNCTION
1	CHANNEL A
2	V_{CC}
3	GROUND
4	N.C. OR GROUND
5	N.C. OR GROUND
6	GROUND
7	V_{CC}
8	CHANNEL B
9	V_{CC}
10	CHANNEL I

MATING CONNECTOR
BERG 65 692-001 OR EQUIVALENT

Figure 7. Connector Specifications

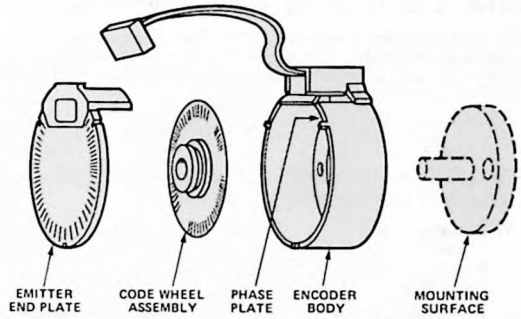


Figure 8. HEDS-6000 Series Encoder Kit

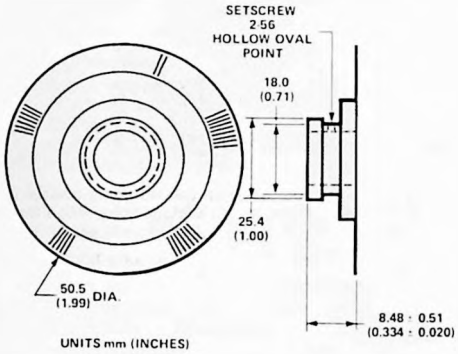


Figure 9. Code Wheel

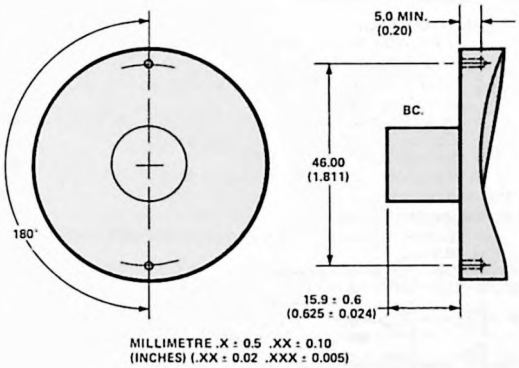


Figure 10. Mounting Requirements

Ordering Information

HEDS-6 ☐☐☐

OPTION* ☐☐

RESOLUTION (CYCLES PER REVOLUTION)

D – 192 CPR	I – 512 CPR
E – 200 CPR	B – 1000 CPR
H – 400 CPR	J – 1024 CPR
A – 500 CPR	

NOTE: OTHER RESOLUTIONS AVAILABLE ON SPECIAL REQUEST

SHAFT DIAMETER

05 – 3/16 IN.
06 – 1/4 IN.
07 – 5/16 IN.
08 – 3/8 IN.
09 – 1/2 IN.
10 – 5/8 IN.
11 – 4 mm
12 – 6 mm
13 – 8 mm
00 – USE WHEN ORDERING ENCODER BODIES

PRODUCT TYPE

0 – 56 mm COMPLETE KIT
1 – 56 mm CODE WHEEL
2 – 56 mm ENCODER BODY
3 – 56 mm EMITTER END PLATE*

OUTPUTS

0 – 2 CHANNEL DIGITAL
1 – 3 CHANNEL DIGITAL

MECHANICAL CONFIGURATION

0 – 0.6 m (24 IN.) CABLE

*NO OPTION IS SPECIFIED WHEN ORDERING EMITTER END PLATES ONLY.

Shaft Encoder Kit Assembly

See Application Note 1011 for further discussion.

The following assembly procedure represents a simple and reliable method for prototype encoder assembly. High volume assembly may suggest modifications to this procedure using custom designed tooling. In certain high volume applications encoder assembly can be accomplished in less than 30 seconds. Consult factory for further details. Note — the code wheel to phase plate gap should be set between 0.015 in. and 0.045 in.

WARNING: THE ADHESIVES USED MAY BE HARMFUL. CONSULT THE MANUFACTURER'S RECOMMENDATIONS.

READ THE INSTRUCTIONS TO THE END BEFORE STARTING ASSEMBLY.

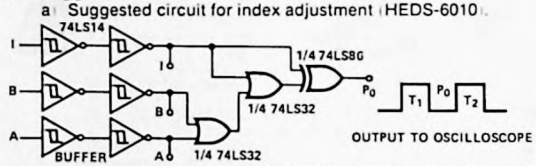
1.0 SUGGESTED MATERIALS

1.1 Encoder Parts
Encoder Body
Emitter End Plate
Code Wheel

1.2 Assembly Materials
RTV-General Electric 162
-Dow Corning 3145
Acetone
Mounting Screws (2)

1.3 Assembly Tools
a) Torque limiting screwdriver, 0.5 cm kg. (7.0 in. oz.).
b) Straight edge. Straight within 0.1 mm (0.004 in.)
c) Oscilloscope. (Phase meter may be optionally used for two channel calibration).
d) Hub puller. Grip-O-Matic-OTC #1000 2-jaw or equivalent. Optional tool for removing code wheels.
e) Syringe applicator for RTV.
f) Torque limiting Allen wrench. 0.5 cm kg (7.0 in. oz.) 0.035 in. hex.

1.4 Suggested Circuits
a) Suggested circuit for index adjustment (HEDS-6010).



For optimal index phase adjust encoder position to equalize T_1 and T_2 pulse widths.

b) Phase Meter Circuit
Recommended for volume assembly. Please see Application Note 1011 for details.

2.0 SURFACE PREPARATION

THE ELAPSED TIME BETWEEN THIS STEP AND THE COMPLETION OF STEP 8 SHOULD NOT EXCEED 1/2 HOUR.

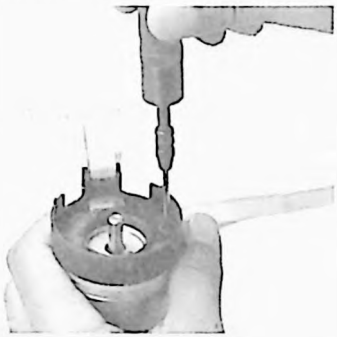
2.1 Clean and degrease with acetone the mounting surface and shaft making sure to keep the acetone away from the motor bearings.

2.2 Load the syringe with RTV.

2.3 Apply RTV into screw threads on mounting surface. Apply more RTV on the surface by forming a daisy ring pattern connecting the screw holes as shown above.

CAUTION: KEEP RTV AWAY FROM THE SHAFT BEARING.

3.0 ENCODER BODY ATTACHMENT



3.1 Place the encoder body on the mounting surface and slowly rotate the body to spread the adhesive. Align the mounting screw holes with the holes in the body base.

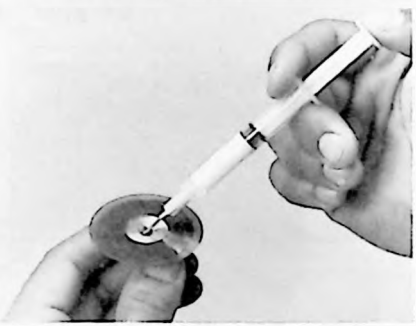
3.2 Place the two mounting screws into the holding bosses in the body base, as shown.

3.3 Thread the screws into the mounting holes and tighten both to 0.5 cm kg (7.0 in. oz.) using the torque limiting screwdriver. (See notes A and B).

3.4 It is not necessary to center the encoder body at this time.

Notes:
a) At this torque value, the encoder body should slide on the mounting surface only with considerable thumb pressure.
b) The torque limiting screwdriver should be periodically calibrated for proper torque.

4.0 APPLICATION OF RTV TO THE HUB



CAUTION: HANDLE THE CODE WHEEL WITH CARE.

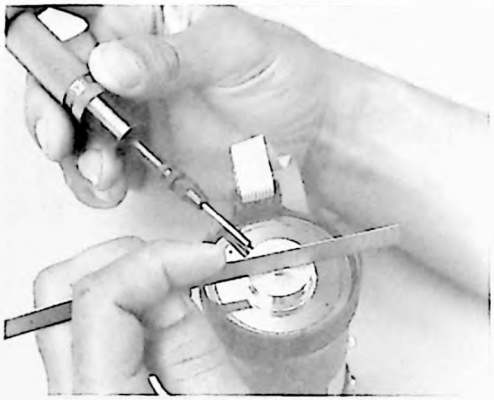
4.1 Make sure that the hex screw on the hub does not enter into the hub bore.

4.2 Apply a small amount of RTV onto the inner surface of the hub bore.

4.3 Spread the RTV evenly inside the entire hub bore.

4.4 Holding the code wheel by its hub, slide it down onto the shaft until the shaft extends at least halfway into the bore.

5.0 CODE WHEEL POSITIONING



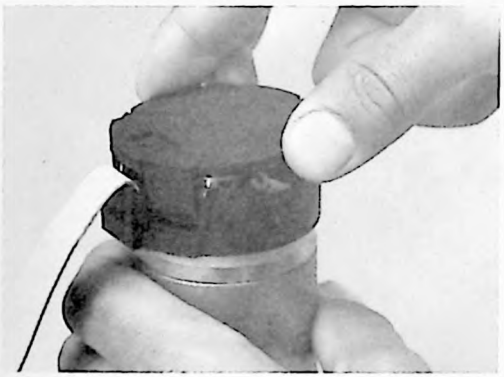
5.1 Position the Allen torque wrench into the hex set screw in the hub, as shown.

5.2 Pull the shaft end down to bottom out axial shaft play. Using the straight edge, push the top of the hub even with the top of the encoder body. The Allen wrench should be used during this movement to apply a slight upward force to the hub, insuring continuous contact between the straight edge and the hub.

5.3 Tighten the hex set screw to approximately 0.5 cm. kg. (7.0 in. oz.) and remove the straight edge.

5.4 The code wheel gap may now be visually inspected to check against gross errors. A nominal gap of 0.8 mm (0.030 in.) should be maintained.

6.0 EMITTER END PLATE

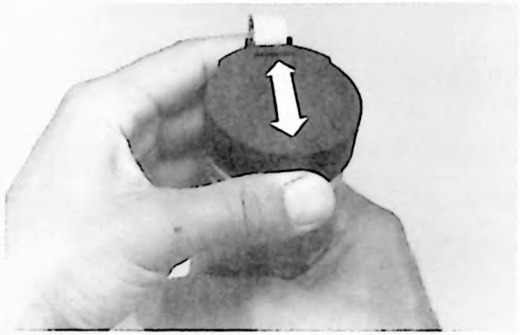


6.1 Visually check that the wire pins in the encoder body are straight and straighten if necessary.

6.2 Align the emitter end plate so that the two flanges straddle the track of the encoder body where the wire pins are located. Press the end plate until it snaps into place.

6.3 Visually check to see if the end plate is properly seated.

7.0 PHASE ADJUSTMENT



7.1 The following procedure should be followed when phase adjusting channels A and B.

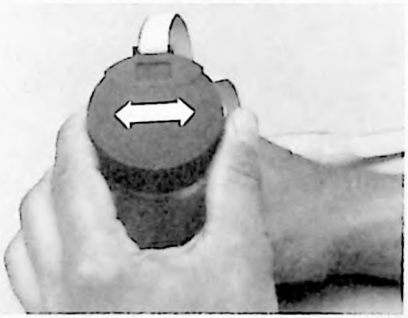
7.2 Connect the encoder cable.

7.3 Run the motor. Phase corresponds to motor direction. See output waveforms and definitions. Using either an oscilloscope or a phase meter, adjust the encoder for minimum phase error by sliding the encoder forward or backward on the mounting surface as shown above. See Application Note 1011 for the phase meter circuit.

7.4 No stress should be applied to the encoder package until the RTV cures. Curve time is 2 hours @ 70° C or 24 hours at room temperature.

Note: After mounting, the encoder should be free from mechanical forces that could cause a shift in the encoder's position relative to its mounting surface.

8.0 INDEX PULSE ADJUSTMENT (HEDS-6010)



8.1 Some applications require that the index pulse be aligned with the main data channels. The index pulse position and the phase must be adjusted simultaneously. This procedure sets index phase to zero.

8.2 Connect the encoder cable.

8.3 Run the motor. Adjust for minimum phase error using an oscilloscope or phase meter. (See 7.3).

8.4 Using an oscilloscope and the circuit shown in 1.4, set the trigger for the falling edge of the P_1 output. Adjust the index pulse so that T_1 and T_2 are equal in width. The physical adjustment is a side to side motion as shown by the arrow.

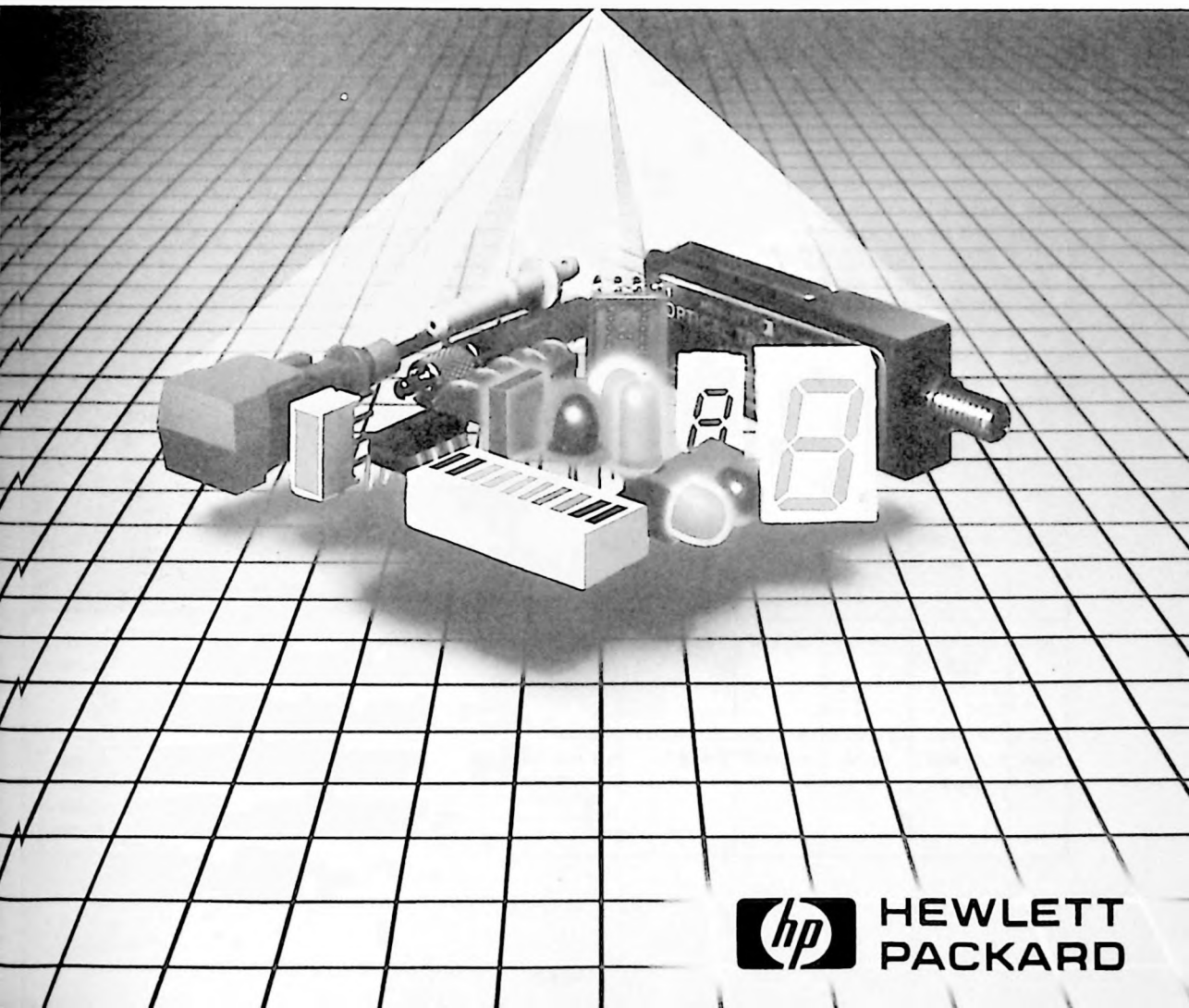
8.5 Recheck the phase adjustment.

8.6 Repeat steps 8.3-8.5 until both phase and index pulse position are as desired.

8.7 No stress should be applied to the encoder package until the RTV has cured. Cure time: 2 hours @ 70° C or 24 hours at room temperature.

5. Optocouplers

- High Speed Optocouplers
- High Gain Optocouplers
- Low Current Optocoupler
- AC/DC to Logic Interface Optocoupler
- 20 mA Current Loop Optocouplers
- Commercial Burn-in for Plastic Optocouplers
- Hermetic Optocouplers



HEWLETT PACKARD

Optocouplers

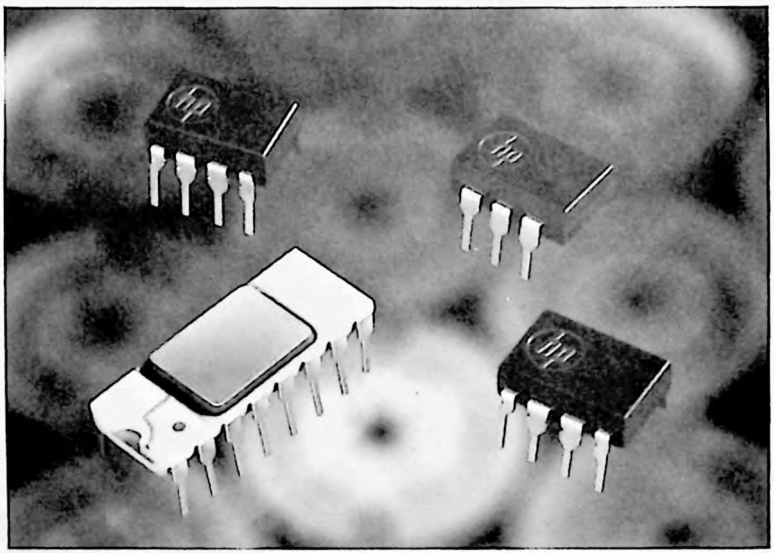
Hewlett-Packard's original approach toward integrated output detectors provides performance not found in conventional phototransistor output devices. A family of optocouplers has been established to provide reliable, economical, high performance solutions to problems caused by ground loops and induced common mode noise for both analog and digital applications in commercial, industrial and military products.

The capabilities of this family span a wide range. Device selections include: programmable AC/DC power sensing input with logic output; speeds up to 10M bits/s; CTR gains as high as 700% and input currents as low as 0.5 mA. HP's HCPL-2200 features guaranteed propagation delay of 400 ns max. from 0 to 85 degrees C with a wide V_{CC} range from 4.5 V to 20 V and I_{CC} of only 6 mA. Additionally, the high CMR of 1000 V/μs and built-in hysteresis help assure reliable circuit design.

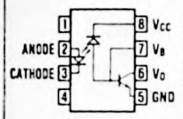
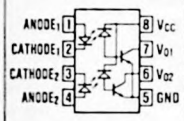
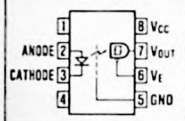
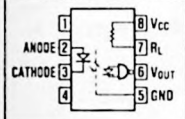
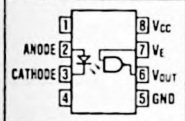
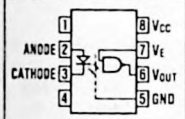
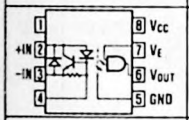
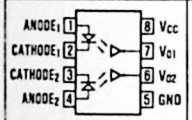
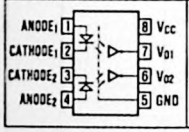
Hewlett-Packard also has available highly linear optocouplers that are useful in analog applications, a unique integrated-input optically coupled line receiver that can be connected directly to twisted pair wires without additional circuitry, and optocouplers that provide complete isolated transmit and receive functions for a 20 mA current loop. Commercial burn-in and screening programs are available for Hewlett-Packard's plastic optocouplers upon special request. See the High Reliability section (page 8-7) for additional details.

Many of these devices are available in dual channel versions, as well as in hermetic DIP packages. For military users, Hewlett-Packard's established, and DESC recognized hi-rel capability facilitates economical, hi-rel purchases.

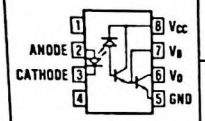
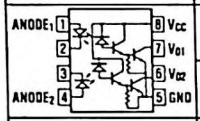
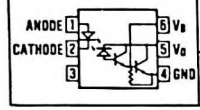
Hewlett-Packard's newest optocoupler, the HCPL-2300, features a guaranteed low threshold current of 0.5 mA with a guaranteed data rate of 5 MBaud over temperature. Additionally, the HCPL-2300 can be selected for threshold current as low as 150 μA.



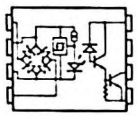
High Speed Optocouplers

Device		Description	Application[1]	Typical Data Rate (NRZ)	Current Transfer Ratio	Specified Input Current	Withstand Test Voltage	Page No.
	6N135	Transistor Output	Line Receiver, Analog Circuits, TTL/CMOS, TTL/LSTTL Ground Isolation	1 M bit/s	7% Min.	16 mA	3000 V dc UL[3]	5-6
	6N136				19% Min.			
	HCPL-2502				15-22%[2]			
	HCPL-2503		LSTTL/LSTTL Logic Interface	250 K bit/s	15% Min.	8 mA		5-10
	SL5505		Telephone circuits, Approved by CNET	1 M bit/s	15% Min. 40% Max.	16 mA	1500 V dc	5-15
	HCPL-2530	Dual Channel Transistor Output	Line Receiver, Analog Circuits, TTL/CMOS, TTL/LSTTL Ground Isolation	1 M bit/s	7% Min.	16 mA	3000 V dc UL[3]	5-17
	HCPL-2531				19% Min.			
	HCPL-2533		TTL/LSTTL Logic Interface	250 K bit/s	12% Min.			5-21
			TTL/LSTTL Logic Interface		15% Min.	8 mA		
	HCPL-2200	Low Input Current Optically Coupled Logic Gate V_{CC} = 20 V Max.	High Speed Logic Ground Isolation, LSTTL, TTL, CMOS Logic Interface	5 M bit/s	3 State Output	1.6 mA		5-26
	HCPL-2300	Low Input Current, High Speed Opto-Coupler	High Speed, Long Distance Line Receiver, Computer Peripheral Interfaces, CMOS Logic Interface	5 M bit/s	1600% Min.	0.5 mA	3000 V dc UL[3]	5-30
	6N137	Optically Coupled Logic Gate	Line Receiver, High Speed Logic Ground Isolation	10 M bit/s	700% Typ.	5.0 mA	3000 V dc UL[3]	5-36
	HCPL-2601	High Common Mode Rejection, Optically Coupled Logic Gate	Line Receiver, High Speed Logic Ground Isolation in High Ground or Induced Noise Environments	10 M bit/s	700% Typ.	5.0 mA	3000 V dc UL[3]	5-40
	HCPL-2602	Optically Coupled Line Receiver	Replace Conventional Line Receivers in High Ground or Induced Noise Environments	10 M bit/s	700% Typ.	5.0 mA	3000 V dc UL[3]	5-44
	HCPL-2630	Dual Channel Optically Coupled Gate	Line Receiver, High Speed Logic Ground Isolation	10 M bit/s	700% Typ.	5.0 mA	3000 V dc UL[3]	5-50
	HCPL-2631	Dual Channel, High Common Mode Rejection, Optically Coupled Logic Gate	Line Receiver, High Speed Logic Ground Isolation in High Ground or Induced Noise Environments	10 M bit/s	700% Typ.	5.0 mA	3000 V dc UL[3]	5-54

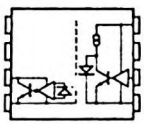
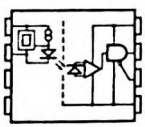
High Gain Optocouplers

Device		Description	Application[1]	Typical Data Rate (NRZ)	Current Transfer Ratio	Specified Input Current	Withstand Test Voltage	Page No.
	6N138	Low Saturation Voltage, High Gain Output, V_{CC} = 7 V Max.	Line Receiver, Low Current Ground Isolation, TTL/TTL, LSTTL/TTL, CMOS/TTL	300k bit/s	300% Min.	1.6 mA	3000 V dc UL[3]	5-58
	6N139	Low Saturation Voltage, High Gain Output, V_{CC} = 18 V Max.	Line Receiver, Ultra Low Current Ground Isolation, CMOS/LSTTL, CMOS/TTL, CMOS/CMOS		400% Min.	0.5 mA		
	HCPL-2730	Dual Channel, High Gain, V_{CC} = 7 V Max.	Line Receiver, Polarity Sensing, Low Current Ground Isolation	300k bit/s	300% Min.	1.6 mA	3000 V dc UL[3]	5-62
	HCPL-2731	Dual Channel, High Gain, V_{CC} = 18 V Max.			400% Min.	0.5 mA		
	4N45	Darlington Output V_{CC} = 7 V Max.	AC Isolation, Relay-Logic Isolation	3k bit/s	250% Min.	1.0 mA	3000 V dc UL[3]	5-66
	4N46	Darlington Output V_{CC} = 20 V Max.			350% Min.	0.5 mA		

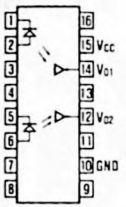
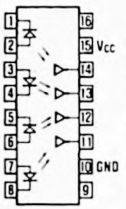
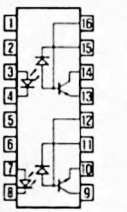
AC/DC to Logic Interface Optocoupler

Device		Description	Application[1]	Typical Data Rates	Input Threshold Current	Output Current	Withstand Test Voltage	Page No.
	HCPL-3700	AC/DC to Logic Threshold Sensing Interface Optocoupler	Limit Switch Sensing, Low Voltage Detector, Relay Contact Monitor	4 KHz	2.5 mA TH^+ 1.3 mA TH^-	4.2 mA	3000 V dc UL[3]	5-70

20 mA Current Loop Optocouplers

Device		Description	Application[1]	Typical Data Rates	Input Characteristics	Output Characteristics	Withstand Test Voltage	Page No.
	HCPL-4100	Optically Coupled 20 mA Current Loop Transmitter	Isolated 20 mA Current Loop in: • Computer Peripherals • Industrial Control Equipment • Data Communication Equipment	20 kBd (at 400 metres)	TTL/CMOS	27 V Max. Compliance Voltage	3000 V dc UL[3]	5-76
	HCPL-4200	Optically Coupled 20 mA Current Loop Receiver			6.5 mA Typ. Threshold Current	3 State Output		5-84

Hermetic Optocouplers

Device		Description	Application	Typical Data Rate (NRZ)	Current Transfer Ratio	Specified Input Current	Withstand Test Voltage	Page No.
	6N134	Dual Channel Hermetically Sealed Optically Coupled Logic Gate	Line Receiver, Ground Isolation for High Reliability Systems	10M bit/s	400% Typ.	10 mA	1500 V dc	5-96
	8102801EC	DESC Approved 6N134	Military/High Reliability					5-99
	6N134TXV	TXV — Screened	8102801EC Recommended for New Designs					5-96
	6N134TXVB	TXVB — Screened with Group B Data						
	6N140	Hermetically Sealed Package Containing 4 Low Input Current, High Gain Optocouplers	Line Receiver, Low Power Ground Isolation for High Reliability Systems	300k bit/s	300% Min.	0.5 mA	1500 V dc	5-103
	6N140/883B	MIL-STD-883 Class B Part	Military/High Reliability					
	6N140TXV	TXV — Hi-Rel Screened	6N140/883B Recommended for New Designs					
	6N140TXVB	TXVB — Hi-Rel Screened with Group B Data						
	4N55	Dual Channel Hermetically Sealed Analog Optical Coupler	Line Receiver, Analog Signal Ground Isolation, Switching Power Supply Feedback Element	700k bit/s	7% Min.	16 mA	1500 V dc	5-107
	4N55/883B	MIL-STD-883 Class B Part	Military/High Reliability					
	4N55TXV	TXV — Hi-Rel Screened	Use 4N55/883B in New Designs					
	4N55TXVB	TXVB — Hi-Rel Screened with Group B Data						

NOTES:

1. For further information, AN-939, AN-948, AN-951-1, and AN-951-2 are available from HP free of charge or can be found starting on page 9-1.
2. The HCPL-2502 Current Transfer Ratio Specification is guaranteed to be 15% minimum and 22% maximum.
3. Recognized under the Component Recognition Program of Underwriters Laboratories Inc. (File NO. E55361). Dielectric withstand voltage is tested at 3000 V dc for a working voltage of 220 Vac. This is a proof test.

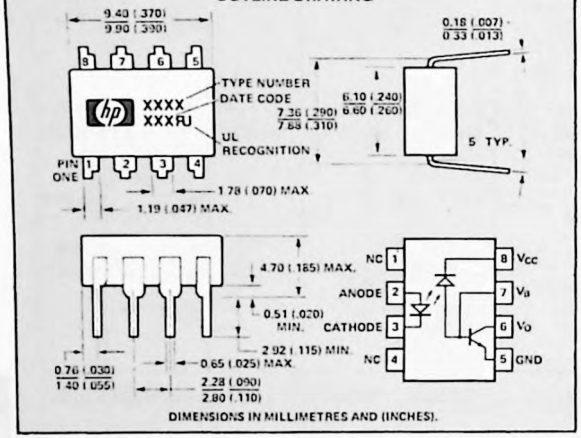
HEWLETT PACKARD

HIGH SPEED OPTOCOUPLERS

6N135
6N136
HCPL-2502

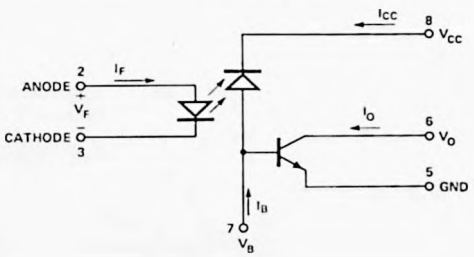
TECHNICAL DATA JANUARY 1984

OUTLINE DRAWING*



DIMENSIONS IN MILLIMETRES AND (INCHES).

SCHEMATIC



Features

- **HIGH SPEED: 1 Mbit/s**
- **TTL COMPATIBLE**
- **HIGH COMMON MODE TRANSIENT IMMUNITY: 1000V/μs**
- **2 MHz BANDWIDTH**
- **OPEN COLLECTOR OUTPUT**
- **DIELECTRIC WITHSTAND TESTED AT 3000 Vdc FOR A WORKING VOLTAGE OF 220 Vac**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES, INC. (FILE NO. E55361)**

Description

These diode-transistor optocouplers use an insulating layer between the light emitting diode and an integrated photon detector to provide electrical insulation between input and output. Separate connection for the photodiode bias and output transistor collector improve the speed up to a hundred times that of a conventional photo-transistor coupler by reducing the base-collector capacitance.

The 6N135 is suitable for use in TTL/CMOS, TTL/LSTTL or wide bandwidth analog applications. Current transfer ratio (CTR) for the 6N135 is 7% minimum at I_F = 16 mA.

The 6N136 is suitable for high speed TTL/TTL applications. A standard 16 mA TTL sink current through the input LED will provide enough output current for 1 TTL load and a 5.6 kΩ pull-up resistor. CTR of the 6N136 is 19% minimum at I_F = 16 mA.

The HCPL-2502 is suitable for use in applications where matched or known CTR is desired. CTR is 15 to 22% at I_F = 16 mA.

Applications

- **Line Receivers** — High common mode transient immunity (>1000V/μs) and low input-output capacitance (0.6pF).
- **High Speed Logic Ground Isolation** — TTL/TTL, TTL/LTTL, TTL/CMOS, TTL/LSTTL.
- **Replace Slow Phototransistor Isolators** — Pins 2-7 of the 6N135/6 series conform to pins 1-6 of 6 pin phototransistor couplers. Pin 8 can be tied to any available bias voltage of 1.5V to 15V for high speed operation.
- **Replace Pulse Transformers** — Save board space and weight.
- **Analog Signal Ground Isolation** — Integrated photon detector provides improved linearity over phototransistor type.

Absolute Maximum Ratings*

Storage Temperature	-55°C to +125°C
Operating Temperature	-55°C to 100°C
Lead Solder Temperature	260°C for 10s (1.6mm below seating plane)
Average Input Current — I_F	25mA[1]
Peak Input Current — I_F	50mA[2] (50% duty cycle, 1 ms pulse width)
Peak Transient Input Current — I_F	1.0A (≤1μs pulse width, 300pps)
Reverse Input Voltage — V_R (Pin 3-2)	5V
Input Power Dissipation	45mW[3]
Average Output Current — I_O (Pin 6)	8mA
Peak Output Current	16mA
Emitter-Base Reverse Voltage (Pin 5-7)	5V
Supply and Output Voltage — V_{CC} (Pin 8-5), V_O (Pin 6-5)	-0.5V to 15V
Base Current — I_B (Pin 7)	5mA
Output Power Dissipation	100mW[4]

CAUTION: The small junction sizes inherent to the design of this bipolar component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

See notes, following page.

*JEDEC Registered Data. (The HCPL-2502 is not registered.)

Electrical Specifications

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified.

Parameter	Sym.	Device	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR*	6N135	7	18		%	I_F = 16mA, V_O = 0.4V, V_{CC} = 4.5V, T_A = 25°C	1,2	5
		6N136	19	24		%			
		HCPL-2502	15		22	%			
	CTR	6N135	5	13		%	I_F = 16mA, V_O = 0.5V, V_{CC} = 4.5V		
		6N136	15	21		%			
Logic Low Output Voltage	V_{OL}	6N135		0.1	0.4	V	I_F = 16mA, I_O = 1.1mA, V_{CC} = 4.5V		
		6N136 HCPL-2502		0.1	0.4	V	I_F = 16mA, I_O = 2.4mA, V_{CC} = 4.5V		
Logic High Output Current	I_{OH}*			3	500	nA	I_F = 0mA, V_O = V_{CC} = 5.5V, T_A = 25°C	6	
				0.01	1	μA	I_F = 0mA, V_O = V_{CC} = 15V, T_A = 25°C		
	I_{OH}				50	μA	I_F = 0mA, V_O = V_{CC} = 15V		
Logic Low Supply Current	I_{CCL}			40		μA	I_F = 16mA, V_O = Open, V_{CC} = 15V		
Logic High Supply Current	I_{CCH}*			0.02	1	μA	I_F = 0mA, V_O = Open, V_{CC} = 15V, T_A = 25°C		
	I_{CCH}				2	μA	I_F = 0mA, V_O = Open, V_{CC} = 15V		
Input Forward Voltage	V_F*			1.5	1.7	V	I_F = 16mA, T_A = 25°C	3	
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.6		mV/°C	I_F = 16mA		
Input Reverse Breakdown Voltage	BV_R*		5			V	I_R = 10μA, T_A = 25°C		
Input Capacitance	C_{IN}			60		pF	f = 1MHz, V_F = 0		
Input-Output Insulation Leakage Current	I_{I-O}*				1.0	μA	45% Relative Humidity, t = 5s, V_{I-O} = 3000Vdc, T_A = 25°C		6, 11
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500Vdc		6
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1MHz		6
Transistor DC Current Gain	h_{FE}			150		–	V_O = 5V, I_O = 3mA		

**All typicals at T_A = 25°C.

Switching Specifications at T_A=25°C V_{CC} = 5V, I_F = 16mA, unless otherwise specified.

Parameter	Sym.	Device	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time To Logic Low at Output	t_{PHL}*	6N135		0.5	1.5	μs	R_L = 4.1kΩ	5,9	8,9
		6N136 HCPL-2502		0.2	0.8	μs	R_L = 1.9kΩ		
Propagation Delay Time To Logic High at Output	t_{PLH}*	6N135		0.4	1.5	μs	R_L = 4.1kΩ	5,9	8,9
		6N136 HCPL-2502		0.3	0.8	μs	R_L = 1.9kΩ		
Common Mode Transient Immunity at Logic High Level Output	CM_H	6N135		1000		V/μs	I_F = 0mA, V_{CM} = 10Vp-p, R_L = 4.1kΩ	10	7,8,9
		6N136 HCPL-2502		1000		V/μs	I_F = 0mA, V_{CM} = 10Vp-p, R_L = 1.9kΩ		
Common Mode Transient Immunity at Logic Low Level Output	CM_L	6N135		-1000		V/μs	V_{CM} = 10Vp-p, R_L = 4.1kΩ	10	7,8,9
		6N136 HCPL-2502		-1000		V/μs	V_{CM} = 10Vp-p, R_L = 1.9kΩ		
Bandwidth	BW			2		MHz	R_L = 100Ω	8	10

NOTES:

1. Derate linearly above 70°C free-air temperature at a rate of 0.8mA/°C.
2. Derate linearly above 70°C free-air temperature at a rate of 1.6mA/°C.
3. Derate linearly above 70°C free-air temperature at a rate of 0.9mW/°C.
4. Derate linearly above 70°C free-air temperature at a rate of 2.0mW/°C.
5. CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
6. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
7. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.0V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8V).
8. The 1.9kΩ load represents 1 TTL unit load of 1.6mA and the 5.6kΩ pull-up resistor.
9. The 4.1kΩ load represents 1 LSTTL unit load of 0.36mA and 6.1kΩ pull-up resistor.
10. The frequency at which the ac output voltage is 3dB below the low frequency asymptote.
11. This is a proof test to validate the UL 220 Vac rating.

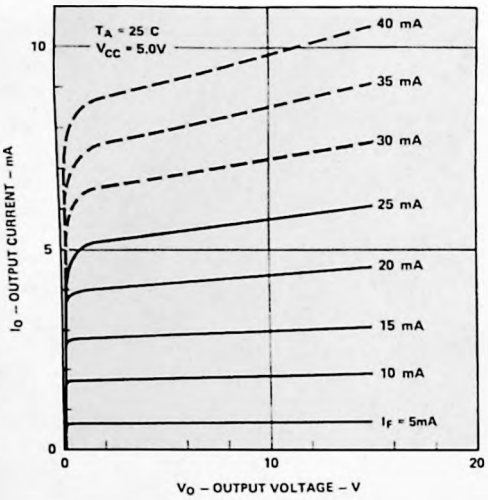


Figure 1. DC and Pulsed Transfer Characteristics.

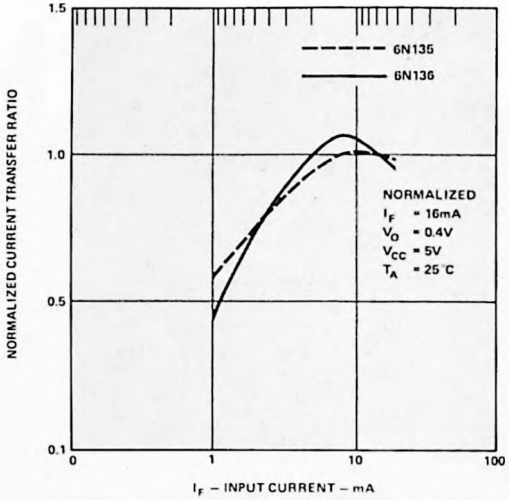


Figure 2. Current Transfer Ratio vs. Input Current.

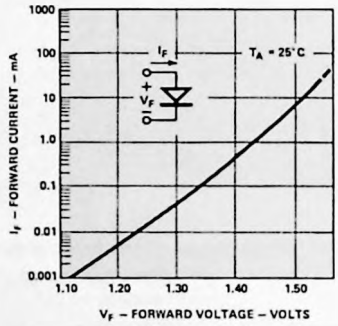


Figure 3. Input Current vs. Forward Voltage.

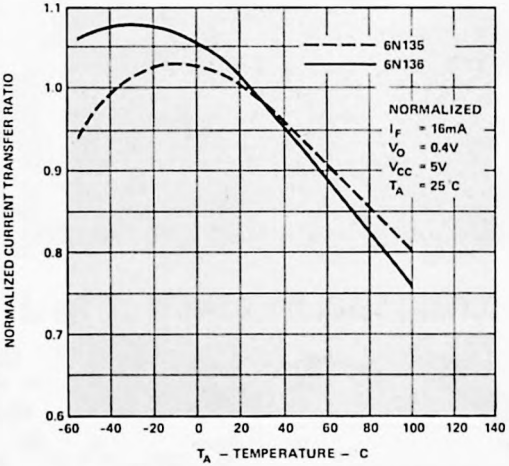


Figure 4. Current Transfer Ratio vs. Temperature.

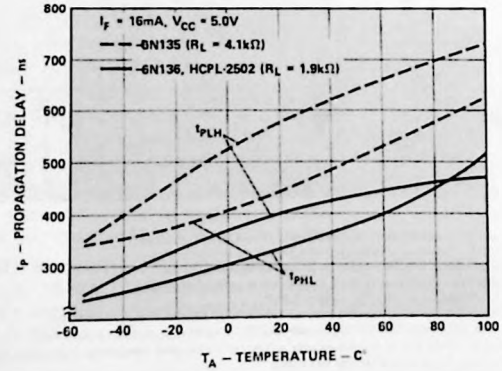


Figure 5. Propagation Delay vs. Temperature.

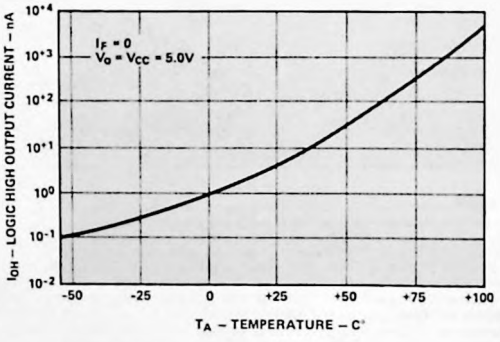


Figure 6. Logic High Output Current vs. Temperature.

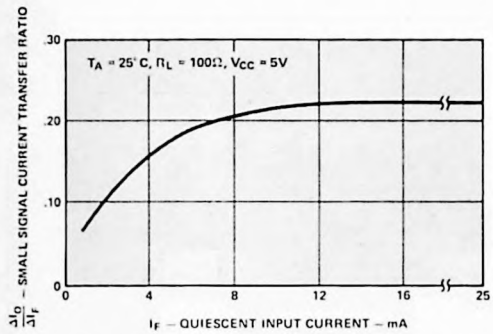
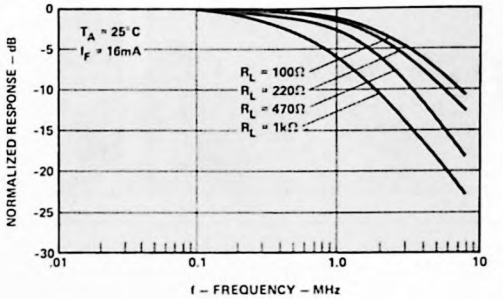


Figure 7. Small-Signal Current Transfer Ratio vs. Quiescent Input Current.



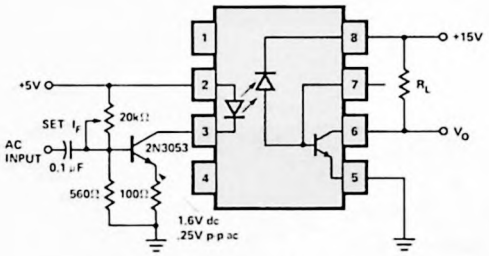
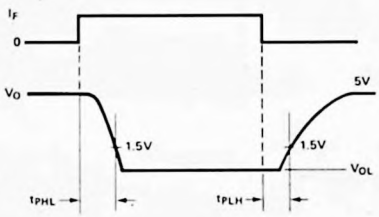


Figure 8. Frequency Response.



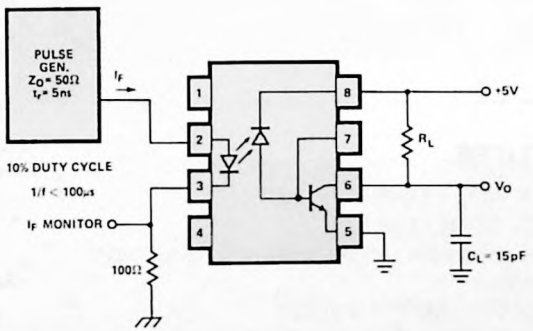
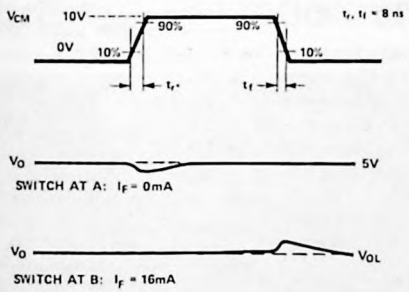
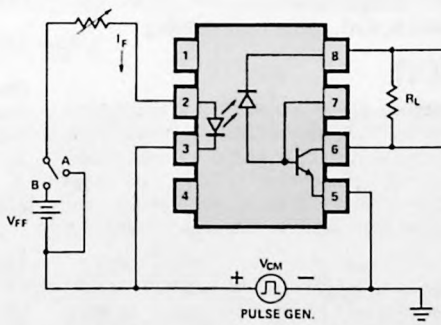


Figure 9. Switching Test Circuit.*





*JEDEC Registered Data

Figure 10. Test Circuit for Transient Immunity and Typical Waveforms.

HEWLETT PACKARD

LOGIC INTERFACE OPTOCOUPLER

HCPL-2503

TECHNICAL DATA JANUARY 1984

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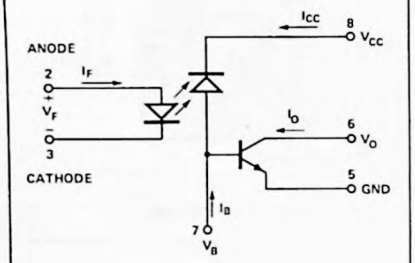
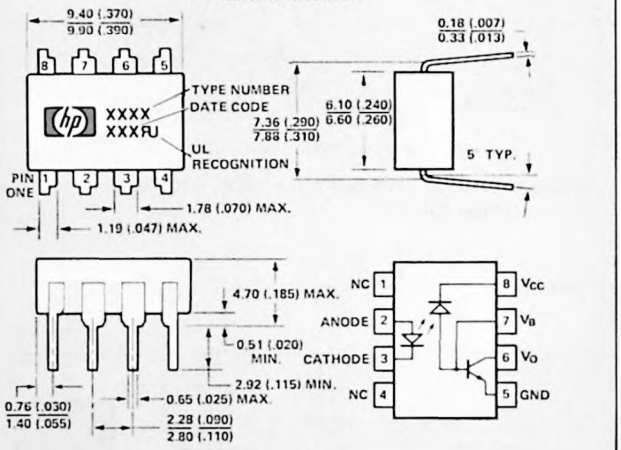


OUTLINE DRAWING*



DIMENSIONS IN MILLIMETRES AND (INCHES).

Features

- **DATA RATES TO 250K b/s NRZ**
- **LSTTL COMPATIBLE**
- **HIGH COMMON MODE TRANSIENT IMMUNITY: >1000V/μs**
- **OPEN COLLECTOR OUTPUT**
- **DIELECTRIC WITHSTAND TESTED AT 3000 Vdc FOR A WORKING VOLTAGE OF 220 Vac**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES, INC. (FILE NO. E55361)**

Description

The HCPL-2503 optocoupler is specified for use in LSTTL to LSTTL and TTL to LSTTL logic interfaces. A nominal 8 mA sink current through the input LED will provide enough output current for proper operation of 1 LSTTL gate under worst-case conditions when used in the recommended circuits. The CTR of the HCPL-2503 is 15% minimum at $I_F = 8$ mA.

The HCPL-2503 contains a light emitting diode and an integrated photon detector with an insulation barrier between input and output. Separate connection for the photo-diode bias and output transistor collector reduce the base-collector capacitance, giving improved speed compared with conventional phototransistor couplers.

Applications

- **HIGH SPEED LOGIC GROUND ISOLATION — LSTTL-TO-LSTTL AND TTL-TO-LSTTL**

Absolute Maximum Ratings

Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... -55°C to +100°C
Lead Solder Temperature ..... 260°C for 10s
(1.6mm below seating plane)
Average Input Current — I_F ..... 25mA[1]
Peak Input Current — I_F ..... 50mA[2]
(50% duty cycle, 1 ms pulse width)
Peak Transient Input Current — I_F ..... 1.0 A
(≤1μs pulse width, 300pps)
Reverse Input Voltage — V_R (Pin 3-2) 5V
Input Power Dissipation ..... 45mW[3]
Average Output Current — I_C (Pin 6) 8mA
Peak Output Current — I_O 16mA
Emitter-Base Reverse Voltage (Pin 5-7) 5V
Supply and Output Voltage — V_{CC} (Pin 8-5),
V_O (Pin 6-5) ..... -0.5V to 7V
Base Current — I_B (Pin 7) 5mA
Output Power Dissipation ..... 100mW[4]
(See notes, following page.)

CAUTION: The small junction sizes inherent to the design of this bipolar component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Electrical Specifications, LSTTL/LSTTL

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified.

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	15	22		%	I_F = 8mA, V_O = 0.5V, V_{CC} = 4.5V, T_A = 25°C	1	5
		11	15		%	I_F = 8mA, V_O = 0.5V, V_{CC} = 4.5V		
Logic Low Output Voltage	V_{OL}		0.2	0.5	V	I_F = 8mA, I_O = 0.7mA, V_{CC} = 4.5V		
Logic Low Supply Current	I_{CCL}		20		μA	I_F = 8mA, V_O = Open, V_{CC} = 5.5V		
Input Forward Voltage	V_F		1.5	1.7	V	I_F = 8mA, T_A = 25°C	2	
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$		-1.6		mV/°C	I_F = 8mA		

Switching Specifications at T_A = 25°C

V_{CC} = 5V, I_F = 8mA, R_L = 7.5kΩ unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}		1.0	1.5	μs		4,6	8
Propagation Delay Time to Logic High at Output	t_{PLH}		1.5	2.5	μs		4,6	8
Common Mode Transient Immunity at Logic High Level Output	CM_H		1000		V/μs	I_F = 0mA, V_{CM} = 10V_{p-p}	7	7,8
Common Mode Transient Immunity at Logic Low Level Output	CM_L		-1000		V/μs	V_{CM} = 10V_{p-p}	7	7,8

Electrical Specifications, TTL/LSTTL

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified.

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	12	18		%	I_F = 16mA, V_O = 0.5V, V_{CC} = 4.5V, T_A = 25°C	1	5
		9	13		%	I_F = 16mA, V_O = 0.5V, V_{CC} = 4.5V		
Logic Low Output Voltage	V_{OL}		0.2	0.5	V	I_F = 16mA, I_O = 1.1mA, V_{CC} = 4.5V		
Logic Low Supply Current	I_{CCL}		40		μA	I_F = 16mA, V_O = Open, V_{CC} = 5.5V		
Input Forward Voltage	V_F		1.5	1.7	V	I_F = 16mA, T_A = 25°C	2	
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$		-1.6		mV/°C	I_F = 16mA		

Switching Specifications at T_A = 25°C

V_{CC} = 5V, I_F = 16mA, R_L = 4.7kΩ unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}		0.4	1.5	μs		4,6	9
Propagation Delay Time to Logic High at Output	t_{PLH}		1.5	2.5	μs		4,6	9
Common Mode Transient Immunity at Logic High Level Output	CM_H		1000		V/μs	I_F = 0mA, V_{CM} = 10V_{p-p}	7	7,9
Common Mode Transient Immunity at Logic Low Level Output	CM_L		-1000		V/μs	V_{CM} = 10V_{p-p}	7	7,9

*All typicals at 25°C.

(See following page for notes.)

Electrical Specifications

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified.

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Logic High Output Current	I_{OH}		0.5		nA	T_A = 25°C, I_F = 0 mA, V_O = V_{CC} = 5.5V	5	
				50	μA	I_F = 0 mA, V_O = V_{CC} = 5.5V		
Logic High Supply Current	I_{CCH}		0.05	4	μA	I_F = 0 mA, V_O = Open, V_{CC} = 5.5V		
Input Reverse Breakdown Voltage	V_R	5			V	I_F = 10 μA, T_A = 25°C		
Input Capacitance	C_{IN}		60		pF	f = 1 MHz, V_F = 0V		
Input-Output Insulation Leakage Current	I_{I-O}			1.0	μA	45% Relative Humidity, t = 5s, V_{I-O} = 3000V dc, T_A = 25°C		6, 10
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	V_{I-O} = 500V dc		6
Capacitance (Input-Output)	C_{I-O}		0.6		pF	f = 1 MHz		6

Notes:

1. Derate linearly above 70°C free-air temperature at a rate of 0.8mA/°C.
2. Derate linearly above 70°C free-air temperature at a rate of 1.6mA/°C.
3. Derate linearly above 70°C free-air temperature at a rate of 0.9mW/°C.
4. Derate linearly above 70°C free-air temperature at a rate of 2.0mW/°C.
5. CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I/O, to the forward LED input current, I_F, times 100%.
6. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
7. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.0V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8V).
8. The 7.5k load represents 1 LSTTL until load of 0.36mA and a 20kΩ pull-up resistor.
9. The 4.7k load represents 1 LSTTL unit load of 0.36mA and an 8.2kΩ pull-up resistor.
10. This is a proof test to validate the UL 220 Vac rating.

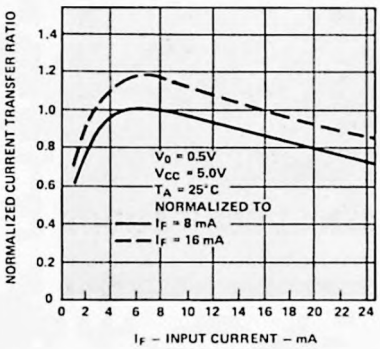


Figure 1. Current Transfer Ratio vs. Input Current

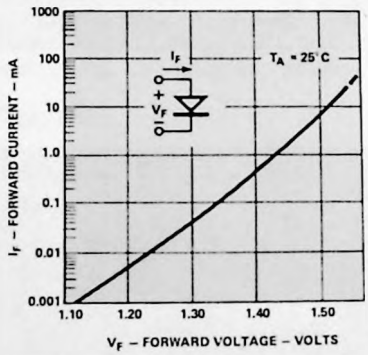


Figure 2. Input Current vs. Forward Voltage

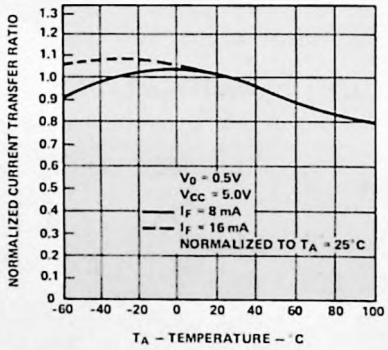


Figure 3. Current Transfer Ratio vs. Temperature

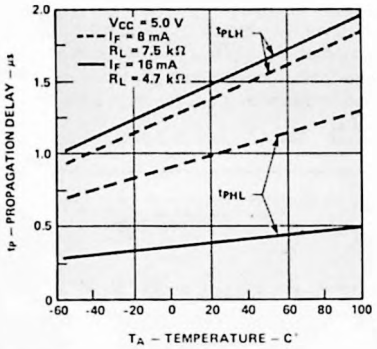


Figure 4. Propagation Delay vs. Temperature

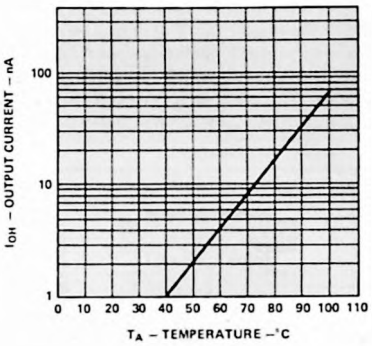


Figure 5. Logic High Output Current vs. Temperature

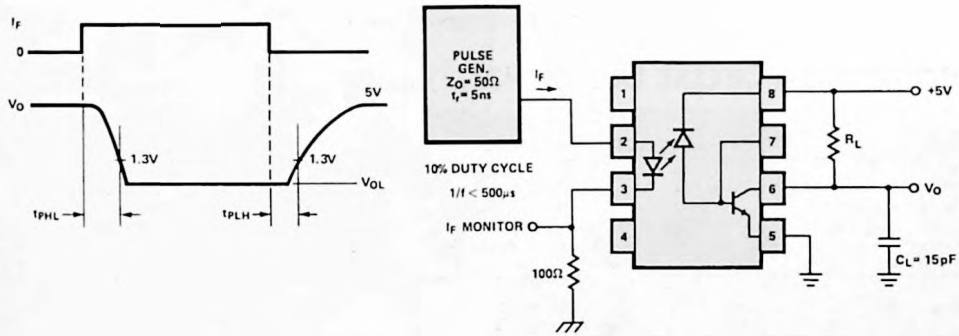


Figure 6. Switching Test Circuit

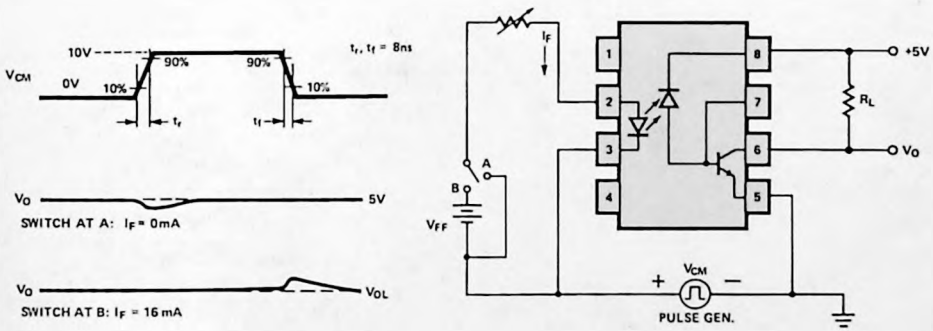


Figure 7. Test Circuit for Transient Immunity and Typical Waveforms

Recommended Operation

The HCPL-2503 optocoupler is specified for use in LSTTL-to-LSTTL and TTL-to-LSTTL interfaces. The recommended circuits show the interface design and give suggested component values. The input current I_F is given as both a nominal value and a range. The range in I_F results from the tolerances in V_{CC} and the input resistor R_{IN}. The CTR of the optocoupler is given as the minimum initial value over temperature, taken directly from the Electrical Specifications. The value given for I_{OL}(min) is based on the minimum CTR and the minimum I_F using worst case values for R_L and V_{CC}. The resulting I_{OL}(min) has ample design margin, allowing more than 20% for CTR degradation even under these worst case conditions. For additional information on CTR degradation see Application Note 1002.

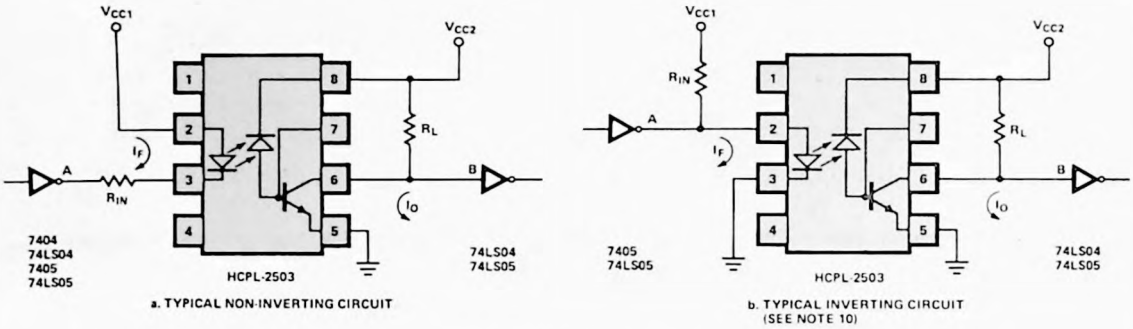


Figure 8. Recommended Circuits

Recommended Circuit Design Parameters

Parameter	Symbol	LSTTL to LSTTL	TTL to LSTTL	Units	Comments	Fig.	Note
INPUT							
Logic Low Output Voltage — Input Gate	$V_{OL(A)}$	0.5	0.4	V	Maximum		
Supply Voltage — Input	V_{CC1}	5.0	5.0	V	±5%		
Input Resistor	R_{IN}	360	180	Ω	±5%	8a	
		430	200			8b	
Input Current	I_F	8	16	mA	Nominal		
Input Current Range	I_F	6.75—10	14.0—20	mA		8a	
			14.5—20			8b	
OUTPUT							
Logic Low Output Voltage — HCPL-2503	$V_{OL(B)}$	0.5	0.5	V	Maximum		
Supply Voltage — Output	V_{CC2}	5.0	5.0	V	±5%		
Pull-Up Resistor	R_L	20	8.2	kΩ	±5%		11
Required Current Sink for Logic Low	I_{OL} (max)	0.61	1.0	mA	Worst Case V_{CC}, R_L, $I_{IL(B)}$		12
HCPL-2503 Current Transfer Ratio	CTR	11	9	%	Minimum T_A = 0°C to +70°C		
Logic Low Output Current — HCPL-2503	I_{OL} (min)	0.74	1.26	mA	Worst Case V_{CC}, CTR, I_F	8a	13
			1.30		T_A = 0°C to +70°C	8b	
Data Rate	f_D	250	250	Kb/s	NRZ, T_A = 25°C		14

Notes:

10. The inverting circuit has higher power consumption and must use open collector gates on the input.
11. The load resistor R_L must be large enough to guarantee logic LOW and small enough to guarantee logic HIGH under worst case conditions:

$$\frac{V_{CC(max)} - V_{OL}}{I_{OL(2503)} - I_{IL(B)}} \leq R_L \leq \frac{V_{CC(min)} - V_{IH(B)}}{I_{OH(2503)} - I_{IH(B)}}$$

The selection of R_L is the same for both inverting and non-inverting circuits.

12. The maximum current sink required for logic LOW is:
$$I_{OL(max)} = I_{IL(B)(max)} + I_{R(max)}$$
where I_R is the current through R_L.
13. The ratio of $I_{OL(min)}$ to $I_{OL(max)}$ gives the design margin for CTR degradation. See Application Note 1002.
14. The maximum data rate is defined as

$$f_D = \frac{1}{t_{PHL} + t_{PLH}} \text{ bits/second NRZ}$$

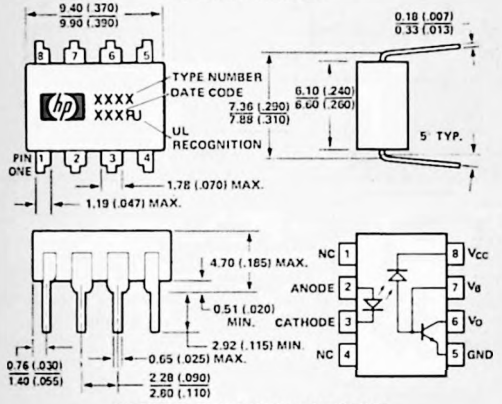
HEWLETT PACKARD

HIGH SPEED OPTOCOUPLER

SL5505

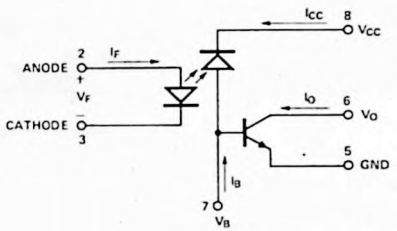
TECHNICAL DATA JANUARY 1984

OUTLINE DRAWING*



DIMENSIONS IN MILLIMETRES AND (INCHES).

SCHEMATIC



Absolute Maximum Ratings

Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... -55°C to 100°C
Lead Solder Temperature ..... 260°C for 10s
(1.6mm below seating plane)
Average Input Current — I_F ..... 25mA[1]
Peak Input Current — I_F ..... 50mA[2]
(50% duty cycle, 1 ms pulse width)
Peak Transient Input Current — I_F 1.0A
($\leq 1\mu s$ pulse width, 300pps)
Reverse Input Voltage — V_R (Pin 3-2) 3V
Input Power Dissipation ..... 45mW[3]
Average Output Current — I_O (Pin 6) 8mA
Peak Output Current 16mA
Emitter-Base Reverse Voltage (Pin 5-7) 5V
Supply and Output Voltage — V_{CC} (Pin 8-5),
V_O (Pin 6-5) ..... -0.5V to 15V
Base Current — I_B (Pin 7) 5mA
Output Power Dissipation ..... 100mW[4]

Electrical Specifications (T_A = 25°C) unless otherwise specified.

Parameter	Symbol	Min.	Max.	Units	Test Conditions	Note
Current Transfer Ratio	CTR	15	40	%	I_F = 16mA, V_O = 0.4V, V_{CC} = 4.5V	5
	CTR	8		%	I_F = 2mA, V_O = 5.0V, V_{CC} = 4.5V	
Logic Low Output Voltage	V_{OL}		0.4	V	I_F = 16mA, I_O = 2.4mA, V_{CC} = 4.5V	
Logic High Output Current	I_{OH}		50	nA	I_F = 0mA, V_O = V_{CC} = 10V	
	I_{OH}		25	μA	I_F = 0mA, V_O = V_{CC} = 10V, T_A = 70°C	
Input Forward Voltage	V_F		1.8	V	I_F = 20mA	
Input Reverse Current	I_R		50	μA	V_R = 3V	
Input-Output Insulation Leakage Current	I_{I-O}		1.0	μA	45% Relative Humidity, t = 5s V_{I-O} = 1500Vdc	6
Resistance (Input-Output)	R_{I-O}	10^9		Ω	V_{I-O} = 100Vdc	6
Transistor DC Current Gain	h_{FE}	100	400	—	V_O = 5V, I_O = 3mA	
Capacitance	C_{I-O}		1.3	pF	f = 1 MHz	6

OPTOCOUPLERS

Switching Specifications at T_A=25°C

V_{CC} = 5V, I_F = 16mA, unless otherwise specified

Parameter	Symbol	Min.	Max.	Units	Test Conditions	Note
Propagation Delay Time to Logic Low at Output (Fig. 1)	t_{PHL}		0.8	μs	R_L = 1.9kΩ	7
Propagation Delay Time to Logic High at Output (Fig. 1)	t_{PLH}		0.8	μs	R_L = 1.9kΩ	7
Breakdown Voltage Collector/Emitter	$V_{(BR)}$ CEO	22		V	I_C = 10mA	8
Breakdown Voltage Collector/Base	$V_{(BR)}$ CBO	40		V	I_C = 10μA	
Breakdown Voltage Emitter/Base	$V_{(BR)}$ EBO	3		V	I_E = 10μA	
Collector/Base Current	I_{CBO}		50	nA	V_{CB} = 22V	

Notes:
1. Derate linearly above 70°C free-air temperature at a rate of 0.8mA/ °C.
2. Derate linearly above 70°C free-air temperature at a rate of 1.6mA/ °C.
3. Derate linearly above 70°C free-air temperature at a rate of 0.9mW/°C.
4. Derate linearly above 70°C free-air temperature at a rate of 2.0mW/°C.
5. CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
6. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
7. The 1.9 KΩ load represents 1 TTL unit load of 1.6 mA and the 5.6 KΩ pull-up resistor.
8. Duty Cycle ≤ 2%, Pulse Width ≤ 300 μs.
9. This is a proof test to validate the UL 220 Vac rating.

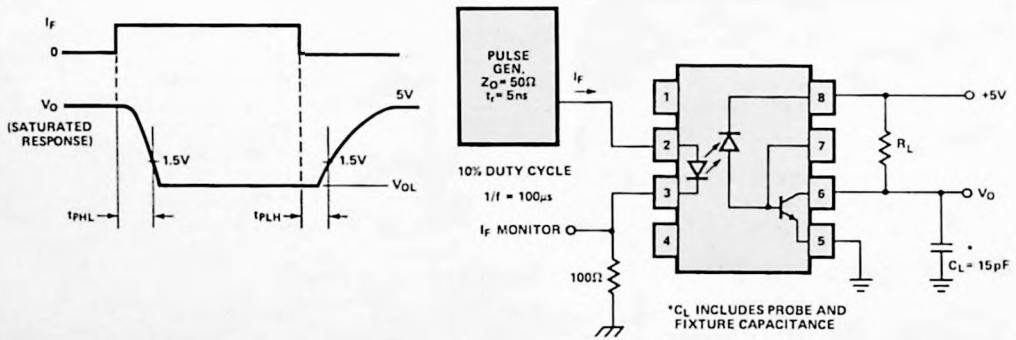


Figure 1. Switching Test Circuit.

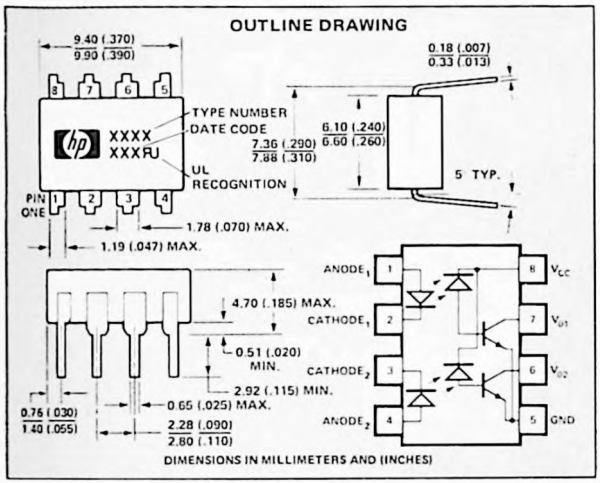
CAUTION: The small junction sizes inherent to the design of this bipolar component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

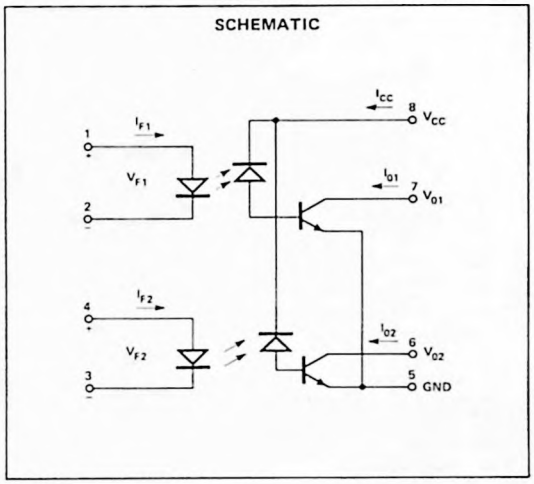
HEWLETT PACKARD

DUAL HIGH SPEED OPTOCOUPLER

HCPL-2530
HCPL-2531

TECHNICAL DATA JANUARY 1984





OPTOCOUPLERS

Features

- **HIGH SPEED: 1 Mbit/s**
- **TTL COMPATIBLE**
- **HIGH COMMON MODE TRANSIENT IMMUNITY: >1000V/μs**
- **HIGH DENSITY PACKAGING**
- **DIELECTRIC WITHSTAND TESTED AT 3000 Vdc FOR A WORKING VOLTAGE OF 220 Vac**
- **3 MHz BANDWIDTH**
- **OPEN COLLECTOR OUTPUTS**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES, INC. (FILE NO. E55361)**

Description

The HCPL-2530/31 dual couplers contain a pair of light emitting diodes and integrated photon detectors with electrical insulation between input and output. Separate connection for the photodiode bias and output transistor collectors improve the speed up to a hundred times that of a conventional phototransistor coupler by reducing the base-collector capacitance.

The HCPL-2530 is suitable for use in TTL/CMOS, TTL/LSTTL or wide bandwidth analog applications. Current transfer ratio (CTR) for the -2530 is 7% minimum at I_F = 16 mA.

The HCPL-2531 is suitable for high speed TTL/TTL applications. A standard 16 mA TTL sink current through the input LED will provide enough output current for 1 TTL load and a 5.6 kΩ pull-up resistor. CTR of the -2531 is 19% minimum at I_F = 16 mA.

Applications

- **Line Receivers** – High common mode transient immunity (>1000V/μs) and low input-output capacitance (0.6pF).
- **High Speed Logic Ground Isolation** – TTL/TTL, TTL/LTTL, TTL/CMOS, TTL/LSTTL.
- **Replace Pulse Transformers** – Save board space and weight.
- **Analog Signal Ground Isolation** – Integrated photon detector provides improved linearity over phototransistor type.
- **Polarity Sensing.**
- **Isolated Analog Amplifier** – Dual channel packaging enhances thermal tracking.

Absolute Maximum Ratings

Storage Temperature . . . . . -55°C to +125°C
Operating Temperature . . . . . -55°C to +100°C
Lead Solder Temperature . . . . . 260°C for 10s
(1.6mm below seating plane)
Average Input Current – I_F (each channel) . . . . . 25mA[1]
Peak Input Current – I_F (each channel) . . . . . 50mA[2]
(50% duty cycle, 1 ms pulse width)
Peak Transient Input Current – I_F (each channel) . . . . 1.0 A
(≤1μs pulse width, 300pps)
Reverse Input Voltage – V_R (each channel) 5V
Input Power Dissipation (each channel) . . . . . 45mW[3]
Average Output Current – I_O (each channel) 8mA
Peak Output Current – I_O (each channel) 16mA
Supply and Output Voltage – V_{CC} (Pin 8-5), V_O (Pin 7,6-5)
. . . . . -0.5V to 15V
Output Power Dissipation (each channel) . . . . . 35mW[4]

See notes, following page.

Electrical Specifications

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified.

Parameter	Sym.	Device HCPL-	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	2530	7	18		%	I_F = 16mA, V_O = 0.5V, V_{CC} = 4.5V, T_A = 25°C	1,2	5,6
		2531	19	24		%			
		2530	5	13		%	I_F = 16mA, V_O = 0.5V, V_{CC} = 4.5V		
		2531	15	21		%			
Logic Low Output Voltage	V_{OL}	2530		0.1	0.5	V	I_F = 16mA, I_O = 1.1mA, V_{CC} = 4.5V, T_A = 25°C		5
		2531		0.1	0.5	V	I_F = 16mA, I_O = 2.4mA, V_{CC} = 4.5V, T_A = 25°C		
Logic High Output Current	I_{OH}			3	500	nA	T_A = 25°C, I_{F1} = I_{F2} = 0, V_{O1} = V_{O2} = V_{CC} = 5.5V	6	5
					50	µA	I_{F1} = I_{F2} = 0, V_{O1} = V_{O2} = V_{CC} = 15V		5
Logic Low Supply Current	I_{CCL}			80		µA	I_{F1} = I_{F2} = 16mA V_{O1} = V_{O2} = Open, V_{CC} = 15V		
Logic High Supply Current	I_{CCH}			0.05	4	µA	I_{F1} = I_{F2} = 0mA V_{O1} = V_{O2} = Open, V_{CC} = 15V		
Input Forward Voltage	V_F			1.5	1.7	V	I_F = 16mA, T_A = 25°C	3	5
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.6		mV/°C	I_F = 16mA		5
Input Reverse Breakdown Voltage	V_R		5			V	I_F = 10µA, T_A = 25°C		5
Input Capacitance	C_{IN}			60		pF	f = 1MHz, V_F = 0		5
Input – Output Insulation Leakage Current	I_{I-O}				1.0	µA	45% Relative Humidity, t = 5 s V_{I-O} = 3000Vdc, T_A = 25°C		7, 13
Resistance (Input–Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500Vdc		7
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1MHz		7
Input–Input Insulation Leakage Current	I_{I-I}			0.005		µA	45% Relative Humidity, t = 5 s V_{I-I} = 500Vdc		8
Resistance (Input–Input)	R_{I-I}			10^{11}		Ω	V_{I-I} = 500Vdc		8
Capacitance (Input-Input)	C_{I-I}			0.25		pF	f = 1MHz		8

**All typicals at 25°C.

Switching Specifications at T_A=25°C V_{CC} = 5V, I_F = 16mA, unless otherwise specified

Parameter	Sym.	Device HCPL-	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time To Logic Low at Output	t_{PHL}	2530		0.3	1.5	µs	R_L = 4.1 kΩ	5,9	10,11
		2531		0.2	0.8	µs	R_L = 1.9kΩ		
Propagation Delay Time to Logic High at Output	t_{PLH}	2530		0.4	1.5	µs	R_L = 4.1 kΩ	5,9	10,11
		2531		0.3	0.8	µs	R_L = 1.9 kΩ		
Common Mode Transient Immunity at Logic High Level Output	CM_H	2530		1000		V/µs	I_F =0mA, R_L=4.1 kΩ, V_{CM}=10V_{p-p}	10	9,10,11
		2531		1000		V/µs	I_F=0mA, R_L=1.9kΩ, V_{CM}=10V_{p-p}		
Common Mode Transient Immunity at Logic Low Level Output	CM_L	2530		-1000		V/µs	V_{CM}=10V_{p-p}, R_L = 4.1kΩ	10	9,10,11
		2531		-1000		V/µs	V_{CM} = 10V_{p-p}, R_L = 1.9kΩ		
Bandwidth	BW			3		MHz	R_L = 100Ω	8	12

NOTES:

1. Derate linearly above 70°C free-air temperature at a rate of 0.8mA/°C.
2. Derate linearly above 70°C free-air temperature at a rate of 1.6mA/°C.
3. Derate linearly above 70°C free-air temperature at a rate of 0.9mW/°C.
4. Derate linearly above 70°C free-air temperature at a rate of 1.0mW/°C.
5. Each channel.
6. CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
7. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
8. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.
9. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.0V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8V).
10. The 1.9kΩ load represents 1 TTL unit load of 1.6mA and the 5.6kΩ pull-up resistor.
11. The 4.1kΩ load represents 1 LSTTL unit load of 0.36mA and 6.1kΩ pull-up resistor.
12. The frequency at which the ac output voltage is 3dB below the low frequency asymptote.
13. This is a proof test to validate the UL 220 Vac rating.

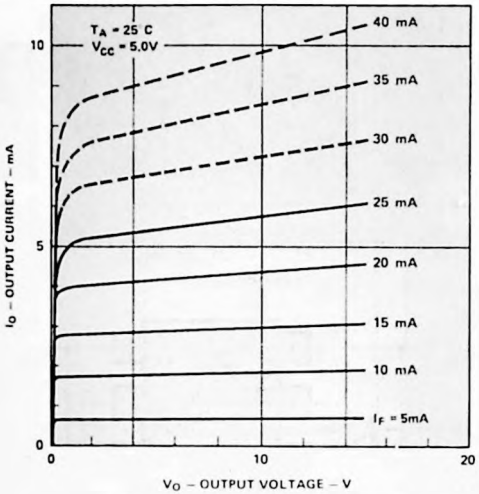


Figure 1. DC and Pulsed Transfer Characteristics.

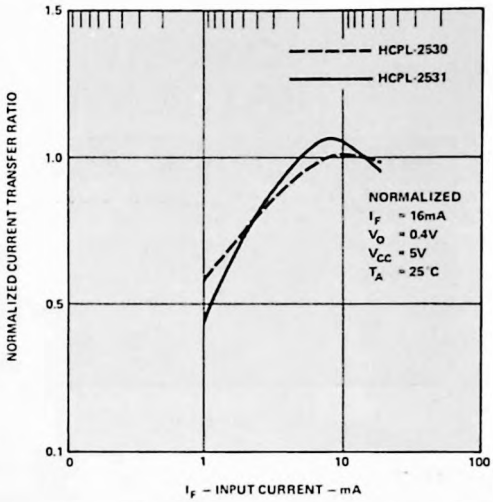


Figure 2. Current Transfer Ratio vs. Input Current.

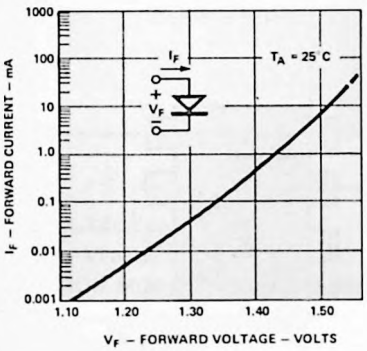


Figure 3. Input Current vs. Forward Voltage.

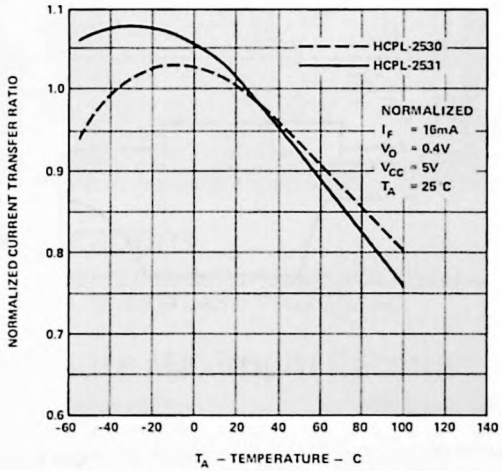


Figure 4. Current Transfer Ratio vs. Temperature.

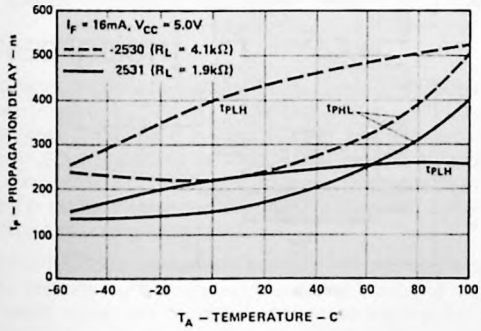


Figure 5. Propagation Delay vs. Temperature.

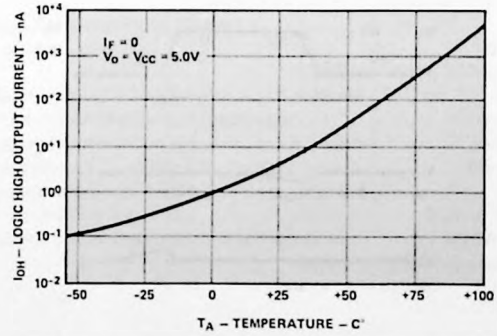


Figure 6. Logic High Output Current vs. Temperature.

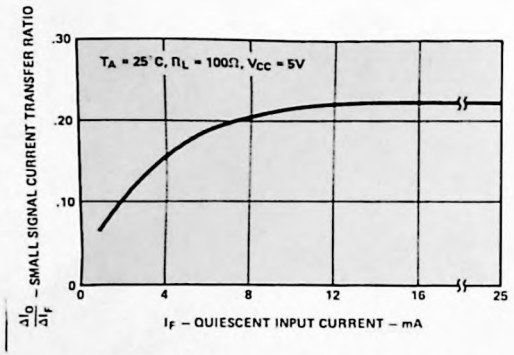
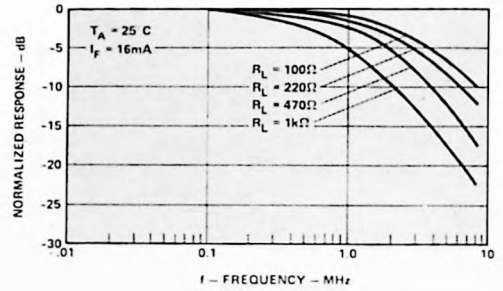


Figure 7. Small-Signal Current Transfer Ratio vs. Quiescent Input Current.



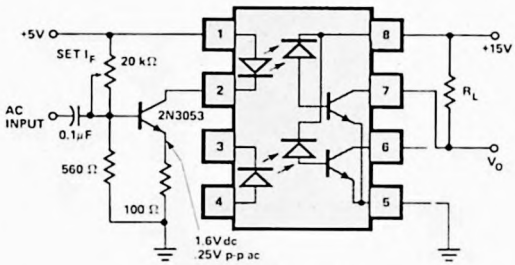


Figure 8. Frequency Response.

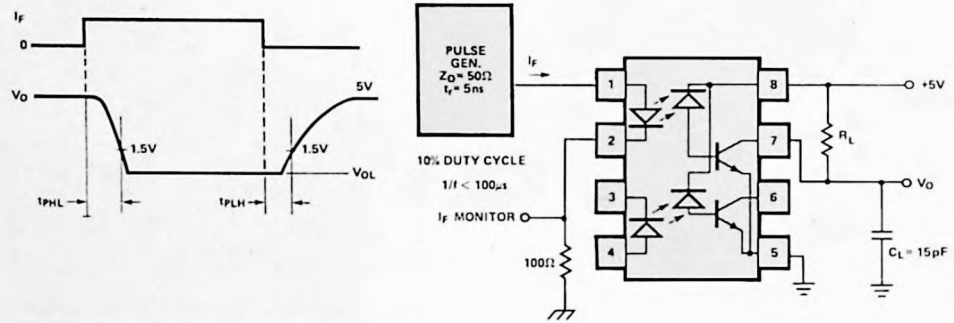


Figure 9. Switching Test Circuit.

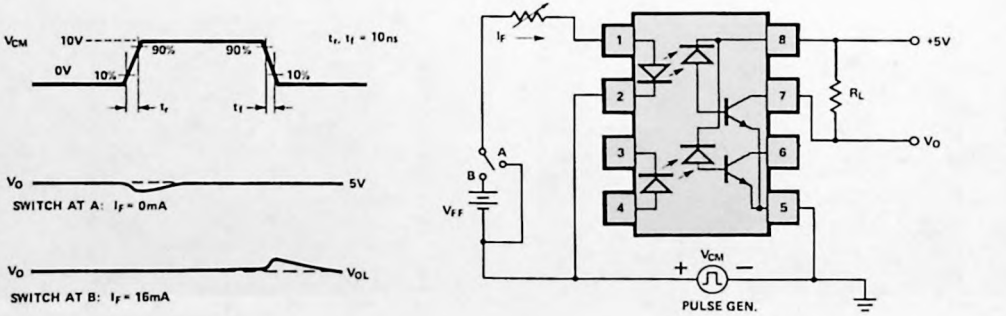


Figure 10. Test Circuit for Transient Immunity and Typical Waveforms.

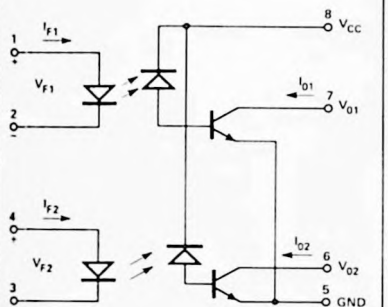
HEWLETT PACKARD

DUAL LOGIC INTERFACE OPTOCOUPLER

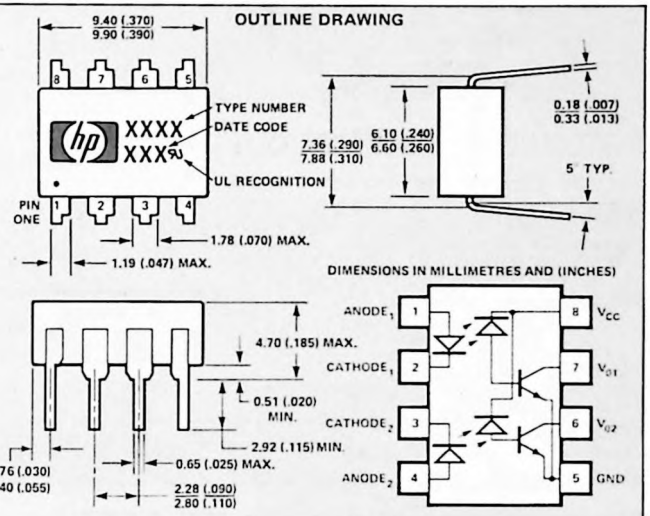
HCPL-2533

TECHNICAL DATA JANUARY 1984

SCHEMATIC



OUTLINE DRAWING



Features

- DATA RATES TO 250k b/s NRZ
- LSTTL COMPATIBLE
- HIGH COMMON MODE TRANSIENT IMMUNITY: >1000V/μs
- HIGH DENSITY PACKAGING
- DIELECTRIC WITHSTAND TESTED AT 3000 Vdc FOR A WORKING VOLTAGE OF 220 Vac
- OPEN COLLECTOR OUTPUTS
- RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES, INC. (FILE NO. E55361)

Description

The HCPL-2533 is a dual channel optocoupler which is specified for use in LSTTL to LSTTL and TTL to LSTTL logic interfaces. A nominal 8 mA LSTTL sink current through the input LED will provide enough output current for proper operation of 1 LSTTL gate under worst-case conditions when used in the recommended circuits. The CTR of the HCPL-2533 is 15% minimum at I_F = 8 mA.

The HCPL-2533 contains a pair of light emitting diodes and integrated photon detectors with an insulating barrier between input and output. Separate connection for the photodiode bias and output transistor collector reduce the base-collector capacitance, giving improved speed compared with conventional phototransistor couplers.

Applications

- HIGH SPEED LOGIC GROUND ISOLATION — LSTTL-TO-LSTTL AND TTL-TO-LSTTL

Absolute Maximum Ratings

Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... -55°C to +100°C
Lead Solder Temperature ..... 260°C for 10s
(1.6mm below seating plane)
Average Input Current — I_F (each channel) ..... 25mA[1]
Peak Input Current — I_F (each channel) ..... 50mA[2]
(50% duty cycle, 1 ms pulse width)
Peak Transient Input Current —
I_F (each channel) ..... 1.0 A
(≤1μs pulse width, 300pps)
Reverse Input Voltage — V_R (each channel) 5V
Input Power Dissipation (each channel) ..... 45mW[3]
Average Output Current — I_O (each channel) 8mA
Peak Output Current — I_O (each channel) 16mA
Supply and Output Voltage — V_{CC} (Pin 8-5),
V_O (Pin 7,6-5) ..... -0.5V to 7V
Output Power Dissipation (each channel) ..... 35mW[4]
(See notes, following page.)

OPTOCOUPLERS

Electrical Specifications, LSTTL/LSTTL

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified.

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	15	22		%	I_F = 8mA, V_O = 0.5V, V_{CC} = 4.5V, T_A = 25°C	1	5,6
		11	15		%	I_F = 8mA, V_O = 0.5V, V_{CC} = 4.5V		
Logic Low Output Voltage	V_{OL}		0.2	0.5	V	I_F = 8mA, I_O = 0.7mA, V_{CC} = 4.5V		5
Logic Low Supply Current	I_{CCL}		40		μA	I_{F1} = I_{F2} = 8mA, V_{O1} = V_{O2} = Open, V_{CC} = 5.5V		
Input Forward Voltage	V_F		1.5	1.7	V	I_F = 8mA, T_A = 25°C	2	5
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$		-1.6		mV/°C	I_F = 8mA		5

Switching Specifications at T_A = 25°C

V_{CC} = 5V, I_F = 8mA, R_L = 7.5kΩ unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}		0.8	1.5	μs		4,6	10
Propagation Delay Time to Logic High at Output	t_{PLH}		1.0	2.5	μs		4,6	10
Common Mode Transient Immunity at Logic High Level Output	CM_H		1000		V/μs	I_F = 0mA, V_{CM} = $10V_{p-p}$	7	9,10
Common Mode Transient Immunity at Logic Low Level Output	CM_L		-1000		V/μs	V_{CM} = $10V_{p-p}$	7	9,10

Electrical Specifications, TTL/LSTTL

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified.

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	12	18		%	I_F = 16mA, V_O = 0.5V, V_{CC} = 4.5V, T_A = 25°C	1	5,5
		9	13		%	I_F = 16mA, V_O = 0.5V, V_{CC} = 4.5V		
Logic Low Output Voltage	V_{OL}		0.2	0.5	V	I_F = 16mA, I_O = 1.1mA, V_{CC} = 4.5V		5
Logic Low Supply Current	I_{CCL}		80		μA	I_{F1} = I_{F2} = 16mA, V_{O1} = V_{O2} = Open, V_{CC} = 5.5V		
Input Forward Voltage	V_F		1.5	1.7	V	I_F = 16mA, T_A = 25°C	2	5
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$		-1.6		mV/°C	I_F = 16mA		5

Switching Specifications at T_A = 25°C

V_{CC} = 5V, I_F = 16mA, R_L = 4.7kΩ unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}		0.3	1.5	μs		4,6	11
Propagation Delay Time to Logic High at Output	t_{PLH}		1.1	2.5	μs		4,6	11
Common Mode Transient Immunity at Logic High Level Output	CM_H		1000		V/μs	I_F = 0mA, V_{CM} = $10V_{p-p}$	7	9,11
Common Mode Transient Immunity at Logic Low Level Output	CM_L		-1000		V/μs	V_{CM} = $10V_{p-p}$	7	9,11

*All typicals at 25°C.

(See following page for notes.)

Electrical Specifications

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Logic High Output Current	I_{OH}		0.5		nA	T_A = 25°C, I_{F1} = I_{F2} = 0mA, V_{O1} = V_{O2} = V_{CC} = 5.5V	5	5
				50	μA	I_{F1} = I_{F2} = 0 mA, V_{O1} = V_{O2} = V_{CC} = 5.5V		5
Logic High Supply Current	I_{CCH}		0.05	4	μA	I_{F1} = I_{F2} = 0 mA, V_{O1} = V_{O2} = Open, V_{CC} = 5.5V		
Input Reverse Breakdown Voltage	V_R	5			V	I_F = 10 μA, T_A = 25°C		5
Input Capacitance	C_{IN}		60		pF	f = 1 MHz, V_F = 0 V		5
Input-Output Insulation Leakage Current	I_{I-O}			1.0	μA	45% Relative Humidity, t = 5s, V_{I-O} = 3000V dc, T_A = 25°C		7, 12
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	V_{I-O} = 500V dc		7
Capacitance (Input-Output)	C_{I-O}		0.6		pF	f = 1 MHz		7
Input-Input Insulation Leakage Current	I_{I-I}		0.005		μA	45% Relative Humidity, t = 5s, V_{I-I} = 500V dc		8
Resistance (Input-Input)	R_{I-I}		10^{11}		Ω	V_{I-I} = 500V dc		8
Capacitance (Input-Input)	C_{I-I}		0.25		pF	f = 1 MHz		8

Notes:

1. Derate linearly above 70° C free-air temperature at a rate of 0.8mA/° C.
2. Derate linearly above 70° C free-air temperature at a rate of 1.6mA/° C.
3. Derate linearly above 70° C free-air temperature at a rate of 0.9mW/° C.
4. Derate linearly above 70° C free-air temperature at a rate of 1.0mW/° C.
5. Each channel.
6. CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
7. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
8. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.
9. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.0V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8V).
10. The 7.5k load represents 1 LSTTL until load of 0.36mA and a 20kΩ pull-up resistor.
11. The 4.7k load represents 1 LSTTL unit load of 0.36mA and an 8.2kΩ pull-up resistor.
12. This is a proof test to validate the UL 220 Vac rating.

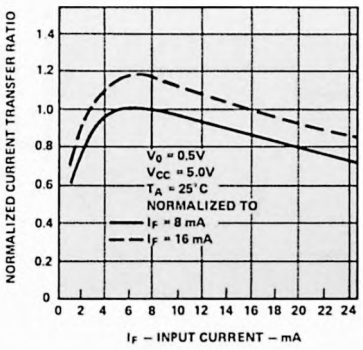


Figure 1. Current Transfer Ratio vs. Input Current

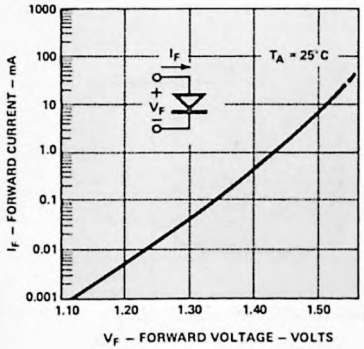


Figure 2. Input Current vs. Forward Voltage

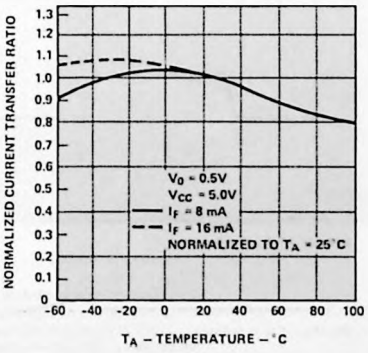


Figure 3. Current Transfer Ratio vs. Temperature

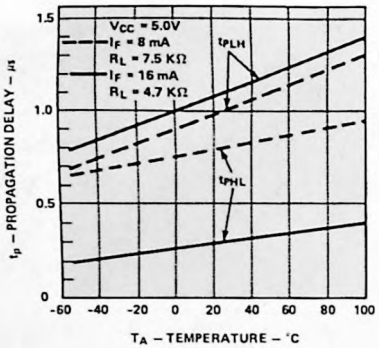


Figure 4. Propagation Delay vs. Temperature

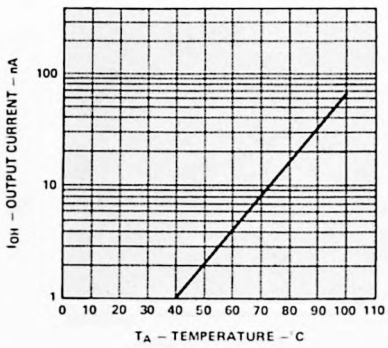


Figure 5. Logic High Output Current vs. Temperature

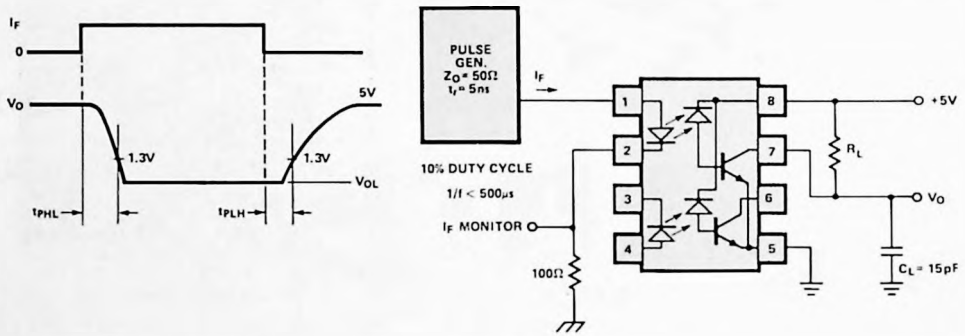


Figure 6. Switching Test Circuit

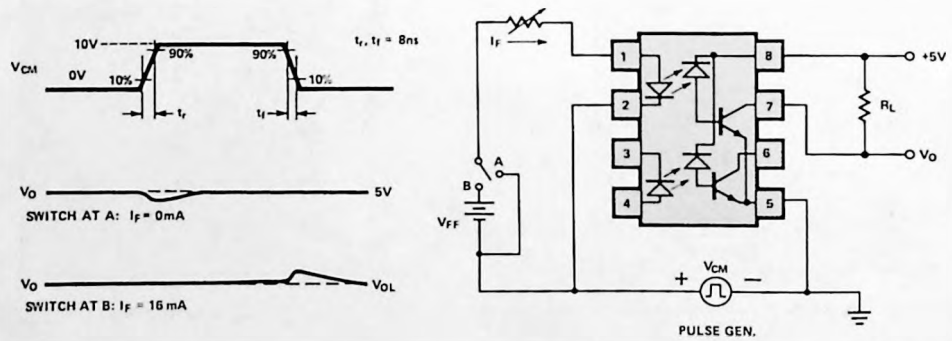


Figure 7. Test Circuit for Transient Immunity and Typical Waveforms

Recommended Operation

The HCPL-2533 optocoupler is specified for use in LSTTL-to-LSTTL and TTL-to-LSTTL interfaces. The recommended circuits show the interface design and give suggested component values. The input current I_F is given as both a nominal value and a range. The range in I_F results from the tolerances in V_{CC} and the input resistor R_{IN}. The CTR of the optocoupler is given as the minimum initial value over temperature, taken directly from the Electrical Specifications. The value given for $I_{OL}(min)$ is based on the minimum CTR and the minimum I_F using worst case values for R_L and V_{CC}. The resulting $I_{OL}(min)$ has ample design margin, allowing more than 20% for CTR degradation even under these worst case conditions. For additional information on CTR degradation see Application Note 1002.

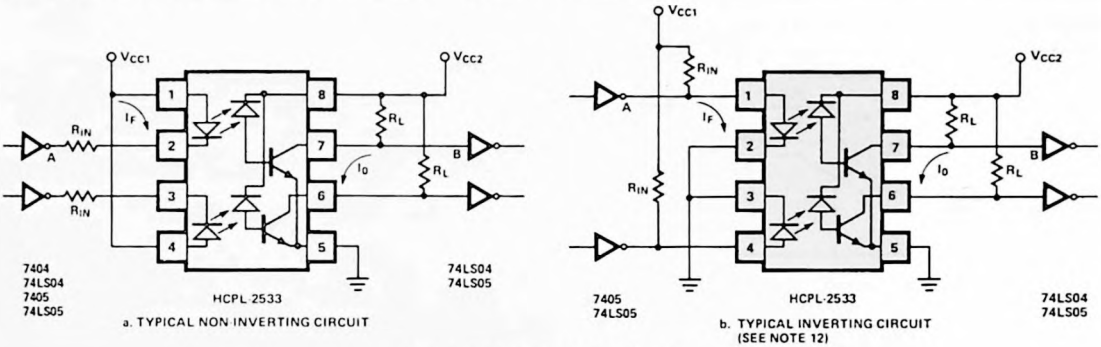


Figure 8. Recommended Circuits

Recommended Circuit Design Parameters

Parameter	Symbol	LSTTL to LSTTL	TTL to LSTTL	Units	Comments	Fig.	Note
INPUT							
Logic Low Output Voltage — Input Gate	$V_{OL(A)}$	0.5	0.4	V	Maximum		
Supply Voltage — Input	V_{CC1}	5.0	5.0	V	±5%		
Input Resistor	R_{IN}	360	180	Ω	±5%	8a	
		430	200			8b	
Input Current	I_F	8	16	mA	Nominal		
Input Current Range	I_F	6.75—10	14.0—20	mA		8a	
			14.5—20			8b	
OUTPUT							
Logic Low Output Voltage — HCPL-2533	$V_{OL(B)}$	0.5	0.5	V	Maximum		
Supply Voltage — Output	V_{CC2}	5.0	5.0	V	±5%		
Pull-Up Resistor	R_L	20	8.2	kΩ	±5%		13
Required Current Sink for Logic Low	I_{OL} (max)	0.61	1.0	mA	Worst Case V_{CC}, R_L, $I_{IL(B)}$		14
HCPL-2533 Current Transfer Ratio	CTR	11	9	%	Minimum T_A = 0°C to +70°C		
Logic Low Output Current — HCPL-2533	I_{OL} (min)	0.74	1.26	mA	Worst Case V_{CC}, CTR, I_F	8a	15
			1.30		T_A = 0°C to +70°C	8b	
Data Rate	f_D	250	250	Kb/s	NRZ, T_A = 25°C		16

Notes:

12. The inverting circuit has higher power consumption and must use open collector gates on the input.
13. The load resistor R_L must be large enough to guarantee logic LOW and small enough to guarantee logic HIGH under worst case conditions:

$$\frac{V_{CC(max)} - V_{OL}}{I_{OL(2533)} - I_{IL(B)}} \le R_L \le \frac{V_{CC(min)} - V_{IH(B)}}{I_{OH(2533)} - I_{IH(B)}}$$

The selection of R_L is the same for both inverting and non-inverting circuits.

14. The maximum current sink required for logic LOW is:
$$I_{OL(max)} = I_{IL(B)(max)} + I_{R(max)}$$
where I_R is the current through R_L.
15. The ratio of $I_{OL(min)}$ to $I_{OL(max)}$ gives the design margin for CTR degradation. See Application Note 1002.
16. The maximum data rate is defined as

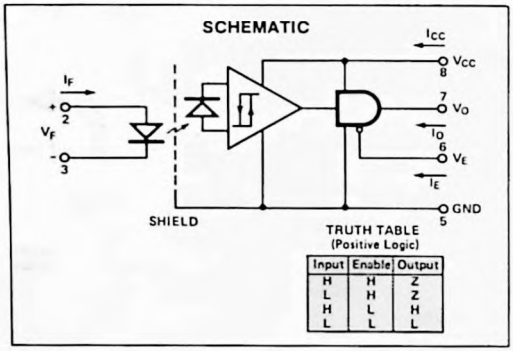
$$f_D = \frac{1}{t_{PHL} + t_{PLH}} \text{ bits/second NRZ}$$

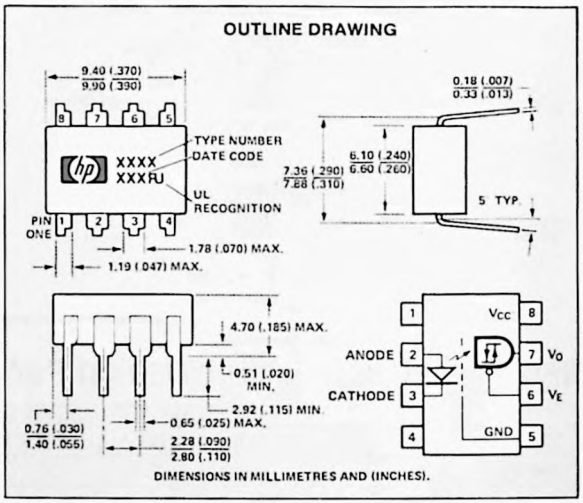
HEWLETT PACKARD

LOW INPUT CURRENT LOGIC GATE OPTOCOUPLER

HCPL-2200

TECHNICAL DATA JANUARY 1984





Features

- COMPATIBLE WITH LSTTL, TTL, AND CMOS LOGIC
- 2.5 MBAUD GUARANTEED OVER TEMPERATURE
- LOW INPUT CURRENT (1.6 mA)
- WIDE V_{CC} RANGE (4.5 TO 20 VOLTS)
- THREE STATE OUTPUT (NO PULLUP RESISTOR REQUIRED)
- GUARANTEED PERFORMANCE FROM 0° C TO +85° C
- RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES, INC. (FILE NO. E55361)
- INTERNAL SHIELD FOR HIGH COMMON MODE REJECTION
- DIELECTRIC WITHSTAND TESTED AT 3000 Vdc FOR A WORKING VOLTAGE OF 220 Vac

Applications

- Isolation of High Speed Logic Systems
- Computer-Peripheral Interfaces
- Microprocessor System Interfaces
- Ground Loop Elimination
- Pulse Transformer Replacement
- Isolated Buss Driver
- High Speed Line Receiver

Description

The HCPL-2200 is an optically coupled logic gate that combines a GaAsP LED and an integrated high gain photon detector. The detector has a three state output stage and has a detector threshold with hysteresis. The three state output eliminates the need for a pullup resistor and allows for direct drive of data busses. The hysteresis provides typically 0.1 mA of differential mode noise immunity and eliminates the potential for output signal chatter. The detector IC has an internal shield that provides a guaranteed common mode transient immunity of 1,000 volts/μsec. Improved power supply rejection eliminates the need for special power supply bypassing precautions.

The Electrical and Switching Characteristics of the HCPL-2200 are guaranteed over the temperature range of 0° C to 85° C. The HCPL-2200 is guaranteed to operate over a V_{CC} range of 4.5 volts to 20 volts. Low I_F and wide V_{CC} range allow compatibility with TTL, LSTTL, and CMOS logic. Low I_F and low I_{CC} result in lower power consumption compared to other high speed optocouplers. Logic signals are transmitted with a typical propagation delay of 160 nsec when a 120 pF peaking capacitor is used in parallel with the 1.1KΩ current limiting resistor.

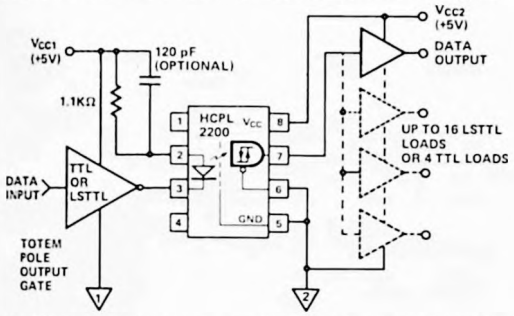
The HCPL-2200 is useful for isolating high speed logic interfaces, buffering of input and output lines, and implementing isolated line receivers in high noise environments.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	4.5	20	Volts
Enable Voltage High	V_{EH}	2.0	20	Volts
Enable Voltage Low	V_{EL}	0	0.8	Volts
Forward Input Current	$I_{F(ON)}$	1.6*	5	mA
Forward Input Current	$I_{F(OFF)}$	—	0.1	mA
Operating Temperature	T_A	0	85	°C
Fan Out	N		4	TTL Loads

*1.6 mA condition includes a CTR degradation guardband.

Recommended Circuit Design



The 120 pF capacitor may be omitted in applications where 500 ns propagation delay is sufficient.

Figure 1. Recommended LSTTL to LSTTL Circuit

Absolute Maximum Ratings

(No Derating Required up to 70° C)

Storage Temperature ..... -55° C to +125° C
Operating Temperature ..... -40° C to +85° C[1]
Lead Solder Temperature ..... 260° C for 10 s
(1.6 mm below seating plane)
Average Forward Input Current — I_F ..... 10 mA
Peak Transient Input Current — I_F 1A
(≤1 μs Pulse Width, 300 pps)
Reverse Input Voltage 5V
Supply Voltage — V_{CC} ..... 0.0V min., 20V max.
Three State Enable Voltage
— V_E ..... -0.5V min., 20V max.
Output Voltage — V_O ..... -0.5V min., 20V max.
Total Package Power
Dissipation — P ..... 210 mW[1]
Average Output Current — I_O ..... 25 mA

Electrical Characteristics

For 0° C ≤ T_A[1] ≤ 85° C, 4.5 V ≤ V_{CC} ≤ 20 V, 1.6 mA ≤ $I_{F(ON)}$ ≤ 5 mA, 2.0 V ≤ V_{EH} ≤ 20 V, 0.0 V ≤ V_{EL} ≤ 0.8 V, 0 mA ≤ $I_{F(OFF)}$ ≤ 0.1 mA. All Typicals at T_A = 25° C, V_{CC} = 5V, $I_{F(ON)}$ = 3 mA unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions		Figure	Note
Logic Low Output Voltage	V_{OL}			0.5	Volts	I_{OL} = 6.4 mA (4 TTL Loads)		2	
Logic High Output Voltage	V_{OH}	2.4			Volts	I_{OH} = -2.6 mA		3	
Output Leakage Current (V_{OUT} > V_{CC})	I_{OHH}			100	μA	V_O = 5.5V	I_F = 5 mA		
				500	μA	V_O = 20V	V_{CC} = 4.5V		
Logic High Enable Voltage	V_{EH}	2.0			Volts				
Logic Low Enable Voltage	V_{EL}			0.8	Volts				
Logic High Enable Current	I_{EH}			20	μA	V_{EN} = 2.7V			
				100	μA	V_{EN} = 5.5V			
			.004	250	μA	V_{EN} = 20V			
Logic Low Enable Current	I_{EL}			-0.32	mA	V_{EN} = 0.4V			
Logic Low Supply Current	I_{CCL}		4.5	6.0	mA	V_{CC} = 5.5V	I_F = 0 mA		
			5.25	7.5	mA	V_{CC} = 20V	V_E = Don't Care		
Logic High Supply Current	I_{CCH}		2.7	4.5	mA	V_{CC} = 5.5V	I_F = 5 mA,		
			3.1	6.0	mA	V_{CC} = 20V	V_E = Don't Care		
High Impedance State Output Current	I_{OZL}			-20	μA	V_O = 0.4V	V_{EN} = 2V, I_F = 5 mA		
	I_{OZH}			20	μA	V_O = 2.4V	V_{EN} = 2V, I_F = 0		
				100	μA	V_O = 5.5V			
				500	μA	V_O = 20V			
Logic Low Short Circuit Output Current	I_{OSL}	25			mA	V_O = V_{CC} = 5.5V	I_F = 0 mA		2
		40			mA	V_O = V_{CC} = 20V			
Logic High Short Circuit Output Current	I_{OSH}	-10			mA	V_{CC} = 5.5V	I_F = 5 mA, V_O = GND		2
		-25			mA	V_{CC} = 20V			
Input Current Hysteresis	I_{HYS}		0.12		mA	V_{CC} = 5V		4	
Input Forward Voltage	V_F		1.5	1.70	Volts	I_F = 5 mA, T_A = 25° C		5	
Input Reverse Breakdown Voltage	V_R	5			Volts	I_R = 10 μA at T_A = 25° C			
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		-1.7		mV/° C	I_F = 5 mA			
Input-Output Insulation Leakage Current	I_{I-O}			1	μA	V_{I-O} = 3000 VDC T_A = 25° C, t = 5s Relative Humidity = 45%			3, 7
Input-Output Resistance	R_{I-O}		10^{12}		ohms	V_{I-O} = 500 VDC			3
Input-Output Capacitance	C_{I-O}		0.6		pF	f = 1 MHz, V_{I-O} = 0 VDC			3
Input Capacitance	C_{IN}		90		pF	f = 1 MHz, V_F = 0V, Pins 2 and 3			

Switching Characteristics

For $0°C \le T_A^{[1]} \le 85°C$, $4.5V \le V_{CC} \le 20V$, $1.6\ mA \le I_{F(ON)} \le 5\ mA$, $0.0\ mA \le I_{F(OFF)} \le 0.1\ mA$. All Typicals at $T_A = 25°C$, $V_{CC} = 5V$, $I_{F(ON)} = 3\ mA$ unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to Logic Low Output Level	t_{PHL}		210		ns	Without Peaking Capacitor	6,7	4,5
			160	400		With Peaking Capacitor		
Propagation Delay Time to Logic High Output Level	t_{PLH}		170		ns	Without Peaking Capacitor	6,7	4,5
			115	400		With Peaking Capacitor		
Output Enable Time to Logic High	t_{PZH}		25		ns		8,10	
Output Enable Time to Logic Low	t_{PZL}		28		ns		8,9	
Output Disable Time from Logic High	t_{PHZ}		105		ns		8,10	
Output Disable Time from Logic Low	t_{PLZ}		60		ns		8,9	
Output Rise Time (10-90%)	t_r		55		ns		6,11	
Output Fall Time (90-10%)	t_f		15		ns		6,11	
Logic High Common Mode Transient Immunity	CM_H	-1000	-10,000		V/μs	$T_A = 25°C$, $I_F = 1.6\ mA$, $V_{CM} = 50\ V$	12,13	6
Logic Low Common Mode Transient Immunity	CM_L	1000	10,000		V/μs	$T_A = 25°C$, $I_F = 0$, $V_{CM} = 50\ V$	12,13	6

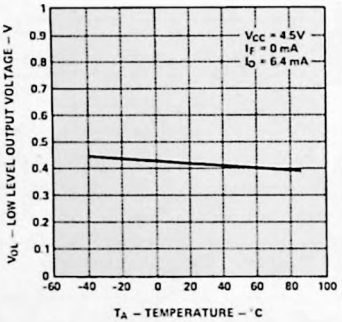


Figure 2. Typical Logic Low Output Voltage vs. Temperature

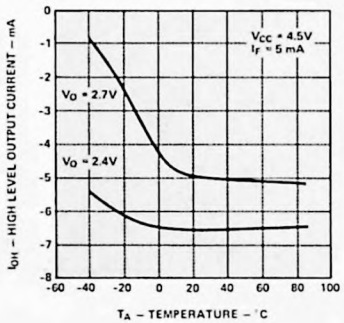


Figure 3. Typical Logic High Output Current vs. Temperature

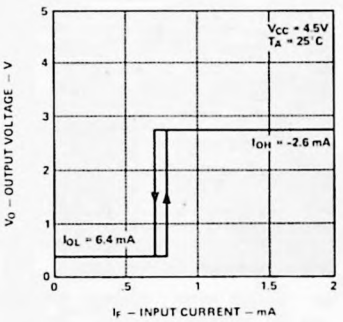


Figure 4. Output Voltage vs. Forward Input Current

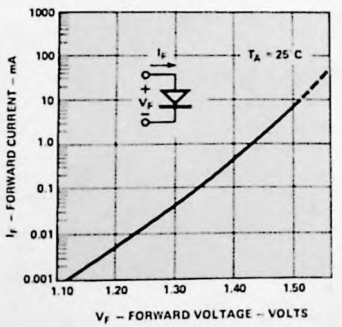
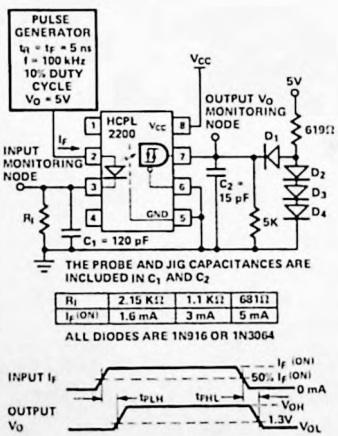


Figure 5. Typical Input Diode Forward Characteristic



R_l	2.15 KΩ	1.1 KΩ	681Ω
$I_{F(ON)}$	1.6 mA	3 mA	5 mA

Figure 6. Test Circuit for t_{PLH}, t_{PHL}, t_r and t_f

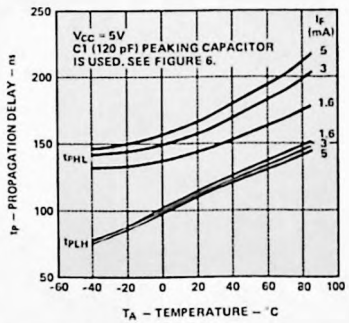


Figure 7. Typical Propagation Delays vs. Temperature

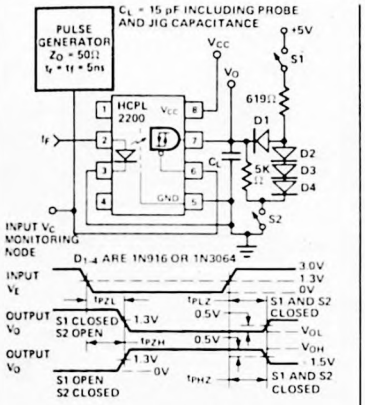


Figure 8. Test Circuit for t_{PHZ}, t_{PZH}, t_{PLZ}, and t_{PZL}

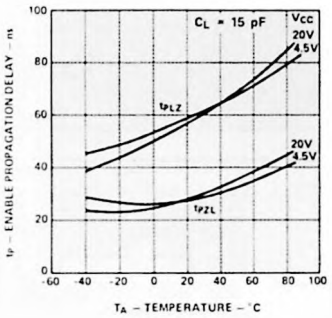


Figure 9. Typical Logic Low Enable Propagation Delay vs. Temperature

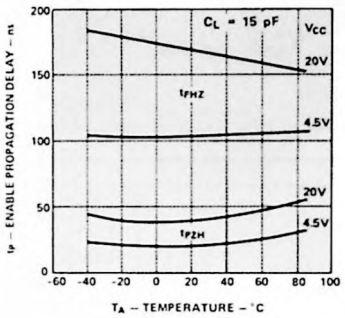


Figure 10. Typical Logic High Enable Propagation Delay vs. Temperature

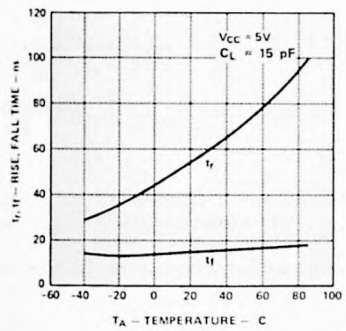


Figure 11. Typical Rise, Fall Time vs. Temperature

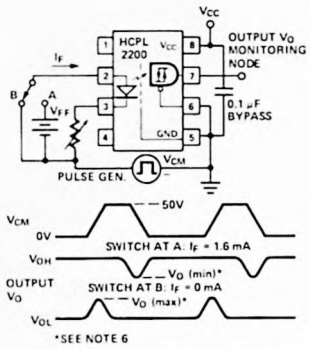


Figure 12. Test Circuit for Common Mode Transient Immunity and Typical Waveforms

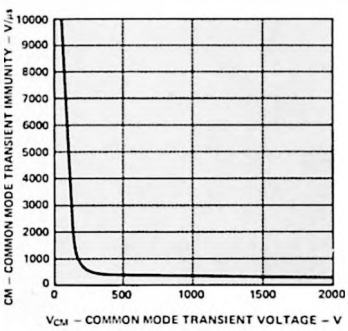


Figure 13. Typical Common Mode Transient Immunity vs. Common Mode Transient Amplitude

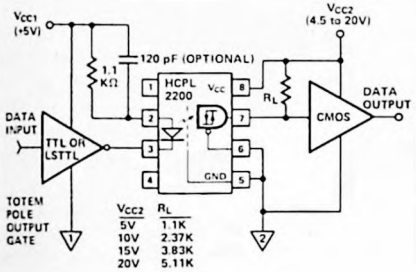


Figure 14. LSTTL to CMOS Interface Circuit

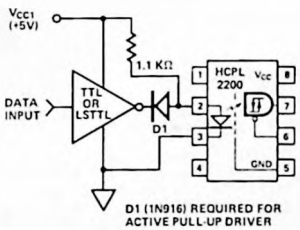


Figure 15. Recommended LED Drive Circuit

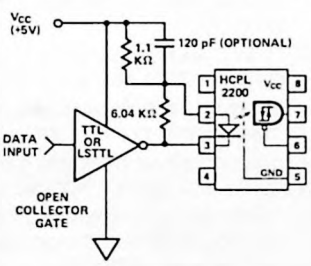


Figure 16. Series LED Drive with Open Collector Gate (6.04 KΩ Resistor Shunts I_{OH} from the LED)

The 120 pF capacitor may be omitted in applications where 500 ns propagation delay is sufficient.

Notes:

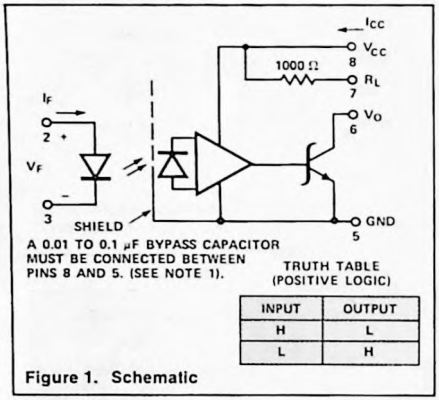
1. Derate total package power dissipation, P, linearly above 70° C free air temperature at a rate of 4.5 mW/° C.
2. Duration of output short circuit time should not exceed 10 ms.
3. Device considered a two terminal device: pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.
4. The t_{PLH} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.3V point on the leading edge of the output pulse. The t_{PHL} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.3V point on the trailing edge of the output pulse.
5. When the peaking capacitor is omitted, propagation delay times may increase by 100 ns.
6. CM_L is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic low state (V_O < 0.8V). CM_H is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic high state (V_O > 2.0V).
7. This is a proof test to validate the UL 220 Vac rating.

HEWLETT PACKARD

LOW INPUT CURRENT HIGH SPEED OPTOCOUPLER

HCPL-2300

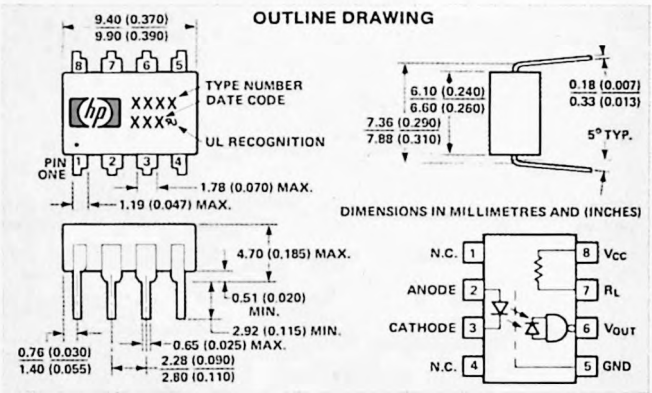
TECHNICAL DATA JANUARY 1984



TRUTH TABLE (POSITIVE LOGIC)

INPUT	OUTPUT
H	L
L	H

Figure 1. Schematic



Features

- GUARANTEED LOW THRESHOLDS: I_F = 0.5 mA, $V_F \leq 1.5$ V
- HIGH SPEED: GUARANTEED 5 MBd OVER TEMPERATURE
- VERSATILE: COMPATIBLE WITH TTL, LSTTL AND CMOS
- NEW, MORE EFFICIENT 820 nm AlGaAs IRED
- INTERNAL SHIELD FOR GUARANTEED COMMON MODE REJECTION
- SCHOTTKY CLAMPED, OPEN COLLECTOR OUTPUT WITH OPTIONAL INTEGRATED PULL-UP RESISTOR
- STATIC AND DYNAMIC PERFORMANCE GUARANTEED FROM -40°C to 85°C
- SPECIAL SELECTION FOR LOW FORWARD CURRENT APPLICATIONS ($I_F \geq 150$ μA)
- DIELECTRIC WITHSTAND TESTED AT 3000 V dc FOR A WORKING VOLTAGE OF 220 Vac
- RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES, INC. (FILE NO. E55361)

Applications

- GROUND LOOP ELIMINATION
- COMPUTER-PERIPHERAL INTERFACES
- LEVEL SHIFTING
- MICROPROCESSOR SYSTEM INTERFACES
- DIGITAL ISOLATION FOR A/D, D/A CONVERSION
- RS-232-C INTERFACE
- HIGH SPEED, LONG DISTANCE ISOLATED LINE RECEIVER

Description

The HCPL-2300 optocoupler combines an 820 nm AlGaAs photon emitting diode with an integrated high gain photon detector. This combination of Hewlett-Packard designed and manufactured semiconductor devices brings new high performance capabilities to designers of isolated logic and data communication circuits.

The new low current, high speed AlGaAs emitter manufactured with a unique diffused junction, has the virtue of fast rise and fall times at low drive currents. The HCPL-2300 has a typical propagation delay of 120 ns at 0.5 mA forward current. With special selection, the device can achieve 80 ns propagation delay at 150 μA. Figure 6 illustrates the propagation delay vs. input current characteristic. These unique characteristics enable this device to be used in an RS-232-C interface with ground loop isolation and improved common mode rejection. As a line receiver, the HCPL-2300 will operate over longer line lengths for a given data rate because of lower I_F and V_F specifications.

The output of the shielded integrated detector circuit is an open collector Schottky clamped transistor. The shield, which shunts capacitively coupled common mode noise to ground, provides a guaranteed transient immunity specification of 100 V/μs. The output circuit includes an optional integrated 1000 Ohm pull-up resistor for the open collector. This gives designers the flexibility to use the internal resistor for pull-up to five volt logic or to use an external resistor for 18 volt CMOS logic.

The Electrical and Switching Characteristics of the HCPL-2300 are guaranteed over a temperature range of -40°C to 85°C. This data sheet will allow users of the HCPL-2300 to confidently implement all necessary static and dynamic performance requirements which may be subjected to a broad range of operating environments.

Recommended Operating Conditions

		Sym.	Min.	Max.	Units
Input Voltage, Low Level		V_{FL}	-2.5	0.8	V
Input Current High Level	0° C to 85° C	I_{FH}	0.5	1.0	mA
	-40° C to 85° C		0.5	0.75	
Supply Voltage, Output		V_{CC}	4.75	5.25	V
Fan Out (TTL Load)		N		5	
Operating Temperature		T_A	-40	85	°C

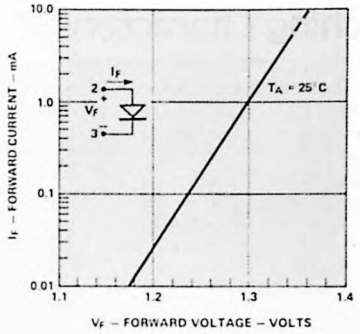


Figure 2. Typical Input Diode Forward Characteristic.

Absolute Maximum Ratings

(No derating required)

Parameter	Symbol	Min.	Max.	Units	Reference
Storage Temperature	T_S	-55	125	°C	
Operating Temperature	T_A	-40	85	°C	
Lead Solder Temperature	260° C for 10 s. (1.6 mm below seating plane)				
Average Forward Input Current	I_F		5	mA	See Note 2
Reverse Input Voltage	V_R		4.5	V	
Supply Voltage	V_{CC}	0.0	7.0	V	
Pull-up Resistor Voltage	V_{RL}	-0.5	V_{CC}	V	
Output Collector Current	I_O	-25	25	mA	
Input Power Dissipation	P_I		10	mW	
Output Collector Power Dissipation	P_O		40	mW	
Output Collector Voltage	V_O	-0.5	18	V	

Electrical Characteristics

For -40° C ≤ T_A ≤ 85° C, 4.75 V ≤ V_{CC} ≤ 5.25 V, V_{FL} ≤ 0.8 V, unless otherwise specified.
All typicals at T_A = 25° C, V_{CC} = 5 V, unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
High Level Output Current	I_{OH}		0.05	250	μA	V_F = 0.8 V, V_O = 18 V	4	
				10		V_F = 0.8 V, V_O = 18 V, T_A = 25° C		
Low Level Output Voltage	V_{OL}		0.4	0.5	V	I_F = 0.5 mA, I_{OL} (Sinking) = 8 mA	3	
High Level Supply Current	I_{CCH}		4.0	6.3	mA	I_F = 0 mA, V_{CC} = 5.25 V		
Low Level Supply Current	I_{CCL}		6.2	10.0	mA	I_F = 1.0 mA, V_{CC} = 5.25 V		
Input Forward Voltage	V_F	1.0	1.3	1.5	V	I_F = 1.0 mA, T_A = 25° C	2	
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		-1.6		mV/° C	I_F = 1.0 mA		
Input Reverse Breakdown Voltage	BV_R	4.5			V	I_R = 10 μA, T_A = 25° C		
Input Capacitance	C_{IN}		18		pF	V_F = 0 V, f = 1 MHz		
Input-Output Leakage Current	I_{I-O}			1	μA	Relative Humidity = 45%, T_A = 25° C, t = 5 s, V_{I-O} = 3000 V DC		3, 9
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 V		3
Capacitance (Input-Output)	C_{I-O}		0.6		pF	f = 1 MHz		3
Internal Pull-up Resistor	R_L	680	1000	1700	Ohms			

Switching Characteristics

For $-40°C \le T_A \le 85°C$, $0.5\ mA \le I_{FH} \le 0.75\ mA$;
For $0°C \le T_A \le 85°C$, $0.5\ mA \le I_{FH} \le 1.0\ mA$; With $4.75\ V \le V_{CC} \le 5.25\ V$, $V_{FL} \le 0.8\ V$, unless otherwise specified.
All typicals at $T_A = 25°C$, $V_{CC} = 5\ V$, $I_{FH} = 0.625\ mA$, unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to Logic High Output Level	t_{PLH}		95		ns	$C_P = 0$ pF	5, 6, 8	4, 8
			85	160		$C_P = 20$ pF	5, 8	
Propagation Delay Time to Logic Low Output Level	t_{PHL}		110		ns	$C_P = 0$ pF	5, 6, 8	5, 8
			35	200		$C_P = 20$ pF	5, 8	
Output Rise Time (10-90%)	t_r		40		ns	$C_P = 20$ pF	7, 8	8
Output Fall Time (90-10%)	t_f		20		ns			
Common Mode Transient Immunity at High Output Level	CM_H	100	400		V/μs	$V_{CM} = 50$ V (peak), V_O (min.) = 2 V, $R_L = 560\Omega$, $I_F = 0$ mA	9, 10	6
Common Mode Transient Immunity at Low Output Level	CM_L	-100	-400		V/μs	$V_{CM} = 50$ V (peak), V_O (max.) = 0.8 V, $R_L = 560\Omega$, $I_F = 0.5$ mA	9, 10	7

(See page 5-35 for Notes)

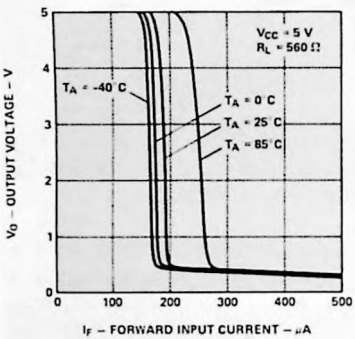


Figure 3. Typical Output Voltage vs. Forward Input Current vs. Temperature.

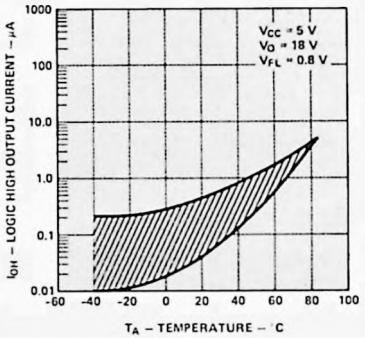


Figure 4. Typical Logic High Output Current vs. Temperature.

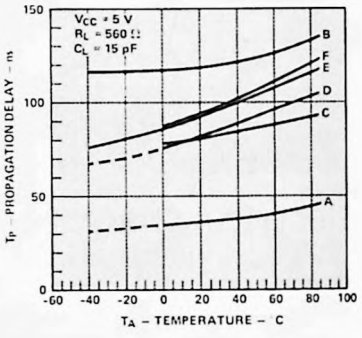


Figure 5. Typical Propagation Delay vs. Temperature and Forward Current With and Without Application of a Peaking Capacitor.

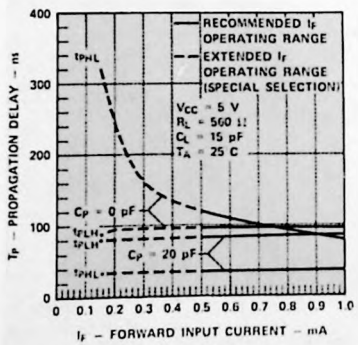


Figure 6. Typical Propagation Delay vs. Forward Current.

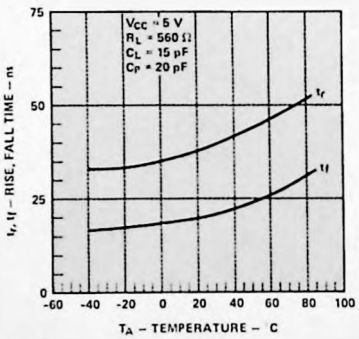


Figure 7. Typical Rise, Fall Time vs. Temperature.

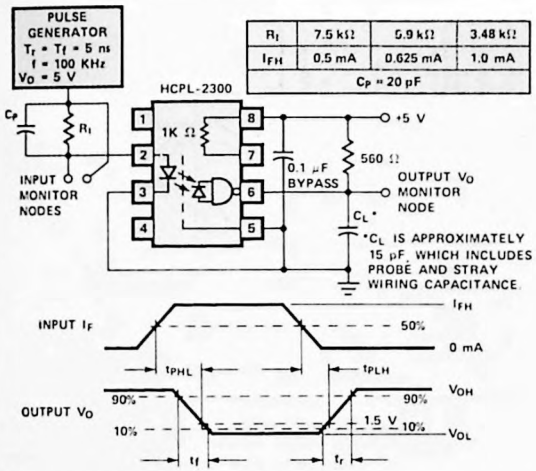


Figure 8. Test Circuit for t_{PHL}, t_{PLH}, t_r and t_f.

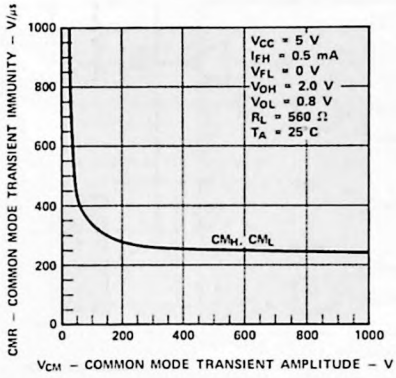


Figure 9. Typical Common Mode Transient Immunity vs. Common Mode Transient Amplitude.

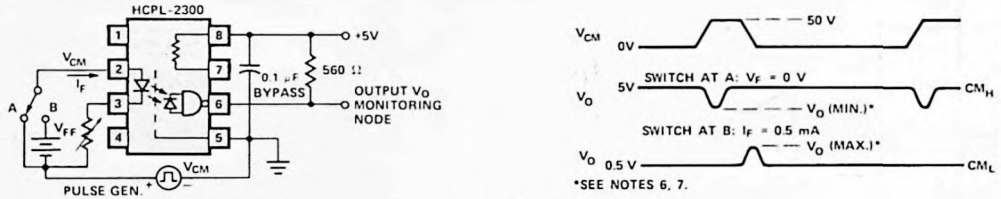


Figure 10. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

Applications

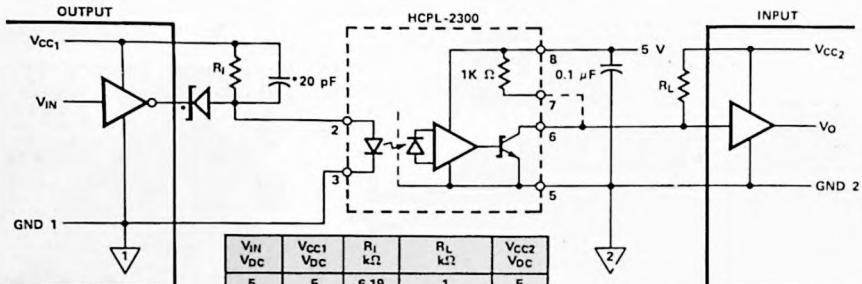
The HCPL-2300 optocoupler has the unique combination of low 0.5 mA LED operating drive current at a 5 MBd speed performance. Low power supply current requirement of 10 mA maximum and the ability to provide isolation between logic systems fulfills numerous applications ranging from logic level translations, line receiver and party line receiver applications, microprocessor I/O port isolation, etc. The open collector output allows for wired-OR arrangement. Specific interface circuits are illustrated in Figures 11 through 18 with corresponding component values, performance data and recommended layout.

For -40°C to 85°C operating temperature range, a mid range LED forward current (I_F) of 0.625 mA is recommended in order to prevent overdriving the integrated circuit detector due to increased LED efficiency at temperatures between 0°C and -40°C. For narrower temperature range of 0°C to 85°C, a suggested operating LED current of 0.75 mA is recommended for the mid range operating point and for minimal propagation delay skew. A peaking capacitance of 20 pF in parallel with the current limiting resistor for the LED shortens t_{PHL} by approximately 33% and t_{PLH} by 13%. Maintaining LED forward voltage (V_F) below 0.8 V will guarantee that the HCPL-2300 output is off.

The recommended shunt drive technique for TTL/LSTTL/CMOS of Figure 11 provides for optimal speed performance, no leakage current path through the LED, and reduced common mode influences associated with series switching of a "floating" LED. Alternate series drive techniques with either an active CMOS inverter or an open collector TTL/LSTTL inverter are illustrated in Figures 12 and 13 respectively. Open collector leakage current of 250 μA has been compensated by the 3.16K Ohms resistor (Figure 13) at the expense of twice the operating forward current.

An application of the HCPL-2300 as an unbalanced line receiver for use in long line twisted wire pair communication links is shown in Figure 14. Low LED I_F and V_F allow longer line length, higher speed and multiple stations on the line in comparison to higher I_F, V_F optocouplers. Greater speed performance along with nearly infinite common mode immunity are achieved via the balanced split phase circuit of Figure 15. Basic balanced (differential) line receiver can be accomplished with one HCPL-2300 in Figure 15, but with a typical 400 V/μs common mode immunity. Data rate versus distance for both the above unbalanced and balanced line receiver applications are compared in Figure 16. The RS-232-C interface circuit of Figure 17 provides guaranteed minimum common mode immunity of 100 V/μs while maintaining the 2:1 dynamic range of I_F.

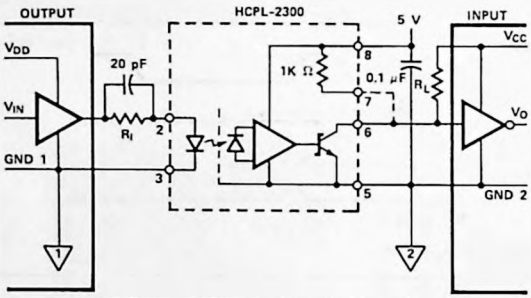
A recommended layout for use with an internal 1000 Ohms resistor or an external pull-up resistor and required V_{CC} bypass capacitor is given in Figure 18. V_{CC1} is used with an external pull-up resistor for output voltage levels (V0) greater than or equal to 5 V. As illustrated in Figure 18, an optional V_{CC} and GND trace can be located between the input and the output leads of the HCPL-2300 to provide additional noise immunity at the compromise of insulation capability (VI-0).



V_{IN} V_{DC}	V_{CC1} V_{DC}	R_I kΩ	R_L kΩ	V_{CC2} V_{DC}
5	5	6.19	1 (INTERNAL)	5
10	10	14.7	2.37	10
15	15	21.5	3.16	15

*SCHOTTKY DIODE (HP 5082-2800, OR EQUIVALENT) AND 20 pF CAPACITOR ARE NOT REQUIRED FOR UNITS WITH OPEN COLLECTOR OUTPUT.

Figure 11. Recommended Shunt Drive Circuit for Interfacing Between TTL/LSTTL/CMOS Logic Systems.



V_{IN} V_{DC}	V_{DD} V_{DC}	R_I kΩ	R_L kΩ	V_{CC} V_{DC}
5	5	5.11	1 (INTERNAL)	5
10	10	13.3	2.37	10
15	15	19.6	3.16	15

Figure 12. Active CMOS Series Drive Circuit.

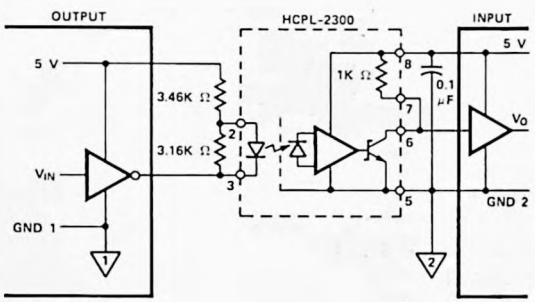


Figure 13. Series Drive from Open Collector TTL/LSTTL Units.

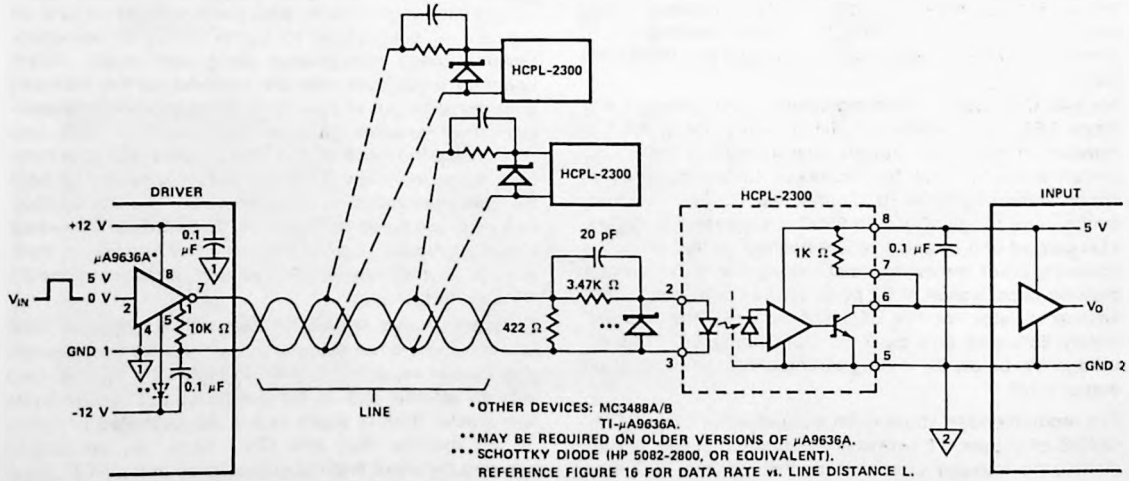
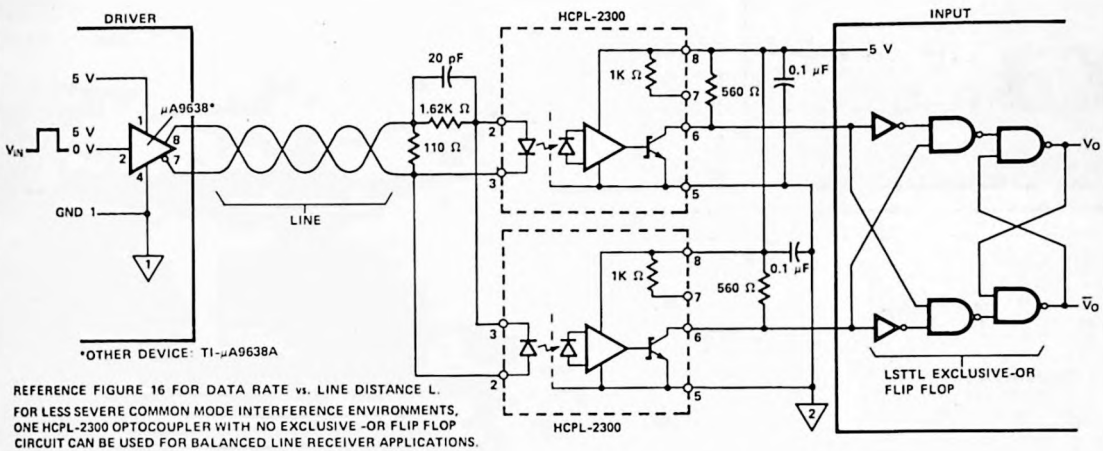


Figure 14. Application of HCPL-2300 as Isolated, Unbalanced Line Receiver(s).



REFERENCE FIGURE 16 FOR DATA RATE vs. LINE DISTANCE L.
FOR LESS SEVERE COMMON MODE INTERFERENCE ENVIRONMENTS, ONE HCPL-2300 OPTOCOUPLER WITH NO EXCLUSIVE -OR FLIP FLOP CIRCUIT CAN BE USED FOR BALANCED LINE RECEIVER APPLICATIONS.
$V_O = V_{IN}$.

Figure 15. Application of Two HCPL-2300 Units Operating as an Isolated, High Speed, Balanced, Split Phase Line Receiver with Significantly Enhanced Common Mode Immunity.

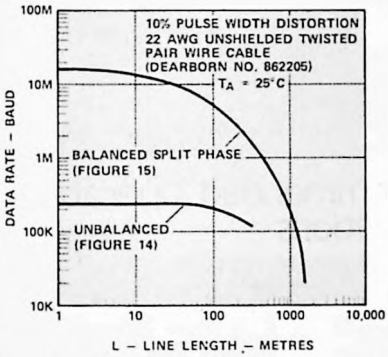


Figure 16. Typical Point to Point Data Rate vs. Length of Line for Unbalanced (Figure 14) and Balanced (Figure 15) Line Receivers using HCPL-2300 Optocouplers.

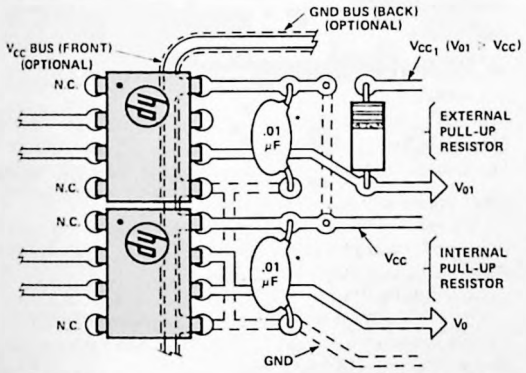


Figure 18. Recommended Printed Circuit Board Layout.

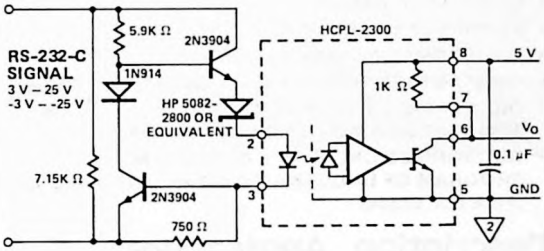


Figure 17. RS-232-C Interface Circuit with HCPL-2300. 0° C = T_A = 85° C.

NOTES:
1. Bypassing of the power supply line is required with a 0.01 μF ceramic disc capacitor adjacent to each optocoupler as illustrated in Figure 18. The power supply bus for the optocoupler(s) should be separate from the bus for any active loads, otherwise a larger value of bypass capacitor (up to 0.1 μF) may be needed to suppress regenerative feedback via the power supply.
2. Peaking circuits may produce transient input currents up to 100 mA, 500 ns maximum pulse width, provided average current does not exceed 5 mA.
3. Device considered a two terminal device: pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.
4. The t_{PLH} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
5. The t_{PHL} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.5 V point on the leading edge of the output pulse.
6. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (i.e., V_{OUT} > 2.0 V).
7. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., V_{OUT} < 0.8 V).
8. C_P is the peaking capacitance. Refer to test circuit in Figure 8.
9. This is a proof test to validate the UL 220 Vac rating.

HEWLETT PACKARD

LSTTL/TTL COMPATIBLE OPTOCOUPLER

6N137

TECHNICAL DATA JANUARY 1984

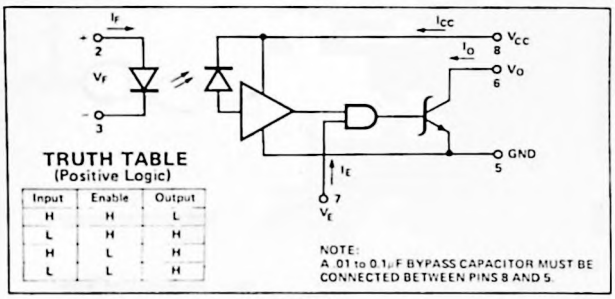


Figure 1.

Features

- LSTTL/TTL COMPATIBLE: 5 V SUPPLY
- ULTRA HIGH SPEED
- LOW INPUT CURRENT REQUIRED
- HIGH COMMON MODE REJECTION
- GUARANTEED PERFORMANCE OVER TEMPERATURE
- DIELECTRIC WITHSTAND TESTED AT 3000 Vdc FOR A WORKING VOLTAGE OF 220 Vac
- RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES, INC. (FILE NO. E55361)

Description Applications

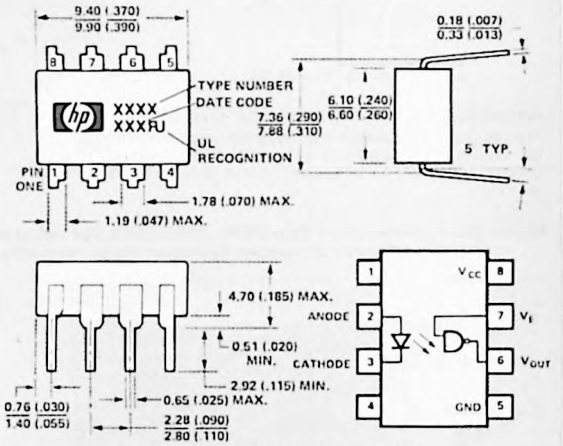
The 6N137 consists of a GaAsP photon emitting diode and a unique integrated detector. The photons are collected in the detector by a photodiode and then amplified by a high gain linear amplifier that drives a Schottky clamped open collector output transistor. The circuit is temperature, current and voltage compensated.

This unique isolator design provides maximum DC and AC circuit isolation between input and output while achieving LSTTL/TTL circuit compatibility. The isolator operational parameters are guaranteed from 0°C to 70°C, such that a minimum input current of 5mA will sink an eight gate fan-out (13mA) at the output with 5 volt V_{CC} applied to the detector. This isolation and coupling is achieved with a typical propagation delay of 45ns. The enable input provides gating of the detector with input sinking and sourcing requirements compatible with LSTTL/TTL interfacing and a propagation delay of 25ns typical.

The 6N137 can be used in high speed digital interfacing applications where common mode signals must be rejected, such as for a line receiver and digital programming of floating power supplies, motors, and other machine control systems. The elimination of ground loops can be accomplished in system interfaces such as between a computer and a peripheral memory, printer, controller, etc.

The open collector output provides capability for bussing, OR'ing and strobing.

OUTLINE DRAWING*



DIMENSIONS IN MILLIMETRES AND (INCHES).

Recommended Operating Conditions

	Sym.	Min.	Max.	Units
Input Current, Low Level Each Channel	I_{FL}	0	250	μA
Input Current, High Level Each Channel	I_{FH}	6.3**	15	mA
High Level Enable Voltage	V_{EH}	2.0	Vcc	V
Low Level Enable Voltage (Output High)	V_{EL}	0	0.8	V
Supply Voltage, Output	V_{CC}	4.5	5.5	V
Fan Out (TTL Load)	N		8	
Operating Temperature	T_A	0	70	°C

Absolute Maximum Ratings*

(No derating required up to 70°C)

Storage Temperature ..... −55°C to +125°C
Operating Temperature ..... 0°C to +70°C
Lead Solder Temperature ..... 260°C for 10s
(1.6mm below seating plane)
Peak Forward Input Current ..... 40mA (t ≤ 1msec Duration)
Average Forward Input Current 20mA
Reverse Input Voltage 5V
Enable Input Voltage 5.5V
(Not to exceed V_{CC} by more than 500mV)
Supply Voltage - V_{CC} ..... 7V (1 Minute Maximum)
Output Current - I_O 50mA
Output Collector Power Dissipation 85mW
Output Voltage - V_O 7V

**6.3mA condition permits at least 20% CTR degradation guardband. Initial switching threshold is 5mA or less.

*JEDEC Registered Data.

Electrical Characteristics

OVER RECOMMENDED TEMPERATURE (T_A = 0°C TO 70°C) UNLESS OTHERWISE NOTED

Parameter	Symbol	Min.	Typ.**	Max.	Units	Test Conditions	Figure	Note
High Level Output Current	I_{OH}*		2	250	μA	V_{CC}=5.5V, V_O=5.5V, I_F=250μA, V_E=2.0V	6	
Low Level Output Voltage	V_{OL}*		0.4	0.6	V	V_{CC}=5.5V, I_F=5mA, V_{EH}=2.0V I_{OL} (Sinking) =13mA	3,5	
High Level Enable Current	I_{EH}		-0.8		mA	V_{CC}=5.5V, V_E=2.0V		
Low Level Enable Current	I_{EL}*		-1.2	-2.0	mA	V_{CC}=5.5V, V_E=0.5V		
High Level Supply Current	I_{CCH}*		7	15	mA	V_{CC}=5.5V, I_F=0 V_E=0.5V		
Low Level Supply	I_{CCL}*		13	18	mA	V_{CC}=5.5V, I_F=10mA V_E=0.5V		
Input-Output Insulation Leakage Current	I_{I-O}*			1.0	μA	Relative Humidity=45% T_A=25°C, t=5s V_{I-O}=3000Vdc		5, 9
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	V_{I-O}=500V, T_A=25°C		5
Capacitance (Input-Output)	C_{I-O}		0.6		pF	f=1MHz, T_A=25°C		5
Input Forward Voltage	V_F*		1.5	1.75	V	I_F=10mA, T_A=25°C	4	8
Input Reverse Breakdown Voltage	BV_R*	5			V	I_R=10μA, T_A=25°C		
Input Capacitance	C_{IN}		60		pF	V_F=0, f=1MHz		
Current Transfer Ratio	CTR		700		%	I_F=5.0mA, R_L=100Ω	2	7

**All typical values are at V_{CC} = 5V, T_A = 25°C

Switching Characteristics at T_A=25°C, V_{CC}=5V

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to High Output Level	t_{PLH}*		45	75	ns	R_L=350Ω, C_L=15pF, I_F=7.5mA	7,9	1
Propagation Delay Time to Low Output Level	t_{PHL}*		45	75	ns	R_L=350Ω, C_L=15pF, I_F=7.5mA	7,9	2
Output Rise-Fall Time (10-90%)	t_r, t_f		20, 30		ns	R_L=350Ω, C_L=15pF, I_F=7.5mA		
Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{ELH}		40		ns	R_L=350Ω, C_L=15pF, I_F=7.5mA, V_{EH}=3.0V, V_{EL}=0.5V	8	3
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{EHL}		25		ns	R_L=350Ω, C_L=15pF, I_F=7.5mA V_{EH}=3.0V, V_{EL}=0.5V	8	4
Common Mode Transient Immunity at Logic High Output Level	CM_H		50		v/μs	V_{CM}=10V R_L=350Ω, V_O(min.)=2V, I_F=0mA	11	6
Common Mode Transient Immunity at Logic Low Output Level	CM_L		-150		v/μs	V_{CM}=10V R_L=350Ω, V_O(max.)=0.8V, I_F=5mA	11	6

*JEDEC Registered Data.

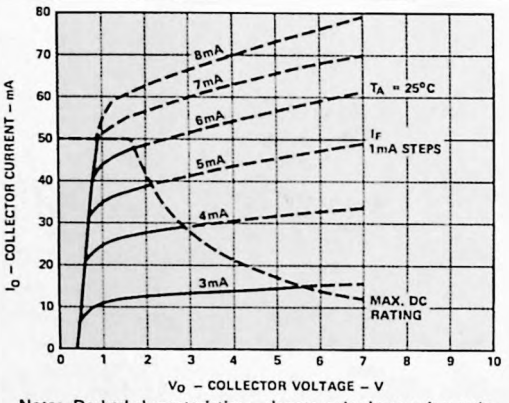
Operating Procedures and Definitions

Logic Convention. The 6N137 is defined in terms of positive logic.

Bypassing. A ceramic capacitor (.01 to 0.1μF) should be connected from pin 8 to pin 5 (Figure 12). Its purpose is to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching properties. The total lead length between capacitor and coupler should not exceed 20mm.

Polarities. All voltages are referenced to network ground (pin 5). Current flowing toward a terminal is considered positive.

Enable Input. No external pull-up required for a logic (1), i.e., can be open circuit.



Note: Dashed characteristics — denote pulsed operation only.

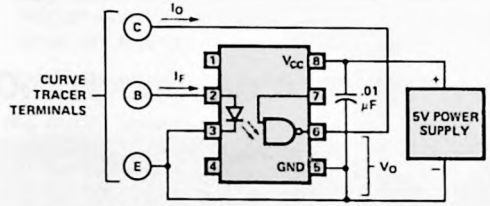
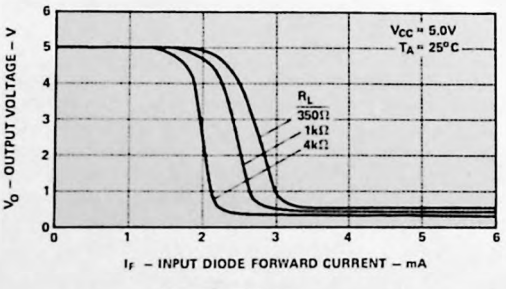


Figure 2. Optocoupler Collector Characteristics.



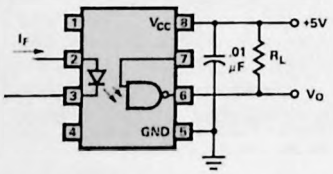


Figure 3. Input-Output Characteristics.

NOTES:

1. The t_{PLH} propagation delay is measured from the 3.75mA point on the trailing edge of the input pulse to the 1.5V point on the trailing edge of the output pulse.
2. The t_{PHL} propagation delay is measured from the 3.75mA point on the leading edge of the input pulse to 1.5V point on the leading edge of the output pulse.
3. The t_{ELH} enable propagation delay is measured from the 1.5V point of the trailing edge of the input pulse to the 1.5V point on the trailing edge of the output pulse.
4. The t_{EHL} enable propagation delay is measured from the 1.5V point on the leading edge of the input pulse to the 1.5V point on the leading edge of the output pulse.
5. Device considered a two terminal device: pins 2 and 3 shorted together, and pins 5, 6, 7, and 8 shorted together.
6. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O>2.0V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O<0.8V).
7. DC Current Transfer Ratio is defined as the ratio of the output collector current to the forward bias input current times 100%.
8. At 10mA V_F decreases with increasing temperature at the rate of 1.6mV/°C.
9. This is a proof test to validate the UL 220 Vac rating.

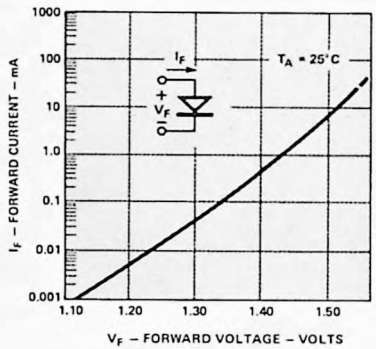


Figure 4. Input Diode Forward Characteristic.

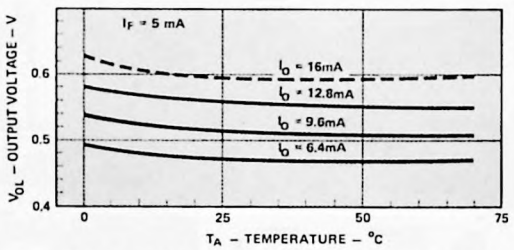


Figure 5. Output Voltage, V_{OL} vs. Temperature and Fan-Out.

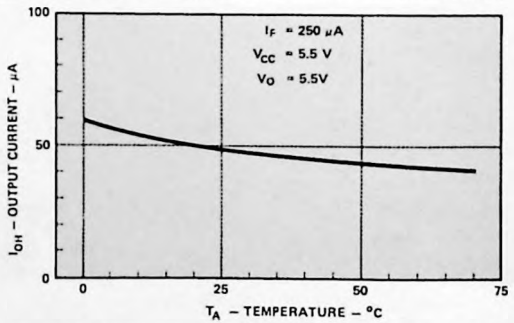


Figure 6. Output Current, I_{OH} vs. Temperature (I_F=250μA).

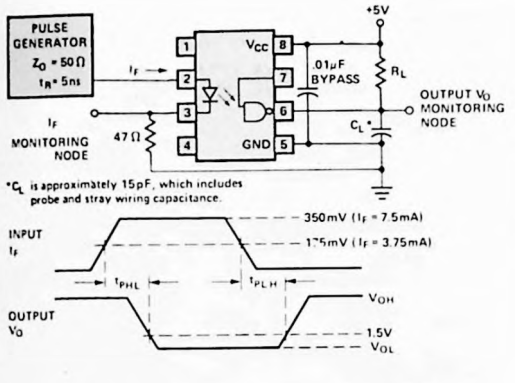


Figure 7. Test Circuit for t_{PHL} and t_{PLH}.**

**JEDEC Registered Data.

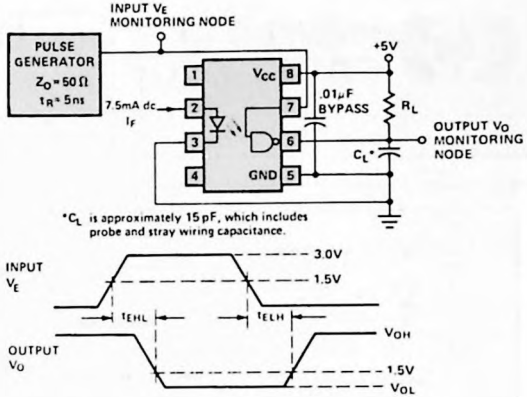


Figure 8. Test Circuit for t_{ELH} and t_{EHL}.

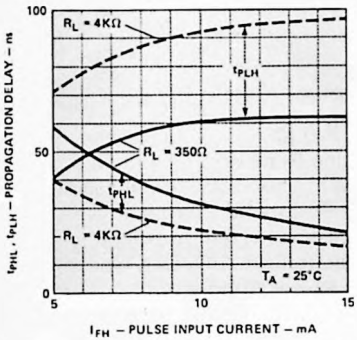


Figure 9. Propagation Delay, t_{PHL} and t_{PLH} vs. Pulse Input Current, I_{FH}.

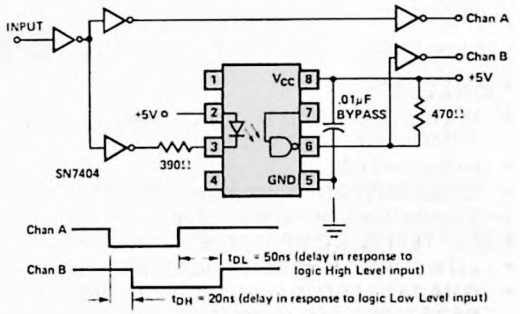


Figure 10. Response Delay Between TTL Gates.

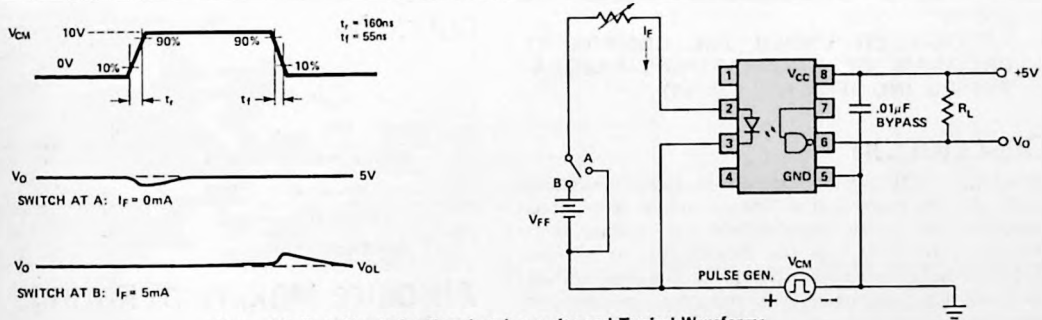


Figure 11. Test Circuit for Transient Immunity and Typical Waveforms.

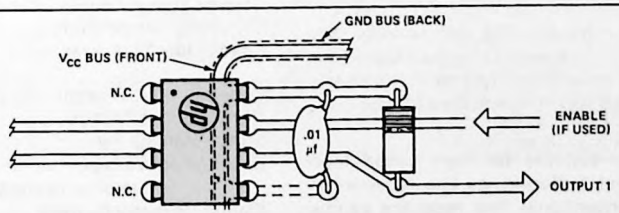


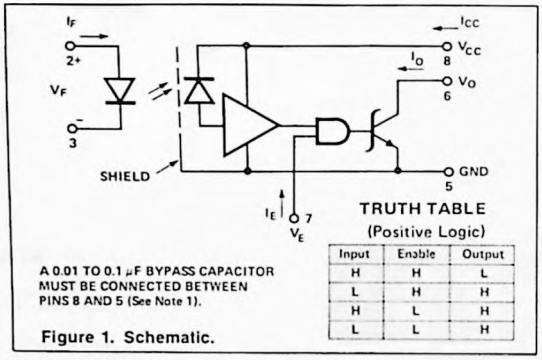
Figure 12. Recommended Printed Circuit Board Layout.

HEWLETT PACKARD

HIGH CMR, HIGH SPEED OPTOCOUPLER

HCPL - 2601

TECHNICAL DATA JANUARY 1984

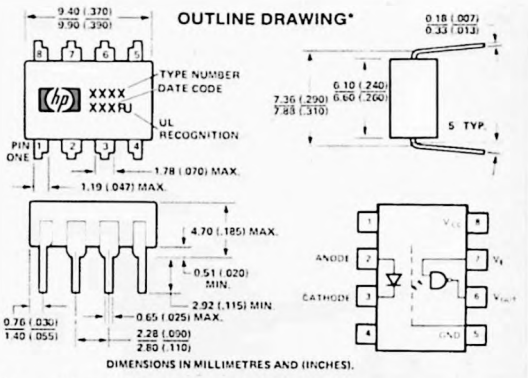


A 0.01 TO 0.1 μF BYPASS CAPACITOR MUST BE CONNECTED BETWEEN PINS 8 AND 5 (See Note 1).

TRUTH TABLE
(Positive Logic)

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H

Figure 1. Schematic.



DIMENSIONS IN MILLIMETRES AND (INCHES).

Features

- **INTERNAL SHIELD FOR HIGH COMMON MODE REJECTION (CMR)**
- **HIGH SPEED**
- **GUARANTEED MINIMUM COMMON MODE TRANSIENT IMMUNITY: 1000V/μs**
- **LSTTL/TTL COMPATIBLE**
- **LOW INPUT CURRENT REQUIRED: 5mA**
- **GUARANTEED PERFORMANCE OVER TEMPERATURE: 0°C to 70°C**
- **STROBABLE OUTPUT**
- **DIELECTRIC WITHSTAND TESTED AT 3000 Vdc FOR A WORKING VOLTAGE OF 220 Vac**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES, INC. (FILE NO. E55361)**

Description

The HCPL-2601 optically coupled gate combines a GaAsP light emitting diode and an integrated high gain photon detector. An enable input allows the detector to be strobed. The output of the detector I.C. is an open collector Schottky clamped transistor. The internal shield provides a guaranteed common mode transient immunity specification of 1000 volts/μsec.

This unique design provides maximum D.C. and A.C. circuit isolation while achieving TTL compatibility. The isolator D.C. operational parameters are guaranteed from 0°C to 70°C allowing troublefree system performance. This isolation is achieved with a typical propagation delay of 40 nsec.

The HCPL-2601's are suitable for high speed logic interfacing, input/output buffering, as line receivers in environments that conventional line receivers cannot tolerate and are recommended for use in extremely high ground or induced noise environments.

Applications

- Isolated Line Receiver
- Simplex/Multiplex Data Transmission
- Computer-Peripheral Interface
- Microprocessor System Interface
- Digital Isolation for A/D, D/A Conversion
- Switching Power Supply
- Instrument Input/Output Isolation
- Ground Loop Elimination
- Pulse Transformer Replacement

Recommended Operating Conditions

	Sym.	Min.	Max.	Units
Input Current, Low Level	I_{FL}	0	250	μA
Input Current, High Level	I_{FH}	6.3*	15	mA
Supply Voltage, Output	V_{CC}	4.5	5.5	V
High Level Enable Voltage	V_{EH}	2.0	Vcc	V
Low Level Enable Voltage	V_{EL}	0	0.8	V
Fan Out (TTL Load)	N		8	
Operating Temperature	T_A	0	70	°C

Absolute Maximum Ratings

(No Derating Required up to 70°C)

Storage Temperature ..... −55°C to +125°C
Operating Temperature ..... 0°C to +70°C
Lead Solder Temperature ..... 260°C for 10 s
(1.6mm below seating plane)
Forward Input Current − I_F (see Note 2) ..... 20 mA
Reverse Input Voltage ..... 5 V
Supply Voltage − V_{CC} ..... 7V (1 Minute Maximum)
Enable Input Voltage − V_E ..... 5.5 V
(Not to exceed V_{CC} by more than 500 mV)
Output Collector Current − I_O ..... 25 mA
Output Collector Power Dissipation ..... 40 mW
Output Collector Voltage − V_O ..... 7 V

*6.3 mA condition permits at least 20% CTR degradation guardband. Initial switching threshold is 5mA or less.

Electrical Characteristics

(Over Recommended Temperature, T_A = 0°C to +70°C, Unless Otherwise Noted)

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Figure	Note
High Level Output Current	I_{OH}		20	250	μA	V_{CC} = 5.5V, V_O = 5.5V, I_F = 250 μA, V_E = 2.0 V	2	
Low Level Output Voltage	V_{OL}		0.4	0.6	V	V_{CC} = 5.5V, I_F = 5 mA V_E = 2.0 V, I_{OL} (Sinking) = 13 mA	3,5	
High Level Supply Current	I_{CCH}		10	15	mA	V_{CC} = 5.5V, I_F = 0, V_E = 0.5 V		
Low Level Supply Current	I_{CCL}		15	19	mA	V_{CC} = 5.5V, I_F = 10 mA, V_E = 0.5 V		
Low Level Enable Current	I_{EL}		−1.4	−2.0	mA	V_{CC} = 5.5 V, V_E = 0.5 V		
High Level Enable Current	I_{EH}		−1.0		mA	V_{CC} = 5.5 V, V_E = 2.0V		
High Level Enable Voltage	V_{EH}	2.0			V			11
Low Level Enable Voltage	V_{EL}			0.8	V			
Input Forward Voitage	V_F		1.5	1.75	V	I_F = 10 mA, T_A = 25°C	4	
Input Reverse Breakdown Voltage	BV_R	5			V	I_R = 10 μA, T_A = 25°C		
Input Capacitance	C_{IN}		60		pF	V_F = 0, f = 1 MHz		
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		−1.6		mV/°C	I_F = 10 mA		
Input-Output Insulation Leakage Current	I_{I-O}			1	μA	Relative Humidity = 45% T_A = 25°C, t = 5 s, V_{I-O} = 3000 Vdc		3, 12
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 V		3
Capacitance (Input-Output)	C_{I-O}		0.6		pF	f = 1 MHz		3

*All typical values are at V_{CC} = 5V, T_A = 25°C

Switching Characteristics (T_A = 25°C, V_{CC} = 5V)

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to High Output level	t_{PLH}		40	75	ns	R_L = 350 Ω, C_L = 15 pF, I_F = 7.5 mA	6	4
Propagation Delay Time to Low Output Level	t_{PHL}		40	75	ns		6	5
Output Rise Time (10–90%)	t_r		20		ns			
Output Fall Time (90–10%)	t_f		30		ns			
Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{ELH}		25		ns	R_L = 350 Ω, C_L = 15 pF, I_F = 7.5 mA, V_{EH} = 3 V, V_{EL} = 0 V	9	6
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{EHL}		25		ns	R_L = 350 Ω, C_L = 15 pF, I_F = 7.5 mA, V_{EH} = 3 V, V_{EL} = 0 V	9	7
Common Mode Transient Immunity at High Output Level	CM_H	1000	10,000		V/μs	V_{CM} = 50 V (peak), V_O (min.) = 2 V, R_L = 350 Ω, I_F = 0 mA	12	8,10
Common Mode Transient Immunity at Low Output Level	CM_L	−1000	−10,000		V/μs	V_{CM} = 50 V (peak), V_O (max.) = 0.8 V, R_L = 350 Ω, I_F = 7.5 mA	12	9,10

NOTES:

1. Bypassing of the power supply line is required, with a 0.01 μF ceramic disc capacitor adjacent to each isolator as illustrated in Figure 15. The power supply bus for the isolator(s) should be separate from the bus for any active loads, otherwise a larger value of bypass capacitor (up to 0.1 μF) may be needed to suppress regenerative feedback via the power supply.
2. Peaking circuits may produce transient input currents up to 50 mA, 50 ns maximum pulse width, provided average current does not exceed 20 mA.
3. Device considered a two terminal device: pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.
4. The t_{PLH} propagation delay is measured from the 3.75 mA point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
5. The t_{PHL} propagation delay is measured from the 3.75 mA point on the leading edge of the input pulse to the 1.5V point on the leading edge of the output pulse.
6. The t_{PLH} enable propagation delay is measured from the 1.5 V point on the trailing edge of the enable input pulse to the 1.5 V point on the trailing edge of the output pulse.
7. The t_{PHL} enable propagation delay is measured from the 1.5 V point on the leading edge of the enable input pulse to the 1.5 V point on the leading edge of the output pulse.
8. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (i.e., V_{OUT} >2.0 V).
9. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., V_{OUT} <0.8 V).
10. For sinusoidal voltages, $\left(\frac{|dv_{CM}|}{dt}\right)_{max} = \pi f_{CM} V_{CM}$ (p-p)
11. No external pull up is required for a high logic state on the enable input.
12. This is a proof test to validate the UL 220 Vac rating.

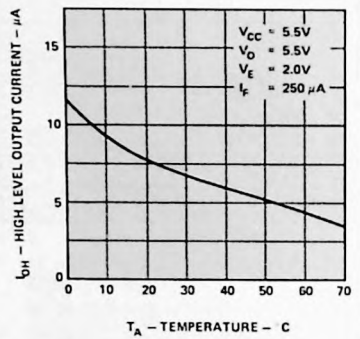


Figure 2. High Level Output Current vs. Temperature.

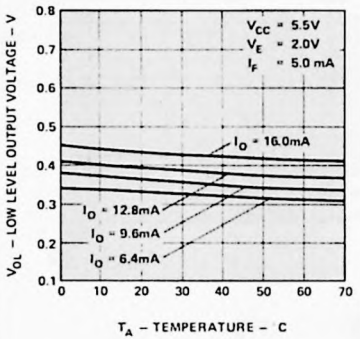


Figure 3. Low Level Output Voltage vs. Temperature.

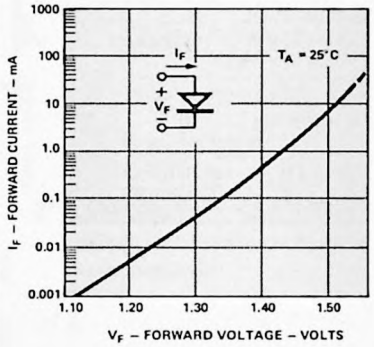


Figure 4. Input Diode Forward Characteristic.

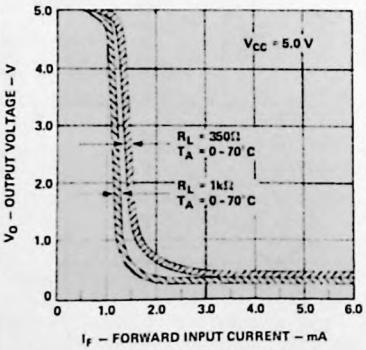


Figure 5. Output Voltage vs. Forward Input Current.

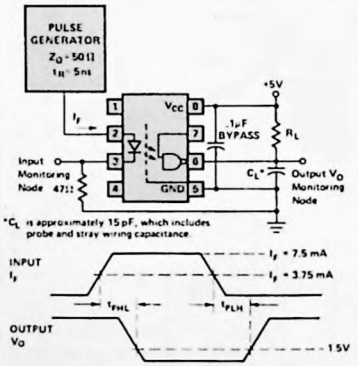


Figure 6. Test Circuit for t_{PHL} and t_{PLH}.

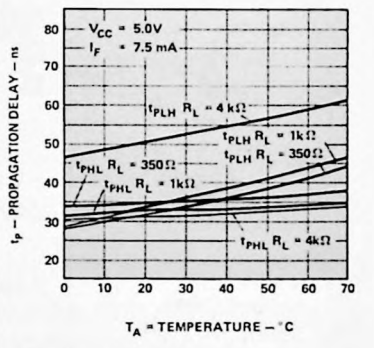


Figure 7. Propagation Delay vs. Temperature.

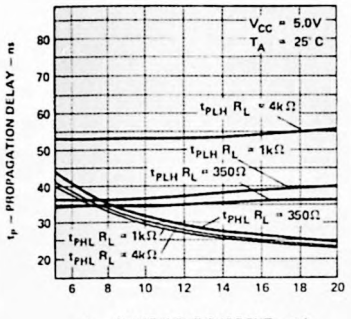


Figure 8. Propagation Delay vs. Pulse Input Current.

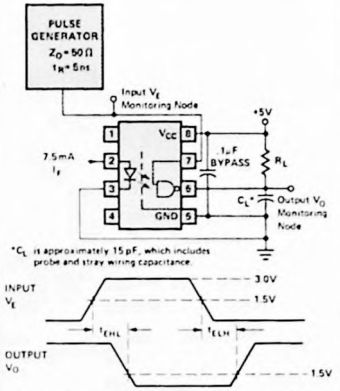


Figure 9. Test Circuit for t_{EHL} and t_{ELH}.

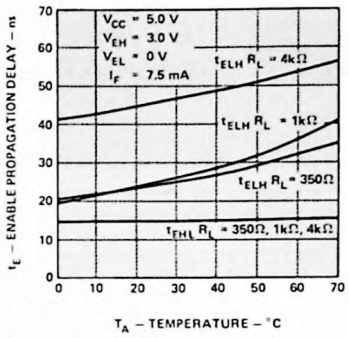


Figure 10. Enable Propagation Delay vs. Temperature.

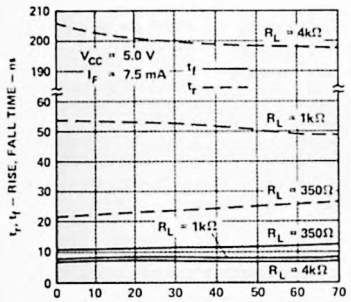


Figure 11. Rise, Fall Time vs. Temperature.

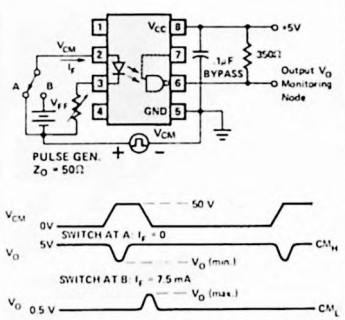


Figure 12. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

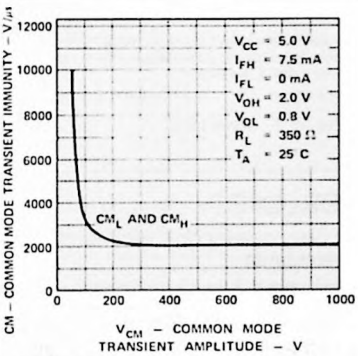


Figure 13. Common Mode Transient Immunity vs. Common Mode Transient Amplitude.

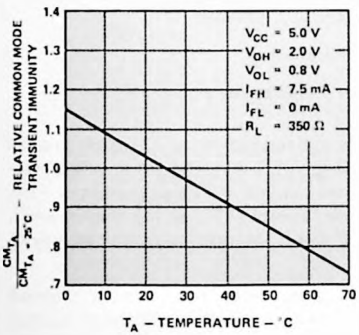


Figure 14. Relative Common Mode Transient Immunity vs. Temperature.

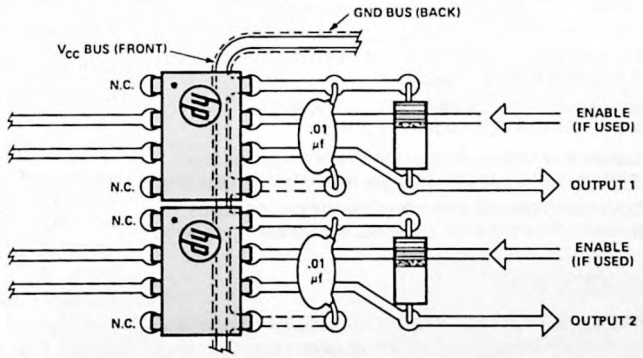


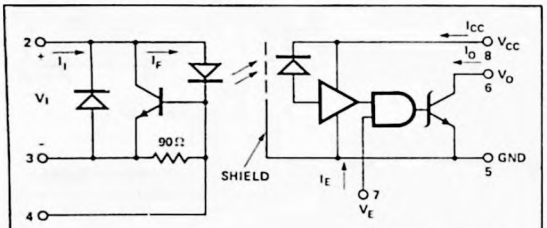
Figure 15. Recommended Printed Circuit Board Layout.

HEWLETT PACKARD

HIGH CMR LINE RECEIVER OPTOCOUPLER

HCPL-2602

TECHNICAL DATA JANUARY 1984

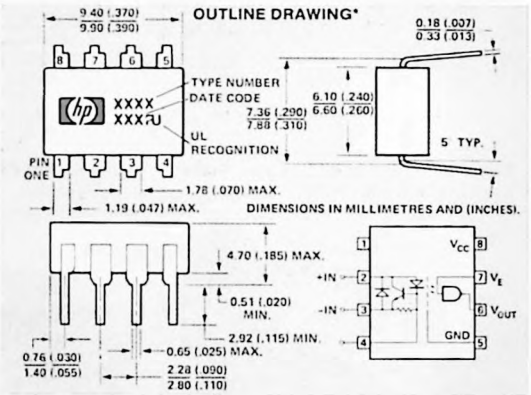


A 0.01 TO 0.1 μF BYPASS CAPACITOR MUST BE CONNECTED BETWEEN PINS 8 AND 5 (See Note 1).

Figure 1. Schematic.

TRUTH TABLE
(Positive Logic)

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H



Features

- LINE TERMINATION INCLUDED — NO EXTRA CIRCUITRY REQUIRED
- ACCEPTS A BROAD RANGE OF DRIVE CONDITIONS
- GUARDBANDED FOR LED DEGRADATION
- LED PROTECTION MINIMIZES LED EFFICIENCY DEGRADATION
- HIGH SPEED — 10Mbs (LIMITED BY TRANSMISSION LINE IN MANY APPLICATIONS)
- INTERNAL SHIELD PROVIDES EXCELLENT COMMON MODE REJECTION
- EXTERNAL BASE LEAD ALLOWS "LED PEAKING" AND LED CURRENT ADJUSTMENT
- DIELECTRIC WITHSTAND TESTED AT 3000 Vdc FOR A WORKING VOLTAGE OF 220 Vac
- RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES, INC. (FILE NO. E55361)
- RECOGNIZED UNDER THE COMPONENT PROGRAM OF VDE, SPECIFICATION 69A (FILE NO. 6591-S-4880-1001/A13I)

Description

The HCPL-2602 optically coupled line receiver combines a GaAsP light emitting diode, an input current regulator and an integrated high gain photon detector. The input regulator serves as a line termination for line receiver applications. It clamps the line voltage and regulates the LED current so line reflections do not interfere with circuit performance.

The regulator allows a typical LED current of 8.5 mA before it starts to shunt excess current. The output of the detector IC is an open collector Schottky clamped transistor. An enable input gates the detector. The internal detector shield provides a guaranteed common mode transient immunity specification of 1000 V/μsec.

Applications

- Isolated Line Receiver
- Simplex/Multiplex Data Transmission
- Computer-Peripheral Interface
- Microprocessor System Interface
- Digital Isolation for A/D, D/A Conversion
- Current Sensing
- Instrument Input/Output Isolation
- Ground Loop Elimination
- Pulse Transformer Replacement

DC specifications are defined similar to TTL logic and are guaranteed from 0°C to 70°C allowing trouble free interfacing with digital logic circuits. An input current of 5 mA will sink an eight gate fan-out (TTL) at the output with a typical propagation delay from input to output of only 45 nsec.

The HCPL-2602's are useful as line receivers in high noise environments that conventional line receivers cannot tolerate. The higher LED threshold voltage provides improved immunity to differential noise and the internally shielded detector provides orders of magnitude improvement in common mode rejection with little or no sacrifice in speed.

CAUTION: The small junction sizes inherent to the design of this bipolar component increase the component's susceptibility to damange from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Recommended Operating Conditions

	Sym.	Min.	Max.	Units
Input Current, Low Level	I_{IL}	0	250	μA
Input Current, High Level	I_{IH}	5	60	mA
Supply Voltage, Output	V_{CC}	4.5	5.5	V
High Level Enable Voltage	V_{EH}	2.0	Vcc	V
Low Level Enable Voltage	V_{EL}	0	0.8	V
Fan Out (TTL Load)	N		8	
Operating Temperature	T_A	0	70	°C

Absolute Maximum Ratings

Storage Temperature ..... −55°C to +125°C
Operating Temperature ..... 0°C to +70°C
Lead Solder Temperature ..... 260°C for 10 s
(1.6mm below seating plane)
Forward Input Current — I_I ..... 60 mA
Reverse Input Current ..... 60 mA
Supply Voltage — V_{CC} ..... 7V (1 Minute Maximum)
Enable Input Voltage — V_E ..... 5.5 V
(Not to exceed V_{CC} by more than 500 mV)
Output Collector Current — I_O ..... 25 mA
Output Collector Power Dissipation ..... 40 mW
Output Collector Voltage — V_O ..... 7 V
Input Current, Pin 4 ..... ±10 mA

NOTES:

1. Bypassing of the power supply line is required, with a 0.01 μF ceramic disc capacitor adjacent to each isolator as illustrated in Figure 15. The power supply bus for the isolator(s) should be separate from the bus for any active loads, otherwise a larger value of bypass capacitor (up to 0.1 μF) may be needed to suppress regenerative feedback via the power supply.
2. The HCPL-2602 is tested such that operation at I_I minimum of 5 mA will provide the user a minimum of 20% guardband for LED light output degradation.
3. Device considered a two terminal device: pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.
4. The t_{PLH} propagation delay is measured from the 3.75 mA point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
5. The t_{PHL} propagation delay is measured from the 3.75 mA point on the leading edge of the input pulse to the 1.5V point on the leading edge of the output pulse.
6. The t_{ELH} enable propagation delay is measured from the 1.5 V point on the trailing edge of the enable input pulse to the 1.5 V point on the trailing edge of the output pulse.
7. The t_{EHL} enable propagation delay is measured from the 1.5 V point on the leading edge of the enable input pulse to the 1.5 V point on the leading edge of the output pulse.
8. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (i.e., V_{OUT} > 2.0 V).
9. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., V_{OUT} < 0.8 V).
10. For sinusoidal voltages, $\left(\frac{|dv_{cm}|}{dt}\right)_{max} = \pi f_{cm} V_{cm}$ (p-p)
11. No external pull up is required for a high logic state on the enable input.
12. This is a proof test to validate the UL 220 Vac rating.

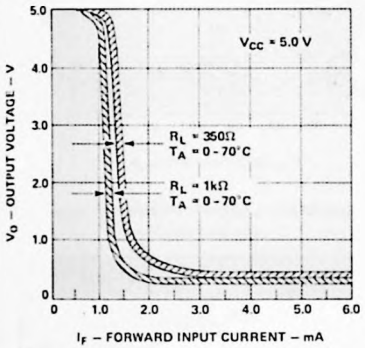


Figure 2. Output Voltage vs. Forward Input Current.

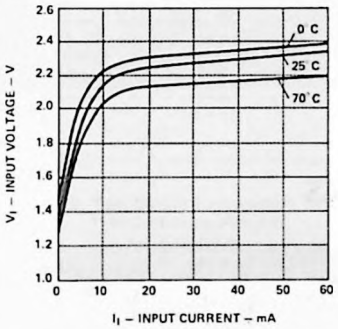


Figure 3. Input Characteristics.

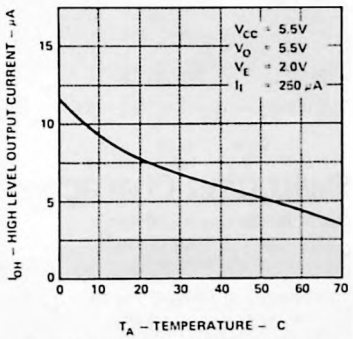


Figure 4. High Level Output Current vs. Temperature.

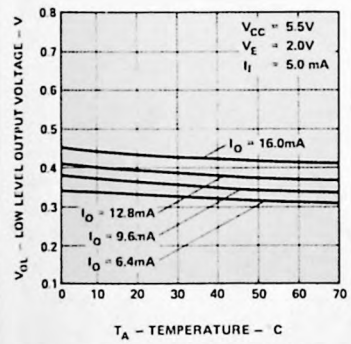


Figure 5. Low Level Output Voltage vs. Temperature.

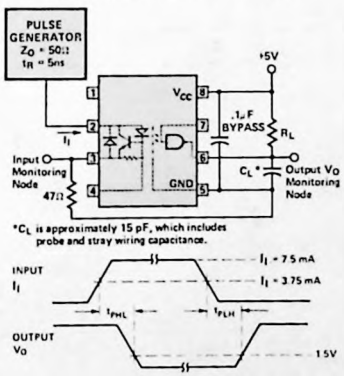


Figure 6. Test Circuit for t_{PHL} and t_{PLH}.

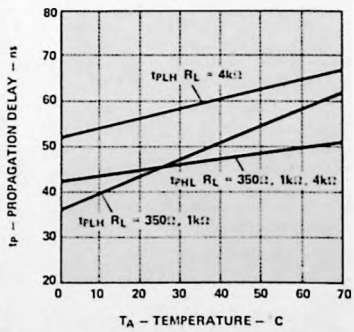


Figure 7. Propagation Delay vs. Temperature.

Electrical Characteristics

(Over Recommended Temperature, T_A = 0° C to +70° C, Unless Otherwise Noted)

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Figure	Note
High Level Output Current	I_{OH}		20	250	μA	V_{CC} = 5.5V, V_O = 5.5V I_I=250 μA, V_E=2.0V	4	
Low Level Output Voltage	V_{OL}		0.4	0.6	V	V_{CC}=5.5V, I_I=5 mA V_E=2.0V, I_{OL} (Sinking)=13 mA	2,5	2
Input Voltage	V_I		2.0	2.4	V	I_I=5 mA	3	
			2.3	2.7		I_I=60 mA	3	
Input Reverse Voltage	V_R		0.75	0.95	V	I_R=5 mA		
Low Level Enable Current	I_{EL}		-1.4	-2.0	mA	V_{CC}=5.5V, V_E=0.5V		
High Level Enable Current	I_{EH}		-1.0		mA	V_{CC}=5.5V, V_E=2.0V		
High Level Enable Voltage	V_{EH}	2.0			V			11
Low Level Enable Voltage	V_{EL}			0.8	V			
High Level Supply Current	I_{CCH}		10	15	mA	V_{CC}=5.5V, I_I=0, V_E=0.5V		
Low Level Supply Current	I_{CCL}		16	19	mA	V_{CC}=5.5V, I_I=60 mA V_E=0.5V		
Input Capacitance	C_{IN}		90		pF	V_I=0, f=1 MHz, (PIN 2-3)		
Input-Output Insulation Leakage Current	I_{I-O}			1	μA	Relative Humidity=45% T_A=25° C, t=5 s, V_{I-O}=3000 Vdc		3, 12
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	V_{I-O}=500V		3
Capacitance (Input-Output)	C_{I-O}		0.6		pF	f = 1 MHz		3

*All typical values are at V_{CC} = 5V, T_A = 25° C.

Switching Characteristics

(T_A = 25° C, V_{CC} = 5V)

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to High Output Level	t_{PLH}		45	75	ns	R_L = 350 Ω C_L = 15 pF I_I = 7.5 mA	6	4
Propagation Delay Time to Low Output Level	t_{PHL}		45	75	ns		6	5
Output Rise Time (10-90%)	t_r		25		ns			
Output Fall Time (90-10%)	t_f		25		ns			
Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{ELH}		25		ns	R_L=350Ω, C_L=15 pF, I_I=7.5 mA, V_{EH}=3 V, V_{EL}=0 V	10	6
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{EHL}		15		ns		10	7
Common Mode Transient Immunity at High Output Level	CM_H	1000	10,000		V/μs	V_{CM}=50 V (peak), V_O (min.)=2 V, R_L=350Ω, I_I=0 mA	12	8
Common Mode Transient Immunity at Low Output Level	CM_L	-1000	-10,000		V/μs	V_{CM}=50 V (peak), V_O (max.)=0.8 V, R_L=350Ω, I_I=7.5 mA	12	9

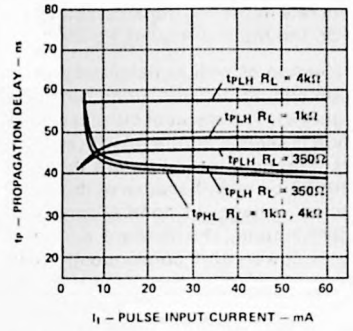


Figure 8. Propagation Delay vs. Pulse Input Current.

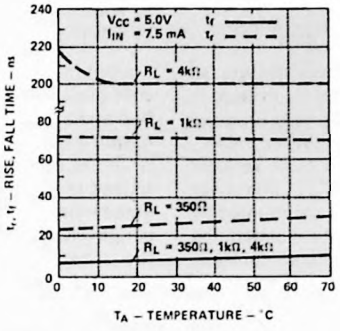


Figure 9. Rise, Fall Time vs. Temperature.

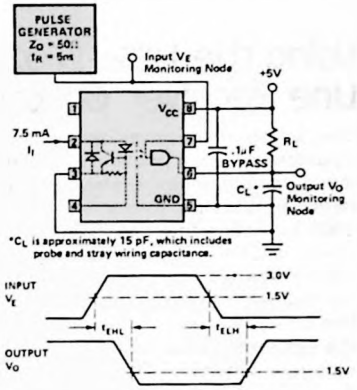


Figure 10. Test Circuit for t_{EHL} and t_{ELH}.

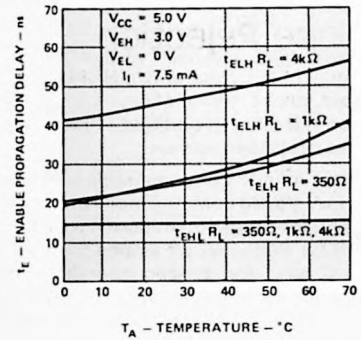


Figure 11. Enable Propagation Delay vs. Temperature.

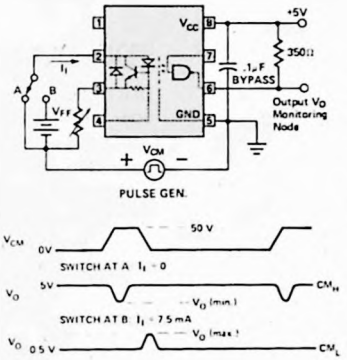


Figure 12. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

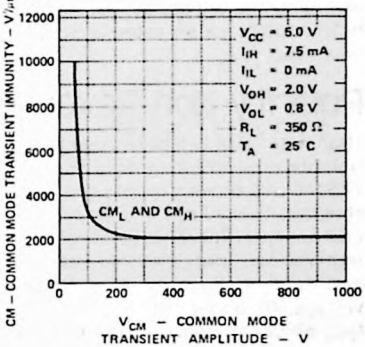


Figure 13. Common Mode Transient Immunity vs. Common Mode Transient Amplitude.

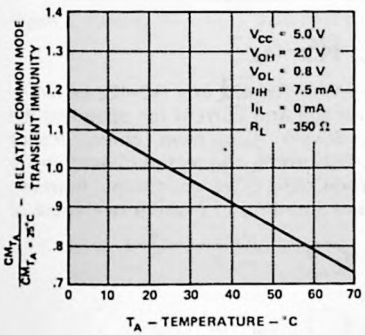


Figure 14. Relative Common Mode Transient Immunity vs. Temperature.

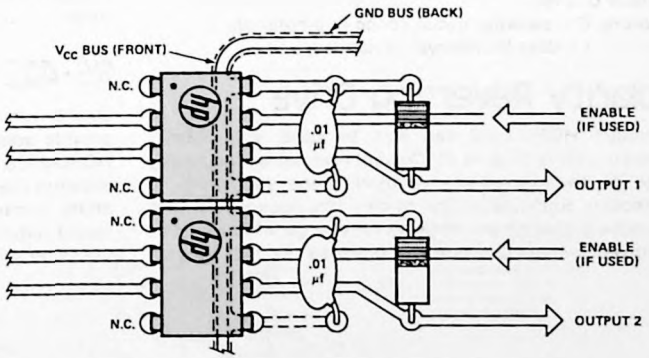


Figure 15. Recommended Printed Circuit Board Layout.

Using the HCPL-2602 Line Receiver Optocoupler

The primary objectives to fulfill when connecting an optocoupler to a transmission line are to provide a minimum, but not excessive, LED current and to properly terminate the line. The internal regulator in the HCPL-2602 simplifies this task. Excess current from variable drive conditions such as line length variations, line driver differences and power supply fluctuations are shunted by the regulator. In fact, with the LED current regulated, the line current can be increased to improve the immunity of the system to differential-mode-noise and to enhance the data rate capability. The designer must keep in mind the 60 mA input current maximum rating of the HCPL-2602, in such cases, and may need to use series limiting or shunting to prevent overstress.

Design of the termination circuit is also simplified; in most cases the transmission line can simply be connected directly to the input terminals of the HCPL-2602 without the need for additional series or shunt resistors. If reversing line drive is used it may be desirable to use two HCPL-2602's, or an external Schottky diode to optimize data rate.

Polarity Non-Reversing Drive

High data rates can be obtained with the HCPL-2602 with polarity non-reversing drive. Figure (a) illustrates how a 74S140 line driver can be used with the HCPL-2602 and shielded, twisted pair or coax cable without any additional components. There are some reflections due to the "active termination" but they do not interfere with circuit performance because the regulator clamps the line voltage. At longer line lengths t_{PLH} increases faster than t_{PHL} since the switching threshold is not exactly halfway between asymptotic line conditions. If optimum data rate is desired, a series resistor and peaking capacitor can be used to equalize t_{PLH} and t_{PHL}. In general, the peaking capacitance should be as large as possible; however, if it is too large it may keep the regulator from achieving turn-off during the negative (or zero) excursions of the input signal. A safe rule:

make $C \leq 16t$
where C = peaking capacitance in picofarads
t = data bit interval in nanoseconds

Polarity Reversing Drive

A single HCPL-2602 can also be used with polarity reversing drive (Figure b). Current reversal is obtained by way of the substrate isolation diode (substrate to collector). Some reduction of data rate occurs, however, because the substrate diode stores charge, which must be removed when the current changes to the forward direction. The effect of this is a longer t_{PHL}. This effect can be eliminated and data rate improved considerably by use of a Schottky diode on the input of the HCPL-2602.

For optimum noise rejection as well as balanced delays a split-phase termination should be used along with a flip-flop at the output (Figure c). The result of current reversal in split-phase operation is seen in Figure (c) with switches A and B both OPEN. The coupler inputs are then connected in ANTI-SERIES; however, because of the higher steady-state termination voltage, in comparison to the single HCPL-2602 termination, the forward current in the substrate diode is lower and consequently there is less junction charge to deal with when switching.

Closing switch B with A open is done mainly to enhance common mode rejection, but also reduces propagation delay slightly because line-to-line capacitance offers a slight peaking effect. With switches A and B both CLOSED, the shield acts as a current return path which prevents either input substrate diode from becoming reversed biased. Thus the data rate is optimized as shown in Figure (c).

Improved Noise Rejection

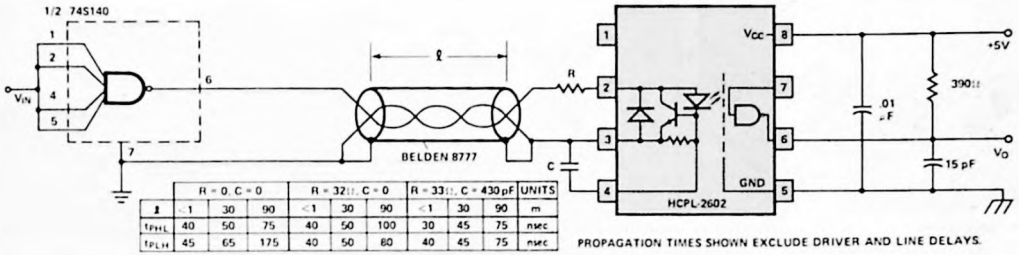
Use of additional logic at the output of two HCPL-2602's operated in the split phase termination, will greatly improve system noise rejection in addition to balancing propagation delays as discussed earlier.

A NAND flip-flop offers infinite common mode rejection (CMR) for NEGATIVELY sloped common mode transients but requires $t_{PHL} > t_{PLH}$ for proper operation. A NOR flip-flop has infinite CMR for POSITIVELY sloped transients but requires $t_{PHL} < t_{PLH}$ for proper operation. An exclusive-OR flip-flop has infinite CMR for common mode transients of EITHER polarity and operates with either $t_{PHL} > t_{PLH}$ or $t_{PHL} < t_{PLH}$.

With the line driver and transmission line shown in Figure (c), $t_{PHL} > t_{PLH}$, so NAND gates are preferred in the R-S flip-flop. A higher drive amplitude or different circuit configuration could make $t_{PHL} < t_{PLH}$, in which case NOR gates would be preferred. If it is not known whether $t_{PHL} > t_{PLH}$ or $t_{PHL} < t_{PLH}$, or if the drive conditions may vary over the boundary for these conditions, the exclusive-OR flip-flop of Figure (d) should be used.

RS-422 and RS-423

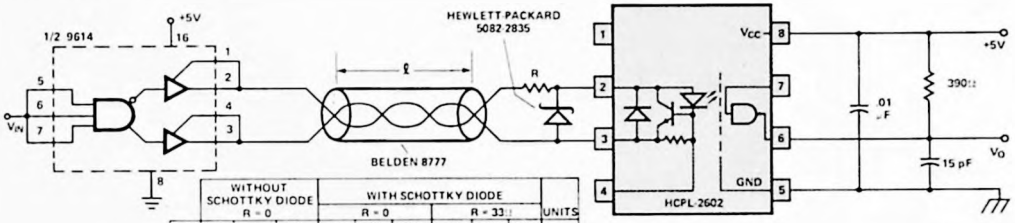
Line drivers designed for RS-422 and RS-423 generally provide adequate voltage and current for operating the HCPL-2602. Most drivers also have characteristics allowing the HCPL-2602 to be connected directly to the driver terminals. Worst case drive conditions, however, would require current shunting to prevent overstress of the HCPL-2602.



	R = 0, C = 0			R = 32Ω, C = 0			R = 33Ω, C = 430 pF			UNITS
ℓ	<1	30	90	<1	30	90	<1	30	90	m
t_{PHL}	40	50	75	40	50	100	30	45	75	nsec
t_{PLH}	45	65	175	40	50	80	40	45	75	nsec

PROPAGATION TIMES SHOWN EXCLUDE DRIVER AND LINE DELAYS.

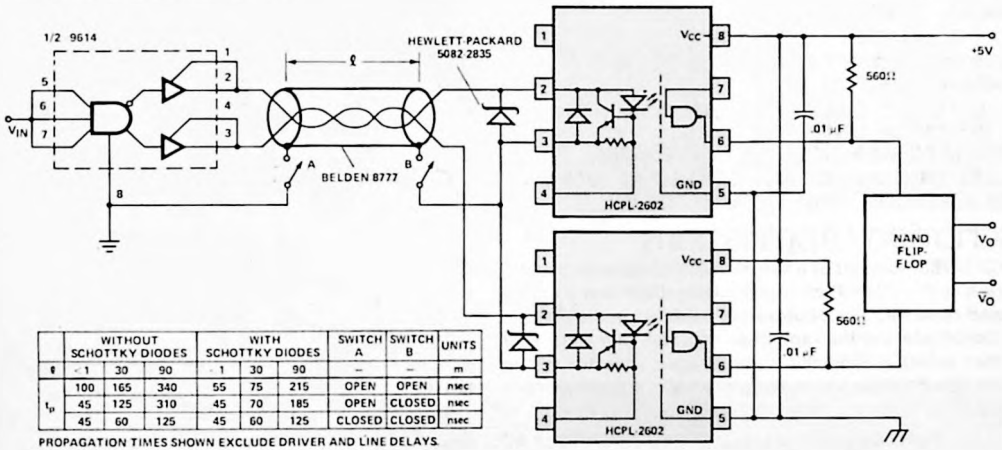
Figure a. Polarity Non-Reversing.



	WITHOUT SCHOTTKY DIODE R = 0			WITH SCHOTTKY DIODE R = 0			WITH SCHOTTKY DIODE R = 33Ω			UNITS
ℓ	<1	30	90	<1	30	90	<1	30	90	m
t_{PHL}	210	365	450	50	80	235	50	70	200	nsec
t_{PLH}	35	45	60	35	45	60	35	45	60	nsec

PROPAGATION TIMES SHOWN EXCLUDE DRIVER AND LINE DELAYS.

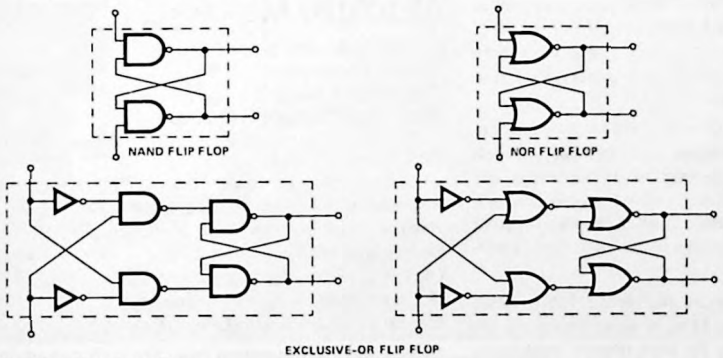
Figure b. Polarity Reversing, Single Ended.



	WITHOUT SCHOTTKY DIODES			WITH SCHOTTKY DIODES			SWITCH A	SWITCH B	UNITS
ℓ	<1	30	90	<1	30	90	–	–	m
t_p	100	165	340	55	75	215	OPEN	OPEN	nsec
	45	125	310	45	70	185	OPEN	CLOSED	nsec
	45	60	125	45	60	125	CLOSED	CLOSED	nsec

PROPAGATION TIMES SHOWN EXCLUDE DRIVER AND LINE DELAYS.

Figure c. Polarity Reversing, Split Phase.



NAND flip flop tolerates simultaneously HIGH inputs; NOR flip flop tolerates simultaneously LOW inputs; EXCLUSIVE-OR flip flop tolerates simultaneously HIGH OR LOW inputs without causing either of the outputs to change.

Figure d. Flip Flop Configurations.

HEWLETT PACKARD

DUAL TTL COMPATIBLE OPTOCOUPLER

HCPL-2630

TECHNICAL DATA JANUARY 1984

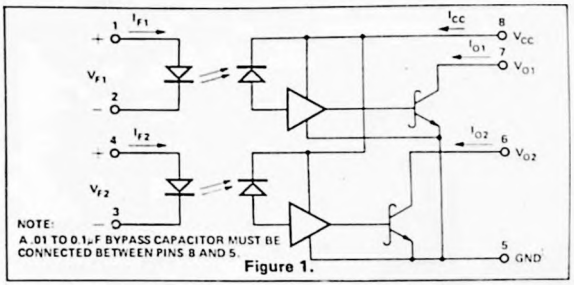
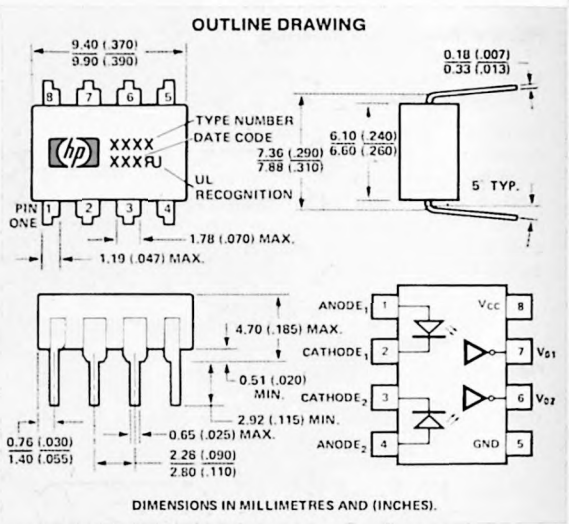


Figure 1.



Features

- HIGH DENSITY PACKAGING
- LSTTL/TTL COMPATIBLE: 5V SUPPLY
- ULTRA HIGH SPEED
- LOW INPUT CURRENT REQUIRED
- HIGH COMMON MODE REJECTION
- GUARANTEED PERFORMANCE OVER TEMPERATURE
- RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES, INC. (FILE NO. E55361)
- DIELECTRIC WITHSTAND TESTED AT 3000 Vdc FOR A WORKING VOLTAGE OF 220 Vac

Description/Applications

The HCPL-2630 consists of a pair of inverting optically coupled gates each with a GaAsP photon emitting diode and a unique integrated detector. The photons are collected in the detector by a photodiode and then amplified by a high gain linear amplifier that drives a Schottky clamped open collector output transistor. Each circuit is temperature, current and voltage compensated.

This unique dual coupler design provides maximum DC and AC circuit isolation between each input and output while achieving LSTTL/TTL circuit compability. The coupler operational parameters are guaranteed from 0°C to 70°C, such that a minimum input current of 5 mA in each channel will sink an eight gate fan-out (13 mA) at the output with 5 volt V_{CC} applied to the detector. This isolation and coupling is achieved with a typical propagation delay of 45 nsec.

The HCPL-2630 can be used in high speed digital interface applications where common mode signals must be rejected such as for a line receiver and digital programming of floating power supplies, motors, and other machine control systems. The elimination of ground loops can be accomplished between system interfaces such as between a computer and a peripheral memory, printer, controller, etc.

The open collector output provides capability for bussing, strobing and "WIRED-OR" connection. In all applications, the dual channel configuration allows for high density packaging, increased convenience and more usable board space.

Recommended Operating Conditions

	Sym.	Min.	Max.	Units
Input Current, Low Level Each Channel	I_{FL}	0	250	μA
Input Current, High Level Each Channel	I_{FH}	6.3*	15	mA
Supply Voltage, Output	V_{CC}	4.5	5.5	V
Fan Out (TTL Load) Each Channel	N		8	
Operating Temperature	T_A	0	70	°C

Absolute Maximum Ratings

(No derating required up to 70°C)

Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... 0°C to +70°C
Lead Solder Temperature ..... 260°C for 10s (1.6mm below seating plane)
Peak Forward Input Current (each channel) ..... 30 mA (≤ 1 msec Duration)
Average Forward Input Current (each channel) ..... 15 mA
Reverse Input Voltage (each channel) 5V
Supply Voltage - V_{CC} ..... 7V (1 Minute Maximum)
Output Current - I_O (each channel) ..... 16 mA
Output Voltage - V_O (each channel) 7V
Output Collector Power Dissipation ..... 60 mW

*6.3mA condition permits at least 20% CTR degradation guardband. Initial switching threshold is 5mA or less.

Electrical Characteristics

OVER RECOMMENDED TEMPERATURE (T_A = 0°C TO 70°C) UNLESS OTHERWISE NOTED

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Figure	Note
High Level Output Current	I_{OH}		2	250	μA	V_{CC} = 5.5V, V_O = 5.5V, I_F = 250μA		3
Low Level Output Voltage	V_{OL}		0.5	0.6	V	V_{CC} = 5.5V, I_F = 5mA I_{OL} (Sinking) = 13mA	3	3
High Level Supply Current	I_{CCH}		14	30	mA	V_{CC} = 5.5V, I_F = 0 (Both Channels)		
Low Level Supply	I_{CCL}		26	36	mA	V_{CC} = 5.5V, I_F = 10mA (Both Channels)		
Input - Output Insulation Leakage Current	I_{I-O}			1.0	μA	Relative Humidity = 45% T_A = 25°C, t = 5s, V_{I-O} = 3000Vdc		4,9
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	V_{I-O} = 500V, T_A = 25°C		4
Capacitance (Input-Output)	C_{I-O}		0.6		pF	f = 1MHz, T_A = 25°C		4
Input Forward Voltage	V_F		1.5	1.75	V	I_F = 10mA, T_A = 25°C	4	7,3
Input Reverse Breakdown Voltage	BV_R	5			V	I_R = 10μA, T_A = 25°C		
Input Capacitance	C_{IN}		60		pF	V_F = 0, f = 1MHz		3
Input-Input Insulation Leakage Current	I_{I-I}		0.005		μA	Relative Humidity = 45%, t=5s, V_{I-I}=500V		8
Resistance (Input-Input)	R_{I-I}		10^{11}		Ω	V_{I-I} = 500V		8
Capacitance (Input-Input)	C_{I-I}		0.25		pF	f = 1MHz		8
Current Transfer Ratio	CTR		700		%	I_F = 5.0mA, R_L = 100Ω	2	6

*All typical values are at V_{CC} = 5V, T_A = 25°C

Switching Characteristics at T_A=25°C, V_{CC}=5V

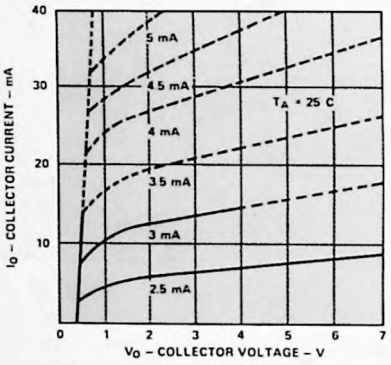
EACH CHANNEL

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to High Output Level	t_{PLH}		45	75	ns	R_L = 350 Ω, C_L = 15pF, I_F = 7.5mA	6,7	1
Propagation Delay Time to Low Output Level	t_{PHL}		45	75	ns	R_L = 350 Ω, C_L = 15pF, I_F = 7.5mA	6,7	2
Output Rise Time (10-90%)	t_r		20		ns	R_L = 350 Ω, C_L = 15pF, I_F = 7.5mA		
Output Fall Time (90-10%)	t_f		30		ns			
Common Mode Transient Immunity at High Output Level	CM_H		50		V/μs	V_{CM} = 10V_{p-p}, R_L = 350 Ω, V_O (min.) = 2V, I_F = 0mA	9	5
Common Mode Transient Immunity at Low Output Level	CM_L		-150		V/μs	V_{CM} = 10V_{p-p}, R_L = 350 Ω, V_O (max.) = 0.8V I_F = 7.5mA	9	5

NOTE: It is essential that a bypass capacitor (.01μF to 0.1μF, ceramic) be connected from pin 8 to pin 5. Total lead length between both ends of the capacitor and the isolator pins should not exceed 20mm. Failure to provide the bypass may impair the switching properties (Figure 5).

NOTES:

1. The t_{PLH} propagation delay is measured from the 3.75 mA point on the trailing edge of the input pulse to the 1.5V point on the trailing edge of the output pulse.
2. The t_{PHL} propagation delay is measured from the 3.75 mA point on the leading edge of the input pulse to the 1.5V point on the leading edge of the output pulse.
3. Each channel.
4. Measured between pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7, and 8 shorted together.
5. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., $V_O > 2.0V$). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., $V_O < 0.8V$).
6. DC Current Transfer Ratio is defined as the ratio of the output collector current to the forward bias input current times 100%.
7. At 10mA VF decreases with increasing temperature at the rate of 1.6mV/°C.
8. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.
9. This is a proof test to validate the UL 220 Vac rating.



NOTE: Dashed characteristics indicate pulsed operation.

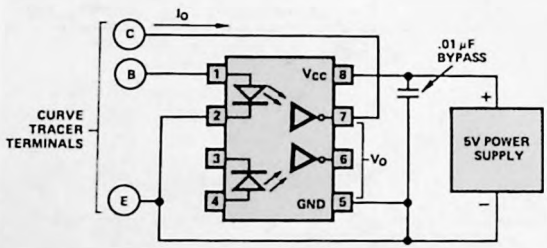
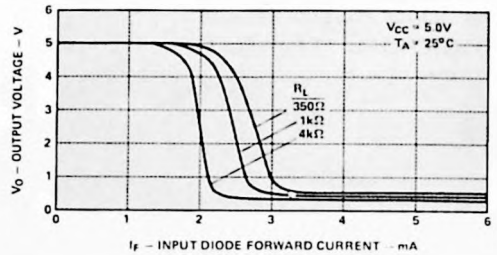


Figure 2. Optocoupler Transfer Characteristics.



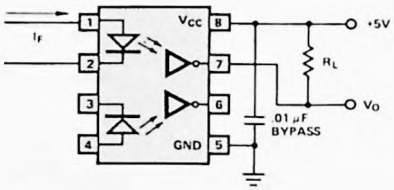


Figure 3. Input-Output Characteristics.

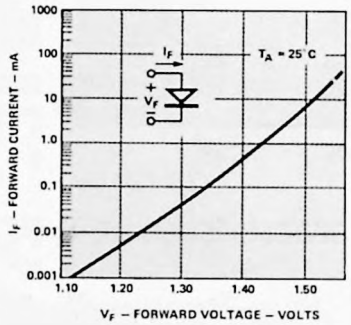


Figure 4. Input Diode Forward Characteristic

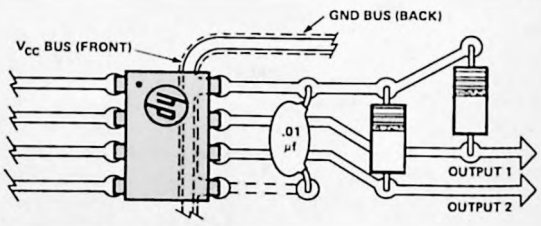


Figure 5. Recommended Printed Circuit Board Layout.

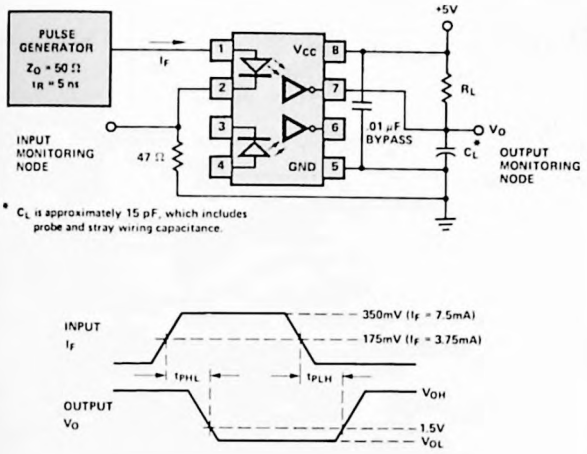


Figure 6. Test Circuit for t_{PHL} and t_{PLH}.

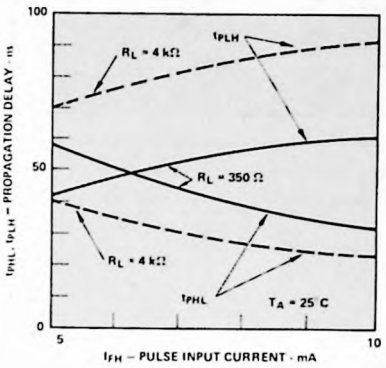


Figure 7. Propagation Delay, t_{PHL} and t_{PLH} vs. Pulse Input Current, I_{FH}.

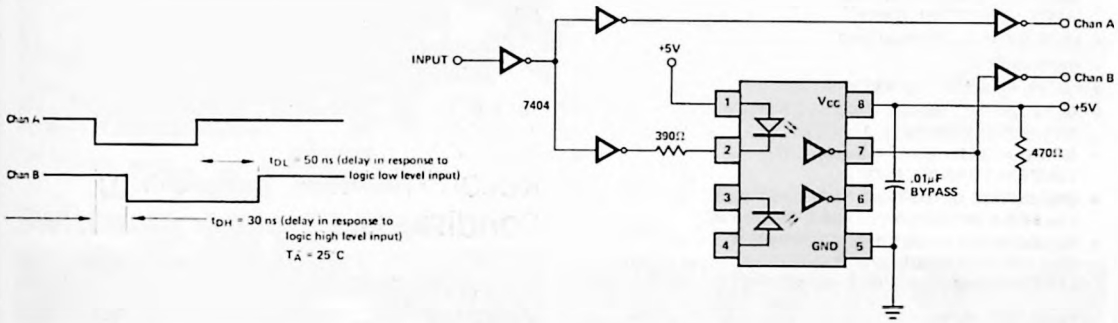


Figure 8. Response Delay Between TTL Gates.

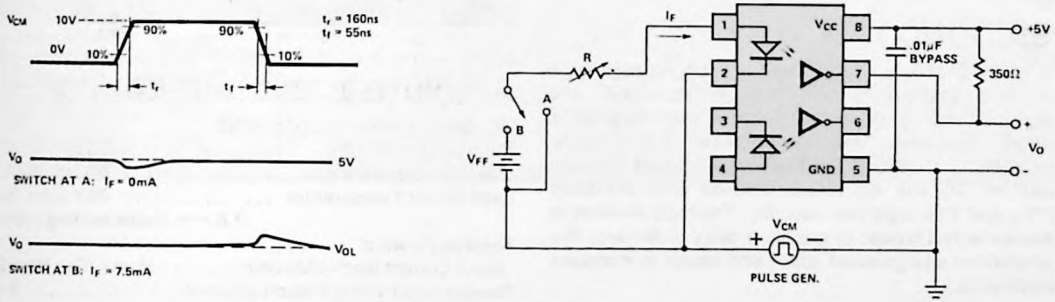


Figure 9. Test Circuit for Transient Immunity and Typical Waveforms.

HEWLETT PACKARD

DUAL CHANNEL HIGH CMR HIGH SPEED OPTOCOUPLER

HCPL-2631

TECHNICAL DATA JANUARY 1984

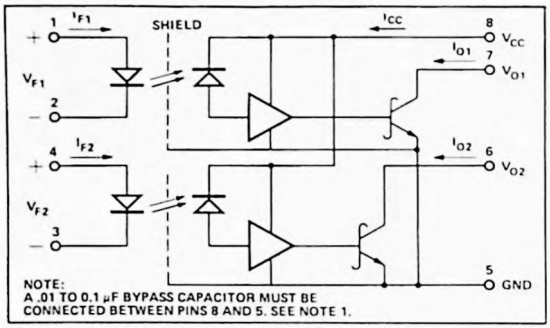


Figure 1. Schematic

Features

- INTERNAL SHIELD FOR HIGH COMMON MODE REJECTION (CMR)
- HIGH DENSITY PACKAGING
- HIGH SPEED
- LSTTL AND TTL COMPATIBLE
- GUARANTEED MINIMUM COMMON MODE TRANSIENT IMMUNITY: 1000 V/μs
- GUARANTEED PERFORMANCE OVER TEMPERATURE 0° C to 70° C
- DIELECTRIC WITHSTAND TESTED AT 3000 Vdc FOR A WORKING VOLTAGE OF 220 Vac
- RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES INC. (FILE NO. E55361)

Applications

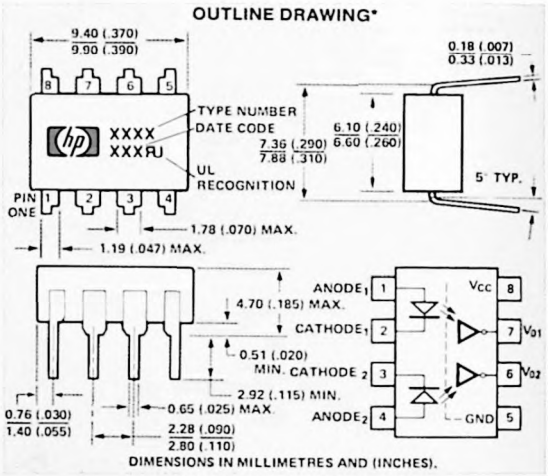
- ISOLATION OF HIGH SPEED LOGIC SYSTEMS
- MICROPROCESSOR SYSTEM INTERFACES
- ISOLATED LINE RECEIVER
- COMPUTER-PERIPHERAL INTERFACES
- GROUND LOOP ELIMINATION

Description

The HCPL-2631 is a dual channel optically coupled logic gate that combines GaAsP light emitting diodes and integrated high gain photodetectors. Internal shields provide a guaranteed common mode transient immunity specification of 1000 V/μs. The unique design provides maximum DC and AC circuit isolation while achieving LSTTL and TTL logic compatibility. The logic isolation is achieved with a typical propagation delay of 40 nsec. The dual channel design saves space and results in increased convenience.

The HCPL-2631 is recommended for high speed logic interfacing, input/output buffering and for use as line receivers in environments that conventional line receivers cannot tolerate. The HCPL-2631 can be used for the digital programming of machine control systems, motors, and floating power supplies. The internal shield makes the HCPL-2631 ideal for use in extremely high ground or induced noise environments.

OUTLINE DRAWING*



Recommended Operating Conditions

	Sym.	Min.	Max.	Units
Input Current, Low Level Each Channel	I_{FL}	0	250	μA
Input Current, High Level Each Channel	I_{FH}	6.3*	15	mA
Supply Voltage, Output	V_{CC}	4.5	5.5	V
Fan Out (TTL Load) Each Channel	N		8	
Operating Temperature	T_A	0	70	°C

*6.3 mA condition permits at least 20% CTR degradation guardband. Initial switching threshold is 5 mA or less.

Absolute Maximum Ratings

(No derating required up to 70° C)

Storage Temperature ..... −55° C to +125° C
Operating Temperature ..... 0° C to +70° C
Lead Solder Temperature ..... 260° C for 10s
(1.6 mm below seating plane)

Average Forward
Input Current (each channel) ..... 15 mA (See Note 2)
Reverse Input Voltage (each channel) ..... 5 V
Supply Voltage — V_{CC} ..... 7 V (1 Minute Maximum)
Output Current — I_O (each channel) ..... 16 mA
Output Voltage — V_O (each channel) ..... 7 V
Output Collector Power Dissipation
(each channel) ..... 40 mW

Electrical Characteristics

(Over Recommended Temperature, T_A = 0°C to +70°C, Unless Otherwise Noted)

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Figure	Note
Low Level Output Voltage	V_{OL}		0.4	0.6	V	V_{CC} = 5.5V, I_F = 5 mA I_{OL} (Sinking) = 13 mA	2, 3	3
High Level Output Current	I_{OH}		20	250	μA	V_{CC} = 5.5V, V_O = 5.5 V, I_F = 250 μA	4	3
High Level Supply Current	I_{CCH}		20	30	mA	V_{CC} = 5.5V, I_F = 0, (Both Channels)		
Low Level Supply Current	I_{CCL}		30	38	mA	V_{CC} = 5.5V, I_F = 10 mA, (Both Channels)		
Input Forward Voltage	V_F		1.5	1.75	V	I_F = 10 mA, T_A = 25°C	5	3
Input Reverse Breakdown Voltage	BV_R	5			V	I_R = 10 μA, T_A = 25°C		3
Input Capacitance	C_{IN}		60		pF	V_F = 0, f = 1 MHz		3
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		−1.6		mV/°C	I_F = 10 mA		
Input-Output Leakage Current	I_{I-O}			1	μA	Relative Humidity = 45% T_A = 25°C, t = 5 s, V_{I-O} = 3000 V dc		4, 5
Input-Input Leakage Current	I_{I-I}		0.005		μA	Relative Humidity = 45% t = 5 s, V_{I-I} = 500 V		6
Resistance (Input-Input)	R_{I-I}		10^{11}		Ω	V_{I-I} = 500 V		6
Capacitance (Input-Input)	C_{I-I}		0.25		pF	f = 1 MHz		
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 V		4
Capacitance (Input-Output)	C_{I-O}		0.6		pF	f = 1 MHz		

*All typical values are at V_{CC} = 5 V, T_A = 25°C, unless otherwise noted.

Switching Characteristics (T_A = 25°C, V_{CC} = 5 V)

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to High Output Level	t_{PLH}		40	75	ns	R_L = 350Ω C_L = 15 pF I_F = 7.5 mA	6	3, 7
Propagation Delay Time to Low Output Level	t_{PHL}		40	75	ns		6	3, 8
Output Rise Time (10-90%)	t_r		20		ns			3
Output Fall Time (90-10%)	t_f		30		ns			3
Common Mode Transient Immunity at High Output Level	CM_H	1000	10,000		V/μs	V_{CM} = 50 V (peak), V_O (min.) = 2 V, R_L = 350 Ω, I_F = 0 mA	10	3, 9, 11
Common Mode Transient Immunity at Low Output Level	CM_L	−1000	−10,000		V/μs	V_{CM} = 50 V (peak), V_O (max.) = 0.8 V, R_L = 350 Ω, I_F = 7.5 mA	10	3, 10, 11

NOTES:

1. Bypassing of the power supply line is required, with a 0.01 μF ceramic disc capacitor adjacent to each isolator as illustrated in Figure 14. Total lead length between both ends of the capacitor and the isolator pins should not exceed 20 mm. The power supply bus for the isolator(s) should be separate from the bus for any active loads, otherwise a larger value of bypass capacitor (up to 0.1 μF) may be needed to suppress regenerative feedback via the power supply. Failure to provide the bypass may impair the switching properties.
2. Peaking circuits may produce transient input currents up to 50 mA, 50 ns maximum pulse width, provided average current does not exceed 15 mA.
3. Each channel.
4. Measured between pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7, and 8 shorted together.
5. This is a proof test.
6. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.
7. The t_{PLH} propagation delay is measured from the 3.75 mA point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
8. The t_{PHL} propagation delay is measured from the 3.75 mA point on the leading edge of the input pulse to the 1.5 V point on the leading edge of the output pulse.
9. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (i.e., $V_{OUT} > 2.0$ V).
10. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., $V_{OUT} < 0.8$ V).
11. For sinusoidal voltages, $\left(\left|\frac{dv_{CM}}{dt}\right|\right)_{max} = \pi f_{CM} V_{CM}$ (p-p)
12. As illustrated in Figure 14, the V_{CC} and GND traces can be located between the input and the output leads of the HCPL-2631 to provide additional noise immunity at the compromise of insulation capability.

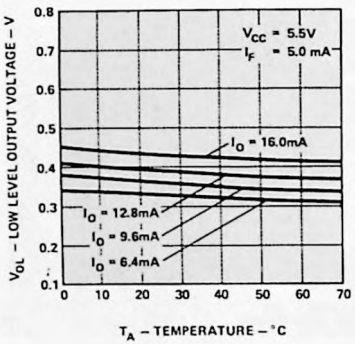


Figure 2. Low Level Output Voltage vs. Temperature

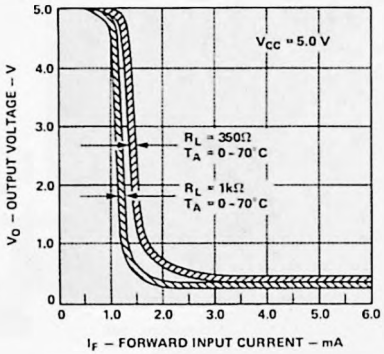


Figure 3. Output Voltage vs. Forward Input Current

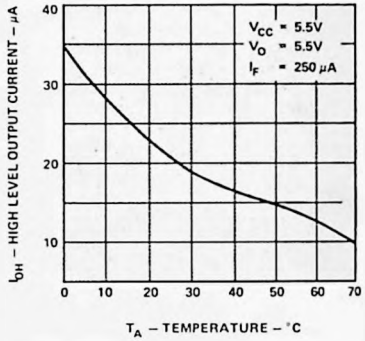


Figure 4. High Level Output Current vs. Temperature

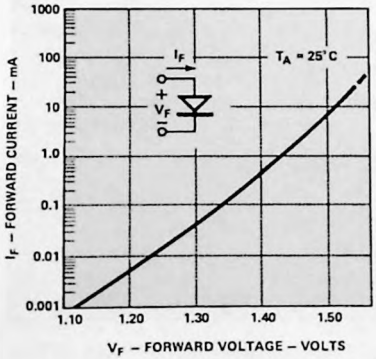


Figure 5. Input Diode Forward Characteristic

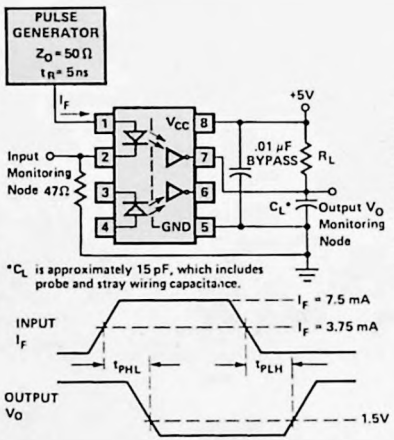


Figure 6. Test Circuit for t_{PHL} and t_{PLH}. Note 3

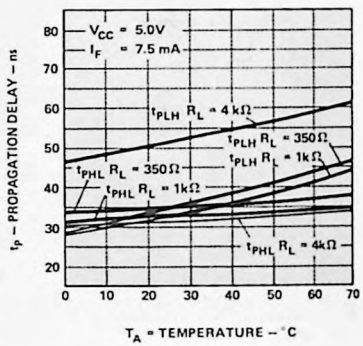


Figure 7. Propagation Delay vs. Temperature

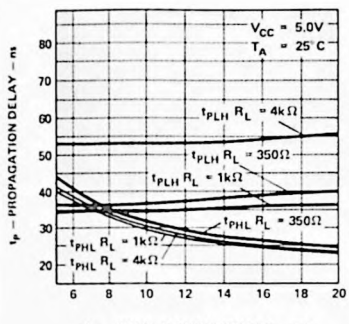


Figure 8. Propagation Delay vs. Pulse Input Current

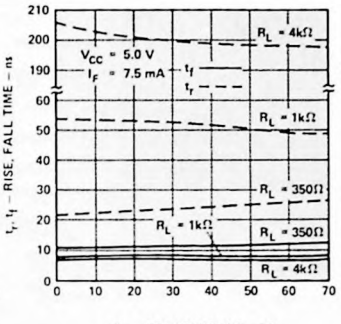


Figure 9. Rise, Fall Time vs. Temperature

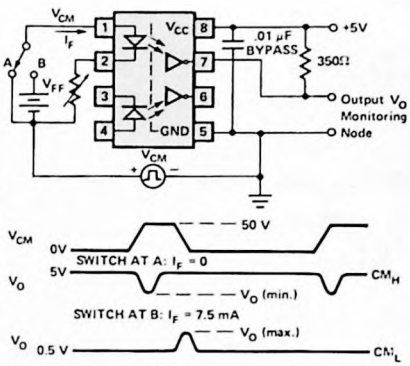


Figure 10. Test Circuit for Common Mode Transient Immunity and Typical Waveforms. Note 3

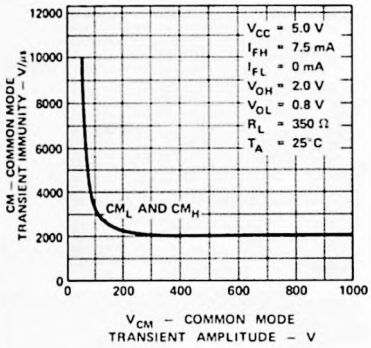


Figure 11. Common Mode Transient Immunity vs. Common Mode Transient Amplitude

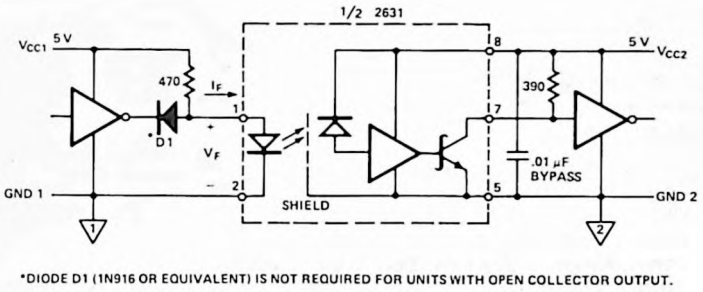


Figure 12. Recommended TTL/LSTTL to TTL/LSTTL Interface Circuit

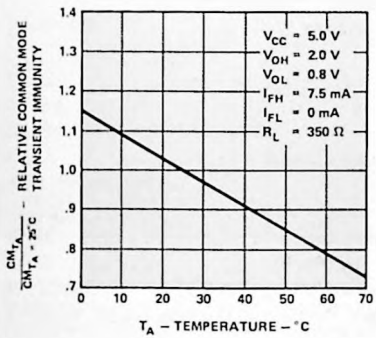


Figure 13. Relative Common Mode Transient Immunity vs. Temperature

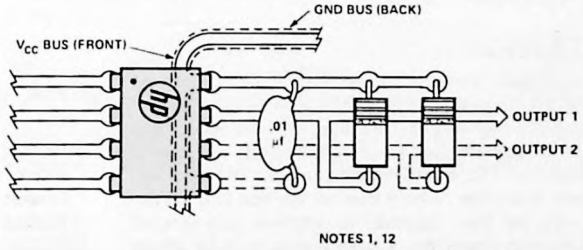


Figure 14. Recommended Printed Circuit Board Layout

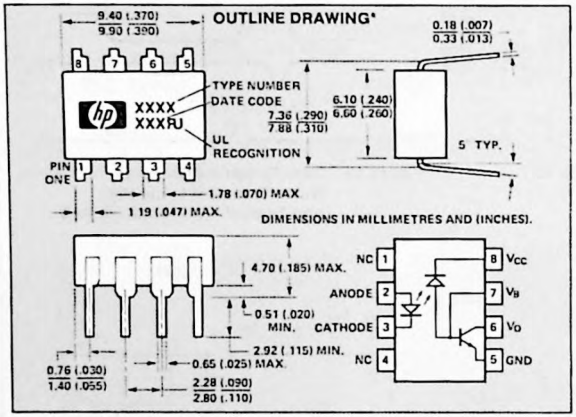
OPTOCOUPLERS

HEWLETT PACKARD

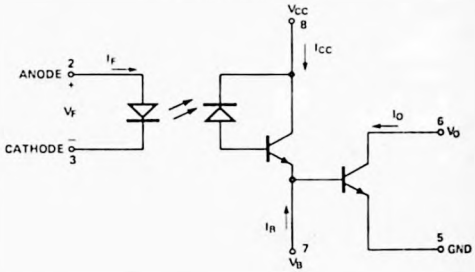
LOW INPUT CURRENT, HIGH GAIN OPTOCOUPLERS

6N138
6N139

TECHNICAL DATA JANUARY 1984



SCHEMATIC



Features

- **HIGH CURRENT TRANSFER RATIO — 800% TYPICAL**
- **LOW INPUT CURRENT REQUIREMENT — 0.5 mA**
- **TTL COMPATIBLE OUTPUT — 0.1 V V_{OL} TYPICAL**
- **HIGH COMMON MODE REJECTION — 500 V/μs**
- **PERFORMANCE GUARANTEED OVER TEMPERATURE 0° C to 70° C**
- **BASE ACCESS ALLOWS GAIN BANDWIDTH ADJUSTMENT**
- **HIGH OUTPUT CURRENT — 60 mA**
- **100K BITS/SEC TYPICAL SPEED AT I_F = 0.5 mA**
- **DIELECTRIC WITHSTAND TESTED AT 3000 Vdc FOR A WORKING VOLTAGE OF 220 Vac**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES, INC. (FILE NO. E55361)**

Description

These high gain series couplers use a Light Emitting Diode and an integrated high gain photon detector to provide extremely high current transfer ratio between input and output. Separate pins for the photodiode and output stage result in TTL compatible saturation voltages and high speed operation. Where desired the V_{CC} and V_O terminals may be tied together to achieve conventional photodarlington operation. A base access terminal allows a gain bandwidth adjustment to be made.

The 6N139 is suitable for use in CMOS, LSTTL or other low power applications. A 400% minimum current transfer ratio is guaranteed over a 0-70° C operating range for only 0.5 mA of LED current.

The 6N138 is suitable for use mainly in TTL applications. Current Transfer Ratio is 300% minimum over 0-70° C for an LED current of 1.6 mA [1 TTL unit load (U.L.)]. A 300% minimum CTR enables operation with 1 U.L. in, 1 U.L. out with a 2.2 kΩ pull-up resistor.

Applications

- Ground Isolate Most Logic Families — TTL/TTL, CMOS/TTL, CMOS/CMOS, LSTTL/TTL, CMOS/LSTTL
- Low Input Current Line Receiver — Long Line or Party line
- EIA RS-232C Line Receiver
- Telephone Ring Detector
- 117 V ac Line Voltage Status Indicator — Low Input Power Dissipation
- Low Power Systems — Ground Isolation

Absolute Maximum Ratings*

Storage Temperature . . . . . −55°C to +125°C
Operating Temperature . . . . . 0°C to +70°C
Lead Solder Temperature . . . . . 260°C for 10s
(1.6mm below seating plane)
Average Input Current — I_F . . . . . 20mA [1]
Peak Input Current — I_F 40mA
(50% duty cycle, 1 ms pulse width)
Peak Transient Input Current — I_F 1.0A
(≤ 1μs pulse width, 300 pps)
Reverse Input Voltage — V_R 5V
Input Power Dissipation . . . . . 35mW [2]
Output Current — I_O (Pin 6) . . . . . 60mA [3]
Emitter-Base Reverse Voltage (Pin 5-7) 0.5V
Supply and Output Voltage — V_{CC} (Pin 8-5), V_O (Pin 6-5)
6N138 . . . . . −0.5 to 7V
6N139 . . . . . −0.5 to 18V
Output Power Dissipation . . . . . 100mW [4]

See notes, following page.

CAUTION: The small junction sizes inherent to the design of this bipolar component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

*JEDEC Registered Data.

Electrical Specifications

OVER RECOMMENDED TEMPERATURE (T_A = 0°C to 70°C), UNLESS OTHERWISE SPECIFIED

Parameter	Sym.	Device	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR*	6N139	400 500	800 900		%	I_F = 0.5mA, V_O = 0.4V, V_{CC} = 4.5V I_F = 1.6mA, V_O = 0.4V, V_{CC} = 4.5V	3	5,6
		6N138	300	600		%	I_F = 1.6mA, V_O = 0.4V, V_{CC} = 4.5V		
Logic Low Output Voltage	V_{OL}	6N139		0.1 0.1 0.2	0.4 0.4 0.4	V	I_F = 1.6mA, I_O = 6.4mA, V_{CC} = 4.5V I_F = 5mA, I_O = 15mA, V_{CC} = 4.5V I_F = 12mA, I_O = 24mA, V_{CC} = 4.5V	1,2	6
		6N138		0.1	0.4	V	I_F = 1.6mA, I_O = 4.8mA, V_{CC} = 4.5V		
Logic High Output Current	I_{OH}*	6N139		0.05	100	µA	I_F = 0mA, V_O = V_{CC} = 18V		6
		6N138		0.1	250	µA	I_F = 0mA, V_O = V_{CC} = 7V		
Logic Low Supply Current	I_{CCL}			0.2		mA	I_F = 1.6mA, V_O = Open, V_{CC} = 5V		6
Logic High Supply Current	I_{CCH}			10		nA	I_F = 0mA, V_O = Open, V_{CC} = 5V		6
Input Forward Voltage	V_F*			1.4	1.7	V	I_F = 1.6mA, T_A = 25°C	4	
Input Reverse Breakdown Voltage	BV_R*		5		V		I_R = 10µA, T_A=25°C		
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			−1.8		mV/°C	I_F = 1.6mA		
Input Capacitance	C_{IN}			60		pF	f=1MHz, V_F = 0		
Input - Output Insulation Leakage Current	I_{I-O}*				1.0	µA	45% Relative Humidity, T_A = 25°C t = 5 s, V_{I-O} = 3000Vdc		7,11
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500Vdc		7
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1MHz		7

*,**All typicals at T_A = 25°C and V_{CC} = 5V, unless otherwise noted.

Switching Specifications

AT T_A = 25°C

Parameter	Sym.	Device	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time To Logic Low at Output	t_{PHL}*	6N139		5 0.2	25 1	µs	I_F = 0.5mA, R_L = 4.7kΩ I_F = 12mA, R_L = 270Ω	9	6,8
		6N138		1	10	µs	I_F = 1.6mA, R_L = 2.2kΩ		
Propagation Delay Time To Logic High at Output	t_{PLH}*	6N139		5 1	60 7	µs	I_F = 0.5mA, R_L = 4.7kΩ I_F = 12mA, R_L = 270Ω	9	6,8
		6N138		4	35	µs	I_F = 1.6mA, R_L = 2.2kΩ		
Common Mode Transient Immunity at Logic High Level Output	CM_H			500		V/µs	I_F = 0mA, R_L = 2.2kΩ, R_{CC} = 0 $\|V_{cm}\|$ = 10V_{p-p}	10	9,10
Common Mode Transient Immunity at Logic Low Level Output	CM_L			−500		V/µs	I_F = 1.6mA, R_L = 2.2kΩ, R_{CC} = 0 $\|V_{cm}\|$ = 10V_{p-p}	10	9,10

NOTES:

1. Derate linearly above 50°C free-air temperature at a rate of 0.4mA/°C.
2. Derate linearly above 50°C free-air temperature at a rate of 0.7mW/°C.
3. Derate linearly above 25°C free-air temperature at a rate of 0.7mA/°C.
4. Derate linearly above 25°C free-air temperature at a rate of 2.0mW/°C.
5. DC CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
6. Pin 7 Open.
7. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
8. Use of a resistor between pin 5 and 7 will decrease gain and delay time. See Application Note 951-1 for more details.
9. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode pulse, V_{cm}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.0V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{cm}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8V).
10. In applications where dV/dt may exceed 50,000V/µs (such as static discharge) a series resistor, R_{CC}, should be included to protect the detector IC from destructively high surge currents. The recommended value is $R_{CC} \approx \frac{1V}{0.15\ I_F\ (mA)}$ kΩ.
11. This is a proof test to validate the UL 220 Vac rating.

*JEDEC Registered Data.

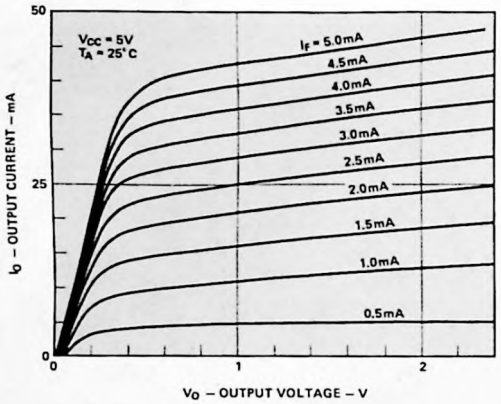


Figure 1. 6N139 DC Transfer Characteristics.

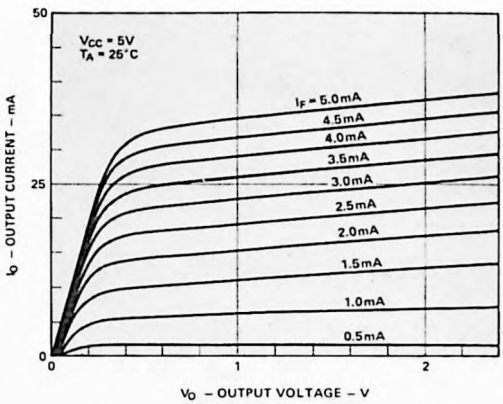


Figure 2. 6N138 DC Transfer Characteristics.

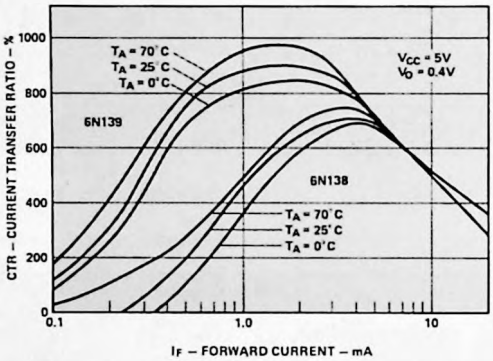


Figure 3. Current Transfer Ratio vs. Forward Current.

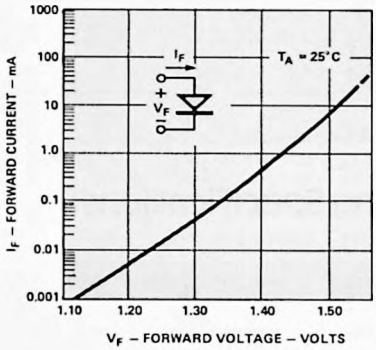


Figure 4. Input Diode Forward Current vs. Forward Voltage.

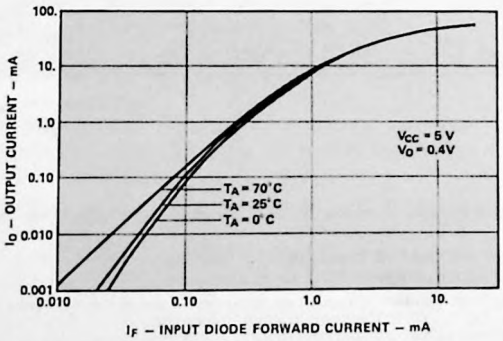


Figure 5. 6N139 Output Current vs. Input Diode Forward Current.

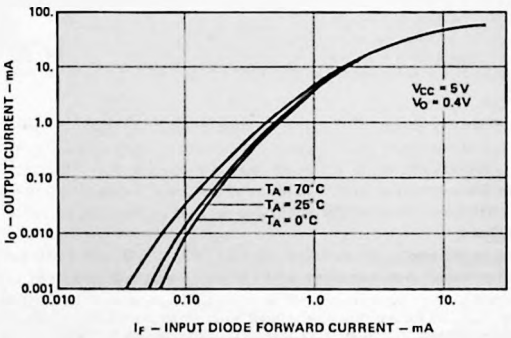


Figure 6. 6N138 Output Current vs. Input Diode Forward Current.

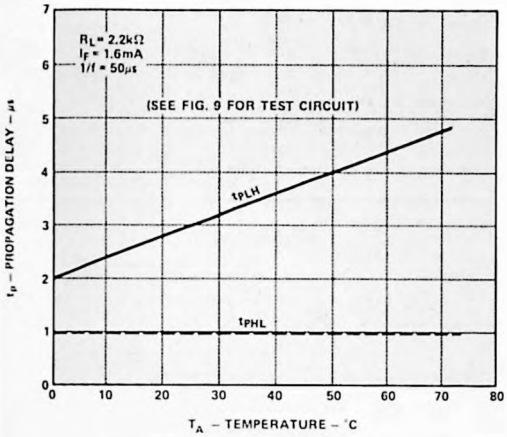


Figure 7. Propagation Delay vs. Temperature.

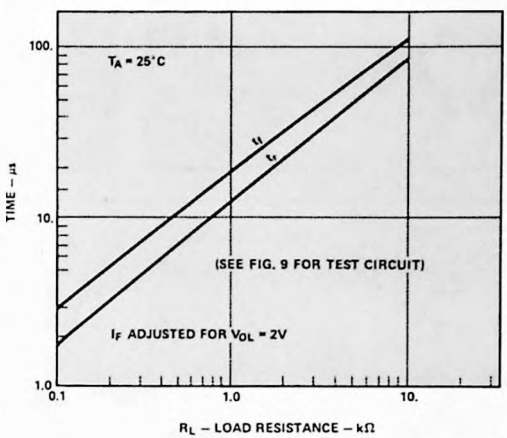


Figure 8. Non Saturated Rise and Fall Times vs. Load Resistance.

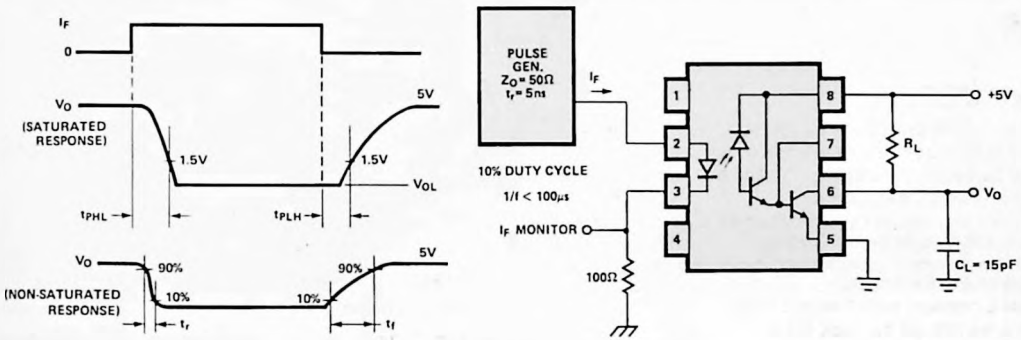


Figure 9. Switching Test Circuit.*

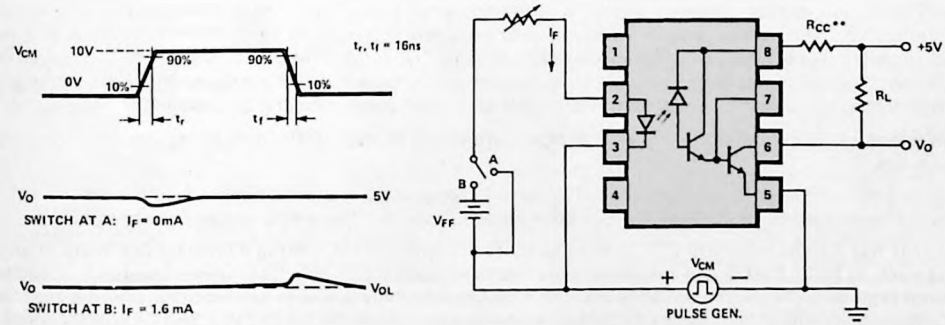


Figure 10. Test Circuit for Transient Immunity and Typical Waveforms.

*JEDEC Registered Data.

**See Note 10

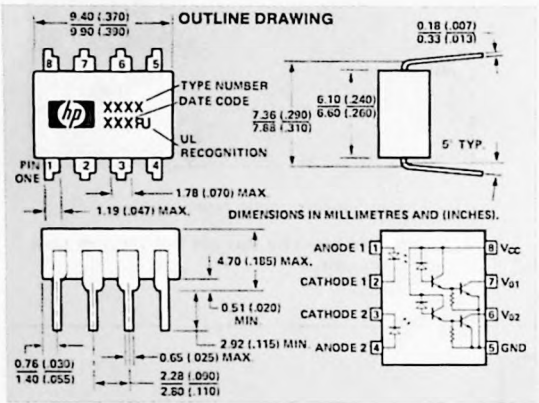
OPTOCOUPLERS

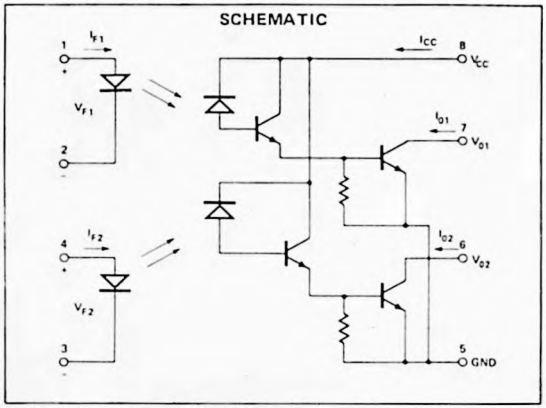
HEWLETT PACKARD

DUAL LOW INPUT CURRENT, HIGH GAIN OPTOCOUPLERS

HCPL-2730
HCPL-2731

TECHNICAL DATA JANUARY 1984





Features

- HIGH CURRENT TRANSFER RATIO — 1000% TYPICAL
- LOW INPUT CURRENT REQUIREMENT — 0.5 mA
- LOW OUTPUT SATURATION VOLTAGE — 0.1V TYPICAL
- HIGH DENSITY PACKAGING
- DIELECTRIC WITHSTAND TESTED AT 3000 V dc FOR A WORKING VOLTAGE OF 220 Vac
- PERFORMANCE GUARANTEED OVER 0°C TO 70°C TEMPERATURE RANGE
- HIGH COMMON MODE REJECTION
- DATA RATES UP TO 200K BIT/s
- LSTTL COMPATIBLE
- RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES, INC. (FILE NO. E55361).

Applications

- Digital Logic Ground Isolation
- Telephone Ring Detector
- EIA RS-232C Line Receiver
- Low Input Current Line Receiver — Long Line or Party Line
- Microprocessor Bus Isolation
- Current Loop Receiver
- Polarity Sensing
- Level Shifting
- Line Voltage Status Indicator — Low Input Power Dissipation

Description

The HCPL-2730/31 dual channel couplers contain a separated pair of GaAsP light emitting diodes optically coupled to a pair of integrated high gain photon detectors. They provide extremely high current transfer ratio, 3000V dc withstand test voltage and excellent input-output common mode transient immunity. A separate pin for the photodiodes and first gain stages (V_{CC}) permits lower output saturation voltage and higher speed operation than possible with conventional photodarlington type isolators. In addition V_{CC} may be as low as 1.6V without adversely affecting the parametric performance.

Guaranteed operation at low input currents and the high current transfer ratio (CTR) reduce the magnitude and effects of CTR degradation.

The outstanding high temperature performance of this split Darlington type output amplifier results from the inclusion of an integrated emitter-base bypass resistor which shunts photodiode and first stage leakage currents to ground.

The HCPL-2731 has a 400% minimum CTR at an input current of only 0.5 mA making it ideal for use in low input current applications such as MOS, CMOS and low power logic interfacing or RS232C data transmission systems. In addition, the high CTR and high output current capability make this device extremely useful in applications where a high fanout is required. Compatibility with high voltage CMOS logic systems is guaranteed by the 18V V_{CC} and V_O specifications and by testing output high leakage (I_{OH}) at 18V.

The HCPL-2730 is specified at an input current of 1.6 mA and has a 7V V_{CC} and V_O rating. The 300% minimum CTR allows TTL to TTL interfacing with an input current of only 1.6 mA.

Important specifications such as CTR, leakage current and output saturation voltage are guaranteed over the 0°C to 70°C temperature range to allow trouble-free system operation.

Electrical Specifications

(Over Recommended Temperature T_A = 0°C to 70°C, Unless Otherwise Specified)

Parameter	Sym.	Device HCPL-	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	2731	400 500	1000 1100		%	I_F = 0.5mA, V_O = 0.4V, V_{CC} = 4.5V I_F = 1.6mA, V_O = 0.4V, V_{CC} = 4.5V	2	6,7
		2730	300	1000		%	I_F = 1.6mA, V_O = 0.4V, V_{CC} = 4.5V	2	
Logic Low Output Voltage	V_{OL}	2731		0.1 0.1 0.2	0.4 0.4 0.4	V	I_F = 1.6mA, I_O = 8mA, V_{CC} = 4.5V I_F = 5mA, I_O = 15mA, V_{CC} = 4.5V I_F = 12mA, I_O = 24mA, V_{CC} = 4.5V	1	6
		2730		0.1	0.4	V	I_F = 1.6mA, I_O = 4.8mA, V_{CC} = 4.5V		
Logic High Output Current	I_{OH}	2731		0.005	100	μA	I_F = 0 mA, V_O = V_{CC} = 18V		6
		2730		0.01	250	μA	I_F = 0mA, V_O = V_{CC} = 7V		
Logic Low Supply Current	I_{CCL}	2731		1.2		mA	I_{F1} = I_{F2} = 1.6mA, V_{CC} = 18V		
		2730		0.9			V_{O1} = V_{O2} = Open, V_{CC} = 7V		
Logic High Supply Current	I_{CCH}	2731		5		nA	I_{F1} = I_{F2} = 0mA, V_{CC} = 18V		
		2730		4			V_{O1} = V_{O2} = Open, V_{CC} = 7V		
Input Forward Voltage	V_F			1.4	1.7	V	I_F = 1.6mA, T_A = 25°C	4	6
Input Reverse Breakdown Voltage	BV_R		5			V	I_R = 10 μA, T_A = 25°C		6
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.8		mV/°C	I_F = 1.6mA		6
Input Capacitance	C_{IN}			60		pF	f = 1 MHz, V_F = 0		6
Input-Output Insulation Leakage Current	I_{I-O}				1.0	μA	45% Relative Humidity, T_A = 25°C t = 5s, V_{I-O} = 3000 Vdc		8,12
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500Vdc		8
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1 MHz		8
Input-Input Insulation Leakage Current	I_{I-I}			0.005		μA	45% Relative Humidity, t=5s, V_{I-I} = 500Vdc		9
Resistance (Input-Input)	R_{I-I}			10^{11}		Ω	V_{I-I} = 500Vdc		9
Capacitance (Input-Input)	C_{I-I}			0.25		pF	f = 1 MHz		9

*All typicals at T_A = 25°C

Switching Specifications at T_A=25°C

Parameter	Sym.	Device HCPL-	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time To Logic Low at Output	t_{PHL}	2731		25	100	μs	I_F = 0.5mA, R_L = 4.7kΩ	9	6
		2730/1		5 0.5	20 2	μs	I_F = 1.6mA, R_L = 2.2kΩ I_F = 12mA, R_L = 270Ω		
Propagation Delay Time To Logic High at Output	t_{PLH}	2731		20	60	μs	I_F = 0.5mA, R_L = 4.7kΩ	9	6
		2730/1		10 1	35 10	μs	I_F = 1.6mA, R_L = 2.2kΩ I_F = 12mA, R_L = 270Ω		
Common Mode Transient Immunity at Logic High Level Output	CM_H			500		V/μs	I_F = 0mA, R_L = 2.2kΩ $\lvert V_{CM} \rvert$ = 10V_{p-p}	10	6, 10, 11
Common Mode Transient Immunity at Logic Low Level Output	CM_L			-500		V/μs	I_F = 1.6mA, R_L = 2.2kΩ $\lvert V_{CM} \rvert$ = 10V_{p-p}	10	6, 10, 11

NOTES:
1. Derate linearly above 50°C free-air temperature at a rate of 0.5mA/°C.
2. Derate linearly above 50°C free-air temperature at a rate of 0.9mW/°C.
3. Derate linearly above 35°C free-air temperature at a rate of 0.6mA/°C.
4. Pin 5 should be the most negative voltage at the detector side.
5. Derate linearly above 35°C free-air temperature at a rate of 1.7mW/°C. Output power is collector output power plus supply power.
6. Each channel.
7. CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
8. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
9. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.
10. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse V_{CM}, to assure that the output will remain in Logic High state (i.e., V_O > 2.0V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM} dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8V).
11. In applications where dV/dt may exceed 50,000 V/μs (such as a static discharge) a series resistor, R_{CC}, should be included to protect the detector IC from destructively high surge currents. The recommended value is $R_{CC} \approx \frac{1V}{0.3\ I_F\ (mA)}$ kΩ.
12. This is a proof test to validate the UL 220 Vac rating.

Absolute Maximum Ratings

Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... -40°C to +85°C
Lead Solder Temperature ..... 260°C for 10 sec
(1.6mm below seating plane)
Average Input Current — I_F
(each channel) ..... 20 mA[1]
Peak Input Current — I_F
(each channel) ..... 40 mA
(50% duty cycle, 1 ms pulse width)
Reverse Input Voltage — V_R
(each channel) 5V
Input Power Dissipation
(each channel) ..... 35 mW[2]
Output Current — I_O
(each channel) ..... 60 mA[3]
Supply and Output Voltage — V_{CC} (Pin 8-5), V_O (Pin 7,6-5)[4]
HCPL-2730 ..... -0.5 to 7V
HCPL-2731 ..... -0.5 to 18V
Output Power Dissipation
(each channel) ..... 100 mW[5]

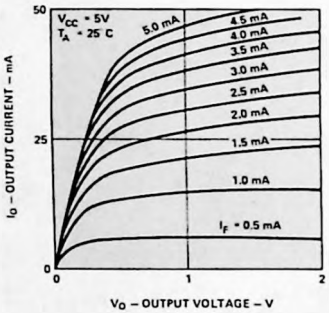


Figure 1. DC Transfer Characteristics.

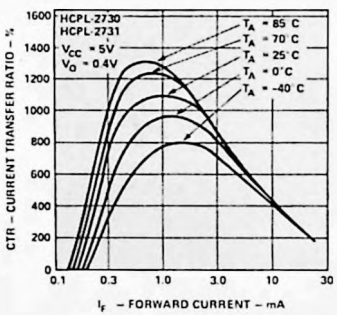


Figure 2. Current Transfer Ratio vs. Forward Current.

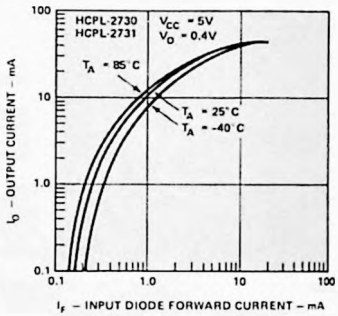


Figure 3. Output Current vs. Input Diode Forward Current.

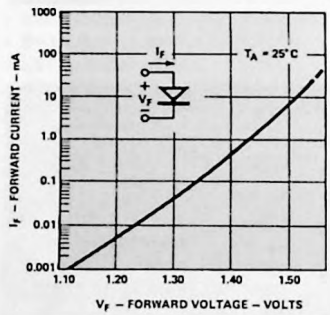


Figure 4. Input Diode Forward Current vs. Forward Voltage.

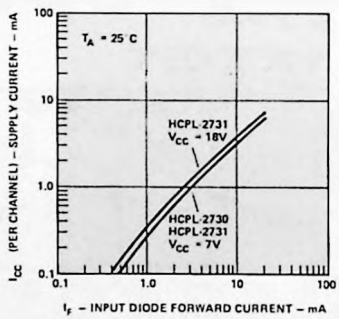


Figure 5. Supply Current Per Channel vs. Input Diode Forward Current.

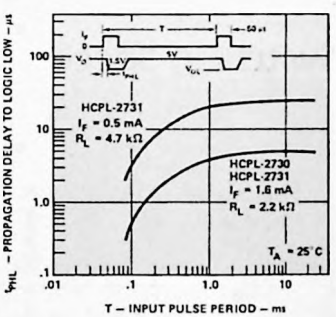


Figure 6. Propagation Delay To Logic Low vs. Pulse Period.

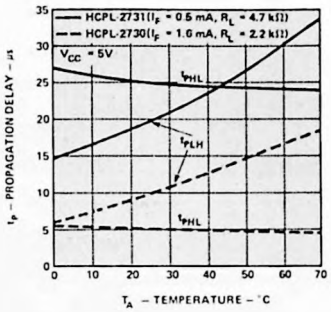


Figure 7. Propagation Delay vs. Temperature.

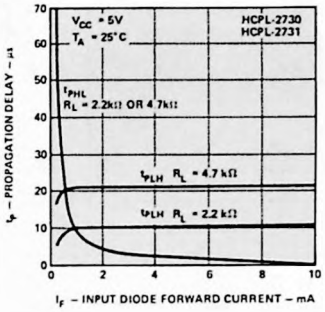


Figure 8. Propagation Delay vs. Input Diode Forward Current.

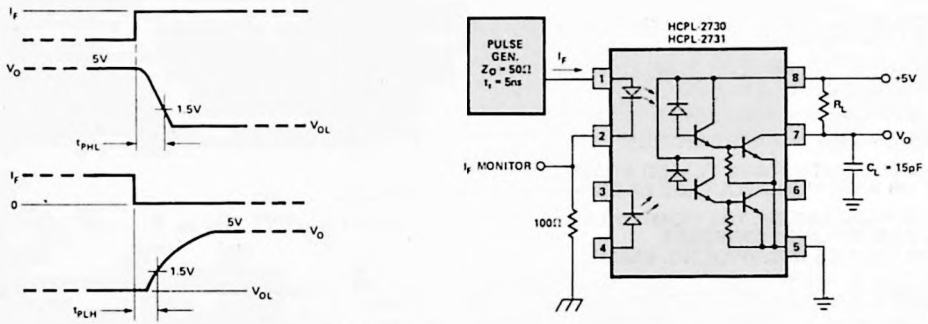
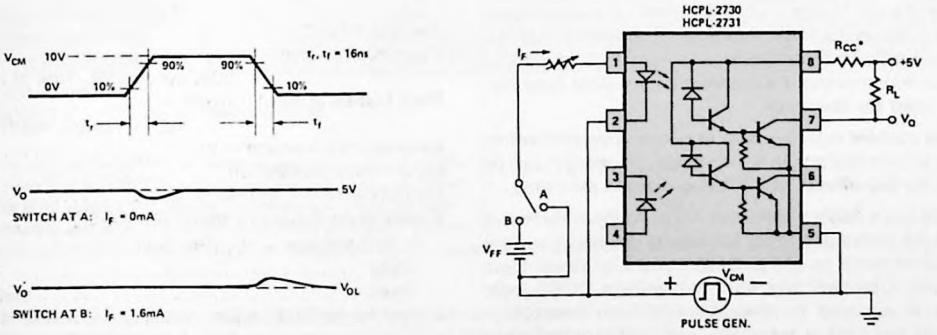


Figure 9. Switching Test Circuit.



*See Note 11.

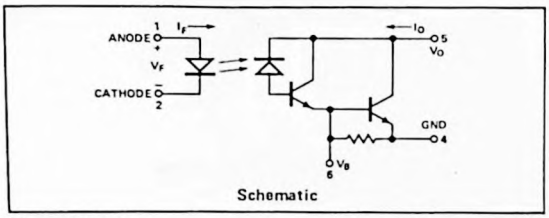
Figure 10. Test Circuit for Transient Immunity and Typical Waveforms.

HEWLETT PACKARD

LOW INPUT CURRENT, HIGH GAIN OPTOCOUPLER

4N45
4N46

TECHNICAL DATA JANUARY 1984



Schematic

Features

- HIGH CURRENT TRANSFER RATIO — 1000% TYPICAL
- LOW INPUT CURRENT REQUIREMENT — 0.5 mA
- PERFORMANCE GUARANTEED OVER 0°C TO 70°C TEMPERATURE RANGE
- INTERNAL BASE-EMITTER RESISTOR MINIMIZES OUTPUT LEAKAGE
- GAIN-BANDWIDTH ADJUSTMENT PIN
- HIGH COMMON MODE REJECTION
- DIELECTRIC WITHSTAND TESTED AT 3000 V dc FOR A WORKING VOLTAGE OF 220 Vac
- RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES INC. (FILE NO. E55361)

Description

The 4N45/46 optocouplers contain a GaAsP light emitting diode optically coupled to a high gain photodetector IC.

The excellent performance over temperature results from the inclusion of an integrated emitter-base bypass resistor which shunts photodiode and first stage leakage currents to ground. External access to the second stage base provides better noise rejection than a conventional photodarlington detector. An external resistor or capacitor at the base can be added to make a gain-bandwidth or input current threshold adjustment. The base lead can also be used for feedback.

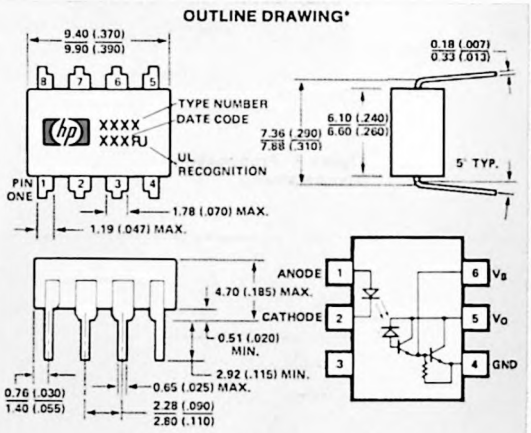
The high current transfer ratio at very low input currents permits circuit designs in which adequate margin can be allowed for the effects of CTR degradation over time.

The 4N46 has a 350% minimum CTR at an input current of only 0.5mA making it ideal for use in low input current applications such as MOS, CMOS and low power logic interfacing. Compatibility with high voltage CMOS logic systems is assured by the 20V minimum breakdown voltage of the output transistor and by the guaranteed maximum output leakage (I_{OH}) at 18V.

The 4N45 has a 250% minimum CTR at 1.0mA input current and a 7V minimum breakdown voltage rating.

*JEDEC Registered Data.

OUTLINE DRAWING*



DIMENSIONS IN MILLIMETRES AND (INCHES).

Applications

- Telephone Ring Detector
- Digital Logic Ground Isolation
- Low Input Current Line Receiver
- Line Voltage Status Indicator — Low Input Power Dissipation
- Logic to Reed Relay Interface
- Level Shifting
- Interface Between Logic Families

Absolute Maximum Ratings*

Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... -40°C to +70°C
Lead Solder Temperature ..... 260°C for 10 s.
(1.6mm below seating plane)
Average Input Current — I_F ..... 20 mA[1]
Peak Input Current — I_F ..... 40 mA
(50% duty cycle, 1ms pulse width)
Peak Transient Input Current — I_F 1.0A
($\leqslant$1 µs pulse width, 300pps)
Reverse Input Voltage — V_R 5V
Input Power Dissipation ..... 35mW[2]
Output Current — I_O (Pin 5) ..... 60 mA[3]
Emitter-Base Reverse Voltage (Pins 4-6) 0.5V
Output Voltage — V_O (Pin 5-4)
4N45 ..... -0.5 to 7V
4N46 ..... -0.5 to 20V
Output Power Dissipation ..... 100mW[4]

See notes, following page

CAUTION: The small junction sizes inherent to the design of this bipolar component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Electrical Specifications

OVER RECOMMENDED TEMPERATURE (T_A = 0°C TO 70°C), UNLESS OTHERWISE SPECIFIED

Parameter	Sym.	Device	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR*	4N46	350 500 200	1500 1500 600		%	I_F = 0.5mA, V_O = 1.0V I_F = 1.0mA, V_O = 1.0V I_F = 10mA, V_O = 1.2V	4	5,6
		4N45	250 200	1200 500		%	I_F = 1.0mA, V_O = 1.0V I_F = 10mA, V_O = 1.2V		
Logic Low Output Voltage	V_{OL}	4N46		.90 .92 .95	1.0 1.0 1.2	V	I_F = 0.5mA, I_{OL} = 1.75mA I_F = 1.0mA, I_{OL} = 5.0mA I_F = 10mA, I_{OL} = 20mA	2	6
		4N45		.90 .95	1.0 1.2	V	I_F = 1.0mA, I_{OL} = 2.5mA I_F = 10mA, I_{OL} = 20mA		
Logic High Output Current	I_{OH}*	4N46		.001	100	µA	I_F = 0mA, V_O = 18V		6
		4N45		.001	250	µA	I_F = 0mA, V_O = 5V		
Input Forward Voltage	V_F*			1.4	1.7	V	I_F = 1.0mA, T_A = 25°C	1	
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.8		mV/°C	I_F = 1.0mA		
Input Reverse Breakdown Voltage	BV_R*		5			V	I_R = 10µA, T_A = 25°C		
Input Capacitance	C_{IN}			60		pF	f = 1MHz, V_F = 0		
Input-Output Insulation Leakage Current	I_{I-O}*				1.0	µA	45% Relative Humidity, T_A=25°C t = 5 s, V_{I-O} = 3000VDC		7,10
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500VDC		7
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1MHz		7

Switching Specifications

AT T_A = 25°C

Parameter	Symbol	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time To Logic Low at Output	t_{PHL}		80		µs	I_F = 1.0mA, R_L = 10kΩ	8	6,8
	t_{PHL}*		5	50	µs	I_F = 10mA, R_L = 220Ω		
Propagation Delay Time To Logic High at Output	t_{PLH}		1500		µs	I_F = 1.0mA, R_L = 10kΩ	8	6,8
	t_{PLH}*		150	500	µs	I_F = 10mA, R_L = 220Ω		
Common Mode Transient Immunity at Logic High Level Output	CM_H		500		V/µs	I_F = 0mA, R_L = 10kΩ $\|V_{cm}\|$ = $10V_{p-p}$	9	9
Common Mode Transient Immunity at Logic Low Level Output	CM_L		-500		V/µs	I_F = 1.0mA, R_L = 10kΩ $\|V_{cm}\|$ = $10V_{p-p}$	9	9

*JEDEC Registered Data.

**All typicals at T_A = 25°C, unless otherwise noted.

NOTES:

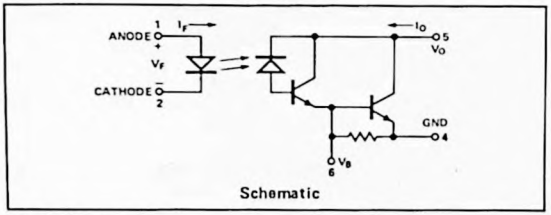
1. Derate linearly above 50°C free-air temperature at a rate of 0.4mA/°C.
2. Derate linearly above 50°C free-air temperature at a rate of 0.7mW/°C.
3. Derate linearly above 25°C free-air temperature at a rate of 0.8mA/°C.
4. Derate linearly above 25°C free-air temperature at a rate of 1.5mW/°C.
5. DC CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
6. Pin 6 Open.
7. Device considered a two-terminal device: Pins 1, 2, 3 shorted together and Pins 4, 5, and 6 shorted together.
8. Use of a resistor between pin 4 and 6 will decrease gain and delay time. (See Figures 10 and 12).
9. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode pulse, V_{cm}, to assure that the output will remain in a Logic High state (i.e., $V_O > 2.5V$). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{cm}, to assure that the output will remain in a Logic Low state (i.e., $V_O < 2.5V$).
10. This is a proof test to validate the UL 220 Vac rating.

HEWLETT PACKARD

LOW INPUT CURRENT, HIGH GAIN OPTOCOUPLER

4N45
4N46

TECHNICAL DATA JANUARY 1984



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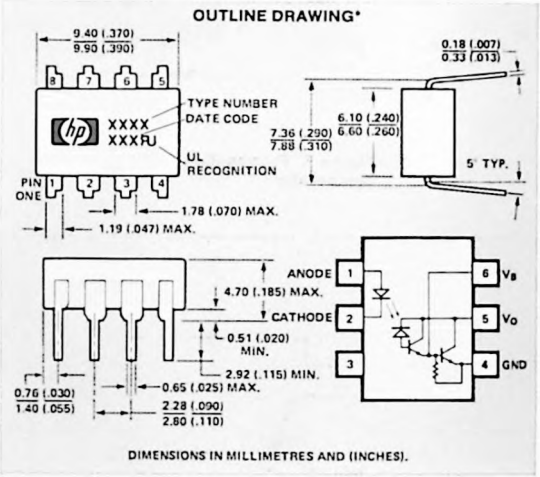

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(1.6mm below seating plane)
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Peak Input Current — I_F ..... 40 mA
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Reverse Input Voltage — V_R 5V
Input Power Dissipation ..... 35mW[2]
Output Current — I_O (Pin 5) ..... 60 mA[3]
Emitter-Base Reverse Voltage (Pins 4-6) 0.5V
Output Voltage — V_O (Pin 5-4)
4N45 ..... -0.5 to 7V
4N46 ..... -0.5 to 20V
Output Power Dissipation ..... 100mW[4]

See notes, following page

CAUTION: The small junction sizes inherent to the design of this bipolar component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

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Logic Low Output Voltage	V_{OL}	4N46		.90 .92 .95	1.0 1.0 1.2	V	I_F = 0.5mA, I_{OL} = 1.75mA I_F = 1.0mA, I_{OL} = 5.0mA I_F = 10mA, I_{OL} = 20mA	2	6
		4N45		.90 .95	1.0 1.2	V	I_F = 1.0mA, I_{OL} = 2.5mA I_F = 10mA, I_{OL} = 20mA		
Logic High Output Current	I_{OH}*	4N46		.001	100	µA	I_F = 0mA, V_O = 18V		6
		4N45		.001	250	µA	I_F = 0mA, V_O = 5V		
Input Forward Voltage	V_F*			1.4	1.7	V	I_F = 1.0mA, T_A = 25°C	1	
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.8		mV/°C	I_F = 1.0mA		
Input Reverse Breakdown Voltage	BV_R*		5			V	I_R = 10µA, T_A = 25°C		
Input Capacitance	C_{IN}			60		pF	f = 1MHz, V_F = 0		
Input-Output Insulation Leakage Current	I_{I-O}*				1.0	µA	45% Relative Humidity, T_A=25°C t = 5 s, V_{I-O} = 3000VDC		7,10
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500VDC		7
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3. Derate linearly above 25° C free-air temperature at a rate of 0.8mA/° C.
4. Derate linearly above 25° C free-air temperature at a rate of 1.5mW/° C.
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10. This is a proof test to validate the UL 220 Vac rating.

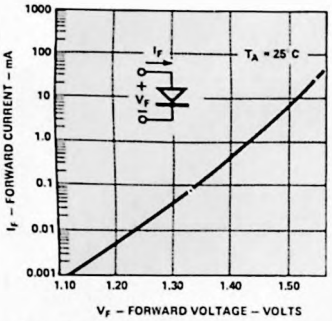


Figure 1. Input Diode Forward Current vs. Forward Voltage.

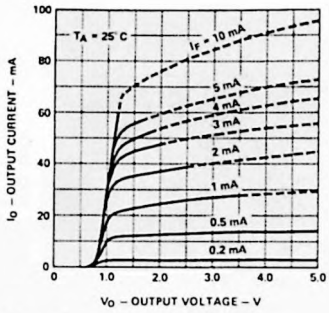


Figure 2. Typical DC Transfer Characteristics.

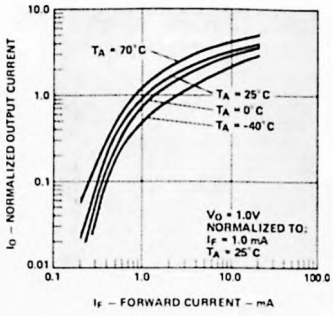


Figure 3. Output Current vs. Input Current.

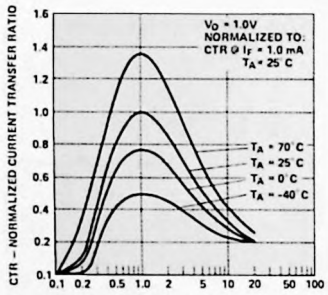


Figure 4. Current Transfer Ratio vs. Input Current.

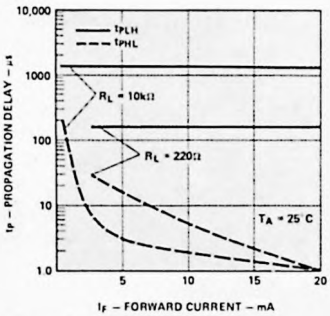


Figure 5. Propagation Delay vs. Forward Current.

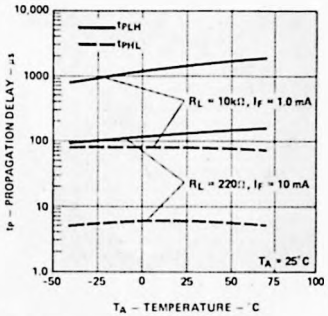


Figure 6. Propagation Delay vs. Temperature.

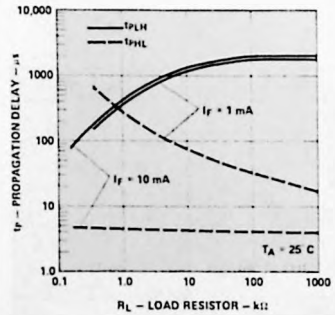
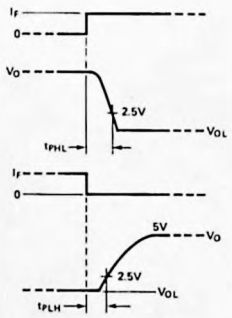


Figure 7. Propagation Delay vs Load Resistor.



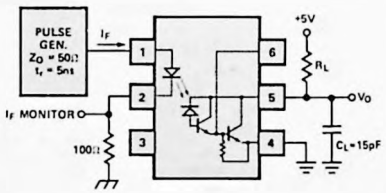
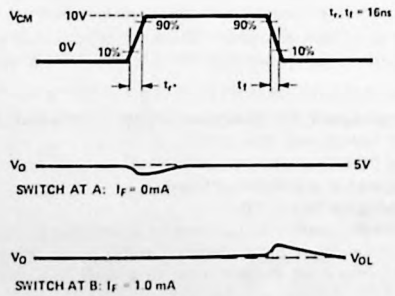


Figure 8. Switching Test Circuit



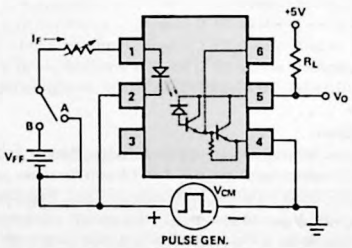


Figure 9. Test Circuit for Transient Immunity and Typical Waveforms.

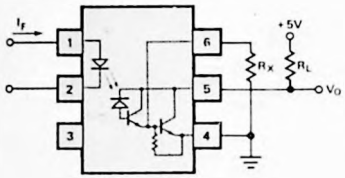


Figure 10. External Base Resistor, R_X

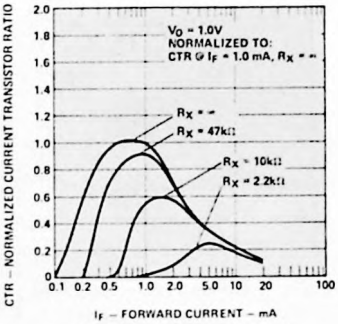


Figure 11. Effect of R_X On Current Transfer Ratio

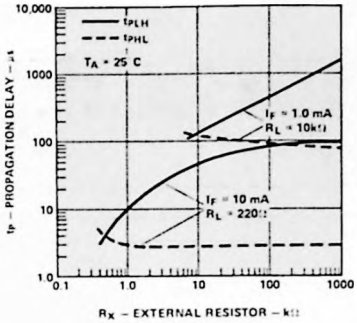
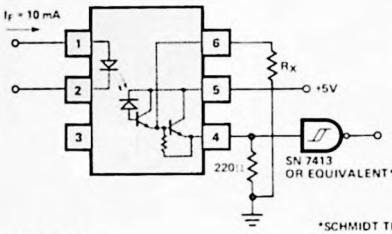


Figure 12. Effect of R_X On Propagation Delay

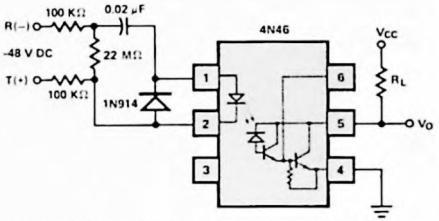
Applications



R_X (kΩ)	t_{PHL} (µs)	t_{PLH} (µs)
∞	5	320
100	5	200
47	5	140
20	6	80
10	6	45

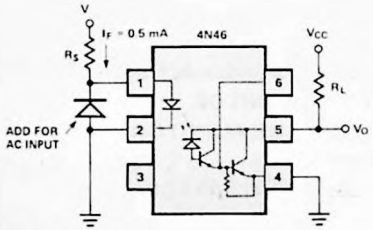
*SCHMIDT TRIGGER RECOMMENDED BECAUSE OF LONG t_r, t_f.

TTL Interface



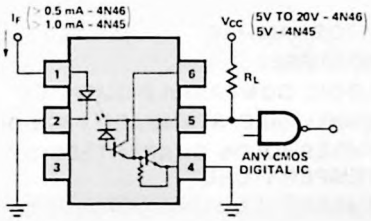
NOTE: AN INTEGRATOR MAY BE REQUIRED AT THE OUTPUT TO ELIMINATE DIALING PULSES AND LINE TRANSIENTS.

Telephone Ring Detector

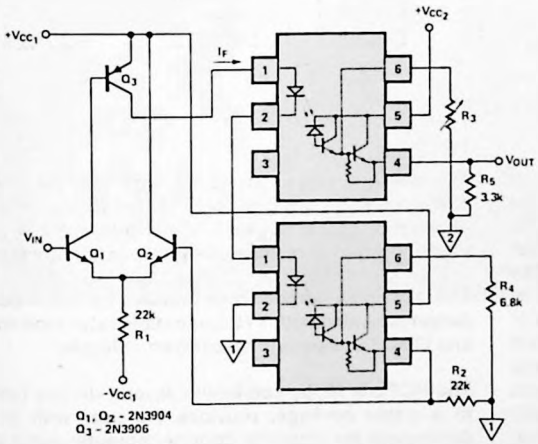


V (Vdc or Vrms)	R_S	V • I_F (mW)
24	47kΩ	11
48	100kΩ	22
115	220kΩ	62
230	470kΩ	113

Line Voltage Monitor



CMOS Interface



Analog Signal Isolation

CHARACTERISTICS

R_{IN} = 30MΩ, R_{OUT} = 50Ω
$V_{IN(MAX)} = V_{CC_1}$ - 1V, LINEARITY BETTER THAN 5%

DESIGN COMMENTS

R_1 - NOT CRITICAL $\left(< \frac{V_{IN\,(MAX)} - (-V_{CC_1}) - V_{BE}}{I_{F\,(MAX)}}\right) h_{FE}\ Q_3$

R_2 - NOT CRITICAL (OMIT IF 0.2 TO 0.3V OFFSET IS TOLERABLE)

$R_4 > \frac{V_{IN\,(MAX)} + V_{BE}}{1\ mA}$

$R_5 > \frac{V_{IN\,(MAX)}}{2.5\ mA}$

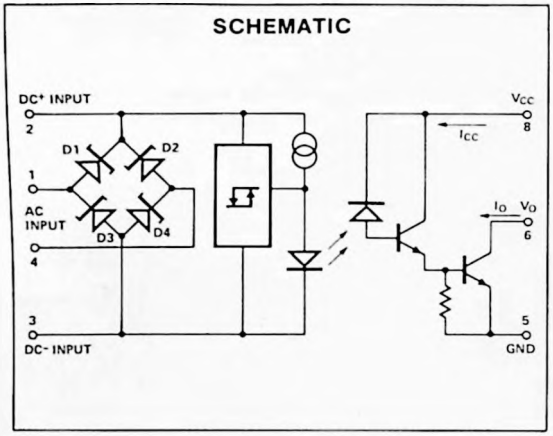
NOTE: ADJUST R_3 SO $V_{OUT} = V_{IN}$ AT $V_{IN} = \frac{V_{IN\,(MAX)}}{2}$

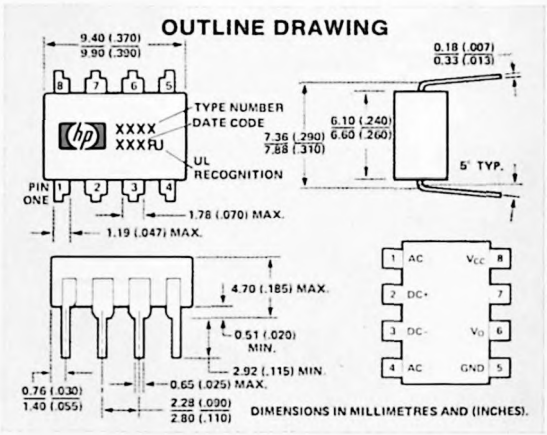
HEWLETT PACKARD

AC/DC TO LOGIC INTERFACE OPTOCOUPLER

HCPL-3700

TECHNICAL DATA JANUARY 1984



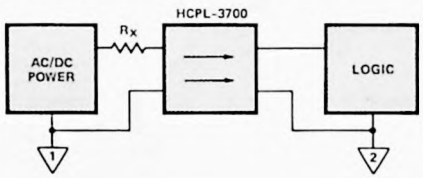


Features

- AC OR DC INPUT
- PROGRAMMABLE SENSE VOLTAGE
- HYSTERESIS
- LOGIC COMPATIBLE OUTPUT
- SMALL SIZE: STANDARD 8 PIN DIP
- THRESHOLDS GUARANTEED OVER TEMPERATURE
- THRESHOLDS INDEPENDENT OF LED DEGRADATION
- DIELECTRIC WITHSTAND TESTED AT 3000 V dc FOR A WORKING VOLTAGE OF 220 Vac
- RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES, INC. (FILE NO. E55361)

Applications

- LIMIT SWITCH SENSING
- LOW VOLTAGE DETECTOR
- 5V—240V AC/DC VOLTAGE SENSING
- RELAY CONTACT MONITOR
- RELAY COIL VOLTAGE MONITOR
- CURRENT SENSING
- MICROPROCESSOR INTERFACING



Description

The HCPL-3700 is a voltage/current threshold detection optocoupler. This optocoupler uses an internal Light Emitting Diode (LED), a threshold sensing input buffer IC, and a high gain photon detector to provide an optocoupler which permits adjustable external threshold levels. The input buffer circuit has a nominal turn on threshold of 2.5 mA (I_{TH+}) and 3.8 volts (V_{TH+}). The addition of one or more external attenuation resistors permits the use of this device over a wide range of input voltages and currents. Threshold sensing prior to the LED and detector elements minimizes effects of different optical gain and LED variations over operating life (CTR degradation). Hysteresis is also provided in the buffer for extra noise immunity and switching stability.

The buffer circuit is designed with internal clamping diodes to protect the circuitry and LED from a wide range of over-voltage and over-current transients while the diode bridge enables easy use with ac voltage input.

The high gain output stage features an open collector output providing both TTL compatible saturation voltages and CMOS compatible breakdown voltages.

The HCPL-3700, by combining several unique functions in a single package, provides the user with an ideal component for industrial control computer input boards and other applications where a predetermined input threshold optocoupler level is desirable.

Absolute Maximum Ratings (No derating required up to 70°C)

Parameter		Symbol	Min.	Max.	Units	Note
Storage Temperature		T_S	-55	125	°C	
Operating Temperature		T_A	-25	85	°C	
Lead Soldering Cycle	Temperature			260	°C	1
	Time			10	sec	
Input Current	Average	I_{IN}		50	mA	2
	Surge			140		2,3
	Transient			500		
Input Voltage (Pins 2-3)		V_{IN}	-0.5		V	
Input Power Dissipation		P_{IN}		230	mW	4
Total Package Power Dissipation		P		305	mW	5
Output Power Dissipation		P_O		210	mW	6
Output Current	Average	I_O		30	mA	7
Supply Voltage (Pins 8-5)		V_{CC}	-0.5	20	V	
Output Voltage (Pins 6-5)		V_O	-0.5	20	V	

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Note
Supply Voltage	V_{CC}	4.5	18	V	
Operating Temperature	T_A	0	70	°C	
Operating Frequency	f	0	4	KHz	8

Switching Characteristics at T_A = 25°C, V_{CC} = 5.0V

Parameter	Symbol	Min.	Typ.[9]	Max.	Units	Conditions	Fig.	Note
Propagation Delay Time to Logic Low Output Level	t_{PHL}		4.0	15	μs	R_L = 4.7 kΩ, C_L = 30 pF	6,9	10
Propagation Delay Time to Logic High Output Level	t_{PLH}		10.0	40	μs	R_L = 4.7 kΩ, C_L = 30 pF		11
Common Mode Transient Immunity at Logic Low Output Level	CM_L		-600		V/μs	I_{IN} = 3.11 mA, R_L = 4.7 kΩ $V_{O\ max.}$ = 0.8V, V_{CM_L} = 140V	8,10	12,13
Common Mode Transient Immunity at Logic High Output Level	CM_H		4000		V/μs	I_{IN} = 0 mA, R_L = 4.7 kΩ $V_{O\ min}$ = 2.0V, V_{CM_H} = 1400V		
Output Rise Time (10-90%)	t_r		20		μs	R_L = 4.7 kΩ, C_L = 30 pF	7	
Output Fall Time (90-10%)	t_f		0.3		μs	R_L = 4.7 kΩ, C_L = 30 pF		

Electrical Characteristics

Over Recommended Temperature ($0°C \le T_A \le 70°C$) Unless Otherwise Specified

Parameter		Symbol	Min.	Typ.[9]	Max.	Units	Conditions	Fig.	Note
Input Threshold Current		I_{TH+}	1.96	2.5	3.11	mA	$V_{IN}=V_{TH+}$; V_{CC} = 4.5V; V_O = 0.4V; $I_O \ge$ 4.2 mA	2,3	14
		I_{TH-}	1.00	1.3	1.62	mA	$V_{IN} = V_{TH-}$; V_{CC} = 4.5V; V_O = 2.4V; $I_{OH} \le 100\ \mu A$		
Input Threshold Voltage	DC (Pins 2, 3)	V_{TH+}	3.35	3.8	4.05	V	$V_{IN} = V_2 - V_3$; Pins 1 & 4 Open V_{CC} = 4.5V; V_O = 0.4V; $I_O \ge$ 4.2 mA		
		V_{TH-}	2.01	2.6	2.86	V	$V_{IN} = V_2 - V_3$; Pins 1 & 4 Open V_{CC} = 4.5V; V_O = 2.4V; $I_O \le 100\ \mu A$		
	AC (Pins 1, 4)	V_{TH+}	4.23	5.1	5.50	V	$V_{IN} = \lvert V_1 - V_4 \rvert$; Pins 2 & 3 Open V_{CC} = 4.5V; V_O = 0.4V; $I_O \ge$ 4.2 mA		14,15
		V_{TH-}	2.87	3.8	4.24	V	$V_{IN} = \lvert V_1 - V_4 \rvert$; Pins 2 & 3 Open V_{CC} = 4.5V; V_O = 2.4V; $I_O \le 100\ \mu A$		
Hysteresis		I_{HYS}		1.2		mA	$I_{HYS} = I_{TH+} - I_{TH-}$	2	
		V_{HYS}		1.2		V	$V_{HYS} = V_{TH+} - V_{TH-}$		
Input Clamp Voltage		V_{IHC1}	5.4	6.0	6.6	V	$V_{IHC1} = V_2 - V_3$; V_3 = GND; I_{IN} = 10 mA; Pin 1 & 4 Connected to Pin 3	1	
		V_{IHC2}	6.1	6.7	7.3	V	$V_{IHC2} = \lvert V_1 - V_4 \rvert$; $\lvert I_{IN} \rvert$ = 10 mA; Pins 2 & 3 Open		
		V_{IHC3}		12.0	13.4	V	$V_{IHC3} = V_2 - V_3$; V_3 = GND; I_{IN} = 15 mA; Pins 1 & 4 Open		
		V_{ILC}		-0.76		V	$V_{ILC} = V_2 - V_3$; V_3 = GND; I_{IN} = -10 mA		
Input Current		I_{IN}	3.0	3.7	4.4	mA	$V_{IN} = V_2 - V_3$ = 5.0V; Pins 1 & 4 Open	5	
Bridge Diode Forward Voltage		$V_{D1,2}$		0.59			I_{IN} = 3 mA (see schematic)		
		$V_{D3,4}$		0.74					
Logic Low Output Voltage		V_{OL}		0.1	0.4	V	V_{CC} = 4.5V; I_{OL} = 4.2 mA	5	14
Logic High Output Current		I_{OH}			100	μA	$V_{OH} = V_{CC}$ = 18V		
Logic Low Supply Current		I_{CCL}		1.0	4	mA	$V_2 - V_3$ = 5.0V; V_O = Open V_{CC} = 5.0V		
Logic High Supply Current		I_{CCH}		2		nA	V_{CC} = 18V; V_O = Open	4	14
Input-Output Insulation Leakage Current		I_{I-O}			1	μA	Relative Humidity = 45%, T_A = 25°C, V_{I-O} = 3000 Vdc; t = 5 sec.		16, 17
Input-Output Resistance		R_{I-O}		10^{12}		Ω	V_{I-O} = 500 Vdc		16
Input-Output Capacitance		C_{I-O}		0.6		pF	f = 1 MHz, V_{I-O} = 0 Vdc		
Input Capacitance		C_{IN}		50		pF	f=1 MHz; V_{IN}=0V, Pins 2 & 3, Pins 1 & 4 Open		

Notes:

1. Measured at a point 1.6 mm below seating plane.
2. Current into/out of any single lead.
3. Surge input current duration is 3 ms at 120 Hz pulse repetition rate. Transient input current duration is 10 μs at 120 Hz pulse repetition rate. Note that maximum input power, P_{IN}, must be observed.
4. Derate linearly above 70° C free-air temperature at a rate of 4.1 mW/° C. Maximum input power dissipation of 250 mW allows an input IC junction temperature of 125° C at an ambient temperature of T_A = 70° C with a typical thermal resistance from junction to ambient of θ_{JA} = 240° C/W. Excessive P_{IN} and T_J may result in IC chip degradation.
5. Derate linearly above 70° C free-air temperature at a rate of 5.4 mW/° C.
6. Derate linearly above 70° C free-air temperature at a rate of 3.9 mW/° C. Maximum output power dissipation of 210 mW allows an output IC junction temperature of 125° C at an ambient temperature of T_A = 70° C with a typical thermal resistance from junction to ambient of θ_{JA_0} = 265° C/W.
7. Derate linearly above 70° C free-air temperature at a rate of 0.6 mA/° C.
8. Maximum operating frequency is defined when output waveform (Pin 6) obtains only 90% of V_{CC} with R_L = 4.7 kΩ, C_L = 30 pF using a 5V square wave input signal.

9. All typical values are at $T_A = 25°C$, $V_{CC} = 5.0V$ unless otherwise stated.
10. The t_{PHL} propagation delay is measured from the 2.5V level of the leading edge of a 5.0V input pulse (1 μs rise time) to the 1.5V level on the leading edge of the output pulse (see Figure 9).
11. The t_{PLH} propagation delay is measured from the 2.5V level of the trailing edge of a 5.0V input pulse (1 μs fall time) to the 1.5V level on the trailing edge of the output pulse (see Figure 9).
12. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to insure that the output will remain in a Logic High state (i.e., $V_O > 2.0V$). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to insure that the output will remain in a Logic Low state (i.e., $V_O < 0.8V$). See Figure 10.
13. In applications where dV_{CM}/dt may exceed 50,000 V/μs (such as static discharge), a series resistor, R_{CC}, should be included to protect the detector IC from destructively high surge currents. The recommended value for R_{CC} is 240Ω per volt of allowable drop in V_{CC} (between Pin 8 and V_{CC}) with a minimum value of 240Ω.
14. Logic low output level at Pin 6 occurs under the conditions of $V_{IN} \geq V_{TH+}$ as well as the range of $V_{IN} > V_{TH-}$ once V_{IN} has exceeded V_{TH+}. Logic high output level at Pin 6 occurs under the conditions of $V_{IN} \leq V_{TH-}$ as well as the range of $V_{IN} < V_{TH+}$ once V_{IN} has decreased below V_{TH-}.
15. AC voltage is instantaneous voltage.
16. Device considered a two terminal device: pins 1, 2, 3, 4 connected together, and Pins 5, 6, 7, 8 connected together.
17. This is a proof test to validate the UL 220 Vac rating.

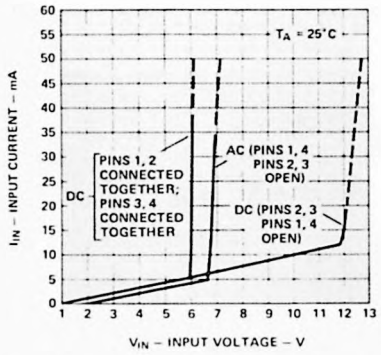


Figure 1. Typical Input Characteristics, I_{IN} vs. V_{IN}. (AC voltage is instantaneous value.)

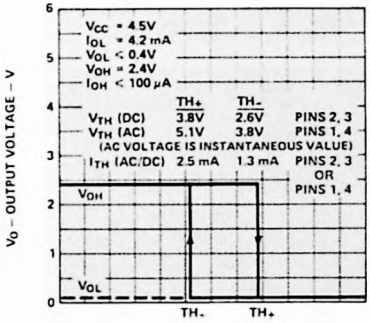


Figure 2. Typical Transfer Characteristics. (AC voltage is instantaneous value.)

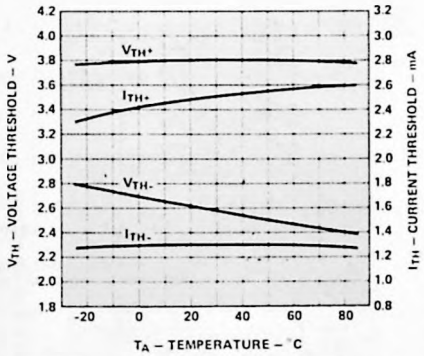


Figure 3. Typical DC Threshold Levels vs. Temperature.

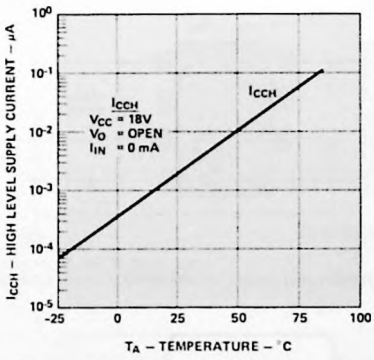


Figure 4. Typical High Level Supply Current, I_{CCH} vs. Temperature.

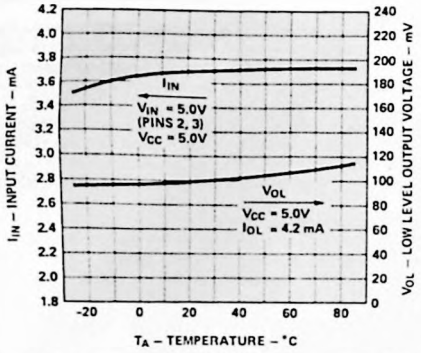


Figure 5. Typical Input Current, I_{IN}, and Low Level Output Voltage, V_{OL}, vs. Temperature.

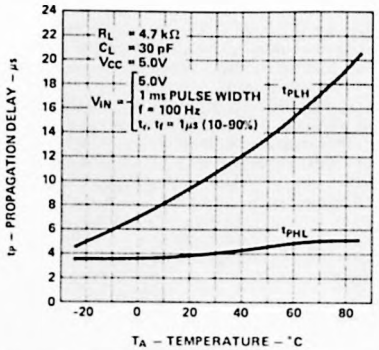


Figure 6. Typical Propagation Delay vs. Temperature.

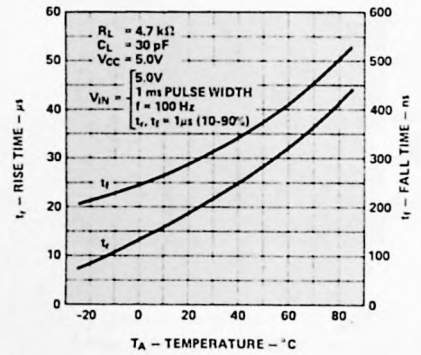


Figure 7. Typical Rise, Fall Times vs. Temperature.

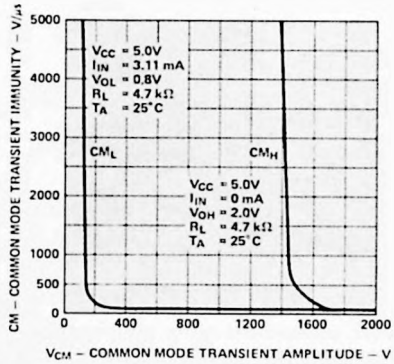
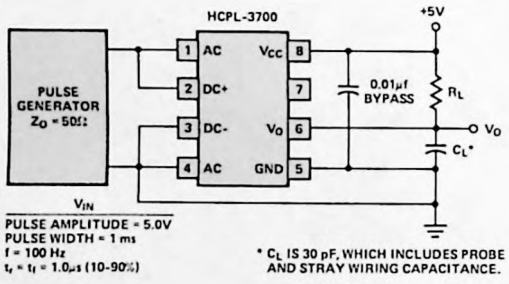


Figure 8. Common Mode Transient Immunity vs. Common Mode Transient Amplitude.



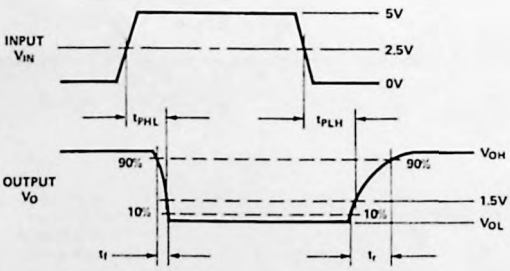
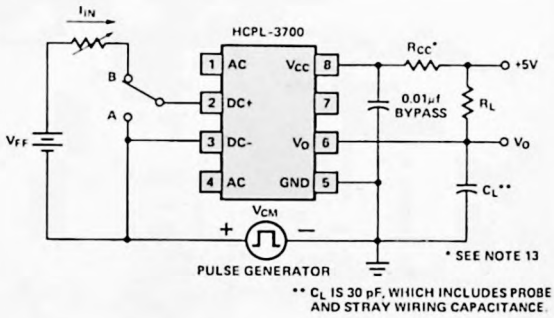


Figure 9. Switching Test Circuit.



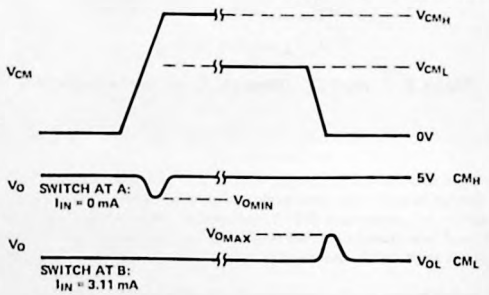


Figure 10. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

Electrical Considerations

The HCPL-3700 optocoupler has internal temperature compensated, predictable voltage and current threshold points which allow selection of an external resistor, R_x, to determine larger external threshold voltage levels. For a desired external threshold voltage, $V_{\pm}$, a corresponding typical value of R_x can be obtained from Figure 11. Specific calculation of R_x can be obtained from Equation (1) of Figure 12. Specification of both V+ and V- voltage threshold levels simultaneously can be obtained by the use of R_x and R_p as shown in Figure 12 and determined by Equations (2) and (3).

R_x can provide over-current transient protection by limiting input current during a transient condition. For monitoring contacts of a relay or switch, the HCPL-3700 in combination with R_x and R_p can be used to allow a specific current to be conducted through the contacts for cleaning purposes (wetting current).

The choice of which input voltage clamp level to choose depends upon the application of this device (see Figure 1). It is recommended that the low clamp condition be used when possible to lower the input power dissipation as well as the LED current, which minimizes LED degradation over time.

In applications where dV_{CM}/dt may be extremely large (such as static discharge), a series resistor, R_{CC}, should be connected in series with V_{CC} and Pin 8 to protect the detector IC from destructively high surge currents. See note 13 for determination of R_{CC}. In addition, it is recommended that a ceramic disc bypass capacitor of 0.01 μf be placed between Pins 8 and 5 to reduce the effect of power supply noise.

For interfacing AC signals to TTL systems, output low pass filtering can be performed with a pullup resistor of 1.5 kΩ and 20 μf capacitor. This application requires a Schmitt trigger gate to avoid slow rise time chatter problems. For AC input applications, a filter capacitor can be placed across the DC input terminals for either signal or transient filtering.

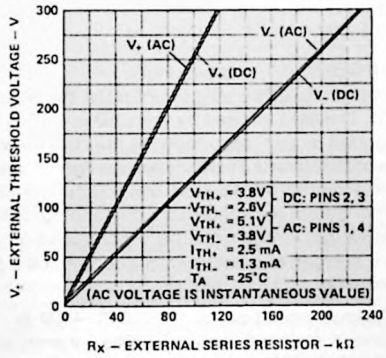


Figure 11. Typical External Threshold Characteristic, $V_{\pm}$ vs. R_X.

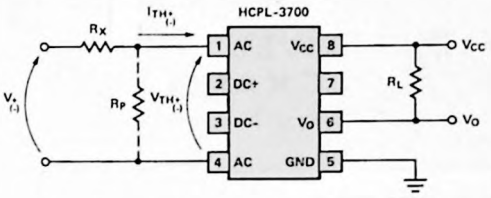


Figure 12. External Threshold Voltage Level Selection.

Either AC (Pins 1, 4) or DC (Pins 2, 3) input can be used to determine external threshold levels.

For one specifically selected external threshold voltage level V+ or V- , R_x can be determined without use of R_p via

$$R_x = \frac{V_{+(-)} - V_{TH+(-)}}{I_{TH+(-)}} \quad (1)$$

For two specifically selected external threshold voltage levels, V+ and V- , the use of R_x and R_p will permit this selection via equations (2), (3) provided the following conditions are met. If the denominator of equation (2) is positive, then

$$\frac{V_+}{V_-} \geq \frac{V_{TH+}}{V_{TH-}} \quad \text{and} \quad \frac{V_+ - V_{TH+}}{V_- - V_{TH-}} < \frac{I_{TH+}}{I_{TH-}}$$

Conversely, if the denominator of equation (2) is negative, then

$$\frac{V_+}{V_-} \leq \frac{V_{TH+}}{V_{TH-}} \quad \text{and} \quad \frac{V_+ - V_{TH+}}{V_- - V_{TH-}} > \frac{I_{TH+}}{I_{TH-}}$$

$$R_x = \frac{V_{TH-}(V_+) - V_{TH+}(V_-)}{I_{TH+}(V_{TH-}) - I_{TH-}(V_{TH+})} \quad (2)$$

$$R_p = \frac{V_{TH-}(V_+) - V_{TH+}(V_-)}{I_{TH+}(V_- - V_{TH-}) + I_{TH-}(V_{TH+} - V_+)} \quad (3)$$

See Application Note 1004 for more information.

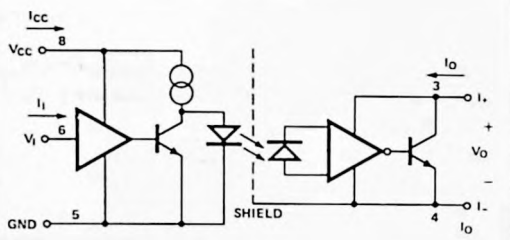
HEWLETT PACKARD

OPTICALLY COUPLED 20 mA CURRENT LOOP TRANSMITTER

HCPL-4100

TECHNICAL DATA JANUARY 1984

SCHEMATIC

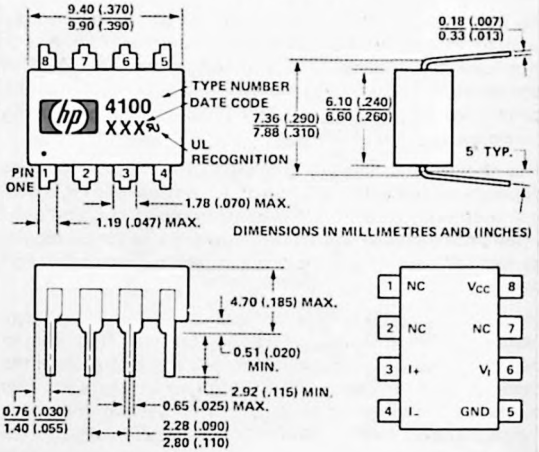


TRUTH TABLE (POSITIVE LOGIC)*

V_I	V_{CC}	I_O
H	ON	H
L	ON	L
H	OFF	H
L	OFF	H

*CURRENT LOOP CONVENTION — H = MARK: $I_O \geq 12$ mA, L = SPACE: $I_O \leq 2$ mA.

OUTLINE DRAWING*



Features

- GUARANTEED 20 mA LOOP PARAMETERS
- DATA INPUT COMPATIBLE WITH LSTTL, TTL AND CMOS LOGIC
- GUARANTEED PERFORMANCE OVER TEMPERATURE (0° C to 70° C)
- INTERNAL SHIELD FOR HIGH COMMON MODE REJECTION
- 20 KBaud DATA RATE AT 400 METRES LINE LENGTH
- GUARANTEED ON AND OFF OUTPUT CURRENT LEVELS
- RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES, INC. (FILE NO. E55361)
- DIELECTRIC WITHSTAND TESTED AT 3000 V dc FOR A WORKING VOLTAGE OF 220 Vac
- OPTICALLY COUPLED 20 mA CURRENT LOOP RECEIVER, HCPL-4200, ALSO AVAILABLE

Applications

- IMPLEMENT AN ISOLATED 20 mA CURRENT LOOP TRANSMITTER IN:
  - Computer Peripherals
  - Industrial Control Equipment
  - Data Communications Equipment

Description

The HCPL-4100 optocoupler is designed to operate as a transmitter in equipment using the 20 mA current loop. 20 mA current loop systems conventionally signal a logic high state by transmitting 20 mA of loop current (MARK), and signal a logic low state by allowing no more than a few milliamperes of loop current (SPACE). Optical coupling of the signal from the logic input to the 20 mA current loop breaks ground loops and provides very high immunity to common mode interference.

The HCPL-4100 data input is compatible with LSTTL, TTL, and CMOS logic gates. The input integrated circuit drives a GaAsP LED. The light emitted by the LED is sensed by a second integrated circuit that allows 20 mA to pass with a voltage drop of less than 2.7 volts when no light is emitted and allows less than 2 mA to pass when light is emitted. The transmitter output is capable of withstanding 27 volts. The input integrated circuit provides a controlled amount of LED drive current and takes into account LED light output degradation.

The Input-Output insulation of the HCPL-4100 is 100% tested at 3000 V dc for 5 seconds. The internal shield allows a guaranteed 1000 V/μs common mode transient immunity.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	4.5	20	Volts
Input Voltage Low	V_{IL}	0	0.8	Volts
Input Voltage High	V_{IH}	2.0	20	Volts
Operating Temperature	T_A	0	70	°C
Output Voltage	V_O	0	27	Volts
Output Current	I_O	0	24	mA

Absolute Maximum Ratings

(No Derating Required up to 55° C)

Storage Temperature ..... -55° C to 125° C
Operating Temperature ..... -40° C to 85° C
Lead Solder Temperature ..... 260° C for 10 sec.
(1.6 mm below seating plane)
Supply Voltage — V_O ..... 0 to 20 V
Average Output Current — I_O ..... -30 mA to 30 mA
Peak Output Current — I_O ..... internally limited
Output Voltage — V_O ..... -0.4 V to 27 V
Input Voltage — V_I ..... -0.5 V to 20 V
Input Power Dissipation — P_I ..... 265 mW[1]
Output Power Dissipation — P_O ..... 125 mW[2]
Total Power Dissipation — P ..... 360 mW[3]

Electrical Characteristics

for 0° C ≤ T_A ≤ 70° C, 4.5 V ≤ V_{CC} ≤ 20 V, all typicals at T_A = 25° C and V_{CC} = 5 V unless otherwise noted

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions		Fig.	Note
Mark State Output Voltage	V_{MO}		1.8 2.2 2.35	2.25 2.7	Volts Volts Volts	I_O = 2 mA I_O = 12 mA I_O = 20 mA	V_I = 2.0 V	1, 2	
Mark State Short Circuit Output Current	I_{SC}	30	85		mA	V_I = 2 V, V_O = 5 V to 27 V			4
Space State Output Current	I_{SO}		1.1	2.0	mA	V_I = 0.8 V, V_O = 27 V		3	
Low Level Input Current	I_{IL}		-0.12	-0.32	mA	V_{CC} = 20 V, V_I = 0.4 V			
Low Level Input Voltage	V_{IL}			0.8	Volts				
High Level Input Voltage	V_{IH}	2.0			Volts				
High Level Input Current	I_{IH}		 0.005	20 100 250	μA μA μA	V_I = 2.7 V V_I = 5.5 V V_I = 20 V			
Supply Current	I_{CC}		7.0 7.8	11.5 13	mA mA	V_{CC} = 5.5 V V_{CC} = 20 V	0 V ≤ V_I ≤ 20 V		
Input-Output Insulation Leakage Current	I_{I-O}			1	μA	Relative Humidity = 45% T_A = 25° C, V_{I-O} = 3000 V dc, t = 5 sec.			5, 6
Resistance (input-output)	R_{I-O}		10^{12}		Ohms	V_{I-O} = 500 V dc			5
Capacitance (input-output)	C_{I-O}		1		pF	f = 1 MHz, V_{I-O} = 0 V dc			5

Notes:
1. Derate linearly above 55° C free air temperature at a rate of 3.8 mW/° C. Proper application of the derating factors will prevent IC junction temperatures from exceeding 125° C for ambient temperatures up to 85° C.
2. Derate linearly above a free-air temperature of 70° C at a rate of 2.3 mW/° C. A significant amount of power may be dissipated in the HCPL-4100 output circuit during the transition from the SPACE state to the MARK state when driving a data line or capacitive load (C_{OUT}). The average power dissipation during the transition can be estimated from the following equation which assumes a linear discharge of a capacitive load: $P = I_{SC}(V_{SO} + V_{MO})/2$, where V_{SO} is the output voltage in the SPACE state. The duration of this transition can be estimated as $t = C_{OUT}(V_{SO} - V_{MO})/I_{SC}$. For typical applications driving twisted pair data lines with NRZ data as shown in Figure 11, the transition time will be less than 10% of one bit time.
3. Derate linearly above 55° C free-air temperature at a rate of 5.1 mW/° C.
4. The maximum current that will flow into the output in the mark state (I_{SC}) is internally limited to protect the device. The duration of the output short circuit shall not exceed 10 ms.
5. The device is considered a two terminal device, pins 1, 2, 3, and 4 are connected together, and pins 5, 6, 7, and 8 are connected together.
6. This is a proof test to validate the UL 220 Vac rating.

Switching Characteristics

for $0 \le T_A \le 70°C$, $4.5\ V \le V_{CC} \le 20\ V$, all typicals at $T_A = 25°C$ and $V_{CC} = 5\ V$ unless otherwise noted

Parameter	Symbol	Min.	Typ.	Max.	Units	Testing Conditions	Fig.	Note
Propagation Delay Time to Logic High Output Level	t_{PLH}		0.3	1.6	μs	$C_O = 1000$ pF, $C_L = 15$ pF, $I_O = 20$ mA	4, 5, 6	7
Propagation Delay Time to Logic Low Output Level	t_{PHL}		0.2	1.0	μs	$C_O = 1000$ pF, $C_L = 15$ pF, $I_O = 20$ mA	4, 5, 6	8
Propagation Delay Time Skew	t_{PLH}-t_{PHL}		0.1		μs	$I_O = 20$ mA		
Output Rise Time (10-90%)	t_r		16		ns	$I_O = 20$ mA, $C_O = 1000$ pF, $C_L = 15$ pF.	5, 7	9
Output Fall Time (90-10%)	t_f		23		ns	$I_O = 20$ mA, $C_O = 1000$ pF, $C_L = 15$ pF.	5, 7	10
Common Mode Transient Immunity at Logic High Output Level	CM_L	-1,000	-10,000		V/μs	$V_I = 2$ V, $T_A = 25°C$ $V_{CM} = 50$ V (peak), $V_{CC} = 5$ V I_O (min.) = 12 mA	8, 9, 10	11
Common Mode Transient Immunity at Logic Low Output Level	CM_H	1,000	10,000		V/μs	$V_I = 0.8$ V, $T_A = 25°C$ $V_{CM} = 50$ V (peak), $V_{CC} = 5$ V I_O (max.) = 3 mA	8, 9, 10	12

Notes:

7. The t_{PLH} propagation delay is measured from the 1.3 volt level on the leading edge of the input pulse to the 10 mA level on the leading edge of the output pulse.
8. The t_{PHL} propagation delay is measured from the 1.3 volt level on the trailing edge of the input pulse to the 10 mA level on the trailing edge of the output pulse.
9. The rise time, t_r, is measured from the 10% to the 90% level on the rising edge of the output current pulse.
10. The fall time, t_f, is measured from the 90% to the 10% level on the falling edge of the output current pulse.
11. The common mode transient immunity in the logic high level is the maximum (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, that can be sustained with the output in a Mark ("H") state (i.e., $I_O > 12$ mA).
12. The common mode transient immunity in the logic low level is the maximum (negative) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, that can be sustained with the output in a Space ("L") state (i.e., $I_O > 3$ mA).

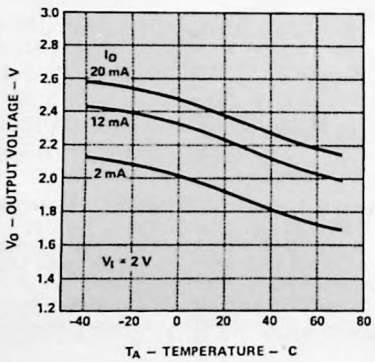


Figure 1. Typical Mark State Output Voltage vs. Temperature

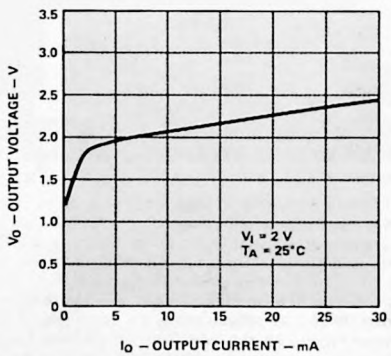


Figure 2. Typical Output Voltage vs. Output Current in Mark State

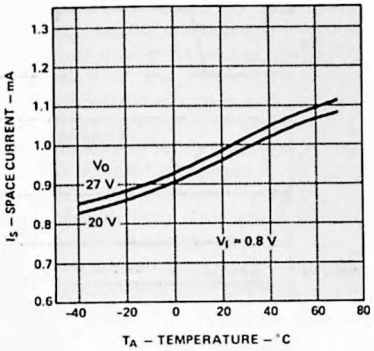


Figure 3. Typical Space State Output Current vs. Temperature

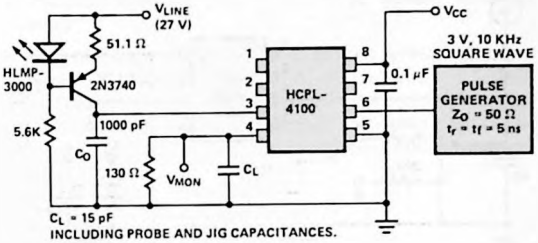


Figure 4. Test Circuit for t_{PLH}, t_{PHL}, t_r, and t_f

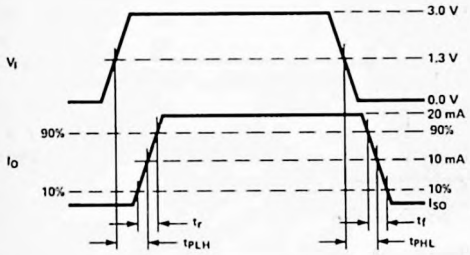


Figure 5. Waveforms for t_{PLH}, t_{PHL}, t_r, and t_f

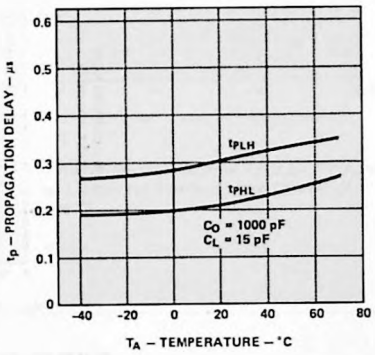


Figure 6. Typical Propagation Delay vs. Temperature

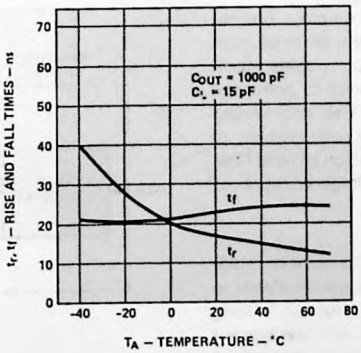


Figure 7. Typical Rise, Fall Times vs. Temperature

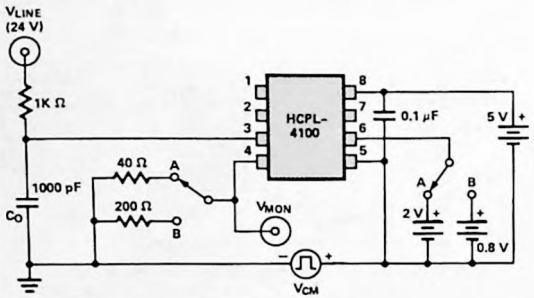


Figure 8. Test Circuit for Common Mode Transient Immunity

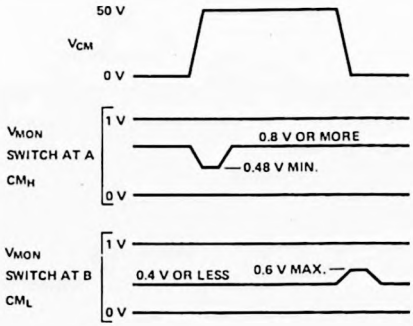


Figure 9. Typical Waveforms for Common Mode Transient Immunity

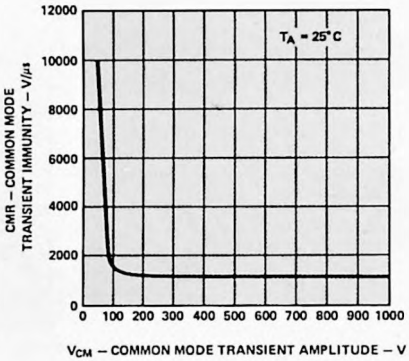


Figure 10. Common Mode Transient Immunity vs. Common Mode Transient Amplitude

Applications

Data transfer between equipment which employs current loop circuits can be accomplished via one of three configurations: simplex, half duplex or full duplex communication. With these configurations, point to point and multidrop arrangements are possible. The appropriate configuration to use depends upon data rate, number of stations, number and length of lines, direction of data flow, protocol, current source location and voltage compliance value, etc.

SIMPLEX

The simplex configuration, whether point to point or multidrop, gives unidirectional data flow from transmitter(s) to receiver. This is the simplest configuration for use in long line length (two wire), moderate data rate, and low current source compliance level applications. A block diagram of simplex point to point arrangement is given in Figure 11 for the HCPL-4100 transmitter optocoupler.

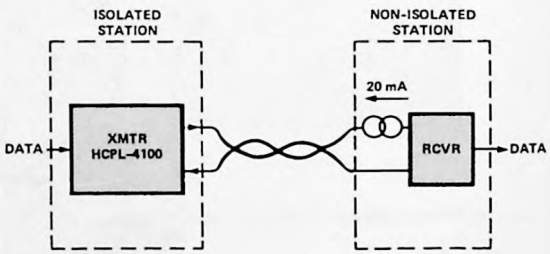


Figure 11. Simplex Point to Point Current Loop System Configuration

Major factors which limit maximum data rate performance for a simplex loop are the location and compliance voltage of the loop current source as well as the total line capacitance. Application of the HCPL-4100 transmitter in a simplex loop necessitates that a non-isolated active receiver (containing current source) be used at the opposite end of the current loop. With long line length, large line capacitance will need to be charged to the compliance voltage level of the current source before the receiver loop current decreases to zero. This effect limits upper data rate performance. Slower data rates will occur with larger compliance voltage levels. The maximum compliance level is determined by the transmitter breakdown characteristic. In addition, adequate compliance of the current source must be available for voltage drops across station(s) during the MARK state in multidrop applications for long line lengths.

In a simplex multidrop application with multiple HCPL-4100 transmitters and one non-isolated active receiver, priority of transmitters must be established.

A recommended non-isolated active receiver circuit which can be used with the HCPL-4100 in point to point or in multidrop 20 mA current loop applications is given in Figure 12. This non-isolated active receiver current threshold must be chosen properly in order to provide adequate noise immunity as well as not to detect SPACE state current (bias current) of the HCPL-4100 transmitter. The receiver input threshold current is Vth/Rth ≈ 10 mA. A simple transistor current source provides a nominal 20 mA loop current over a V_{CC} compliance range of 6 V dc to 27 V dc. A resistor can be used in place of the constant current source for simple applications where the wire loop distance and number of stations on the loop are fixed. A minimum transmitter output load capacitance of 1000 pF is required between pins 3 and 4 to ensure absolute stability.

Length of the current loop (one direction) versus minimum required DC supply voltage, V_{CC}, of the circuit in Figure 12 is graphically illustrated in Figure 13. Multidrop configurations will require larger V_{CC} than Figure 13 predicts in order to account for additional station terminal voltage drops.

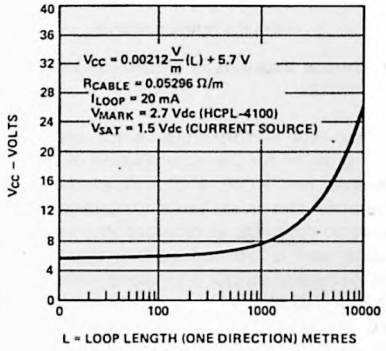


Figure 13. Minimum Required Supply Voltage, V_{CC}, vs. Loop Length for Current Loop Circuit of Figure 12

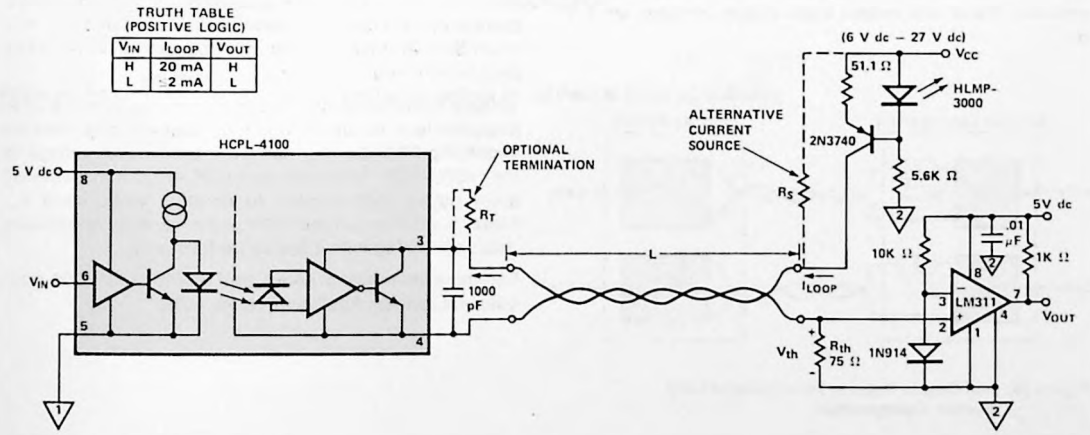


Figure 12. Recommended Non-Isolated Active Receiver with HCPL-4100 Isolated Transmitter for Simplex Point to Point 20 mA Current Loop

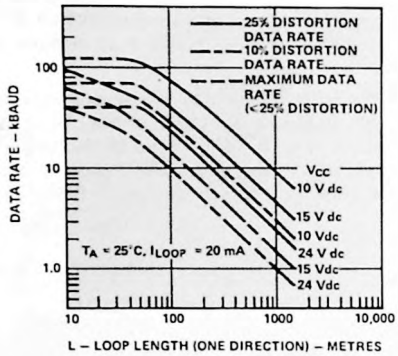


Figure 14. Typical Data Rate vs. Distance and Supply Voltage

Typical data rate performance versus distance is illustrated in Figure 14 for the combination of a non-isolated active receiver and HCPL-4100 optically coupled current loop transmitter shown in Figure 12. Curves are shown for 25% distortion data rate at different V_{CC} values. 25% distortion data rate is defined as that rate at which 25% distortion occurs to output bit interval with respect to the input bit interval. Maximum data rate (dotted line) is restricted by device characteristics. An input Non-Return-to-Zero (NRZ) test waveform of 16 bits (0000001011111101) was used for data rate distortion measurements. Enhanced speed performance of the loop system can be obtained with lower V_{CC} supply levels, as illustrated in Figure 14. In addition, when loop current is supplied through a resistor instead of by a current source, an additional series termination resistance equal to the characteristic line impedance can be used at the HCPL-4100 transmitter end to enhance speed of response by approximately 20%.

The cable used contained five pairs of unshielded, twisted, 22 AWG wire (Dearborn #862205). Loop current is 20 mA nominal. Input and output logic supply voltages are 5 V dc.

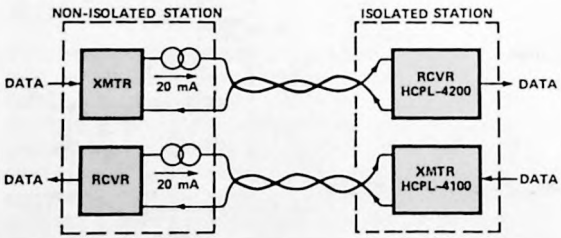


Figure 15. Full Duplex Point to Point Current Loop System Configuration

FULL DUPLEX

Full duplex point to point communication of Figure 15 uses a four wire system to provide simultaneous, bi-directional data communication between local and remote equipment. Basic application uses two simplex point to point loops which have two separate, active, non-isolated units at one common end of the loops. The other end of each loop is isolated.

As Figure 15 illustrates, the combination of Hewlett-Packard current loop optocouplers, HCPL-4100 transmitter and HCPL-4200 receiver, can be used at the isolated end of current loops. Cross talk and common mode coupling are greatly reduced when optical isolation is implemented at the same end of both loops, as shown. Full duplex data rate is limited by the non-isolated active receiver current loop. Comments mentioned under simplex configuration apply to the full duplex case. Consult the HCPL-4200 receiver optocoupler data sheet for specified device performance.

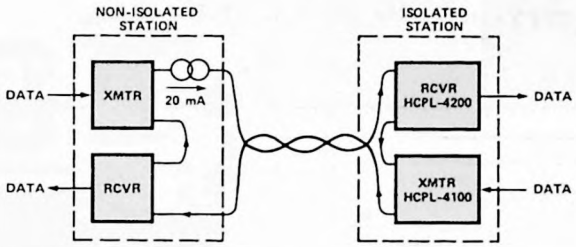
HALF DUPLEX

The half duplex configuration, whether point to point or multidrop, gives non-simultaneous bidirectional data flow from transmitters to receivers shown in Figures 16a and 16b. This configuration allows the use of two wires to carry data back and forth between local and remote units. However, protocol must be used to determine which specific transmitter can operate at any given time. Maximum data rate for a half duplex system is limited by the loop current charging time. These considerations were explained in the Simplex configuration section.

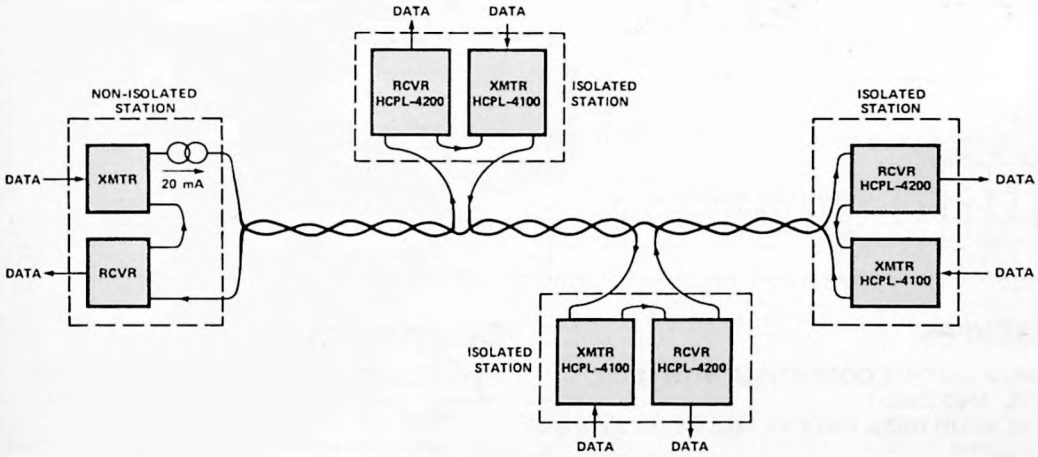
Figures 16a and 16b illustrate half duplex application for the combination of HCPL-4100/-4200 optocouplers. The unique and complementary designs of the HCPL-4100 transmitter and HCPL-4200 receiver optocouplers provide many designed-in benefits. For example, total optical isolation at one end of the current loop is easily accomplished, which results in substantial removal of common mode influences, elimination of ground potential differences and reduction of power supply requirements. With this combination of HCPL-4100/-4200 optocouplers, specific current loop noise immunity is provided, i.e., minimum SPACE state current noise immunity is 1 mA, MARK state noise immunity is 8 mA.

Voltage compliance of the current source must be of an adequate level for operating all units in the loop while not exceeding 27 V dc, the maximum breakdown voltage for the HCPL-4100. Note that the HCPL-4100 transmitter will allow output loop current to conduct when input V_{CC} power is off. Consult the HCPL-4200 receiver optocoupler data sheet for specified device performance.

For more informaton about the HCPL-4100/-4200 optocouplers, consult Application Note 1018.



(a) POINT TO POINT



(b) MULTIDROP

Figure 16. Half Duplex Current Loop System Configurations for (a) Point to Point, (b) Multidrop

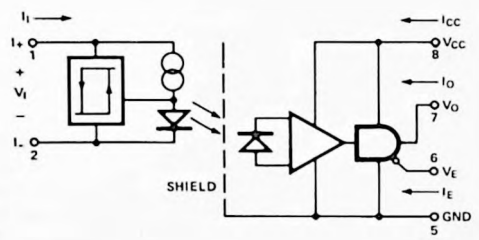
HEWLETT PACKARD

OPTICALLY COUPLED 20 mA CURRENT LOOP RECEIVER

HCPL-4200

TECHNICAL DATA JANUARY 1984

SCHEMATIC



TRUTH TABLE (POSITIVE LOGIC)*

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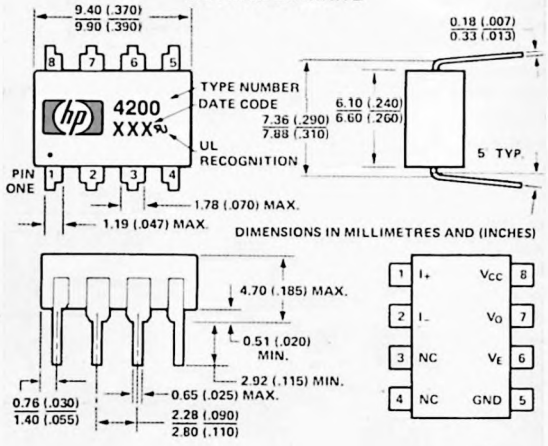
L	H	Z
H	L	H
L	L	L

*CURRENT LOOP CONVENTION – H = MARK: I_I > 12 mA, L = SPACE: I_I < 3 mA, Z = OFF (HIGH IMPEDANCE) STATE.

OUTLINE DRAWING*



Features

- DATA OUTPUT COMPATIBLE WITH LSTTL, TTL, AND CMOS
- 20K BAUD DATA RATE AT 1400 METRES LINE LENGTH
- GUARANTEED PERFORMANCE OVER TEMPERATURE (0° C TO 70° C)
- GUARANTEED ON AND OFF THRESHOLDS
- LED IS PROTECTED FROM EXCESS CURRENT
- INPUT THRESHOLD HYSTERESIS
- THREE-STATE OUTPUT COMPATIBLE WITH DATA BUSES
- INTERNAL SHIELD FOR HIGH COMMON MODE REJECTION
- RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES, INC. (FILE NO. E55361)
- DIELECTRIC WITHSTAND TESTED AT 3000 V dc FOR A WORKING VOLTAGE OF 220 Vac
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  - Industrial Control Equipment
  - Data Communications Equipment

Description

The HCPL-4200 optocoupler is designed to operate as a receiver in equipment using the 20 mA Current Loop. 20 mA current loop systems conventionally signal a logic high state by transmitting 20 mA of loop current (MARK), and signal a logic low state by allowing no more than a few milliamperes of loop current (SPACE). Optical coupling of the signal from the 20 mA current loop to the logic output breaks ground loops and provides for a very high common mode rejection. The HCPL-4200 aids in the design process by providing guaranteed thresholds for logic high state and logic low state for the current loop, providing an LSTTL, TTL, or CMOS compatible logic interface, and providing guaranteed common mode rejection. The buffer circuit on the current loop side of the HCPL-4200 provides typically 0.8 mA of hysteresis which increases the immunity to common mode and differential mode noise. The buffer also provides a controlled amount of LED drive current which takes into account LED light output degradation.

Input-Output insulation of the HCPL-4200 is 100% tested at 3000 V dc for 5 seconds. The internal shield allows a guaranteed 1000 V/μs common mode transient immunity.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	4.5	20	Volts
Forward Input Current (SPACE)	I_{SI}	0	2.0	mA
Forward Input Current (MARK)	I_{MI}	14	24	mA
Operating Temperature	T_A	0	70	°C
Fan Out	N	0	4	TTL Loads
Logic Low Enable Voltage	V_{EL}	0	0.8	Volts
Logic High Enable Voltage	V_{EH}	2.0	20	Volts

Absolute Maximum Ratings

(No Derating Required up to 70° C)

Storage Temperature ..... —55° C to 125° C
Operating Temperature ..... —40° C to 85° C
Lead Solder Temperature ..... 260° C for 10 sec.
(1.6 mm below the seating plane)
Supply Voltage — V_{CC} ..... 0 V to 20 V
Average Input Current — I_I ..... —30 mA to 30 mA
Peak Transient Input Current — I_I ..... 0.5 A[1]
Enable Input Voltage — V_E ..... —0.5 V to 20 V
Output Voltage — V_O ..... —0.5 V to 20 V
Average Output Current — I_O ..... 25 mA
Input Power Dissipation — P_I ..... 90 mW[2]
Output Power Dissipation — P_O ..... 210 mW[3]
Total Power Dissipation — P ..... 255 mW[4]

Electrical Characteristics

For 0° C ≤ T_A ≤ 70° C, 4.5 V ≤ V_{CC} ≤ 20 V, V_E = 0.8 V, all typicals at T_A = 25° C and V_{CC} = 5 V unless otherwise noted

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions		Fig.	Note
Mark State Input Current	I_{MI}	12			mA			1, 2, 3	
Mark State Input Voltage	V_{MI}		2.52	2.75	Volts	I_I = 20 mA	V_E = Don't Care	3, 4	
Space State Input Current	I_{SI}			3	mA			1, 2, 3	
Space State Input Voltage	V_{SI}		1.6	2.2	Volts	I_I = 2 mA	V_E = Don't Care	1, 3	
Input Hysteresis Current	I_{HYS}	0.3	0.8		mA			1	
Logic Low Output Voltage	V_{OL}			0.5	Volts	I_{OL} = 6.4 mA (4 TTL Loads) I_I = 3 mA		5	
Logic High Output Voltage	V_{OH}	2.4			Volts	I_{OH} = -2.6 mA,	I_I = 12 mA	6	
Output Leakage Current (V_{OUT} > V_{CC})	I_{OHH}			100	μA	V_O = 5.5 V	I_I = 20 mA		
				500	μA	V_O = 20 V	V_{CC} = 4.5 V		
Logic High Enable Voltage	V_{EH}	2.0			Volts				
Logic Low Enable Voltage	V_{EL}			0.8	Volts				
Logic High Enable Current	I_{EH}			20	μA	V_E = 2.7 V			
				100	μA	V_E = 5.5 V			
			.004	250	μA	V_E = 20 V			
Logic Low Enable Current	I_{EL}			-0.32	mA	V_E = 0.4 V			
Logic Low Supply Current	I_{CCL}		4.5	6.0	mA	V_{CC} = 5.5 V	I_I = 0 mA		
			5.25	7.5	mA	V_{CC} = 20 V	V_E = Don't Care		
Logic High Supply Current	I_{CCH}		2.7	4.5	mA	V_{CC} = 5.5 V	I_I = 20 mA		
			3.1	6.0	mA	V_{CC} = 20 V	V_E = Don't Care		
High Impedance State Output Current	I_{OZL}			-20	μA	V_O = 0.4 V	V_E = 2.0 V, I_I = 20 mA		
	I_{OZH}			20	μA	V_O = 2.4 V	V_E = 2 V, I_I = 0 mA		
				100	μA	V_O = 5.5 V			
				500	μA	V_O = 20 V			
Logic Low Short Circuit Output Current	I_{OSL}	25			mA	V_O = V_{CC} = 5.5 V	I_I = 0 mA		5
		40			mA	V_O = V_{CC} = 20 V			
Logic High Short Circuit Output Current	I_{OSH}	-10			mA	V_{CC} = 5.5 V	I_I = 20 mA		5
		-25			mA	V_{CC} = 20 V	V_O = GND		
Input-Output Insulation Leakage Current	I_{I-O}			1	μA	V_{I-O} = 3000 V dc T_A = 25° C, t = 5s Relative Humidity = 45%			6, 7
Input-Output Resistance	R_{I-O}		10^{12}		ohms	V_{I-O} = 500 V dc			6
Input-Output Capacitance	C_{I-O}		1.0		pF	f = 1 MHz, V_{I-O} = 0 V dc			6
Input Capacitance	C_{IN}		120		pF	f = 1 MHz, V_I = 0 V dc, Pins 1 and 2			

Switching Characteristics

For $0°C \le T_A \le 70°C$, $4.5\ V \le V_{CC} \le 20\ V$, $V_E = 0.8\ V$, all typicals at $T_A = 25°C$ and $V_{CC} = 5\ V$ unless otherwise noted

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic High Output Level	t_{PLH}		0.23	1.6	μs	$V_E = 0\ V$, $C_L = 15\ pF$	7, 8, 9	8
Propagation Delay Time to Logic Low Output Level	t_{PHL}		0.17	1.0	μs	$V_E = 0\ V$, $C_L = 15\ pF$	7, 8, 9	9
Propagation Delay Time Skew	t_{PLH}-t_{PHL}		60		ns	$I_I = 20\ mA$, $C_L = 15\ pF$	7, 8, 9	
Output Enable Time to Logic Low Level	t_{PZL}		25		ns	$I_I = 0\ mA$, $C_L = 15\ pF$	11, 12, 14	
Output Enable Time to Logic High Level	t_{PZH}		28		ns	$I_I = 20\ mA$, $C_L = 15\ pF$	11, 12, 13	
Output Disable Time from Logic Low Level	t_{PLZ}		60		ns	$I_I = 0\ mA$, $C_L = 15\ pF$	11, 12, 14	
Output Disable Time from Logic High Level	t_{PHZ}		105		ns	$I_I = 20\ mA$, $C_L = 15\ pF$	11, 12, 13	
Output Rise Time (10-90%)	t_r		55		ns	$V_{CC} = 5\ V$, $C_L = 15\ pF$	7, 8, 10	10
Output Fall Time (90-10%)	t_f		15		ns	$V_{CC} = 5\ V$, $C_L = 15\ pF$	7, 8, 10	11
Common Mode Transient Immunity at Logic High Output Level	CM_H	-1,000	-10,000		V/μs	$V_{CM} = 50\ V$ (peak) $I_I = 12\ mA$, $T_A = 25°C$	15, 16	12
Common Mode Transient Immunity at Logic Low Output Level	CM_L	1,000	10,000		V/μs	$V_{CM} = 50\ V$ (peak) $I_I = 3\ mA$, $T_A = 25°C$	15, 16	13

NOTES:

1. ≤ 1 μs pulse width, 300 pps.
2. Derate linearly above 70° C free air temperature at a rate of 1.6 mW/° C. Proper application of the derating factors will prevent IC junction temperatures from exceeding 125° C for ambient temperatures up to 85° C.
3. Derate linearly above 70° C free air temperature at a rate of 3.8 mW/° C.
4. Derate linearly above 70° C free air temperature at a rate of 4.6 mW/° C.
5. Duration of output short circuit time shall not exceed 10 ms.
6. The device is considered a two terminal device, pins 1, 2, 3, and 4 are connected together and pins 5, 6, 7, and 8 are connected together.
7. This is a proof test to validate the UL 220 Vac rating.
8. The t_{PLH} propagation delay is measured from the 10 mA level on the leading edge of the input pulse to the 1.3 V level on the leading edge of the output pulse.
9. The t_{PHL} propagation delay is measured from the 10 mA level on the trailing edge of the input pulse to the 1.3 V level on the trailing edge of the output pulse.
10. The rise time, t_r, is measured from the 10% to the 90% level on the rising edge of the output logic pulse.
11. The fall time, t_f, is measured from the 90% to the 10% level on the falling edge of the output logic pulse.
12. Common mode transient immunity in the logic high level is the maximum (negative) dV_{CM}/dt on the trailing edge of the common mode pulse, V_{CM}, which can be sustained with the output voltage in the logic high state (i.e., $V_O \ge 2\ V$).
13. Common mode transient immunity in the logic low level is the maximum (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, which can be sustained with the output voltage in the logic low state (i.e., $V_O \le 0.8\ V$).

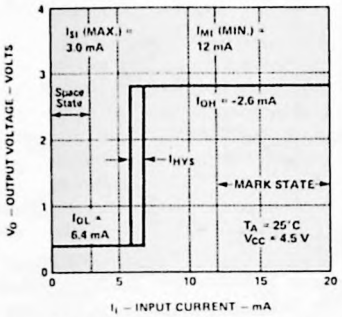


Figure 1. Typical Output Voltage vs. Loop Current

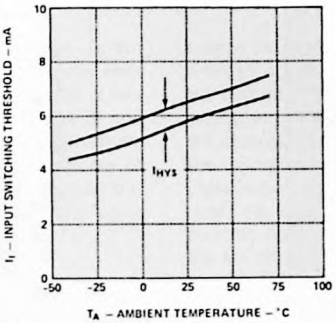


Figure 2. Typical Current Switching Threshold vs. Temperature

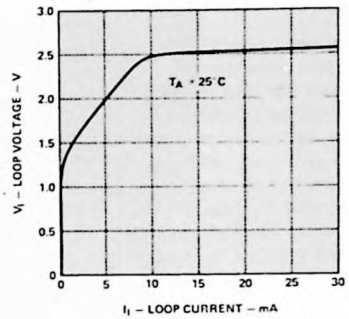


Figure 3. Typical Input Loop Voltage vs. Input Current

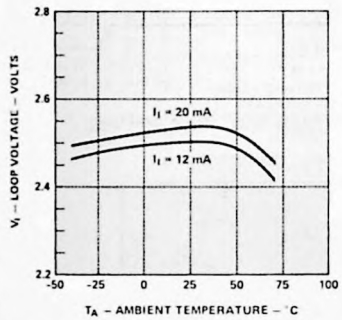


Figure 4. Typical Input Voltage vs. Temperature

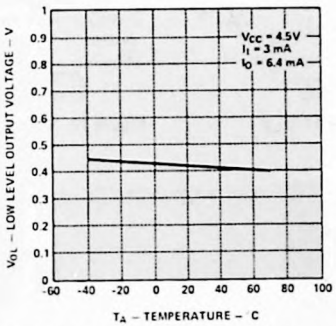


Figure 5. Typical Logic Low Output Voltage vs. Temperature

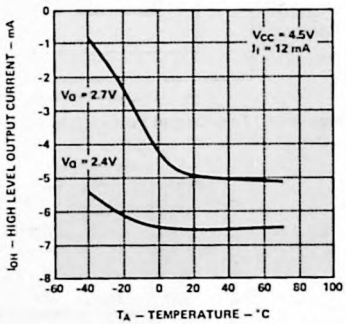


Figure 6. Typical Logic High Output Current vs. Temperature

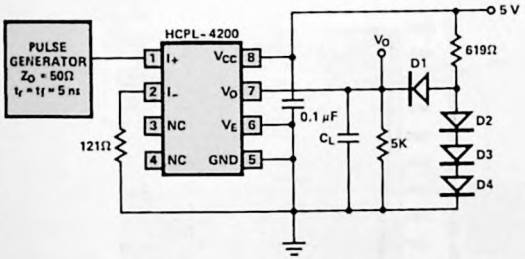


Figure 7. Test Circuit for t_{PHL}, t_{PLH}, t_r, and t_f

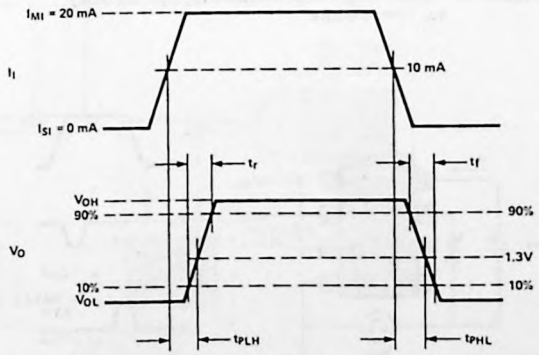


Figure 8. Waveforms for t_{PHL}, t_{PLH}, t_r, and t_f

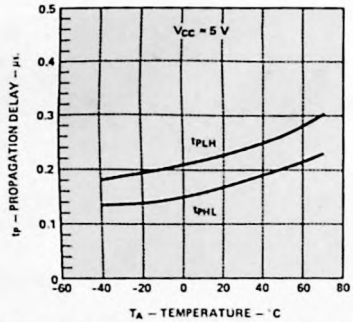


Figure 9. Typical Propagation Delay vs. Temperature

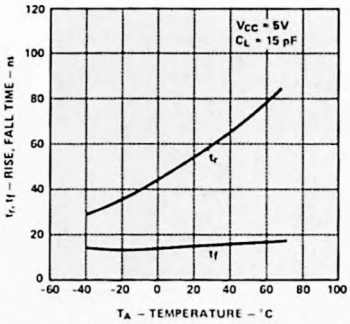


Figure 10. Typical Rise, Fall Time vs. Temperature

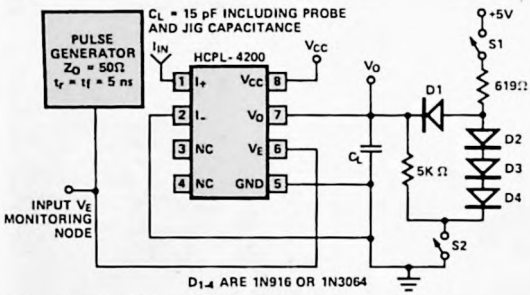


Figure 11. Test Circuit for t_{PZH}, t_{PZL}, t_{PHZ}, and t_{PLZ}

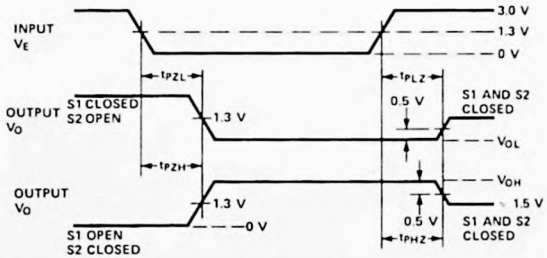


Figure 12. Waveforms for t_{PZH}, t_{PZL}, t_{PHZ}, and t_{PLZ}

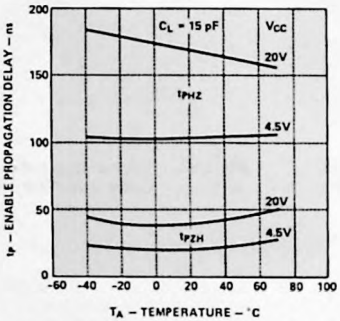


Figure 13. Typical Logic High Enable Propagation Delay vs. Temperature

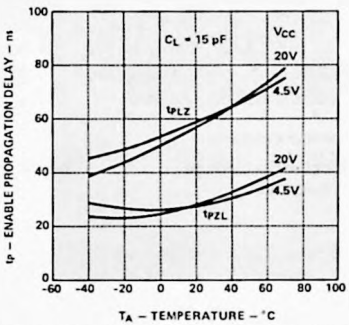


Figure 14. Typical Logic Low Enable Propagation Delay vs. Temperature

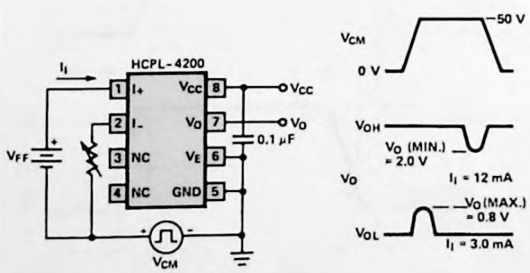


Figure 15. Test Circuit for Common Mode Transient Immunity

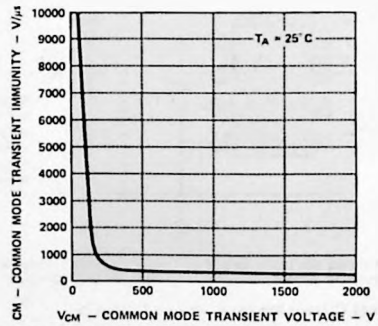


Figure 16. Typical Common Mode Transient Immunity vs. Common Mode Transient Amplitude

Applications

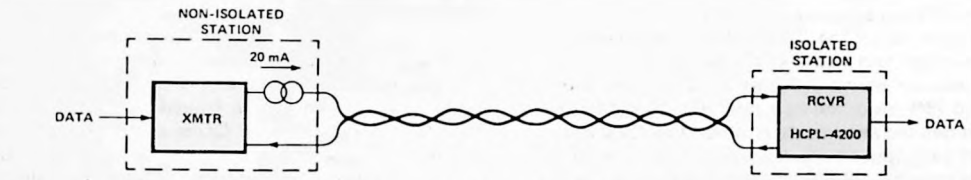
Data transfer between equipment which employs current loop circuits can be accomplished via one of three configurations: simplex, half duplex or full duplex communication. With these configurations, point-to-point and multidrop arrangements are possible. The appropriate configuration to use depends upon data rate, number of stations, number and length of lines, direction of data flow, protocol, current source location and voltage compliance value, etc.

SIMPLEX

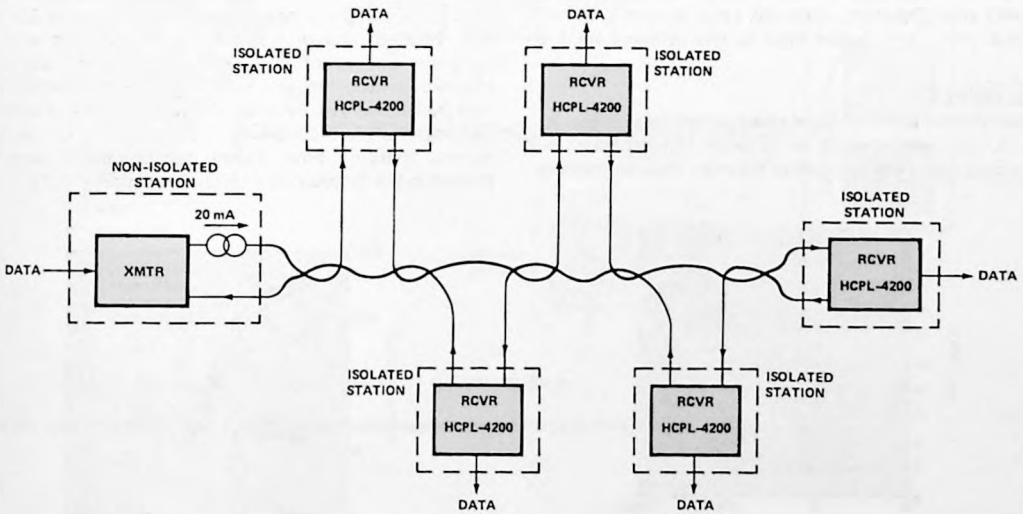
The simplex configuration, whether point to point or multidrop, gives unidirectional data flow from transmitter to receiver(s). This is the simplest configuration for use in long line length (two wire), for high data rate, and low current source compliance level applications. Block diagrams of simplex point-to-point and multidrop arrangements are given in Figures 17a and 17b respectively for the HCPL-4200 receiver optocoupler.

For the highest data rate performance in a current loop, the configuration of a non-isolated active transmitter (containing current source) transmitting data to a remote isolated receiver(s) should be used. When the current source is located at the transmitter end, the loop is charged approximately to V_{MI} (2.5 V). Alternatively, when the current source is located at the receiver end, the loop is charged to the full compliance voltage level. The lower the charged voltage level the faster the data rate will be. In the configurations of Figures 17a and 17b, data rate is independent of the current source voltage compliance level. An adequate compliance level of current source must be available for voltage drops across station(s) during the MARK state in multidrop applications or for long line length. The maximum compliance level is determined by the transmitter breakdown characteristic.

A recommended non-isolated active transmitter circuit which can be used with the HCPL-4200 in point-to-point or in multidrop 20 mA current loop applications is given in Figure 18. The current source is controlled via a standard TTL 7407 buffer to provide high output impedance of current source in both the ON and OFF states. This non-isolated active transmitter provides a nominal 20 mA loop current for the listed values of V_{CC}, R2 and R3 in Figure 18.



(a) POINT-TO-POINT



(b) MULTIDROP

Figure 17. Simplex Current Loop System Configurations for (a) Point-to-Point, (b) Multidrop

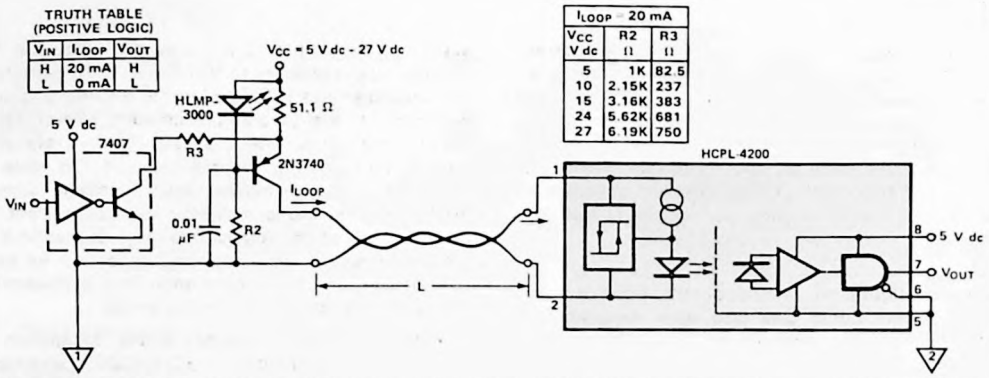


Figure 18. Recommended Non-Isolated Active Transmitter with HCPL-4200 Isolated Receiver for Simplex Point-to-Point 20 mA Current Loop

Length of current loop (one direction) versus minimum required DC supply voltage, V_{CC}, of the circuit in Figure 18 is graphically illustrated in Figure 19. Multidrop configurations will require larger V_{CC} than Figure 19 predicts in order to account for additional station terminal voltage drops.

Typical data rate performance versus distance is illustrated in Figure 20 for the combination of a non-isolated active transmitter and HCPL-4200 optically coupled current loop receiver shown in Figure 18. Curves are shown for 10% and 25% distortion data rate. 10% (25%) distortion data rate is defined as that rate at which 10% (25%) distortion occurs to output bit interval with respect to input bit interval. An input Non-Return-to-Zero (NRZ) test waveform of 16 bits (0000001011111101) was used for data rate distortion measurements. Data rate is independent of current source supply voltage, V_{CC}.

The cable used contained five pairs of unshielded, twisted, 22 AWG wire (Dearborn #862205). Loop current is 20 mA nominal. Input and output logic supply voltages are 5 V dc.

FULL DUPLEX

The full duplex point-to-point communication of Figure 21 uses a four wire system to provide simultaneous, bi-directional data communication between local and remote equipment. The basic application uses two simplex point-to-point loops which have two separate, active, non-isolated units at one common end of the loops. The other end of each loop is isolated.

As Figure 21 illustrates, the combination of Hewlett-Packard current loop optocouplers, HCPL-4100 transmitter and HCPL-4200 receiver, can be used at the isolated end of current loops. Cross talk and common mode coupling are greatly reduced when optical isolation is implemented at the same end of both loops, as shown. The full duplex data rate is limited by the non-isolated active receiver current loop. Comments mentioned under simplex configuration apply to the full duplex case. Consult the HCPL-4100 transmitter optocoupler data sheet for specified device performance.

HALF DUPLEX

The half duplex configuration, whether point-to-point or multidrop, gives non-simultaneous bidirectional data flow from transmitters to receivers shown in Figures 22a and 22b. This configuration allows the use of two wires to carry data back and forth between local and remote units. However, protocol must be used to determine which specific transmitter can operate at any given time. Maximum data rate for a half duplex system is limited by the loop current charging time. These considerations were explained in the Simplex configuration section.

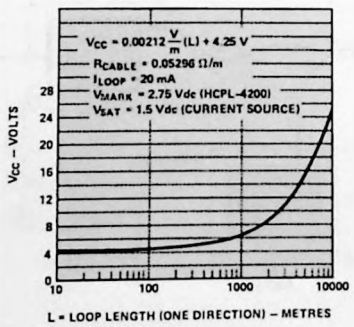


Figure 19. Minimum Required Supply Voltage, V_{CC}, vs. Loop Length for Current Loop Circuit of Figure 18

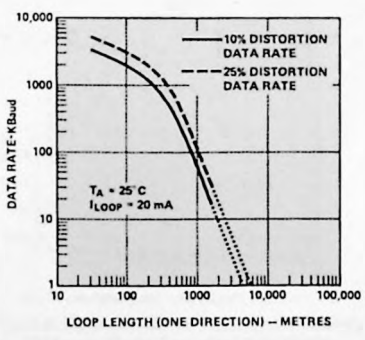


Figure 20. Typical Data Rate vs. Distance

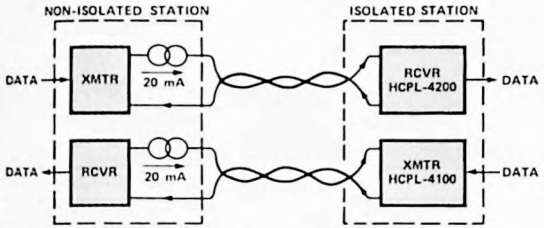


Figure 21. Full Duplex Point-to-Point Current Loop System Configuration

Figures 22a and 22b illustrate half duplex application for the combination of HCPL-4100/-4200 optocouplers. The unique and complementary designs of the HCPL-4100 transmitter and HCPL-4200 receiver optocouplers provide many designed-in benefits. For example, total optical isolation at one end of the current loop is easily accomplished, which results in substantial removal of common mode influences, elimination of ground potential differences and reduction of power supply requirements. With this combination of HCPL-4100/-4200 optocouplers, specific current loop noise immunity is provided, i.e., minimum SPACE state current noise immunity is 1 mA, MARK state noise immunity is 8 mA.

Voltage compliance of the current source must be of an adequate level for operating all units in the loop while not exceeding 27 V dc, the maximum breakdown voltage for the HCPL-4100. Note that the HCPL-4100 transmitter will allow loop current to conduct when input V_{CC} power is off. Consult the HCPL-4100 transmitter optocoupler data sheet for specified device performance.

For more information about the HCPL-4100/-4200 optocouplers, consult Application Note 1018.

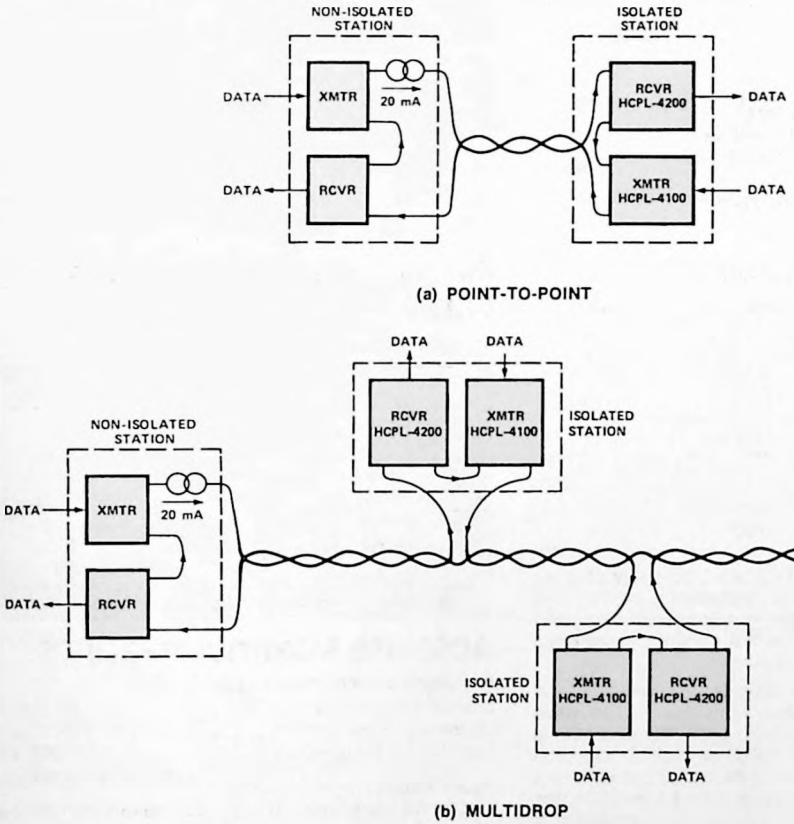


Figure 22. Half Duplex Current Loop System Configurations for (a) Point-to-Point, (b) Multidrop

HEWLETT PACKARD

DUAL CHANNEL HERMETICALLY SEALED OPTOCOUPLER

6N134

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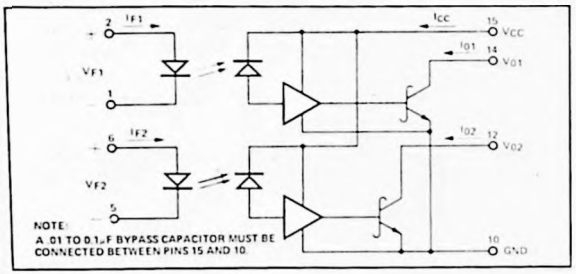


Features

- HERMETICALLY SEALED
- HIGH SPEED
- PERFORMANCE GUARANTEED OVER -55°C TO +125°C AMBIENT TEMPERATURE RANGE
- STANDARD HIGH RELIABILITY SCREENED PARTS AVAILABLE
- TTL COMPATIBLE INPUT AND OUTPUT
- HIGH COMMON MODE REJECTION
- DUAL-IN-LINE PACKAGE
- 1500 VDC WITHSTAND TEST VOLTAGE
- EIA REGISTRATION
- HIGH RADIATION IMMUNITY

Applications

- Logic Ground Isolation
- Line Receiver
- Computer - Peripheral Interface
- Vehicle Command/Control Isolation
- High Reliability Systems
- System Test Equipment Isolation

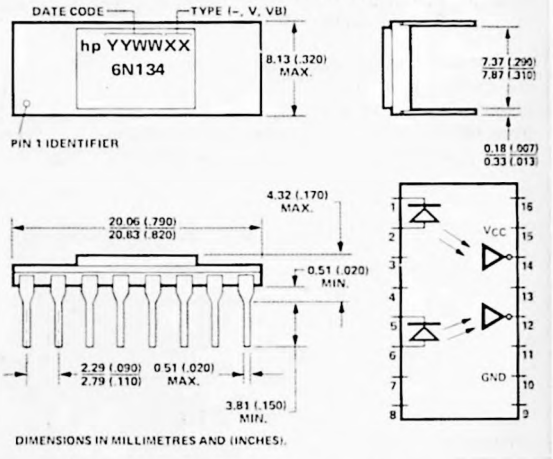
Description

The 6N134 consists of a pair of inverting optically coupled gates, each with a light emitting diode and a unique high gain integrated photon detector in a hermetically sealed ceramic package. The output of the detector is an open collector Schottky clamped transistor.

This unique dual coupler design provides maximum DC and AC circuit isolation between each input and output while achieving TTL circuit compability. The isolator operational parameters are guaranteed from −55° C to +125° C, such that a minimum input current of 10 mA in each channel will sink a six gate fanout (10 mA) at the output with 4.5 to 5.5 V Vcc applied to the detector. This isolation and coupling is achieved with a typical propagation delay of 55 nsec.

Hewlett-Packard's new high reliability part type 8102801EC meets Class B testing requirements of MIL-STD-883. This part is the recommended and preferred device from the 6N134 product family for use in high reliability applications. Details of the 8102801EC test program may be seen in the data sheet for this part. The 6N134TXV and 6N134TXVB parts remain available. For further information on these parts contact your field salesman.

OUTLINE DRAWING*



DIMENSIONS IN MILLIMETRES AND (INCHES).

Recommended Operating Conditions

TABLE I

	Sym.	Min.	Max.	Units
Input Current, Low Level Each Channel	I_{FL}	0	250	μA
Input Current, High Level Each Channel	I_{FH}	12.5†	20	mA
Supply Voltage	V_{CC}	4.5	5.5	V
Fan Out (TTL Load) Each Channel	N		6	
Operating Temperature	T_A	−55	125	°C

Absolute Maximum Ratings*

(No derating required up to 125°C)

Storage Temperature ..... -65°C to +150°C
Operating Temperature ..... -55°C to +125°C
Lead Solder Temperature ..... 260°C for 10s (1.6mm below seating plane)
Peak Forward Input Current (each channel) ..... 40 mA (≤ 1 ms Duration)
Average Input Forward Current (each channel) ..... 20 mA
Input Power Dissipation (each channel) ..... 35 mW
Reverse Input Voltage (each channel) 5V
Supply Voltage - V_{CC} ..... 7V (1 minute maximum)
Output Current - I_O (each channel) ..... 25 mA
Output Power Dissipation (each channel) ..... 40 mW
Output Voltage - V_O (each channel) 7V
Total Power Dissipation (both channels) ..... 350 mW

†12.5 mA condition permits at least 20% CTR degradation guardband. Initial switching threshold is 10mA or less.

*JEDEC Registered Data

TABLE II

Electrical Characteristics

OVER RECOMMENDED TEMPERATURE (T_A = –55°C TO +125°C) UNLESS OTHERWISE NOTED

Parameter	Symbol	Min.	Typ.**	Max.	Units	Test Conditions	Figure	Note
High Level Output Current	I_{OH}*		5	250	μA	V_{CC} = 5.5V, V_O = 5.5V, I_F = 250μA		1
Low Level Output Voltage	V_{OL}*		0.5	0.6	V	V_{CC} = 5.5V, I_F = 10mA I_{OL} (Sinking) = 10mA	4	1, 9
High Level Supply Current	I_{CCH}*		18	28	mA	V_{CC} = 5.5V, I_F = 0 (Both Channels)		
Low Level Supply Current	I_{CCL}*		26	36	mA	V_{CC} = 5.5V, I_F = 20mA (Both Channels)		
Input Forward Voltage	V_F*		1.5	1.75	V	I_F = 20 mA, T_A = 25°C	1	1
	V_F			1.85	V	I_F = 20 mA	1	1
Input Reverse Breakdown Voltage	BV_R*	5			V	I_R = 10μA, T_A = 25°C		1
Input-Output Leakage Current	I_{I-O}*			1.0	μA	V_{I-O} = 1500Vdc, Relative Humidity = 45% T_A = 25°C, t = 5s		2
Propagation Delay Time to High Output Level	t_{PLH}*		65	90	ns	R_L = 510Ω, C_L = 15pF, I_F = 13mA, T_A = 25°C	2,3	1, 5
Propagation Delay Time to Low Output Level	t_{PHL}*		55	90	ns	R_L = 510Ω, C_L = 15pF I_F = 13mA, T_A = 25°C	2,3	1, 6

**All typical values are at V_{CC} = 5V, T_A = 25°C

TABLE III

Typical Characteristics AT T_A = 25°C, V_{CC} = 5V EACH CHANNEL

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Input Capacitance	C_{IN}		60		pF	V_F = 0, f = 1MHz		1
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		-1.9		mV/°C	I_F = 20mA		1
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	V_{I-O} = 500V		3
Capacitance (Input-Output)	C_{I-O}		1.7		pF	f = 1MHz		3
Input-Input Leakage Current	I_{I-I}		0.5		nA	Relative Humidity = 45% V_{I-I} = 500V, t = 5s		4
Resistance (Input-Input)	R_{I-I}		10^{12}		Ω	V_{I-I} = 500V		4
Capacitance (Input-Input)	C_{I-I}		0.55		pF	f = 1MHz		4
Output Rise Time (10-90%)	t_r		35		ns	R_L = 510Ω, C_L = 15pF I_F = 13mA		1
Output Fall Time (90-10%)	t_f		35		ns			
Common Mode Transient Immunity at High Output Level	CM_H		100		V/μs	V_{CM} = 10V (peak), V_O (min.) = 2V, R_L = 510Ω, I_F = 0mA	6	1, 7
Common Mode Transient Immunity at Low Output Level	CM_L		-400		V/μs	V_{CM} = 10V (peak), V_O (max.) = 0.8V R_L = 510Ω, I_F = 10mA	6	1, 8

NOTES:

1. Each channel.
2. Measured between pins 1 through 8 shorted together and pins 9 through 16 shorted together.
3. Measured between pins 1 and 2 or 5 and 6 shorted together, and pins 9 through 16 shorted together.
4. Measured between pins 1 and 2 shorted together, and pins 5 and 6 shorted together.
5. The t_{PLH} propagation delay is measured from the 6.5mA point on the trailing edge of the input pulse to the 1.5V point on the trailing edge of the output pulse.
6. The t_{PHL} propagation delay is measured from the 6.5mA point on the leading edge of the input pulse to the 1.5V point on the leading edge of the output pulse.
7. CM_H is the max. tolerable common mode transient to assure that the output will remain in a high logic state (i.e., V_O > 2.0V).
8. CM_L is the max. tolerable common mode transient to assure that the output will remain in a low logic state (i.e., V_O < 0.8V).
9. It is essential that a bypass capacitor (.01 to 0.1μF, ceramic) be connected from pin 10 to pin 15. Total lead length between both ends of the capacitor and the isolator pins should not exceed 20mm.

JEDEC Registered Data.

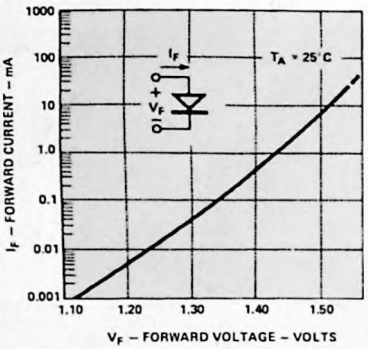


Figure 1. Input Diode Forward Characteristic

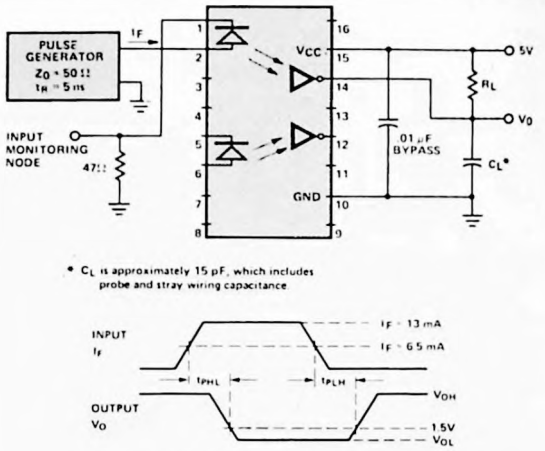


Figure 2. Test Circuit for t_{PHL} and t_{PLH}*

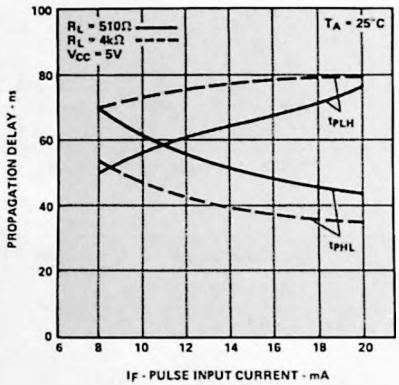


Figure 3. Propagation Delay, t_{PHL} and t_{PLH} vs. Pulse Input Current, I_{FH}

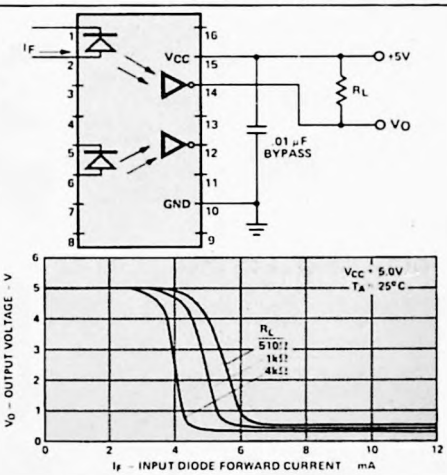


Figure 4. Input-Output Characteristics

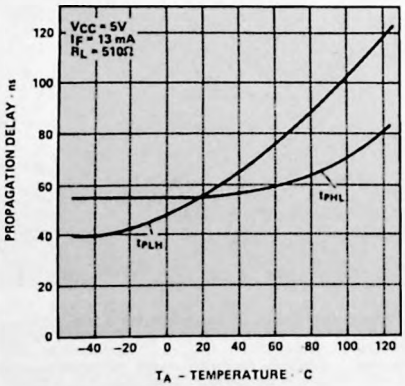


Figure 5. Propagation Delay vs. Temperature

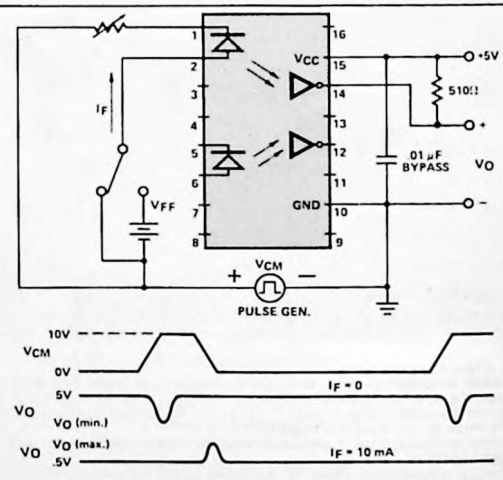


Figure 6. Typical Common Mode Rejection Characteristics/Circuit

*JEDEC Registered Data.

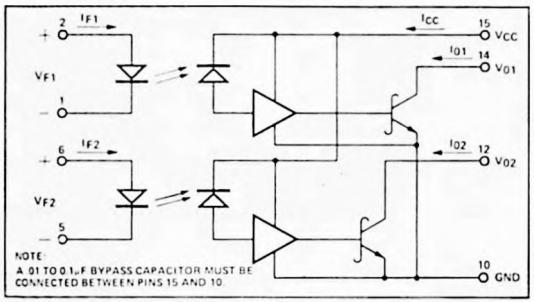
HEWLETT PACKARD

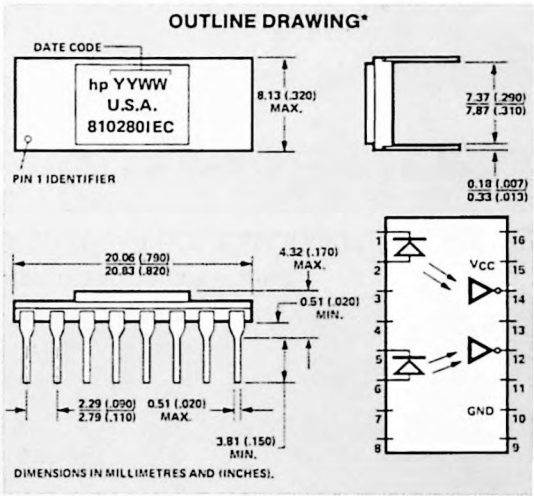
DUAL CHANNEL HERMETICALLY SEALED OPTOCOUPLER

DESC APPROVED

8102801EC

TECHNICAL DATA JANUARY 1984





Features

- RECOGNIZED BY DESC*
- HERMETICALLY SEALED
- MIL-STD-883 CLASS B TESTING
- HIGH SPEED
- PERFORMANCE GUARANTEED OVER -55° C TO +125° C AMBIENT TEMPERATURE RANGE
- TTL COMPATIBLE INPUT AND OUTPUT
- DUAL-IN-LINE PACKAGE
- 1500 VDC WITHSTAND TEST VOLTAGE
- HIGH RADIATION IMMUNITY

Applications

- MILITARY/HIGH RELIABILITY SYSTEMS
- LOGIC GROUND ISOLATION
- LINE RECEIVER
- COMPUTER — PERIPHERAL INTERFACE
- VEHICLE COMMAND/CONTROL ISOLATION
- SYSTEM TEST EQUIPMENT ISOLATION

Description

The 8102801EC is the DESC selected item drawing assigned by DOD for the 6N134 optocoupler which is in accordance with MIL-STD-883 class B testing. Operating characteristic curves for this port can be seen in the 6N134 data sheet.

The 8102801EC consists of a pair of inverting optically coupled gates, each with a light emitting diode and a unique high gain integrated photon detector in a hermetically sealed ceramic package. The output of the detector is an open collector Schottky clamped transistor.

This unique dual coupler design provides maximum DC and AC circuit isolation between each input and output while achieving TTL circuit compatibility. The isolator operational parameters are guaranteed from -55° C to +125° C, such that a minimum input current of 10 mA in each channel will sink a six gate fanout (10 mA) at the output with 4.5 to 5.5 V V_{CC} applied to the detector. This isolation and coupling is achieved with a typical propagation delay of 55 nsec.

The photo ICs used in this device are less susceptible to radiation damage than PIN photo diodes or photo transistors due to their relatively thinner photo region.

The following test program is performed on the 8102801EC.

Recommended Operating Conditions

Supply Voltage	4.5 V dc minimum to 5.5 V dc maximum
High Level Input Current[1]	12.5 mA dc minimum (each channel)
Low Level Input Current	250 μA dc maximum (each channel)
Normalized Fanout (TTL Load)	6 maximum (each channel)
Operating Temperature Range	-55° C to +125° C

1. This condition permits at least 20 percent h_F (CTR) degradation. The initial switching threshold is 10 mA dc or less.

Absolute Maximum Ratings

Supply Voltage Range	7 V dc
Input Current (each channel)	20 mA dc
Storage Temperature Range	-65° C to +150° C
Maximum Power Dissipation (both channels)	350 mW
Lead Temperature (soldering 10 seconds)	300° C for 10 seconds
Junction Temperature (T_J)	175° C

* *Defense Electronic Supply Center (DESC) is an agency of the Department of Defense (DOD).

100% Screening

MIL-STD-883, METHOD 5004 (CLASS B DEVICES)

Test Screen	Method	Conditions
1. Precap Internal Visual	2010	Condition B
2. High Temperature Storage	1008	Condition C, T_A= 150°C, Time = 24 hours minimum
3. Temperature Cycling	1010	Condition C, -65°C to +150°C, 10 cycles
4. Constant Acceleration	2001	Condition A, 5KG's, Y_1 axis only
5. Fine Leak	1014	Condition A
6. Gross Leak	1014	Condition C
7. Interim Electrical Test	—	Optional
8. Burn-In	1015	Condition B, Time = 160 hours minimum T_A = +125°C, V_{CC} = 5.5V, I_F = 13 mA, I_O = 25 mA (Figure 1)
9. Final Electrical Test Electrical Test Electrical Test	—	Group A, Subgroup 1, 10% PDA applies Group A, Subgroup 2 Group A, Subgroup 3
10. External Visual	2009	

Quality Conformance Inspection

GROUP A ELECTRICAL PERFORMANCE CHARACTERISTICS

Test	Symbol	Conditions	Group A Subgroups[6]	Limits Min.	Limits Max.	Unit
Low Level Output Voltage	V_{OL}	V_{CC} = 5.5 V; I_F = 10 mA[1]; I_{OL} = 10 mA	1, 2, 3	—	0.6	V
Current Transfer Ratio	h_F (CTR)	V_O = 0.6 V; I_F = 10 mA;[1] V_{CC} = 5.5 V	1, 2, 3	100	—	%
High Level Output Voltage	I_{OH}	V_{CC} = 5.5 V; V_O = 5.5 V[1]; I_F = 250 μA	1, 2, 3	—	250	μA dc
High Level Supply Current	I_{CCH}	V_{CC} = 5.5 V; I_{F1} = I_{F2} = 0 mA	1, 2, 3	—	28	mA dc
Low Level Supply Current	I_{CCL}	V_{CC} = 5.5 V; I_{F1} = I_{F2} = 20 mA	1, 2, 3	—	36	mA dc
Input Forward Voltage	V_F	I_F = 20 mA[1]	1, 2	—	1.75	V dc
			3	—	1.85	
Input Reverse Breakdown Voltage	V_{BR}	I_R = 10 μA[1]	1, 2, 3	5.0	—	V dc
Input to Output Leakage Current	I_{I-O}	V_{IO} = 1500 V dc[2]; Relative Humidity = 45 percent t = 5 seconds	1	—	1.0	μA dc
Capacitance Between Input/Output	C_{I-O}	f = 1 MHz; T_C = 25°C[3]	4	—	4.0	pF
Propagation Delay Time, Low to High Output Level	t_{PLH}	R_L = 510 Ω; C_L = 50 pF[1,4]; I_F = 13 mA	9	—	100	ns
			10, 11	—	140	
Propagation Delay Time, High to Low Output Level	t_{PHL}	R_L = 510 Ω; C_L = 50 pF[1,5]; I_F = 13 mA	9	—	100	ns
			10, 11	—	120	
Output Rise Time	t_{LH}	R_L = 510 Ω[1]; C_L = 50 pF; I_F = 13 mA	9, 10, 11	—	90	ns
Output Fall Time	t_{HL}			—	40	
Common Mode Transient Immunity at High Output Level	CM_H	V_{CM} = 10 V (peak);[1] V_O = 2 V (minimum); R_L = 510 Ω; I_F = 0 mA	9, 10, 11	40	—	V/μs
Common Mode Transient Immunity at Low Output Level	CM_L	V_{CM} = 10 V (peak);[1] V_O = 0.8 V (maximum); R_L = 510 Ω; I_F = 10 mA	9, 10, 11	-60	—	V/μs

See notes on following page.

Notes: 1. Each channel.
2. Measured between pins 1 through 8 shorted together and pins 9 through 16 shorted together.
3. Measured between input pins 1 and 2, or 5 and 6 shorted together and output pins 10, 12, 14 and 15 shorted together.
4. The t_{PLH} propagation delay is measured from the 6.5 mA point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
5. The t_{PHL} propagation delay is measured from the 6.5 mA point on the leading edge of the input pulse to the 1.5 V point on the leading edge of the output pulse.
6. Conditions of Group A subgroups may be seen in the High Reliability section of this catalog.

GROUP B TESTING MIL-STD-883, METHOD 5005 (CLASS B DEVICES)

Test	Method	Conditions	LTPD
Subgroup 1 Physical Dimensions (Not required if Group D is to be performed)	2016		2 Devices (0 failures)
Subgroup 2 Resistance to Solvents	2015		4 Devices (0 failures)
Subgroup 3 Solderability (LTPD applies to number of leads inspected — no fewer than 3 devices shall be used).	2003	Soldering Temperature of 260 ± 10°C for 10 seconds	15 (3 Devices)
Subgroup 4 Internal Visual and Mechanical (May be performed at precap)	2014		1 Device (0 failures)
Subgroup 5 Bond Strength Thermocompression: (Performed at precap, prior to seal LTPD applies to number of bond pulls from a minimum of 4 devices).	2011	Test Condition D	15 (4 Devices)
Subgroup 6 Internal Water Vapor Content (Not applicable — does not contain desiccant)	—		—
Subgroup 7 Fine Leak Gross Leak (Not applicable — performed in 100% screen)	—		—
Subgroup 8* Electrical Test Electrostatic Discharge Sensitivity Electrical Test *(To be performed at initial qualification only)	3015	Group A, Subgroup 1, except I_{I-O} Group A, Subgroup 1	15

GROUP C TESTING MIL-STD-883, METHOD 5005 (CLASS B DEVICES)

Test	Method	Conditions	LTPD
Subgroup 1 Steady State Life Test	1005	Condition B, Time = 1000 hours total T_A = +125°C, V_{CC} = 5.5 V, I_F = 13 mA, I_O = 25 mA (Figure 1)	5
Endpoint Electricals at 1000 hours		Group A, Subgroup 1, 2, 3	
Subgroup 2 Temperature Cycling	1010	Condition C, -65°C to +150°C, 10 cycles	15
Constant Acceleration	2001	Condition A, 5KGs, Y_1 axis only	
Fine Leak	1014	Condition A	
Gross Leak	1014	Condition C	
Visual Examination	1010	Per Visual Criteria of Method 1010	
Endpoint Electricals		Group A, Subgroup 1, 2, 3	

GROUP D TESTING MIL-STD-883, METHOD 5005 (CLASS B DEVICES)

Test	Method	Conditions	LTPD
Subgroup 1			
Physical Dimensions	2016		15
Subgroup 2			
Lead Integrity	2004	Test Condition B2 (lead fatigue)	15
Fine Leak	1014	Condition A	
Gross Leak	1014	Condition C	
Lid Torque*	2024		
*(Not applicable — solder seal)			
Subgroup 3			
Thermal Shock	1011	Condition B, (-55°C to +125°C) 15 cycles min.	15
Temperature Cycling	1010	Condition C, (-65°C to +150°C) 100 cycles min.	
Moisture Resistance	1004		
Fine Leak	1014	Condition A	
Gross Leak	1014	Condition C	
Visual Examination		Per Visual Criteria of Method 1004	
Endpoint Electricals		Group A, Subgroup 1, 2, 3	
Subgroup 4			
Mechanical Shock	2002	Condition B, 1500G, t = 0.5 ms, 5 blows in each orientation	15
Vibration Variable Frequency	2007	Condition A	
Constant Acceleration	2001	Condition A, 5KGs, Y_1 axis only	
Fine Leak	1014	Condition A	
Gross Leak	1014	Condition C	
Visual Examination	1010	Per Visual Criteria of Method 1010	
Endpoint Electricals		Group A, Subgroup 1, 2, 3	
Subgroup 5			
Salt Atmosphere	1009	Condition A min.	15
Fine Leak	1014	Condition A	
Gross Leak	1014	Condition C	
Visual Examination	1009	Per Visual Criteria of Method 1009	
Subgroup 6			
Internal Water Vapor Content	1018		3 Devices (0 failures) 5 Devices (1 failure)
Subgroup 7			
Adhesion of Lead Finish	2025		15

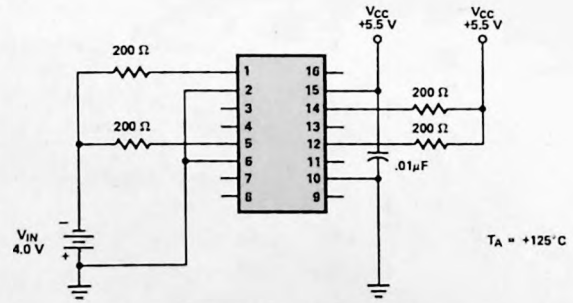


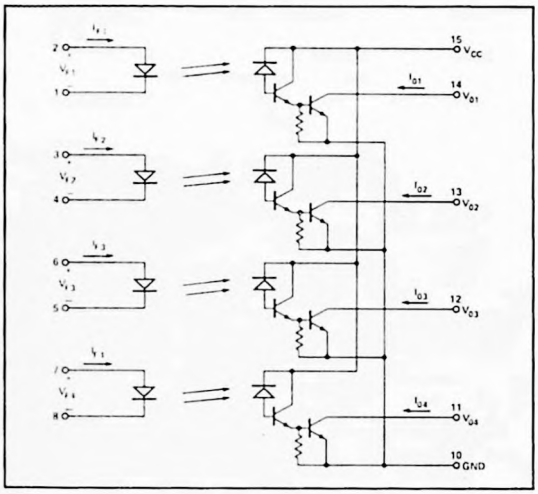
Figure 1. Burn-In Circuit

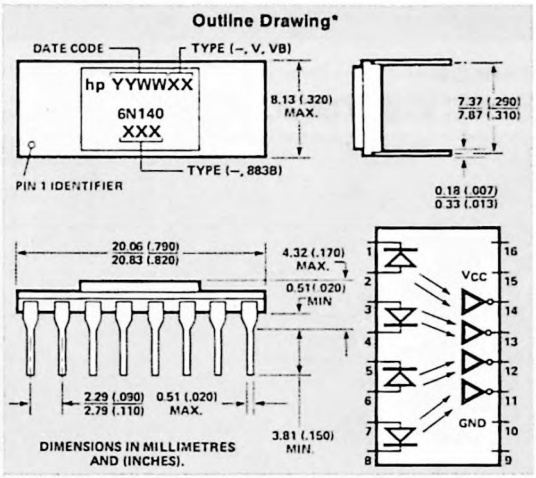
HEWLETT PACKARD

HERMETICALLY SEALED, FOUR CHANNEL, LOW INPUT CURRENT OPTOCOUPLER

6N140
6N140/883B

TECHNICAL DATA JANUARY 1984





Features

- 125° C EXTENDED TEMPERATURE PART AVAILABLE[1]
- HERMETICALLY SEALED
- CONFORMANCE TO MIL-STD-883
- HIGH DENSITY PACKAGING
- HIGH CURRENT TRANSFER RATIO: 500% TYPICAL
- CTR AND I_{OH} GUARANTEED OVER -55°C TO 100°C AMBIENT TEMPERATURE RANGE[1]
- STANDARD HIGH RELIABILITY SCREENED PARTS AVAILABLE
- 1500 Vdc WITHSTAND TEST VOLTAGE
- LOW INPUT CURRENT REQUIREMENT: 0.5 mA
- LOW OUTPUT SATURATION VOLTAGE: 0.1V TYPICAL
- LOW POWER CONSUMPTION
- HIGH RADIATION IMMUNITY

Applications

- Isolated Input Line Receiver
- System Test Equipment Isolation
- Digital Logic Ground Isolation
- Vehicle Command/Control Isolation
- EIA RS-232C Line Receiver
- Microprocessor System Interface
- Current Loop Receiver
- Level Shifting
- Process Control Input/Output Isolation

Description

The 6N140 contains four GaAsP light emitting diodes, each of which is optically coupled to a corresponding integrated high gain photon detector. A common pin for the photodiodes and first stage of each detector IC (V_{CC}) permits lower output saturation voltage and higher speed operation than possible with conventional photodarlington type optocouplers. Also, the separate V_{CC} pin can be operated with supply voltages as low as 2.0V without adversely affecting the parametric performance.

The outstanding high temperature performance of this split Darlington type output amplifier results from the inclusion of an integrated emitter-base bypass resistor which shunts photodiode and first stage leakage currents to ground.

The high current transfer ratio at very low input currents permits circuit designs in which adequate margin can be allowed for the effects of CTR degradation over time.

The 6N140 has a 300% minimum CTR at an input current of only 0.5mA making it ideal for use in low input current applications such as MOS, CMOS and low power logic interfacing or RS-232C data transmission systems. Compatibility with high voltage CMOS logic systems is assured by the 18V V_{CC} and by the guaranteed maximum output leakage (I_{OH}) at 18V.

Important specifications such as CTR, leakage current, supply current and output saturation voltage are guaranteed over the –55° C to 100° C temperature range[1] to allow trouble free system operation.

Hewlett-Packard's new high reliablity part type 6N140/883B meets Class B testing requirements of MIL-STD-883. This part is the recommended and preferred device from the 6N140 product family for use in high reliability applications. The 6N140TXV and 6N140TXVB parts remain available. For further information on these parts contact your field salesman.

*JEDEC Registered Data.

TABLE I

Recommended Operating Conditions

	Symbol	Min.	Max.	Units
Input Current, Low Level (Each Channel)	I_{FL}		2	μA
Input Current, High Level (Each Channel)	I_{FH}	0.5	5	mA
Supply Voltage	V_{CC}	2.0	18	V

Absolute Maximum Ratings*

Storage Temperature ..... -65°C to +150°C
Operating Temperature ..... -55°C to +100°C[1]
Lead Solder Temperature ..... 260°C for 10 s. (1.6mm below seating plane)
Output Current, I_O (each channel) ..... 40 mA
Output Voltage, V_O (each channel) ..... -0.5 to 20 V[2]
Supply Voltage, V_{CC} ..... -0.5 to 20 V[2]
Output Power Dissipation (each channel) ... 50 mW[3]
Peak Input Current (each channel, ≤1 ms duration) ..... 20 mA
Average Input Current, I_F (each channel) ..... 10 mA[4]
Reverse Input Voltage, V_R (each channel) 5V

TABLE II.

Electrical Characteristics T_A = -55°C to 100°C[1], Unless Otherwise Specified

Parameter	Symbol	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR*	300 300 200	1000 750 400		% % %	I_F=0.5mA, V_O=0.4V, V_{CC}=4.5V I_F=1.6mA, V_O=0.4V, V_{CC}=4.5V I_F=5mA, V_O=0.4V, V_{CC}=4.5V	3	5, 6
Logic Low Output Voltage	V_{OL}		.1 .2	.4 .4	V V	I_F=.5mA, I_{OL}=1.5mA, V_{CC}=4.5V I_F=5mA, I_{OL}=10mA, V_{CC}=4.5V	2	5
Logic High Output Current	I_{OHX}		.005	250	μA	I_F = 2 μA (channel under test) V_O = V_{CC} = 18 V		5, 7
	I_{OH}*							5
Logic Low Supply Current	I_{CCL}*		2	4	mA	I_{F1}=I_{F2}=I_{F3}=I_{F4}=1.6mA V_{CC}=18V		
Logic High Supply Current	I_{CCH}*		.010	40	μA	I_{F1}=I_{F2}=I_{F3}=I_{F4}=0 V_{CC}=18V		
Input Forward Voltage	V_F*		1.4	1.7	V	I_F=1.6mA, T_A=25°C	1	5
Input Reverse Breakdown Voltage	BV_R*	5			V	I_R=10μA, T_A=25°C		5
Input-Output Insulation Leakage Current	I_{I-O}*			1.0	μA	45% Relative Humidity, T_A=25°C, t=5s., V_{I-O}=1500 Vdc		8
Propagation Delay Time To Logic High At Output	t_{PLH}*		25	60	μs	I_F=0.5mA, R_L=4.7kΩ, V_{CC}=5.0V, T_A=25°C	8	5
			10	20	μs	I_F=5mA, R_L=680Ω, V_{CC}=5.0V, T_A=25°C	8	5
Propagation Delay Time To Logic Low At Output	t_{PHL}*		35	100	μs	I_F=0.5mA, R_L=4.7kΩ, V_{CC}=5.0V, T_A=25°C	8	5
			2	5	μs	I_F=5mA, R_L=680Ω, V_{CC}=5.0V, T_A=25°C	8	5
Common Mode Transient Immunity At Logic High Level Output	CM_H	500	1000		V/μs	I_F=0, R_L=1.5kΩ, R_{CC}=0 $\|V_{CM}\|$=50V_{p-p}, V_{CC}=5.0V, T_A=25°C	9	5, 11, 13
Common Mode Transient Immunity At Logic Low Level Output	CM_L	-500	-1000		V/μs	I_F=1.6 mA, R_L=1.5kΩ, R_{CC}=0 $\|V_{CM}\|$=50V_{p-p}, V_{CC}=5.0V, T_A=25°C	9	5, 12, 13

**All typical values are at V_{CC} = 5V, T_A = 25°C.

TABLE III.

Typical Characteristics T_A = 25°C, V_{CC} = 5V Each Channel

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	V_{I-O}=500 Vdc, T_A=25°C		5, 9
Capacitance (Input-Output)	C_{I-O}		1.5		pF	f=1MHz, T_A=25°C		5, 9
Input-Input Insulation Leakage Current	I_{I-I}		0.5		nA	45% Relative Humidity, V_{I-I}=500 Vdc, T_A=25°C, t=5s.		10
Resistance (Input-Input)	R_{I-I}		10^{12}		Ω	V_{I-I}=500Vdc, T_A=25°C		10
Capacitance (Input-Input)	C_{I-I}		1		pF	f=1MHz, T_A=25°C		10
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$		-1.8		mV/°C	I_F=1.6mA		5
Input Capacitance	C_{IN}		60		pF	f=1MHz, V_F=0, T_A=25°C		5

NOTES
1. 125°C part also available, contact HP field sales office for ordering information.
2. Pin 10 should be the most negative voltage at the detector side. Keeping V_{CC} as low as possible, but greater than 2.0 volts, will provide lowest total I_{OH} over temperature.
3. Output power is collector output power plus one fourth of total supply power. Derate at 1.25 mW/°C above 80°C.
4. Derate I_F at 0.25 mA/°C above 80°C.
5. Each channel.
6. CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
7. I_F=2μA for channel under test. For all other channels, I_F=10mA.
8. Device considered a two-terminal device: Pins 1 through 8 are shorted together and pins 9 through 16 are shorted together.
9. Measured between each input pair shorted together and all output pins.
10. Measured between adjacent input pairs shorted together, i.e. between pins 1 and 2 shorted together and pins 3 and 4 shorted together, etc.
11. CM_H is the maximum tolerable common mode transient to assure that the output will remain in a high logic state (i.e. V_O > 2.0V).
12. CM_L is the maximum tolerable common mode transient to assure that the output will remain in a low logic state (i.e. V_O < 0.8V).
13. In applications where dV/dt may exceed 50,000 V/μs (such as a static discharge) a series resistor, R_{CC}, should be included to protect the detector IC's from destructively high surge currents. The recommended value is $R_{CC} \approx \frac{1V}{0.6\ I_F\ (mA)}$ kΩ.

*JEDEC Registered Data.

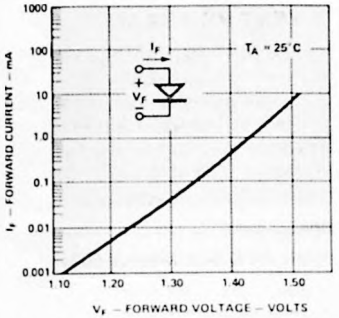


Figure 1. Input Diode Forward Current vs. Forward Voltage.

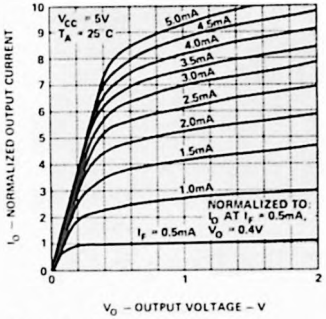


Figure 2. Normalized DC Transfer Characteristics.

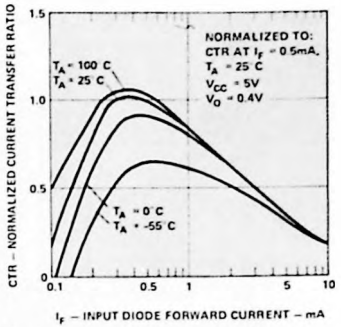


Figure 3. Normalized Current Transfer Ratio vs. Input Diode Forward Current.

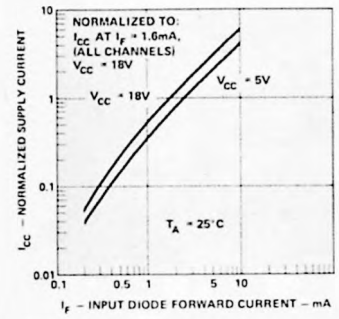


Figure 4. Normalized Supply Current vs. Input Diode Forward Current.

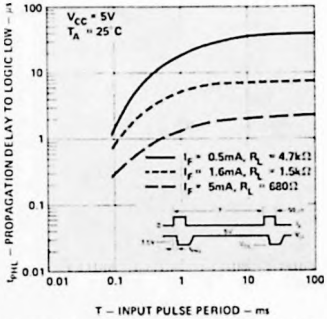


Figure 5. Propagation Delay to Logic Low vs. Input Pulse Period.

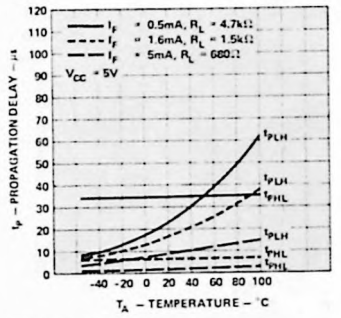


Figure 6. Propagation Delay vs. Temperature

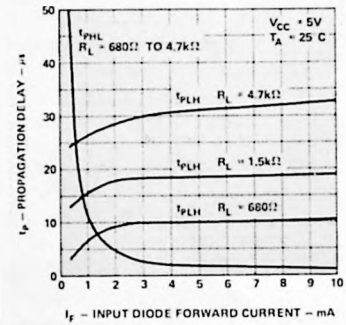


Figure 7. Propagation Delay vs. Input Diode Forward Current.

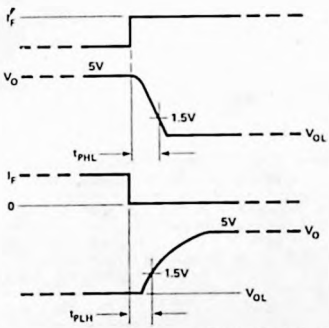
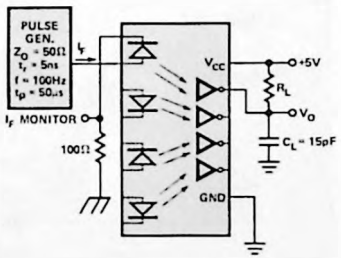


Figure 8. Switching Test Circuit.*
(f, t_p not JEDEC registered)



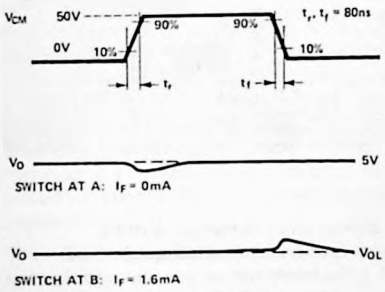
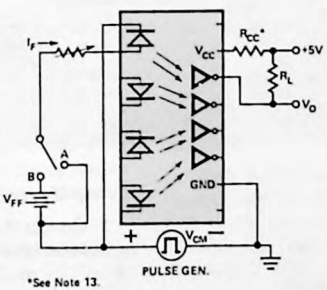


Figure 9. Test Circuit for Transient Immunity and Typical Waveforms.



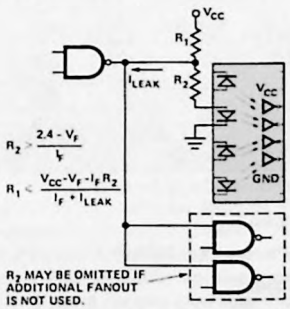


Figure 10. Recommended drive circuitry using TTL logic.

OPTOCOUPLERS

*JEDEC Registered Data.

PART NUMBERING SYSTEM

Commercial Product	Method 5004 and 5005 of MIL-STD-883
6N140	6N140/883B

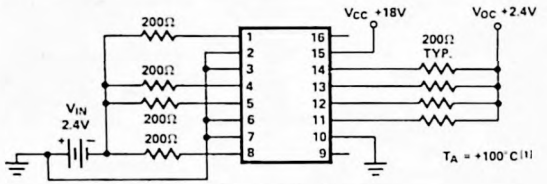


Figure 11. Burn-In Circuit

HIGH RELIABILITY TEST PROGRAM

Hewlett-Packard has upgraded their standard high reliability testing programs to conform with MIL-M-38510. With certain clarifications of testing conditions listed below, the 883B part fully complies with Class B testing of MIL-STD-883. Testing consists of 100% screening to Method 5004 and Quality Conformance to Method 5005 of MIL-STD-883. The 883B suffix identifies this Class B equivalent.

6N140/883B Clarifications:

I. 100% screening per MIL-STD-883, Method 5004
   1. Constant acceleration — condition A not E
   2. Burn-in conditions per Figure 11.

II. Quality Conformance per MIL-STD-883, Method 5005

Group A

Subgroup 1 — LTPD: 5

Static tests at $T_A = 25°C$, I_{OH}, I_{CCL}, I_{CCH}, CTR, V_F, BV_R and $I_{I/O}$

Subgroup 2 — LTPD: 7

Static tests at $T_A = +100°C$[1], I_{OH}, I_{CCL}, I_{CCH}, CTR

Symbol	Min.	Max.	Units	Test Conditions
V_F		1.8	V	$I_F = 1.6$ mA
BV_R	3		V	$I_R = 10\ \mu A$

Subgroup 3 — LTPD: 7

Static tests at $T_A = -55°C$, I_{OH}, I_{CCL}, I_{CCH}, CTR

Symbol	Min.	Max.	Units	Test Conditions
V_F		1.8	V	$I_F = 1.6$ mA
BV_R	3		V	$I_R = 10\ \mu A$

Subgroup 4, 5, 6, 7 and 8

These subgroups are non-applicable to this device type.

Subgroup 9 — LTPD: 7

Switching tests at $T_A = 25°C$, t_{PLH1}, t_{PHL1}, t_{PLH2}, t_{PHL2}, CM_H and CM_L

Subgroup 10 — LTPD: 10

Switching tests at $T_A = +100°C$[1]

Symbol	Max.	Units	Test Conditions	
t_{PLH1}	300	μs	$I_F = 0.5$ mA, $R_L = 4.7\Omega$	$V_{CC} = 5.0V$
t_{PLH2}	80	μs	$I_F = 5$ mA, $R_L = 680\Omega$	$V_{CC} = 5.0V$
t_{PHL1}	200	μs	$I_F = 0.5$ mA, $R_L = 4.7\Omega$	$V_{CC} = 5.0V$
t_{PHL2}	10	μs	$I_F = 5$ mA, $R_L = 680\Omega$	$V_{CC} = 5.0V$

Subgroup 11 — LTPD: 10

Switching tests at $T_A = -55°C$

Symbol	Max.	Units	Test Conditions	
t_{PLH1}	300	μs	$I_F = 0.5$ mA, $R_L = 4.7\Omega$	$V_{CC} = 5.0V$
t_{PLH2}	80	μs	$I_F = 5$ mA, $R_L = 680\Omega$	$V_{CC} = 5.0V$
t_{PHL1}	200	μs	$I_F = 0.5$ mA, $R_L = 4.7\Omega$	$V_{CC} = 5.0V$
t_{PHL2}	10	μs	$I_F = 5$ mA, $R_L = 680\Omega$	$V_{CC} = 5.0V$

Limits and Conditions per Table II

Group B

Per Method 5005

Group C

1. Steady state life conditions per Figure 11.
2. Constant acceleration — condition A not E.

Group D

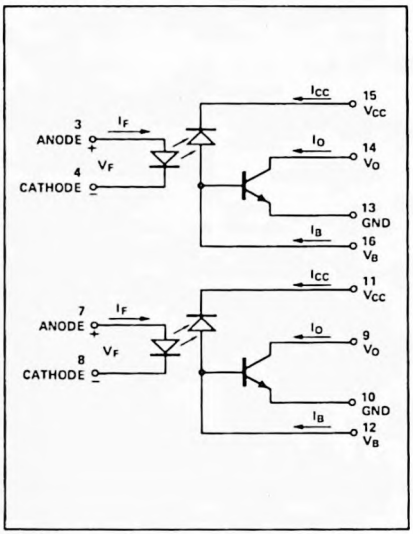
1. Constant acceleration — condition A not E.
2. Internal water vapor content — not performed.

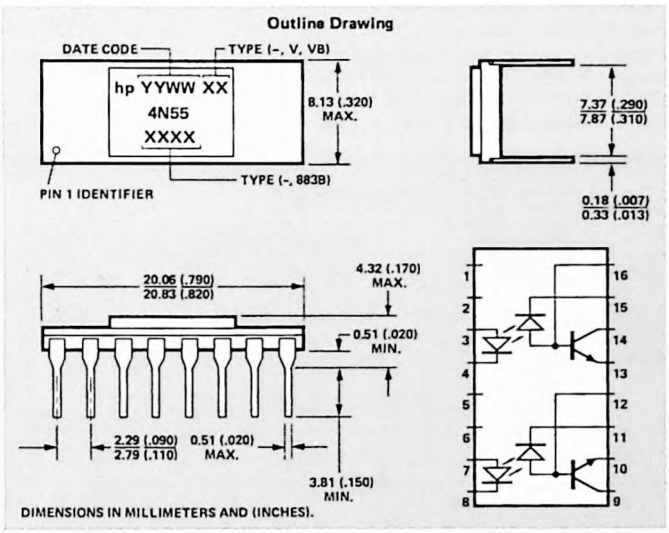
HEWLETT PACKARD

DUAL CHANNEL HERMETICALLY SEALED OPTOCOUPLER

4N55
4N55/883B

TECHNICAL DATA JANUARY 1984





Features

- HERMETICALLY SEALED
- CONFORMANCE TO MIL-STD-883
- HIGH SPEED: TYPICALLY 400k bit/s
- PERFORMANCE GUARANTEED OVER -55° C TO +125° C AMBIENT TEMPERATURE RANGE
- STANDARD HIGH RELIABILITY SCREENED PARTS AVAILABLE
- 2 MHz BANDWIDTH
- OPEN COLLECTOR OUTPUTS
- 18 VOLT V_{CC}
- DUAL-IN-LINE PACKAGE
- 1500 Vdc WITHSTAND TEST VOLTAGE
- HIGH RADIATION IMMUNITY

Applications

- HIGH RELIABILITY SYSTEMS
- LINE RECEIVERS
- DIGITAL LOGIC GROUND ISOLATION
- ANALOG SIGNAL GROUND ISOLATION
- SWITCHING POWER SUPPLY FEEDBACK ELEMENT
- VEHICLE COMMAND/CONTROL
- SYSTEM TEST EQUIPMENT
- LEVEL SHIFTING

Description

The 4N55 consists of two completely isolated optocouplers in a hermetically sealed ceramic package. Each channel has a light emitting diode and an integrated photon detector providing 1500 Vdc electrical isolation between input and output. Separate connections for the photodiodes and output transistor collectors improve the speed up to a hundred times that of a conventional phototransistor optocoupler by reducing the base-collector capacitance.

The 4N55 is suitable for wide bandwidth analog applications, as well as for interfacing TTL to LSTTL or CMOS. Current Transfer Ratio (CTR) is 9% minimum at I_F = 16mA over the full military operating temperature range, -55° C to +125° C. The 18V V_{CC} capability will enable the designer to interface any TTL family to CMOS. The availability of the base lead allows optimized gain/bandwidth adjustment in analog applications. The shallow depth of the IC photodiode provides better radiation immunity than conventional phototransistor couplers.

Hewlett-Packard's new high reliability part type 4N55/883B meets Class B testing requirements for MIL-STD-883. This part is the recommended and preferred device from the 4N55 product family for use in high reliability applications. The 4N55TXV and 4N55TXVB parts remain available. For further information on these parts contact your field salesman.

Absolute Maximum Ratings

Storage Temperature ..... -65°C to +150°C
Operating Temperature ..... -55°C to +125°C
Lead Solder Temperature ..... 260°C for 10 s (1.6mm below seating plane)
Average Input Current, I_F (each channel) 20mA
Peak Input Current, I_F (each channel, ≤ 1ms duration) 40mA
Reverse Input Voltage, V_R (each channel) 5V
Input Power Dissipation (each channel) 36mW
Average Output Current, I_O (each channel) 8mA
Peak Output Current, I_O (each channel) 16mA
Supply Voltage, V_{CC} (each channel) ..... -0.5V to 20V
Output Voltage, V_O (each channel) ..... -0.5V to 20V
Emitter Base Reverse Voltage, V_{EBO} 3.0V
Base Current, I_B (each channel) 5mA
Output Power Dissipation (each channel) 50mW
Derate linearly above 100°C free air temperature at a rate of 1.4mW/°C.

CAUTION: The small junction sizes inherent to the design of this bipolar component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

TABLE I.

Recommended Operating Conditions (EACH CHANNEL)

	Symbol	Min.	Max.	Units
Input Current, Low Level	I_{FL}		250	μA
Supply Voltage	V_{CC}	2	18	V

TABLE II.

Electrical Characteristics T_A = -55°C to +125°C, unless otherwise specified

Parameter	Symbol	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR*	9	20		%	I_F=16mA, V_O=0.4V, V_{CC}=4.5V	2,3	1,2
Logic High Output Current	I_{OH}		20	100	μA	I_F=0, I_F (other channel)=20mA V_O=V_{CC}=18V	4	1
Output Leakage Current	I_{OH1}*		70	250	μA	I_F=250μA, I_F (other channel)=20mA V_O=V_{CC}=18V	4	1
Logic Low Supply Current	I_{CCL}*		35	200	μA	I_{F1}=I_{F2}=20mA, V_{CC}=18V	5	1
Logic High Supply Current	I_{CCH}*		0.2	10	μA	I_F=0mA, I_F (other channel)=20mA V_{CC}=18V		1
Input Forward Voltage	V_F*		1.5	1.8	V	I_F=20mA	1	1
Input Reverse Breakdown Voltage	B_{VR}*	3			V	I_R=10μA		1
Input-Output Leakage Current	I_{I-O}*			1.0	μA	45% Relative Humidity, T_A=25°C, t=5s, V_{I-O}=1500Vdc		3
Propagation Delay Time to Logic High at Output	t_{PLH}*		2.0	6.0	μs	R_L=8.2KΩ, C_L=50pF I_F=16mA, V_{CC}=5V	6,9	1
Propagation Delay Time to Logic Low at Output	t_{PHL}*		0.4	2.0	μs	R_L=8.2KΩ, C_L=50pF I_F=16mA, V_{CC}=5V	6,9	1

*JEDEC Registered Data.
**All typical values are at V_{CC} = 5V, T_A = 25°C.

Notes:
1. Each channel.
2. Current Transfer Ratio is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%. CTR is known to degrade slightly over the unit's lifetime as a function of input current, temperature, signal duty cycle and system on time. Refer to Application Note 1002 for more detail. In short it is recommended that designers allow at least 20-25% guardband for CTR degradation.
3. Measured between pins 1 through 8 shorted together and pins 9 through 16 shorted together.

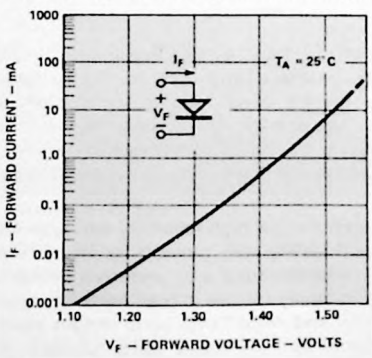


Figure 1. Input Diode Forward Characteristic.

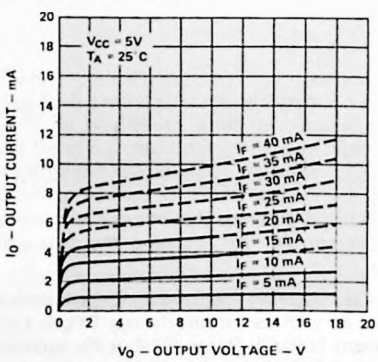


Figure 2. DC and Pulsed Transfer Characteristic

TABLE III.

Typical Characteristics at T_A=25°C

Parameter	Symbol	Typ.	Units	Test Conditions	Fig.	Note
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$	-1.9	mV/°C	I_F=18mA		1
Input Capacitance	C_{in}	120	pF	f=1 MHz, V_F=0		1
Resistance (Input-Output)	R_{I-O}	10^{12}	Ω	V_{I-O}=500 Vdc		1
Capacitance (Input-Output)	C_{I-O}	1.0	pF	f=1 MHz		1,4
Input-Input Insulation Leakage Current	I_{I-I}	1	pA	45% Relative Humidity, V_{I-I}=500Vdc, t=5s		5
Capacitance (Input-Input)	C_{I-I}	.55	pF	f=1 MHz		5
Transistor DC Current Gain	h_{FE}	150	—	V_O=5V, I_O=3mA		1
Small Signal Current Transfer Ratio	$\frac{\Delta I_O}{\Delta I_F}$	21	%	V_{CC}=5V, V_O=2V	7	1
Common Mode Transient Immunity at Logic High Level Output	CM_H	1000	V/μs	I_F=0, R_L=8.2kΩ V_{CM}=10V_{p-p} V_O (min.) = 2.0 V	10	1,6
Common Mode Transient Immunity at Logic Low Level Output	CM_L	-1000	V/μs	I_F=16mA, R_L=8.2kΩ V_{CM}=10V_{p-p} V_O (max.) = 0.8 V	10	1,7
Bandwidth	BW	2	MHz	R_L=100Ω	8	8

Notes (cont.):

4. Measured between each input pair shorted together and the output pins for that channel shorted together.
5. Measured between pins 3 and 4 shorted together and pins 7 and 8 shorted together.
6. CM_H is the steepest slope (dV/dt) on the leading edge of the common mode pulse, V_{CM}, for which the output will remain in the logic high state (i.e. V_O > 2.0 V).
7. CM_L is the steepest slope (dV/dt) on the trailing edge of the common mode pulse, V_{CM}, for which the output will remain in the logic low state (i.e. V_O < 0.8 V).
8. Bandwidth is the frequency at which the ac output voltage is 3dB below the low frequency asymptote.

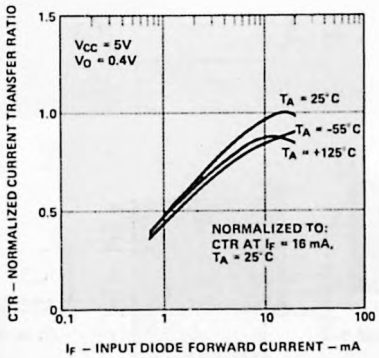


Figure 3. Normalized Current Transfer Ratio vs. Input Diode Forward Current.

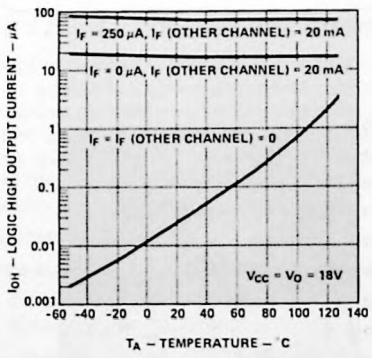


Figure 4. Logic High Output Current vs. Temperature.

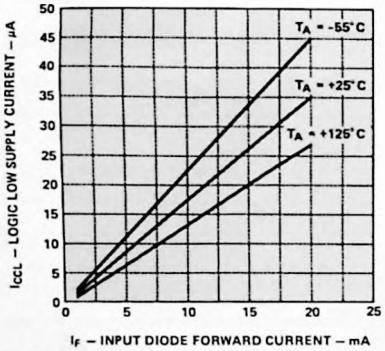
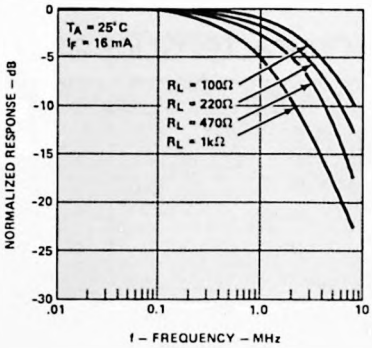


Figure 5. Logic Low Supply Current vs. Input Diode Forward Current.



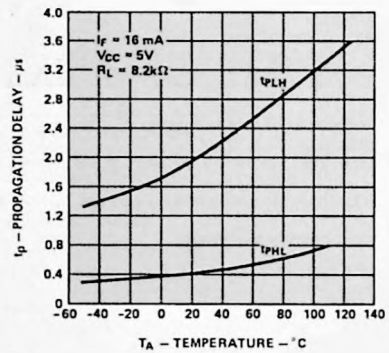


Figure 6. Propagation Delay vs. Temperature.

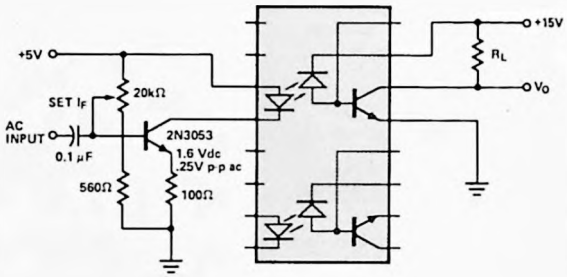


Figure 8. Frequency Response.

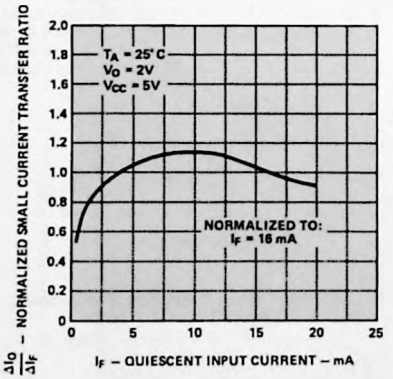
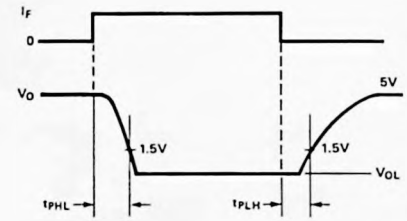


Figure 7. Normalized Small Signal Current Transfer Ratio vs. Quiescent Input Current.



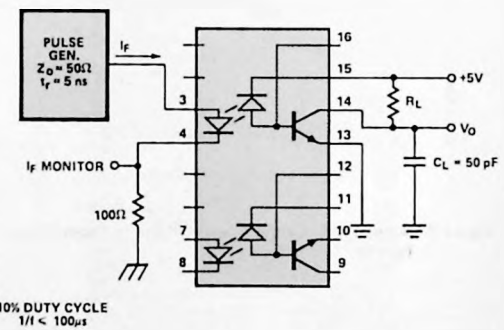


Figure 9. Switching Test Circuit*.

*JEDEC Registered Data.

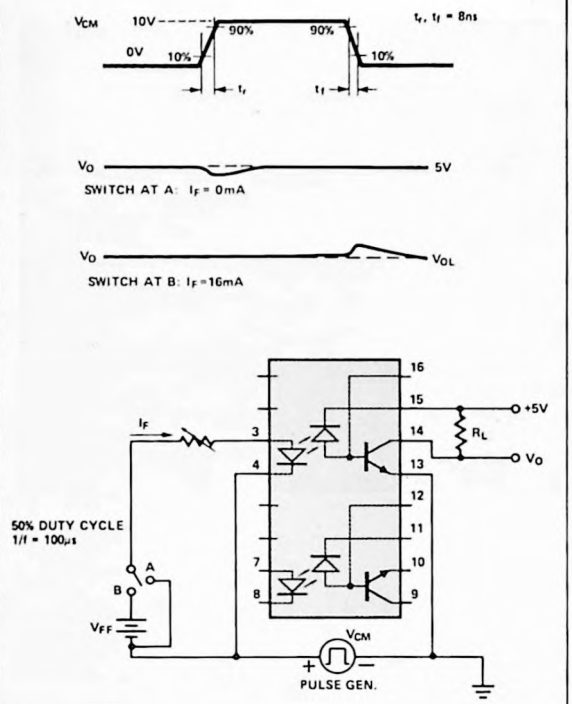
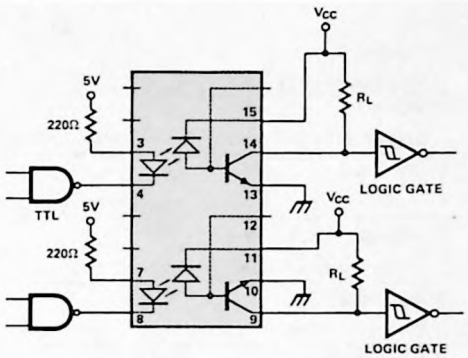


Figure 10. Test Circuit for Transient Immunity and Typical Waveforms.



LOGIC FAMILY	LSTTL	CMOS	
DEVICE NO.	54LS14	CD40106BM	
VCC	5V	5V	15V
RL 5% TOLERANCE	*18kΩ	8.2kΩ	22kΩ

*THE EQUIVALENT OUTPUT LOAD RESISTANCE IS AFFECTED BY THE LSTTL INPUT CURRENT AND IS APPROXIMATELY 8.2kΩ.

This is a worst case design which takes into account 25% degradation of CTR. See App. Note 1002 to assess actual degradation and lifetime.

Figure 11. Recommended Logic Interface.

PART NUMBERING SYSTEM

Commercial Product	Method 5004 and 5005 of MIL-STD-883
4N55	4N55/883B

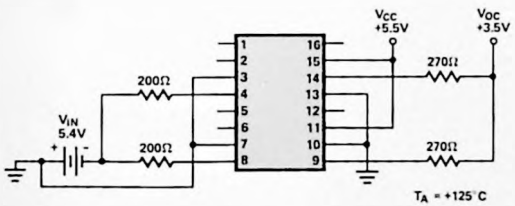


Figure 12. Burn-In Circuit

HIGH RELIABILITY TEST PROGRAM

Hewlett-Packard has upgraded their standard high reliability testing programs to conform with MIL-M-38510. With certain clarifications of testing conditions listed below, the 883B part fully complies with Class B testing of MIL-STD-883. Testing consists of 100% screening to Method 5004 and Quality Conformance to Method 5005 of MIL-STD-883. The 883B suffix identifies this Class B equivalent.

4N55/883B Clarifications:

I. 100% screening per MIL-STD-883, Method 5004.
   1. Constant acceleration — condition A not E.
   2. Burn-in conditions per Figure 12.

II. Quality Conformance per MIL-STD-883, Method 5005.

Group A

	LTPD
Subgroup 1 Static tests at $T_A = 25°C$, I_{OH}, BV_R, I_{CCL}, I_{CCH}, CTR, V_F, I_{OH1} and $I_{I/O}$	5
Subgroup 2 Static tests at $T_A = +125°C$, I_{OH}, BV_R I_{CCL}, I_{CCH}, CTR, V_F and I_{OH1}	7
Subgroup 3 Static tests at $T_A = -55°C$, I_{OH}, BV_R I_{CCL}, I_{CCH}, CTR, V_F and I_{OH1}	7
Subgroups 4, 5, 6, 7 and 8 These subgroups are non-applicable to this device type	
Subgroup 9 Switching tests at $T_A = 25°C$, t_{PLH} and t_{PHL}	7
Subgroup 10 Switching tests at $T_A = +125°C$, t_{PLH} and t_{PHL}	10
Subgroup 11 Switching tests at $T_A = -55°C$, t_{PLH} and t_{PHL}	10

Group B

Per Method 5005

Group C

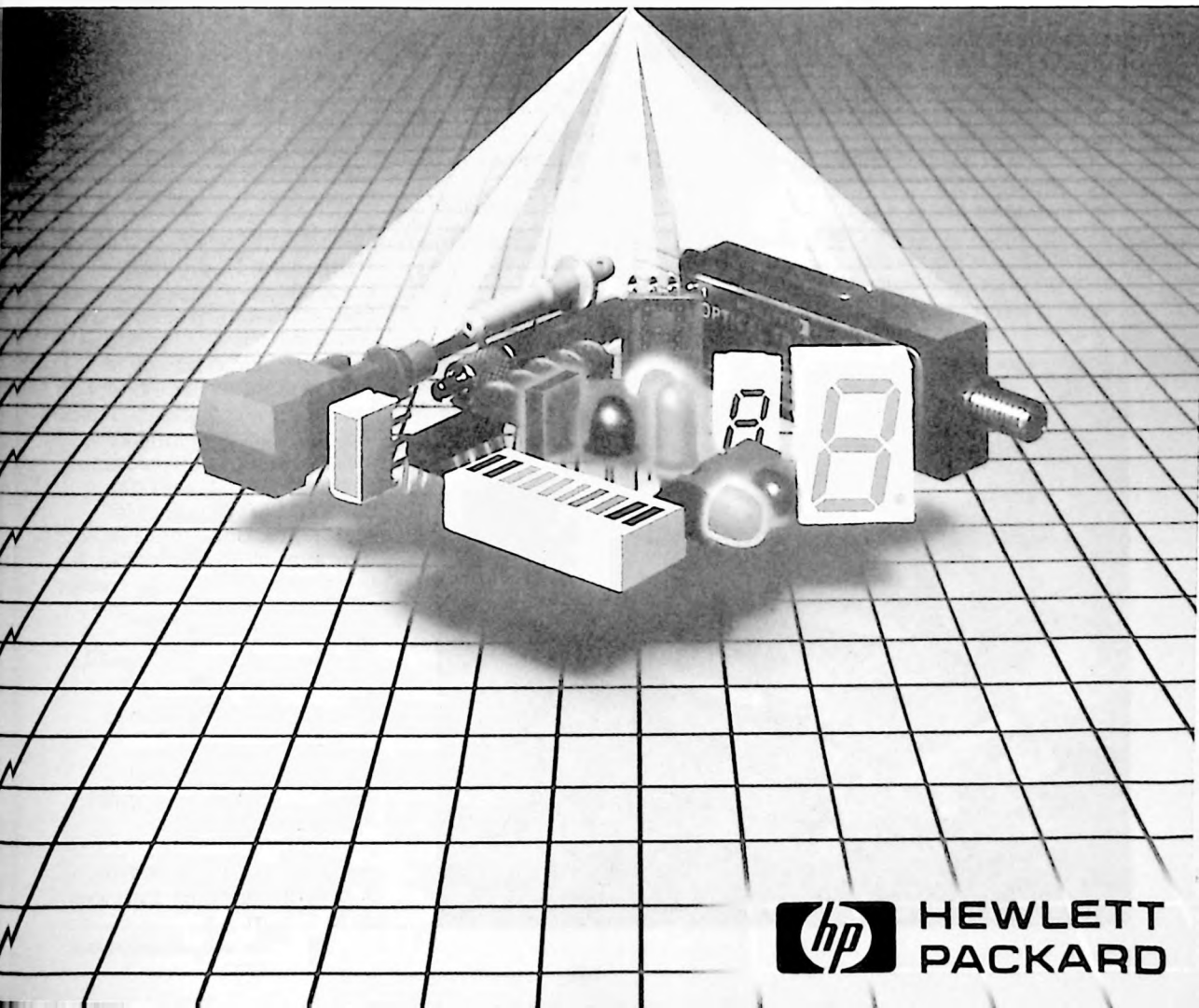
1. Steady state life conditions per Figure 12.
2. Constant acceleration — condition A not E.

Group D

1. Constant acceleration — condition A not E.
2. Internal water vapor content — not performed.

6. Fiber Optics

- Snap-in Fiber Optic Link
- Miniature Fiber Optic Link
- High Performance Modules
- Cables
- Connector Assembly Tooling Kit
- Multiplexer
- Detectors



HEWLETT PACKARD

Fiber Optics

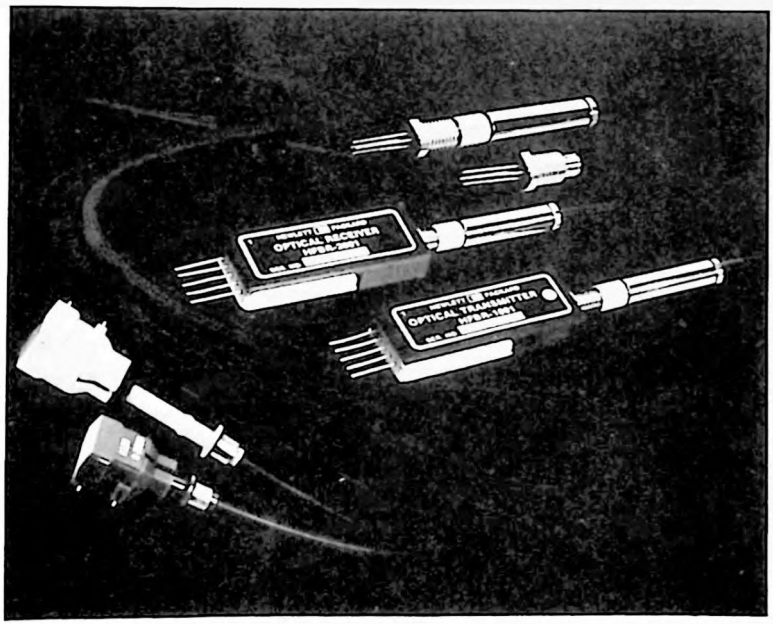
Three major families of fiber optic components offer a wide range of application solutions. The design and specification of each of these three families allow easy design-in and provide guaranteed end-to-end performance.

Hewlett-Packard's method of specification assures guaranteed link performance and easy design-in. The transmitter optical output power and receiver sensitivity are specified at the end of a length of test cable. These specifications take into account variations over temperature and connector tolerances. All families of components incorporate the fiber optic connector receptacle in the transmitter and receiver packages. Factory alignment of the emitter inside the connector receptacle minimizes the variation of optical output power, resulting in smaller dynamic range requirements for the receiver. The guaranteed distance and data rates for various transmitter/receiver pairs are shown in the following selection guide.

Hewlett-Packard offers a choice of fiber optic cable, either glass fiber or plastic, simplex or duplex, factory-connectored or bulk. Connector attachment in each case has been designed for your production-line economy.

Plastic Snap-In Link Components

Low-cost and ease of use make this family of link components well-suited for applications connecting computers to terminals, printers, plotters and industrial-control equipment. These links are rugged, 1 millimetre diameter plastic fiber cable. Assembling the plastic snap-in connectors onto the cable is extremely easy. The HFBR-0500 evaluation kit contains a complete working link including transmitter, receiver, 5 metres of connectored cable, extra connectors, polishing kit and technical literature.



Miniature Link Components

This family offers a wide range of performance choices for computer, industrial-control and military applications. The design of the optical coupling system between lens and small-diameter glass fiber makes this family of components very reliable. Both HP-style and SMA-style connectors are available. The HFBR-0200 evaluation kit contains transmitter, receiver, 10 metres of connectored cable and technical literature.

High Performance Modules

Transparent TTL-TTL link capability and independence from data format restrictions make this family of modules easy to use in a variety of applications. A link monitor on the receiver provides a digital indication of link continuity, independent of the presence of data. The modules are compatible with HP-style connectors and small-diameter glass fiber cable. A transmitter, receiver, 10 metres of connectored cable and technical literature are contained in the HFBR-0010 evaluation kit.

RS-232/V.24 to Fiber Optic Multiplexer

The 39301A 16-channel RS-232C/V.24 to fiber optic multiplexer allows the extension of up to 16 independent 19.2 Kbps full duplex channels to distances up to 1250m.

Fiber Optic Selection Guide

Snap-In Link Family: Features — Plastic fiber (1 mm dia.), Plastic Snap-in connectors, TTL compatible output.

Products/Part Nos.	Description	Page No.
Evaluation Kit HFBR-0500	HFBR-1501 Transmitter, HFBR-2501 Receiver, 5 metre connectored cable, connectors, polishing kit, literature	6-5
Transmitter/Receiver Pairs HFBR-1501/HFBR-2501 HFBR-1502/HFBR-2502	Guaranteed Distance*: 17 metre, 29 metre Guaranteed Data-Rate*: 5 MBd, 1 MBd	
Cables Simplex / Duplex / Cable Length HFBR-3501 / — / 0.1 metre HFBR-3502 / HFBR-3602 / 0.5 metre HFBR-3503 / HFBR-3603 / 1.0 metre HFBR-3504 / HFBR-3604 / 5.0 metre HFBR-3505 / HFBR-3605 / 10.0 metre HFBR-3506 / HFBR-3606 / 15.0 metre HFBR-3507 / HFBR-3607 / 20.0 metre HFBR-3508 / HFBR-3608 / 25.0 metre HFBR-3589 / HFBR-3689 / 25.0 metre HFBR-3590 / HFBR-3690 / 100.0 metre HFBR-3591 / HFBR-3691 / 500.0 metre	connectored unconnectored	
Connectors HFBR-4501 HFBR-4511	Gray Connector/Crimp Ring Blue Connector/Crimp Ring	
Polishing Kit HFBR-4595	Polishing fixture, abrasive paper	

Miniature Link Family: Features — Glass fiber (100/400 μm). Precision metal connectors.

Products/Part Nos.	Description	Page No.
Evaluation Kit HFBR-0200	HFBR-1201 Transmitter, HFBR-2201 Receiver, 10 metre HFBR-3001 Mounting Hardware	6-13
Transmitter/Receiver Pairs HP Style Connectors / SMA Style Connectors HFBR-1201/-2201 / HFBR-1202/-2202 HFBR-1201/-2203 / HFBR-1202/-2204 HFBR-1203/-2201 / HFBR-1204/-2202 HFBR-1203/-2203 / HFBR-1204/-2204	Guaranteed Distance* / Guaranteed Data Rate* 800 metre / 5 MBd 1200 metre / 40 MBd 1800 metre / 5 MBd 2100 metre / 40 MBd	6-21, 6-25
Transceivers, 20 MBd (modified to 40 MBd) HP Style Connectors / SMA Style Connectors HFBR-0221 / HFBR-0222 HFBR-0223 / HFBR-0224	Guaranteed Distance / Data Format 1100 metre / 33 to 67% duty factor (for use with code schemes such as Manchester) 625 metre / STD 95% duty factor (for use with code schemes such as NRZ)	6-33
Cables Simplex / Duplex HFBR-3000 (OPT001) / HFBR-3100 (OPT001)	Customer specified length, connectored (HFBR-4000 connector)	6-53
HFBR-3000 (OPT002) / HFBR-3100 (OPT002)	Customer specified length, connectored (SMA style connector)	
HFBR-3200 / HFBR-3300	Customer specified length, unconnectored	6-55
HFBR-3001	10 metres connectored (HFBR-4000 connector)	
HFBR-3021	10 metres connectored (SMA style connector)	
Connectors HFBR-4000	Metal body, metal ferrule	6-57
HFBR-3099	Connector-connector junction, bulkhead feedthrough for HFBR-4000 connector	

*Link performance at 25°C.

FIBER OPTICS

Miniature Link Family: Features — Glass fiber (100/400 μm). Precision metal connectors. (Cont.)

Products/Part Nos.	Description	Page No.
Connector Assembly Tools HFBR-0100 HFBR-0101 HFBR-0102	Field installation kit for HFBR-4000 connectors (includes case, tools, consumables) Replacement consumables for HFBR-0100 Kit Custom tool set only	6-59
Mounting Hardware HFBR-4201 HFBR-4202	PCB mounting bracket, EMI shield, misc. hardware for HFBR-1201/-1203/-2201/-2203 PCB mounting bracket, EMI shield, misc. hardware for HFBR-1202/-1204/-2202/-2204	6-13

High Performance Module Family: Glass fiber (100/140 μm), Precision metal connectors, TTL compatible output, Link monitor, Transparent 3-level code

Products/Part Nos.		Description			Page No.
Evaluation Kit HFBR-0010		HFBR-1001 Transmitter, HFBR-2001 Receiver, 10 metre connectored cable, literature			
Transmitter/Receiver Pairs		Guaranteed Distance*	Guaranteed Data Rate*	Connector Style	
HFBR-1001/-2001		180 metre	10 MBd	HFBR-4000	6-41
HFBR-1002/-2001		1500 metre	10 MBd	HFBR-4000	6-45
Cables					
Simplex	Duplex				
HFBR-3000 (OPT001)	HFBR-3100 (OPT001)	Customer specified length, connectored (HFBR-4000 connector)			6-53
HFBR-3000 (OPT002)	HFBR-3100 (OPT002)	Customer specified length, connectored (SMA style connector)			
HFBR-3200	HFBR-3300	Customer specified length, unconnectored			6-55
HFBR-3001		10 metres connectored (HFBR-4000 connector)			
HFBR-3021		10 metres connectored (SMA style connector)			
Connectors HFBR-4000 HFBR-3099		Metal body, metal ferrule Connector-connector junction, bulkhead feedthrough for HFBR-4000 connector			6-57
Connector Assembly Tools HFBR-0100 HFBR-0101 HFBR-0102		Field installation kit for HFBR-4000 connectors (includes case, tools, consumables) Replacement consumables for HFBR-0100 Kit Custom tool set only			6-59

Data Communications Equipment

Products/Part Nos.	Description	Page No.
RS-232-C/V.24 to Fiber Optic Multiplexer 39301A Multiplexer	1250 metres length, 19.2 kbps/channel data rate, 16 channels RS-232-C Input/Output	6-61

PIN Photodiodes: Variety of packages, high speed, low capacitance, low noise.

Products/Part Nos.	Description	Page No.
5082-4200 Series	High Speed PIN Photodiodes for use in Fiber Optic Applications	6-67

*Link performance at 25°C.

HEWLETT PACKARD

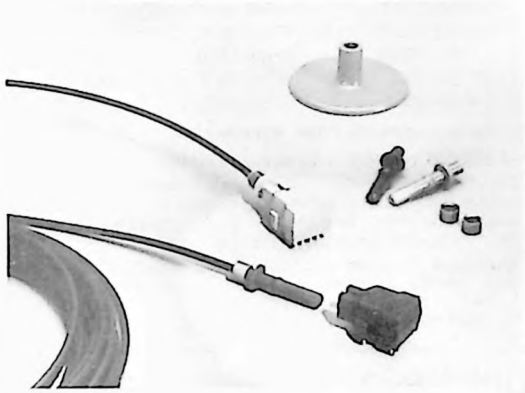
SNAP-IN FIBER OPTIC LINK

HFBR-0500 TO HFBR-4595

TECHNICAL DATA JANUARY 1984

Features

- LOW COST PLASTIC DUAL-IN-LINE PACKAGE
- SNAP-IN CONNECTOR
- 665 nm EMITTER OPTIMIZED FOR PLASTIC CABLE
- EASY FIELD TERMINATIONS
- SHIELDED RECEIVER FOR HIGH NOISE IMMUNITY
- OPERATION TO 22 METRES — GUARANTEED OVER TEMPERATURE
- DC TO 5 MBaud DATA RATE
- LSTTL/TTL COMPATIBLE OUTPUT LEVEL
- CHOICE OF INTERNAL PULL-UP OR OPEN COLLECTOR OUTPUT
- STANDARD OR SPECIAL LENGTH CABLES
- SINGLE +5V RECEIVER POWER SUPPLY
- COLOR CODED TRANSMITTER AND RECEIVER
- SIMPLEX AND ZIP CORD STYLE DUPLEX CABLE



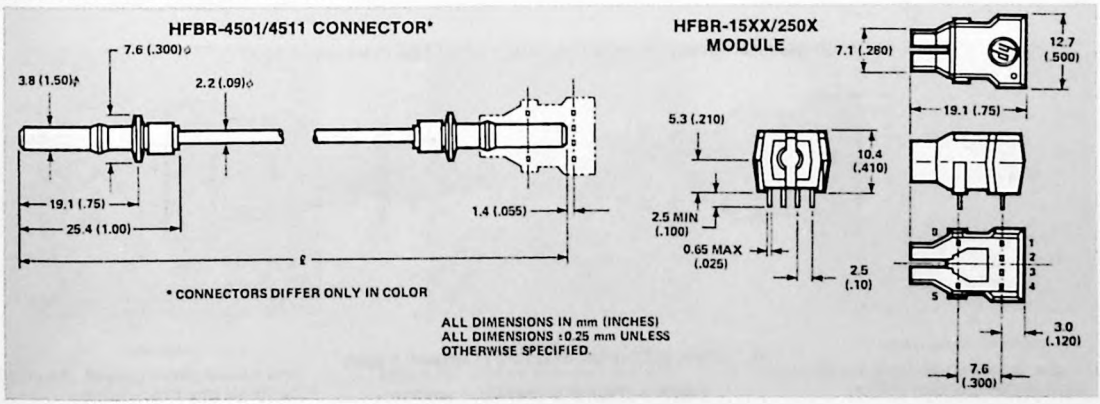
Description

The HFBR-0500 series is a complete family of fiber optic link components for configuring low-cost, short distance digital data transmission links. These components are designed to mate with plastic snap-in connectors and low-cost plastic fiber cable. Link design is simplified by the logic compatible receivers and the ease of terminating the plastic fiber cable. The key parameters of links configured with the HFBR-0500 family are fully guaranteed. The HFBR-0500 evaluation kit contains all the components and literature necessary to evaluate a working link.

Applications

- EMC REGULATED SYSTEMS (FCC, VDE)
- INTER/INTRA-SYSTEM DATA LINK
- STATIC PROTECTION
- HIGH VOLTAGE ISOLATION
- MEDICAL EQUIPMENT
- SECURE DATA COMMUNICATIONS

Mechanical Dimensions



FIBER OPTICS

Ordering Guide

Connectored Plastic Fiber Optic Cable

Single Channel	Dual Channel	Length* (metres)
HFBR-3500**	HFBR-3600**	Customer Specified
HFBR-3501	——	0.1
HFBR-3502	HFBR-3602	0.5
HFBR-3503	HFBR-3603	1
HFBR-3504	HFBR-3604	5
HFBR-3505	HFBR-3605	10
HFBR-3506	HFBR-3606	15
HFBR-3507	HFBR-3607	20
HFBR-3508	HFBR-3608	25

*All cable lengths are +10%, -0% tolerance.

**HFBR-3500, HFBR-3600 Ordering Information

These cable assemblies of customer specified length, have factory installed connectors. The length must be specified in 1 metre increments. The mandatory OPT 001, specifies the number of assemblies of equal length ordered.

EXAMPLE: To order 3 Duplex cable assemblies, 21 metres each, specify

HFBR-3600	Quantity 63
OPT 001	Quantity 3

Modules/Connectors

HFBR-1510/1501/1502 Transmitters
HFBR-2501/2502 Receivers
HFBR-4501 Gray Connector/Crimp Ring
HFBR-4511 Blue Connector/Crimp Ring

Unconnectored Plastic Fiber Optic Cable

Single Channel	Dual Channel	Length* (metres)
HFBR-3589	HFBR-3689	25
HFBR-3590	HFBR-3690	100
HFBR-3591	HFBR-3691	500

HFBR-4595 Polishing Kit

Polishing Fixture — Abrasive Paper

HFBR-0500 Evaluation Kit

HFBR-1510	Transmitter (Gray)
HFBR-2501	Receiver (Blue)
HFBR-3504	5m Connectored Cable
HFBR-4501	Connector/Crimp Ring (Gray)
HFBR-4511	Connector/Crimp Ring (Blue)
HFBR-4595	Polishing Kit

Technical Literature

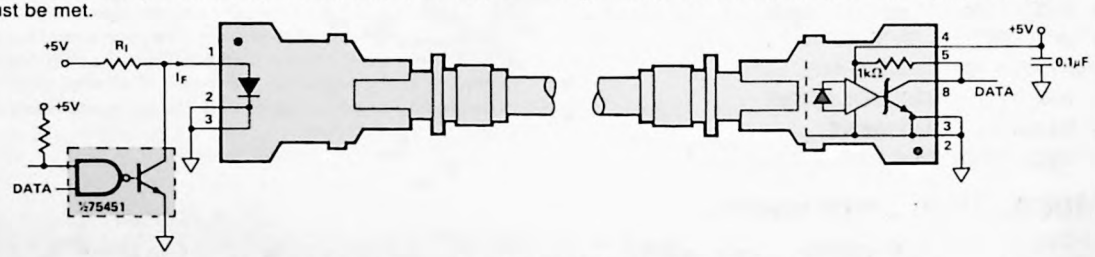
Link Design Considerations

The first step in designing the link is to choose either the HFBR-1510/2501, HFBR-1501/2501 or the HFBR-1502/2502 Transmitter/Receiver pair based on the data-rate and distance requirements. The value of the transmitter drive current, I_F, must be determined next from Figure 2. For the HFBR-1510/2501 and HFBR-1501/2501 pairs (Figure 2A and 2B), note that there is an upper as well as a lower limit on the value of I_F for any given distance. The dotted lines in Figure 2A, 2B and 2C represent pulsed operation. When operating in the pulsed mode, the conditions in Note 1 must be met.

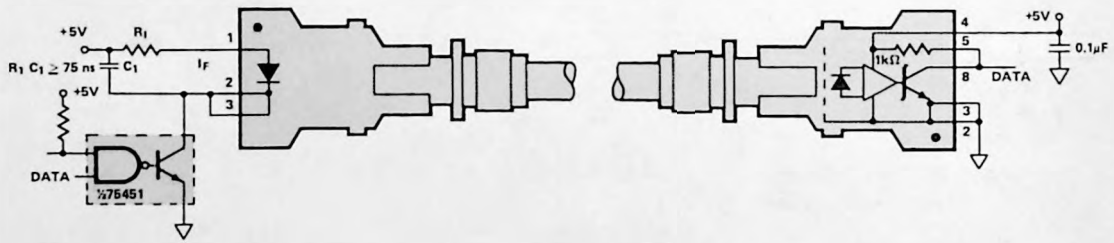
After selecting a value for the transmitter drive current I_F, the value of R_1 in Figure 1 can be calculated as follows:

$$R_1 = \frac{V_{CC} - V_F}{I_F}$$

For the HFBR-1502/2502 pair, the value of the capacitor, C_1 (Figure 1B), must be chosen such that $R_1 C_1 \geq 75$ ns.



A. HFBR-1510/HFBR-2501, HFBR-1501/HFBR-2501 Link (5 MBaud, ≤ 10m)



B. HFBR-1502/HFBR-2502 Link (1 MBaud, ≤ 22m)

Figure 1. Typical Circuit Configuration

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Ref.
AMBIENT TEMPERATURE	T_A	0	70	°C	
TRANSMITTER Peak Forward Current	$I_{F\,PK}$	10	750	mA	Note 1
Avg. Forward Current	$I_{F\,AV}$		60	mA	
RECEIVER Supply Voltage	V_{CC}	4.75	5.25	V	Note 2
Fan-Out (TTL)	N		5		
CABLE Long Term Bend Radius	r	35		mm	Note 3
Long Term Tensile Load	F_T		1	N	

System Performance

Parameter	Symbol	Min.	Typ. (17)	Max.	Units	Conditions	Ref.
HFBR-1510/HFBR-2501, HFBR-1501/HFBR-2501							
Data Rate		dc		5	MBd	BER ≤ 10^{-9}	
Transmission Distance HFBR-1510/HFBR-2501	ℓ	8 13			m m	I_{FPK} = 60 mA, 0-70° C I_{FPK} = 60 mA, 25° C	
Transmission Distance HFBR-1501/HFBR-2501	ℓ	10 17			m m	I_{FPK} = 60 mA, 0-70° C I_{FPK} = 60 mA, 25° C	
Propagation Delay	t_{PLH} t_{PHL}			140 140	ns ns	R_L = 560 Ω, C_L = 30 pF −21.6 ≤ ϕ_R ≤ −9.5 dBm	Fig. 5, 3 Note 4
Pulse Width Distortion	t_{SK}		30		ns	ϕ_R = −15 dBm	Fig. 4 Note 5
HFBR-1502/HFBR-2502							
Data Rate		dc		1	MBd	BER ≤ 10^{-9}	
Transmission Distance HFBR-1502/HFBR-2502	ℓ	16 23			m m	I_{FPK} = 60 mA, 0-70° C I_{FPK} = 60 mA, 25° C	
Transmission Distance (50% Duty Factor Max.)	ℓ	22 29			m m	I_{FPK} = 120 mA, 0-70° C I_{FPK} = 120 mA, 25° C	
Propagation Delay	t_{PLH} t_{PHL}			250 140	ns ns	R_L = 560Ω, C_L = 30 pF P_R = -24 dBm	Fig. 5, 3 Note 4
Pulse Width Distortion	t_{SK}		80		ns	P_R = -24 dBm	Fig. 4 Note 5
HFBR-150X/250X							
EMI Immunity			8000		V/m	BER ≤10^{-9}	

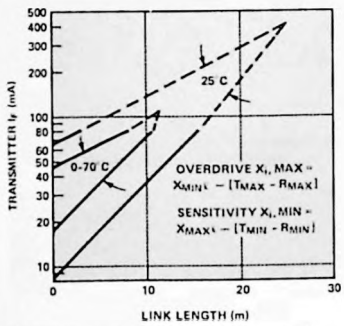


Figure 2A. System Performance with HFBR-1510 and HFBR-2501

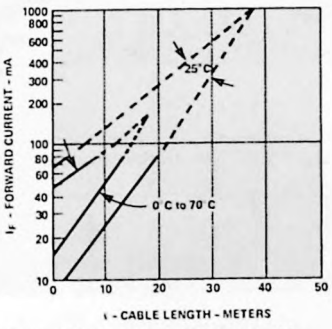


Figure 2B. System Performance with HFBR-1501 and HFBR-2501

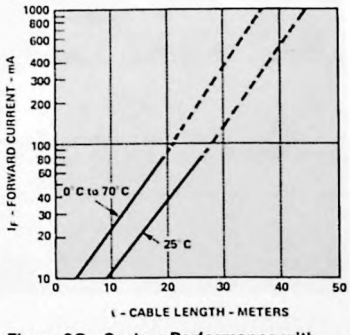
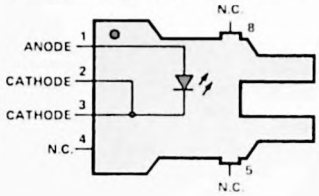


Figure 2C. System Performance with HFBR-1502 and HFBR-2502

Transmitters

The gray plastic HFBR-1510/1501/1502 Transmitter modules incorporate a 665nm LED targeted at the low attenuation window for the HFBR-3500/3600 plastic fiber optic cable. The transmitters can be easily interfaced to standard TTL logic. The optical power output of the HFBR-1510/1501/1502 is specified at the end of 0.5m of cable.

HFBR-1510/1501/1502 Transmitter



Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Ref.
Storage Temperature		T_S	-40	+75	°C	
Operating Temperature		T_A	0	+70	°C	
Lead Soldering Cycle	Temp			260	°C	Note 6
	Time			10	sec	
Peak Forward Input Current		$I_{F\,PK}$		1000	mA	Note 7
Average Forward Input Current		$I_{F\,AV}$		80	mA	
Reverse Input Voltage		V_R		5	V	

Electrical/Optical Characteristics (Cont.) 0° C to +70° C Unless Otherwise Specified

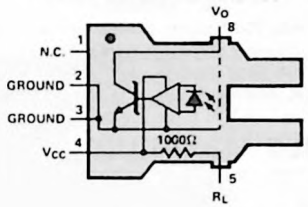
Parameter		Symbol	Min.	Typ.[17]	Max.	Units	Conditions	Ref.
Transmitter Output Optical Power	HFBR-1510	P_T	-16.5		-8.4	dBm	I_F = 60 mA, 0-70° C	Note 8 Note 9
			-13.3		-9.2	dBm	I_F = 60 mA, 25° C	
	HFBR-1501	P_T	-14.8		-8.4	dBm	I_F = 60mA, 0-70° C	
			-11.7		-9.3	dBm	I_F = 60mA, 25° C	
	HFBR-1502	P_T	-13.6		-5.5	dBm	I_F = 60mA, 0-70° C	
			-10.4		-6.4	dBm	I_F = 60mA, 25° C	
Output Optical Power Temperature Coefficient		$\frac{\Delta P_T}{\Delta T}$		-0.026		dB/° C		
Peak Emission Wavelength		λ_{PK}		665		nm		
Forward Voltage		V_F	1.45	1.67	2.02	V	I_F = 60 mA	
Forward Voltage Temperature Coefficient		$\frac{\Delta V_F}{\Delta T}$		-1.37		mV/° C		
Effective Diameter		D_T		1		mm		
Numerical Aperture		N.A.		0.5				
Reverse Input Breakdown Voltage		V_{BR}	5.0	12.4		V	I_F = -10 μA, T_A = 25° C	
Diode Capacitance		C_O		86		pF	V_F = 0, f = 1 MHz	

WARNING: When viewed under some conditions, the optical port of the Transmitter may expose the eye beyond the Maximum Permissible Exposure recommended in ANSI Z-136-1, 1981. Under most viewing conditions there is no eye hazard.

Receivers

The blue plastic HFBR-2501/2502 Receiver modules feature a shielded integrated photodetector and wide bandwidth DC amplifier for high EMI immunity. A Schottky clamped open-collector output transistor allows interfacing to common logic families and enables "wired-OR" circuit designs. The open collector output is specified up to 18V. An integrated 1000 ohm resistor internally connected to V_{CC} may be externally jumpered to provide a pull-up for ease-of-use with +5V logic. The combination of high optical power levels and fast transitions falling edge could result in distortion of the output signal (HFBR-2502 only), that could lead to multiple triggering of following circuitry. Optical power waveshaping circuitry as in Figure 1B may be required for proper link operation.

HFBR-2501/2502 Receiver



Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Ref.
Storage Temperature		T_S	-40	+75	°C	
Operating Temperature		T_A	0	+70	°C	
Lead Soldering Cycle	Temp			260	°C	Note 6
	Time			10	sec	
Supply Voltage		V_{CC}	-0.5	7	V	
Output Collector Current		I_O		25	mA	
Output Collector Power Dissipation		P_{OD}		40	mW	
Output Voltage		V_O	-0.5	18	V	
Pullup Voltage		V_{RL}	-0.5	V_{CC}	V	

Electrical/Optical Characteristics (Cont.) 0°C to +70°C Unless Otherwise Specified

Parameter		Symbol	Min.	Typ.(17)	Max.	Units	Conditions	Ref.
Receiver Input Optical Power Level for Logic "0"	HFBR-2501	$P_{R(L)}$	-21.6		-9.5	dBm	0-70°C, V_{OL} = 0.5V I_{OL} = 8 mA	Note 9, 10
			-21.6		-8.7	dBm	25°C, V_{OL} = 0.5V I_{OL} = 8 mA	
	HFBR-2502	$P_{R(L)}$	-24			dBm	0-70°C, V_{OL} = 0.5V I_{OL} = 8 mA	
			-24			dBm	25°C, V_{OL} = 0.5V I_{OL} = 8 mA	
Input Optical Power Level for Logic "1"		$P_{R(H)}$			-43	dBm	V_{OH} = 5.25V, $I_{OH} \leq 250\ \mu A$	Note 9
High Level Output Current		I_{OH}		5	250	μA	V_O = 18V, P_R = 0	Note 16
Low Level Output Voltage		V_{OL}		0.4	0.5	V	I_{OL} = 8 mA, $P_R = P_{RL\ MIN}$	Note 16
High Level Supply Current		I_{CCH}		3.5	6.3	mA	V_{CC} = 5.25V, ϕ_R = 0	Note 16
Low Level Supply Current		I_{CCL}		6.2	10	mA	V_{CC} = 5.25V, P_R = -12.5 dBm	Note 16
Effective Diameter		D_R		1		mm		
Numerical Aperture		N.A.R		0.5				
Internal Pull-Up Resistor		R_L		1000		Ohms		

FIBER OPTICS

Plastic Fiber Cable

The HFBR-3500/3600 series cables contain 1mm diameter plastic fibers. These cables are extremely easy to connector. Simplex (HFBR-3500) and Duplex (HFBR-3600) cables are available with or without factory installed connectors.

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Ref.
Storage Temperature		T_S	-40	+75	°C	
Installation Temperature		T_I	-20	+70	°C	
Tensile Force	(Single Channel)	F_T		50	N	Note 11
	(Dual Channel)	F_T		100	N	
	Cable/Connector	F_T		5	N	
Bend Radius		r	10		mm	Note 12
Flexing				1000	Cycles	Note 13
Impact		m		1	kg	Note 14
		h		15	mm	

Electrical/Optical Characteristics 0°C to +70°C Unless Otherwise Specified

Parameter	Symbol	Min.	Typ. (17)	Max.	Units	Conditions	Ref.
Link Coupling Variation	$\Delta\alpha_{LC}$		0.9	2.0	dB		Note 15
Cable Attenuation	α_0	0.3	0.45	0.63	dB/m	@665 nm Source NA = 0.5	
Numerical Aperture	N.A.		0.5			$\ell > 2$ m	
Diameter, Core	D_C		1.0		mm		
Diameter, Jacket	D_J		2.3		mm	Simplex Cable	
Travel Time Constant	I/V		5.0		nsec/m		
Mass per Unit Length/Channel	m/ℓ		4.6		g/m	Without Connectors	
Cable Leakage Current	I_L		1		nA	50 kV, $\ell = 0.3$m	

CABLE TERMINATIONS

Connectoring the cable is accomplished with the Hewlett-Packard HFBR-4595 Polishing Kit consisting of a Polishing Fixture and 600 grit abrasive paper. No adhesive material is needed to secure the cable in the connector, and the connector can be used immediately after polishing.

Connectors may be easily installed on the cable ends with readily available tools. Materials needed for the terminating procedure are:

1) HFBR-3500/3600 Fiber Optic Cable
2) HFBR-4595 Polishing Fixture, 600 grit sand paper
3) HFBR-4501 Connector crimp ring (gray)
4) HFBR-4511 Connector crimp ring (blue)
5) Industrial Razor Blade
6) 16 gauge latching wire strippers
7) Crimp Tool, AMP 90364-2

The zip cord structure of the HFBR-3600 duplex cable permits easy separation of the channels. The channels should be separated approximately 50 mm back from the ends to permit connectoring and polishing.

After cutting the cable to the desired length, strip off approximately 7 mm (0.275 in) of the outer jacket with the 16 guage wire strippers.

Place the crimp ring and connector over the end of the cable; the fiber should protrude about 3 mm (0.120 in) through the end of the connector. Carefully position the ring so that it is entirely on the connector and then crimp the ring in place with the crimping tool.

NOTE: Place the gray connector on the cable end to be connected to the transmitter and the blue connector on the cable end to be connected to the receiver to maintain the color coding (both connectors are the same mechanically).

Any excess fiber protruding from the connector end may be trimmed with the razor blade; however, the trimmed fiber should extend at least 1.5 mm (0.060 in) from the connector end.

Insert the connector fully into the polishing fixture with the connector end protruding from the bottom of the fixture.

NOTE: The four dots on the bottom of the polishing fixture are wear indicators. Replace the polishing fixture when any dot is no longer visible.

Using a figure-eight motion of the polishing fixture on the 600 grit abrasive, trim the fiber and the connector until the connector is flush with the end of the polishing fixture. The fiber end should be flat and smooth with no large irregularities.

The cable can now be used.

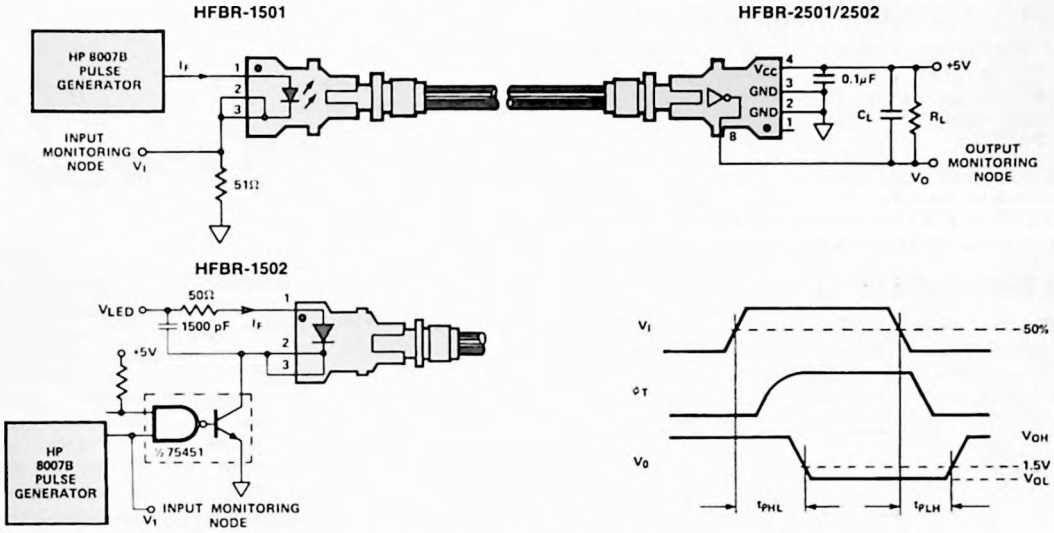


Figure 3. AC Test Circuit

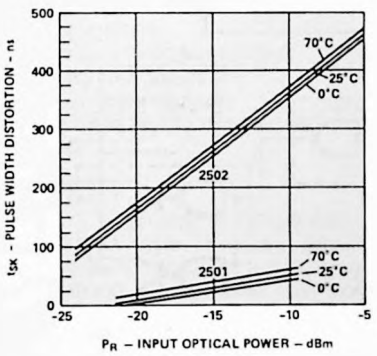


Figure 4. Pulse Width Distortion vs. Optical Power

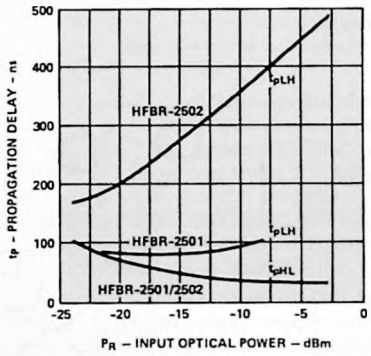


Figure 5. Propagation Delay vs. Optical Power

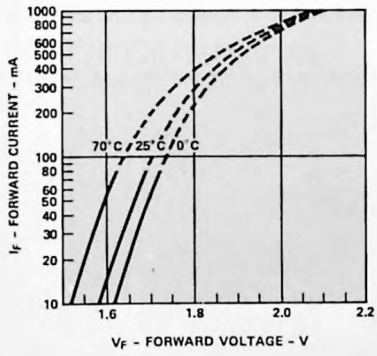


Figure 6. Forward Current vs. Forward Voltage

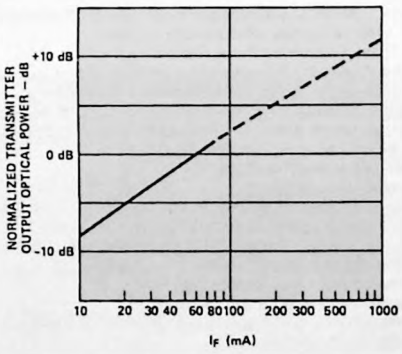


Figure 7. Normalized Transmitter Output Optical Power vs. Input Current

FIBER OPTICS

Optic Power Measurement

The optical power at the end of the HFBR-3500 series Fiber Optic Cable can be easily measured using a large area Radiometer such as the EG&G-550, Photodyne 88XL, or United Detector Technology S550, that has been calibrated at 665 nm.

The output optical power for the Transmitter has been specified at the end of 0.5 metres of HFBR-3500 Fiber Optic Cable and can therefore be easily measured using one of the above instruments.

Extended Distance Operation

Distances greater than 22m (0 - 70°C), are achievable by using high peak current pulses to drive the Transmitter. I_{FAV} must be limited to 80 mA and I_{FPK} to 1000 mA. The pulse width must be controlled. (Note 1).

Figure 8 shows a simple circuit suitable for RS-232 applications using the HFBR-1502 Transmitter and HFBR-2502 Receiver for 30 metre operation.

I_{FPK} = 500 mA (From Figure 2B, ℓ = 31m); I_{FAV} = 25 mA at a Data Rate of 55 Kbd or less, Pulse Width Distortion < 25% (4.5 μs max.)

NOTE: I_{FPK} up to 1000 mA may be used for distances up to 35m.

An MOS clock driver may be used to provide transient current sinking capability up to 1000 mA.

Even longer distances can be achieved using specially selected components — contact your local Hewlett-Packard Sales Representative.

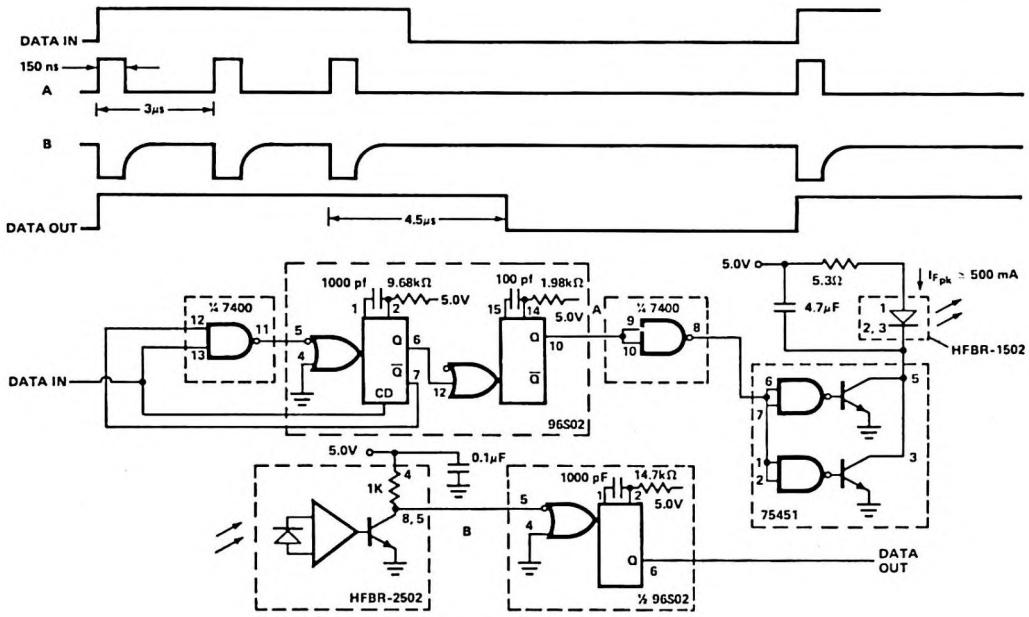


Figure 8. Pulsed Operation

NOTES:

1. For I_{FPK} > 80 mA, the duty factor must be such as to keep $I_{FAV} \leq$ 80 mA. In addition, for I_{FPK} > 80 mA, the following rules for pulse width apply:
   $I_{FPK} \leq$ 160 mA : Pulse width $\leq$ 1 ms
   I_{FPK} > 160 mA : Pulse width $\leq$ 1 μs
2. It is essential that a bypass capacitor (0.01 μF to 0.1 μF ceramic) be connected from pin 3 to pin 4 of the receiver. Total lead length between both ends of the capacitor and the pins should not exceed 20 mm.
3. See cable absolute maximum ratings for short-term bend radius and tensile load.
4. The propagation delay of 1m of cable (5 ns) is included.
5. $t_{SK} = t_{PLH} - t_{PHL}$; R_L = 560Ω, C_L = 30 pF.
6. 1.6 mm below seating plane.
7. 1 μs pulse, 20 μs period.
8. Measured at the end of 0.5m HFBR-3502 Fiber Optic Cable with a large area detector.
9. Optical flux, P (dBm) = 10 Log P (μW)/1000 μW.
10. Measured at the end of HFBR-3500 Fiber Optic Cable with large area detector.
11. Less than 30 minutes.
12. Less than 1 hour, non-operating.
13. 90° bend on 10 mm radius mandrel.
14. 1 Kg weight dropped from 15 mm height on 2.5 mm radius mandrel laid on cable.
15. Included in P_T and P_R.
16. R_L is open.
17. Typical data at 25°C, V_{CC} = 5 V_{dc}.

HEWLETT PACKARD

MINIATURE FIBER OPTIC LOGIC LINK

HFBR-0200
HFBR-1201/2
HFBR-2201/2
HFBR-4201/2

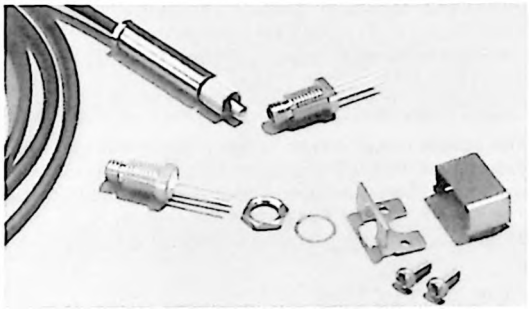
TECHNICAL DATA JANUARY 1984

Features

- DC TO 5 MBAUD DATA RATE
- MAXIMUM LINK LENGTH
  625 Metres (Guaranteed)
  1600 Metres (Typical)
- TTL/CMOS COMPATIBLE OUTPUT
- MINIATURE, RUGGED METAL PACKAGE
- SINGLE +5V RECEIVER POWER SUPPLY
- INTERNALLY SHIELDED RECEIVER FOR EMI/RFI IMMUNITY
- PCB AND PANEL MOUNTABLE
- LOW POWER CONSUMPTION

Applications

- EMC REGULATED SYSTEMS (FCC, VDE)
- EXPLOSION PROOF SYSTEMS IN OIL INDUSTRY/CHEMICAL PROCESS CONTROL INDUSTRY
- SECURE DATA COMMUNICATIONS
- WEIGHT SENSITIVE SYSTEMS (e.g. Avionics, Mobile Stations)
- HIGH VOLTAGE ISOLATION IN POWER GENERATION



Description

The HFBR-1201/2 Transmitter and HFBR-2201/2 Receiver are HFBR-4000/SMA style connector compatible fiber optic link components. Distances to 1600 metres at data rates up to 5 MBaud are achievable with these components and the HFBR-3000/3100 series fiber optic cable assemblies.

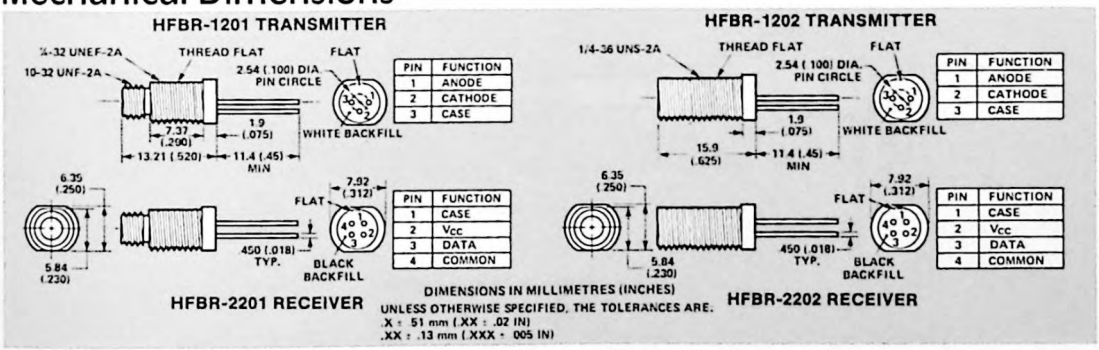
A complete evaluation kit is available (HFBR-0200) containing an HFBR-1201 transmitter, HFBR-2201 receiver, HFBR-4201 mounting hardware, 10m of HFBR-3000 option 001 cable/connector assembly and technical literature.

The HFBR-1201/2 Transmitter contains a high efficiency GaAlAs emitter operating at 820 nm. Consistent coupling efficiency is assured by factory alignment of the LED with the optical axis of the package. Power coupled into the fiber varies less than 4 dB from part to part at a given temperature and drive current. The benefit of this is reduced dynamic range requirements on the receiver.

The HFBR-2201/2 Receiver incorporates a photo IC containing a photodetector and dc amplifier. An open collector Schottky transistor on the IC provides logic compatibility. The combination of an internal EMI shield, the metal package and an isolated case ground provides excellent immunity to EMI/RFI. For unusually severe EMI/ESD environments, a snap-on metal shield is available. The receiver is easily identified by the black epoxy backfill.

The HFBR-1201 Transmitter and the HFBR-2201 Receiver are compatible with the HFBR-4000 Connector and HFBR-3000 series, Option 001 connectored cable. The HFBR-1202 Transmitter and HFBR-2202 Receiver are compatible with SMA style connectors, types A and B (see Figure 12), and HFBR-3000 series, Option 002 connectored cable. HFBR-3000 series cable can be ordered with or without connectors. The HFBR-0100 connector assembly kit is available if field installation of HFBR-4000 connectors is desired.

Mechanical Dimensions



FIBER OPTICS

System Design Considerations

The Miniature Fiber Optic Logic Link is guaranteed to work over the entire range of 0 to 625 metres at a data rate of dc -5 MBd, with arbitrary data format and typically less than 25% pulse width distortion, if the Transmitter is driven with I_F = 40 mA, R_1 = 82Ω. If it is desired to economize on power or achieve lower pulse distortion, then a lower drive current (I_F) may be used. The following example will illustrate the technique for optimizing I_F.

EXAMPLE: Maximum distance required = 250 metres. From Figure 2 the worst case drive current = 20 mA. From the Transmitter data — V_F = 1.8V (max.).

$$R_1 = \frac{V_{CC} - V_F}{I_F} = \frac{5 - 1.8V}{20\ mA} = 160\Omega$$

The optical power margin between the typical and worst case curves (Figure 2) at 250 metres is 4 dB. To calculate the worst case pulse width distortion at 250 metres, see Figure 8. The power into the Receiver is P_{RL} + 4 dB = -20 dBm. Therefore, the typical distortion is 40 ns or 20% at 5 MBd.

CABLE SELECTION

The link performance specifications on the following page are based on using the HFBR-3000/HFBR-3100 cable/connector assemblies. These cables contain glass-clad silica fibers with a 100 μm core diameter and 140 μm cladding diameter. This fiber type is now a user accepted standard for local data communications links (RS-458, Class I, Type B). The HFBR-1201/2 Transmitter and HFBR-2201/2 Receiver are optimized for use with the 100/140 μm fiber. There is, however, no fundamental restriction against using other fiber types. Before selecting an alternate fiber type, several parameters need to be carefully evaluated.

The attenuation (dB/km) of the selected fiber, in conjunction with the amount of optical power coupled into it will determine the achievable link length. The parameters that will significantly affect the optical power coupled into the fiber are as follows:

a. **Fiber Core Diameter.** As the core diameter is increased, the optical power coupled increases, leveling off at about 250 μm diameter.
b. **Numerical Aperture (NA).** As the NA is increased, the optical power coupled increases, leveling off at an NA of about 0.34.
c. **Index Profile (α).** The Index profile parameter of fibers varies from 2 (fully graded index) to infinite (step index). Some gains in coupled optical power can be achieved at the expense of bandwidth, when α is increased.

In addition to the optical parameters, the environmental performance of the selected fiber/cable must be evaluated. Finally, the ease of installing connectors on the selected fiber/cable must be considered. Given the large number of parameters that must be evaluated when using a non-standard fiber, it is recommended that the 100/140 μm fiber be used unless unusual circumstances warrant the use of an alternate fiber/cable type.

SMA STYLE CONNECTORS

The HFBR-1202/2202 is compatible with either the Type A or Type B SMA style fiber optic conector (see Figure 12). The basic difference between the two connectors is the plastic half-sleeve on the stepped ferrule tip of the Type B connector. This step provides the capability to use a full length plastic sleeve to ensure good alignment of two connectors for an inline splice. The HFBR-3000/HFBR-3100, OPT 002 series connectored cable utilizes the Type A connector system because of the inherent environmental advantages of metal-to-metal interfaces.

The HFBR-1201/2201 is compatible with HFBR-4000 connectors and HFBR-3000/HFBR-3000 Option 001 series connectored cable

Typical Circuit Configuration

NOTE:
IT IS ESSENTIAL THAT A BYPASS CAPACITOR (0.01 μF to 0.1 μF CERAMIC) BE CONNECTED FROM PIN 2 TO PIN 4 OF THE RECEIVER. TOTAL LEAD LENGTH BETWEEN BOTH ENDS OF THE CAPACITOR AND THE PINS SHOULD NOT EXCEED 20 mm.

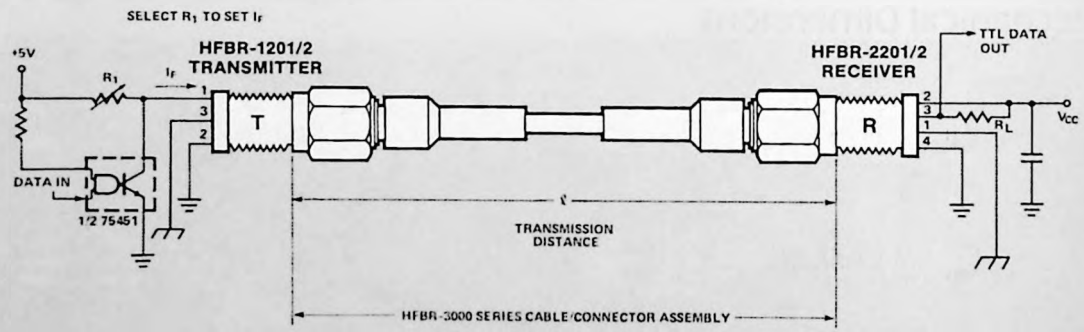


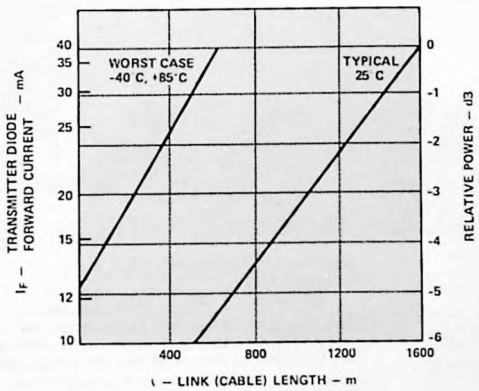
Figure 1.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Reference
TRANSMITTER					
Ambient Temperature	T_A	-40	+85	°C	
Peak Forward Input Current	$I_{F,PK}$		40	mA	Note 7
Average Forward Input Current	I_{FAV}		40	mA	Note 7
RECEIVER					
Ambient Temperature	T_A	-40	+85	°C	
Supply Voltage	V_{CC}	4.75	5.25	V	
Fan Out (TTL)	N		5		Note 3, Fig. 1
CABLE (see HFBR-3000/HFBR-3100 data sheet)					

System Performance -40° C to +85° C unless otherwise specified

Parameter	Symbol	Min.[1]	Typ.	Max.	Units	Conditions	Reference
Transmission Distance	ℓ	625	1600		Metres		Fig. 2, Note 9
Data Rate Synchronous		dc		5	MBaud		Note 10
Asynchronous		dc		2.5	MBaud		Note 10, Fig. 8
Propagation Delay LOW to HIGH	t_{PLH}		82		nsec	T_A = 25° C, P_R = -21 dBm $I_{F,PK}$ = 15 mA ℓ = 1 metre	Fig. 7, 8, 9
Propagation Delay HIGH to LOW	t_{PHL}		55		nsec		
System Pulse Width Distortion	t_D		27		nsec		
Bit Error Rate	BER			10^{-9}		Data Rate ≤5 MBaud P_R > -24 dBm (4μW)	



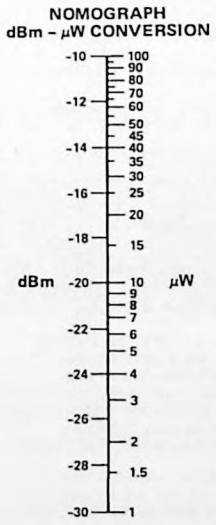


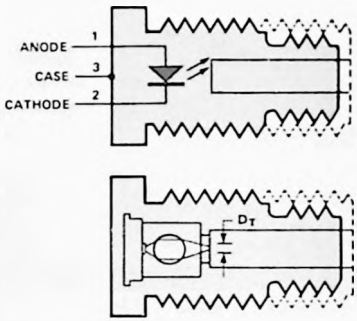
Figure 2. System Performance: HFBR-1201/2/HFBR-2201/2 with HFBR-3000/3100 Cable Assembly

FIBER OPTICS

HFBR-1201/1202 TRANSMITTER

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Unit	Reference
Storage Temperature		T_S	-55	+85	°C	
Operating Temperature		T_A	-40	+85	°C	Note 13
Lead Soldering Cycle	Temp.			+260	°C	Note 2
	Time			10	sec	
Forward Input Current	Peak	$I_{F\ PK}$		40	mA	Note 7
	Average	$I_{F\ AV}$		40	mA	
Reverse Input Voltage		V_R		2.5	V	



Electrical/Optical Characteristics

-40° C to +85° C unless otherwise specified

Parameter	Symbol	Min.	Typ.[1]	Max.	Units	Conditions	Reference
Forward Voltage	V_F		1.5	1.8	V	I_F = 40 mA	Figure 5
Forward Voltage Temperature Coefficient	$\Delta V_F/\Delta T$		-0.91		mV/° C	I_F = 40 mA	Figure 5
Reverse Breakdown Voltage	V_{BR}	2.5	4.0		V	I_R = 100 μA	
Numerical Aperture	NA		.34				
Optical Port Diameter	D_T		250		μm		Note 11
Peak Emission Wavelength	λ_P		820		nm		Figure 6
Output Optical Power Coupled into HFBR-3000 Fiber Cable/Connector Assembly, 100/140 μm	P_T	-17	-16	-13	dBm	I_F = 40 mA	Figure 3
		20	25	50	μW	T_A = 25° C	Notes 4, 15
		-18		-12.3	dBm	I_F = 40 mA	
		15.8		59	μW	-40° C < T_A < 85° C	
Output Optical Power Coupled into 50/125 μm Fiber	P_T		-24		dBm	I_F = 40 mA	Figure 3
			4		μW	T_A = 25° C	Notes 14, 15
Optical Power Temperature Coefficient	$\Delta P_T/\Delta T$		-.017		dB/° C		Figure 4

Dynamic Characteristics

-40° C to +85° C unless otherwise specified

Parameter	Symbol	Min.	Typ.[1]	Max.	Units	Conditions	Reference
Propagation Delay LOW to HIGH	t_{PLH}		17		nsec	$I_{F\ PK}$ = 10 mA	Note 8 Figure 7
Propagation Delay HIGH to LOW	t_{PHL}		6		nsec		

Notes:

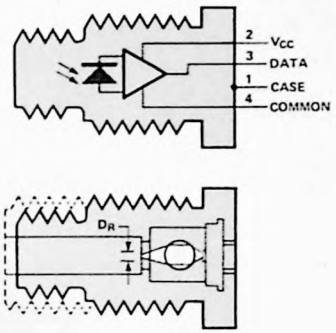
1. Typical data at T_A = 25° C, V_{CC} = 5.0V dc.
2. 2.0 mm from where leads enter case.
3. 8 mA load (5 x 1.6 mA), R_L = 560Ω.
4. Measured at the end of 1.0 metre HFBR-3000 Fiber Optic Cable (NA = 0.28) with large area detector and cladding modes stripped (NA = 0.28). This approximates a Standard Test Fiber.
5. Measured at the end of HFBR-3000 Fiber Optic Cable with large area detector.
6. When changing microwatts to dBm, the optical flux is referenced to one milliwatt (1000 μW).
   Optical Flux, P (dBm) = $10 \log \frac{P\ (\mu W)}{1000\ \mu W}$
7. I_{FPK} should not be less than 10 mA in the "ON" state. This is to avoid the long turn-on time that occurs at low input current. I_{FAV} may be arbitrarily low, as there is no duty factor restriction.

WARNING: OBSERVING THE TRANSMITTER OUTPUT POWER UNDER MAGNIFICATION MAY CAUSE INJURY TO THE EYE. When viewed with the unaided eye, the infrared output is radiologically safe; however, when viewed under magnification, precaution should be taken to avoid exceeding the limits recommended in ANSI Z136.1-1981.

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Reference
Storage Temperature		T_S	-55	+85	°C	
Operating Temperature		T_A	-40	+85	°C	
Lead Soldering Cycle	Temp.			+260	°C	Note 2
	Time			10	sec	
Supply Voltage		V_{CC}	-0.5	+7.0	V	
Output Current		I_O		25	mA	
Output Voltage		V_O	-0.5	+18.0	V	
Output Collector Power Dissipation		$P_{O,AV}$		40	mW	

HFBR-2201/2202 RECEIVER



Electrical/Optical Characteristics -40°C to +85°C unless otherwise specified

Parameter	Symbol	Min.	Typ.[1]	Max.	Units	Conditions	Reference
High Level Output Current	I_{OH}		5	250	μA	V_O = 18V P_R < -40 dBm	
Low Level Output Voltage	V_{OL}		0.4	0.5	V	I_O = 8 mA P_R > -24 dBm	
High Level Supply Current	I_{CCH}		3.5	6.3	mA	V_{CC} = 5.25 V P_R < -40 dBm	
Low Level Supply Current	I_{CCL}		6.2	10	mA	V_{CC} = 5.25 V P_R > -24 dBm	
Optical Port Diameter	D_R		700		μm		Note 12
Numerical Aperture	NA		.32				

Dynamic Characteristics -40°C to +85°C unless otherwise specified

Parameter	Symbol	Min.	Typ.[1]	Max.	Units	Conditions	Reference
Input Power Level Logic HIGH	P_{RH}			-40 0.1	dBm μW	λ_P = 820 nm	Note 5
Input Power Level Logic LOW	P_{RL}	-25.4		-11.2	dBm	T_A = +25°C	Fig. 4, Note 5
		2.9		76	μW		
		-24		-12.0	dBm	-40 < T_A < 85°C	
		4.0		63	μW		
Propagation Delay LOW to HIGH	t_{PLHR}		65		nsec	T_A = 25°C, P_R = -21 dBm	Note 8, Fig. 7
Propagation Delay HIGH to LOW	t_{PHLR}		49		nsec		

Notes:

8. Propagation delay through the system is the result of several sequentially-occurring phenomena. Consequently it is a combination of data-rate-limiting effects and of transmission-time effects. Because of this, the data-rate limit of the system must be described in terms of time differentials between delays imposed on falling and rising edges.

   As the cable length is increased, the propagation delays increase at 5 ns per metre of length increase. Data rate, as limited by pulse width distortion, is not affected by increasing cable length if the optical power level at the Receiver is maintained.
9. Worst case system performance is based on worst case performance of individual components: transmitter at +85° C, receiver at -40° C and cable at- 20° C.
10. Synchronous data rate limit is based on these assumptions: (a) 50% duty factor modulation, e.g. Manchester I or BiPhase (Manchester II); (b) continuous data; (c) PLL (Phase Lock Loop) demodulation; (d) TTL threshold.

    Asynchronous data rate limit is based on these assumptions: (a) NRZ data; (b) arbitrary timing — no duty factor restriction; (c) TTL threshold.

    The EYE pattern describes the timing range within which there is no uncertainty of the logic state, relative to a specific threshold, due to either noise or intersymbol (prop. delay) effects.
11. D_T is measured at the plane of the fiber face and defines a diameter where the optical power density is within 10 dB of its maximum.
12. D_R is the effective diameter of the detector image on the plane of the fiber face. The numerical value is the product of the actual detector diameter and the lens magnification.
13. HFBR-3000 series Fiber Cable is specified at a narrower temperature range, -20° C to 85° C.
14. Measured at the end of 1.0 metre 50/125 μm fiber with large area detector and cladding modes stripped (NA = 0.22). This fiber approximates a Standard Test Fiber. The test fiber is terminated with an SMA style connector.
15. Output Optical Power into connectored fiber cable other than HFBR-3000 Fiber Optic Cable/Connector Assemblies may be different than specified because of mechanical tolerances of the connector, quality of the fiber surface, and other variables.

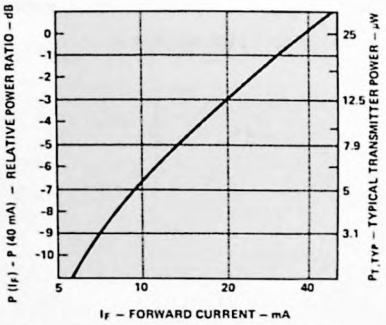


Figure 3. Normalized Transmitter Output vs. Forward Current

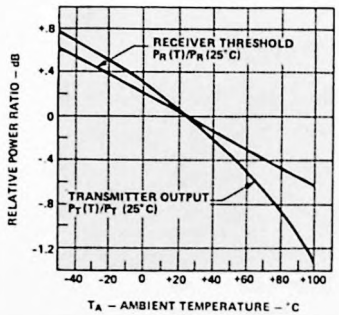


Figure 4. Normalized Thermal Effects in Transmitter Output, Receiver Threshold, and Link Performance (Relative Threshold)

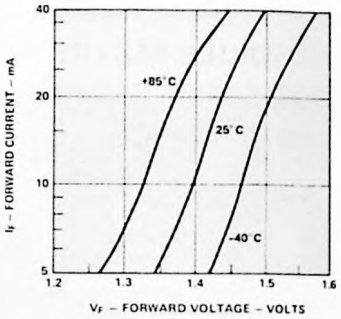


Figure 5. Forward Voltage and Current Characteristics for the Transmitter LED.

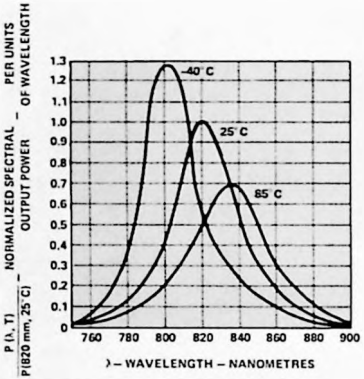


Figure 6. Transmitter Spectrum Normalized to the Peak at 25°C

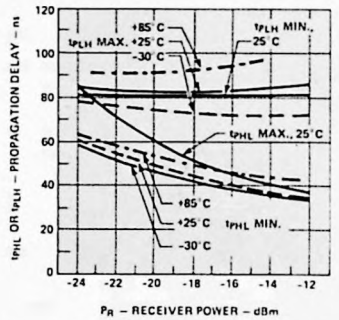


Figure 7. Propagation Delay through System with One Metre of Cable

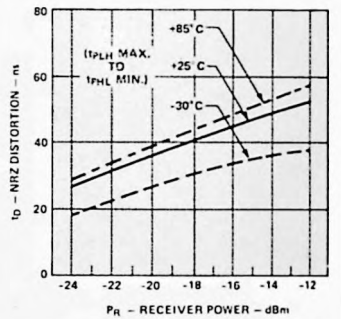
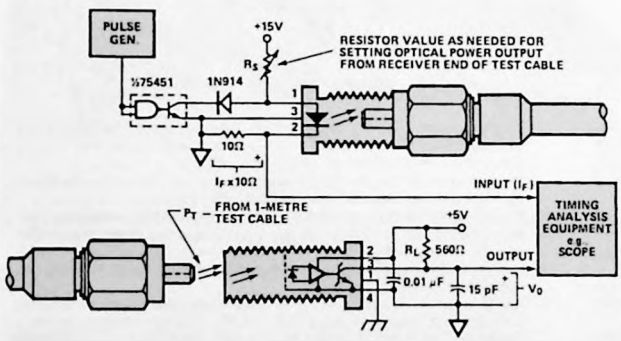


Figure 8. Worst-Case Distortion of NRZ EYE-pattern with Pseudo Random Data at 10 Mb/s. (see note 10).



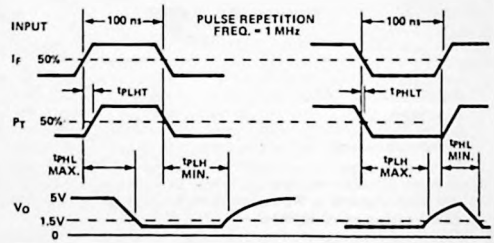


Figure 9. System Propagation Delay Test Circuit and Waveform Timing Definitions

Electrical Description

The HFBR-1201/2 Transmitter contains a GaAlAs infrared emitter. Both the anode and cathode of the emitter are insulated from the case. This configuration permits the use of a variety of drive circuitry such as series switching, shunt-switching and high frequency peaking. There is no internal drive circuit or current limiter.

The HFBR-2201/2 Receiver incorporates an integrated photo IC containing a photodetector and dc amplifier driving an open-collector Schottky output transistor. The HFBR-2201/2 is designed for direct interfacing to popular logic families. The absence of an internal pull-up resistor allows the open-collector output to be used with logic families such as CMOS requiring voltage excursions much higher than V_{CC}. Both the open-collector "Data" output (Pin 3) and V_{CC} (Pin 2) are referenced to "Com" (Pin 4). The "Data" output allows busing, strobing and wired "OR" circuit configurations. Both the transmitter and receiver are designed to operate from a single +5V supply. Note that the "Com" and "Case" pins are not connected internally.

The HFBR-1201/2 and HFBR-2201/2 optical receptacles contain a lens to optimize the coupling between the fiber and the active optical device.

Horizontal PCB Mounting

Mounting at the edge of a printed circuit board with the lock nut overhanging the edge is recommended.

When bending the leads, avoid sharp bends right where the lead enters the backfill. Use needle nose pliers to support the leads at the base of the package and bend the leads as desired.

When soldering, it is advisable to leave the protective cap on the unit to keep the optics clean.

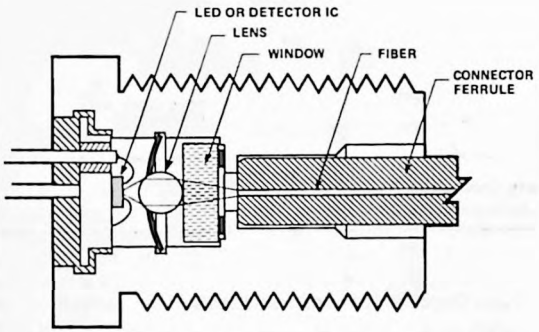


Figure 10. Cross Sectional View

Mechanical Description

The HFBR-1201/2 fiber optic transmitter and HFBR-2201/2 receiver are housed in rugged metal packages intended for use with the HFBR-3000/HFBR-3100 cable assemblies. The low profile package is designed for direct mounting on printed circuit boards or through panels without additional heat sinking. A flat on the mounting threads of the device is provided to prevent rotation in all mounting configurations and to provide an orientation reference for the pin-out. Hardware is available for horizontal mounting applications on printed circuit boards. The hardware consists of a stainless steel mounting bracket fastened directly to the printed circuit board with two stainless steel self-tapping screws and a nut and washer for fastening the device in the bracket. A metal shield which snaps directly on the mounting bracket is also available for unusually severe EMI/ESD environments. When mounted in the horizontal configuration, the overall height of the component conforms with guidelines allowing printed circuit board spacing on 12.7 mm (.500) centers. A thorough environmental characterization has been performed on these products. The test data as well as information regarding operation beyond the specified limits is available from any Hewlett-Packard sales office.

Good system performance requires clean port optics and cable ferrules to avoid obstructing the optical path. Clean compressed air often is sufficient to remove particles of dirt; methanol or Freon™ on a cotton swab also works well.

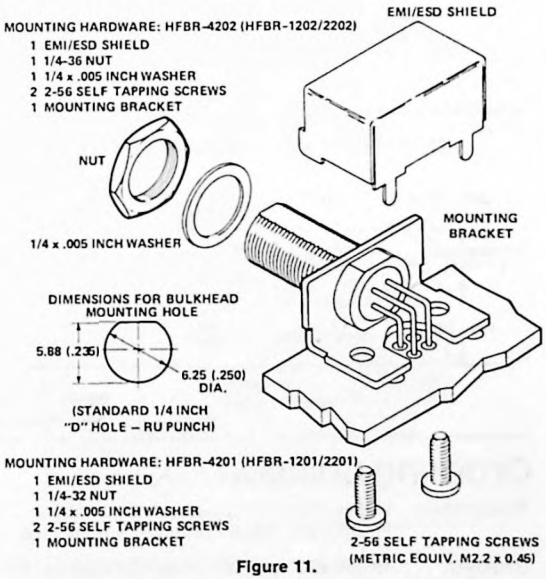


Figure 11.

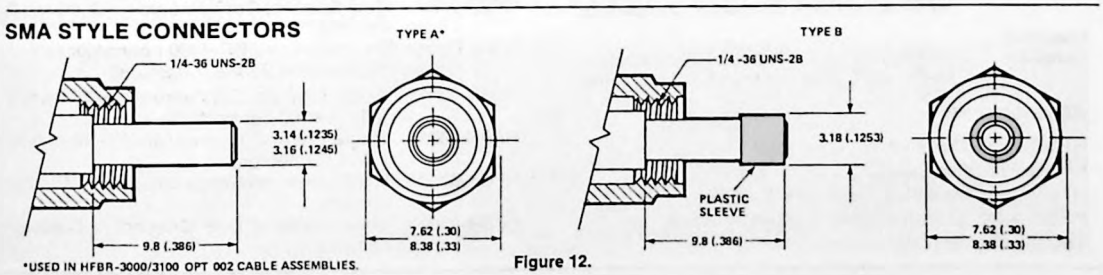
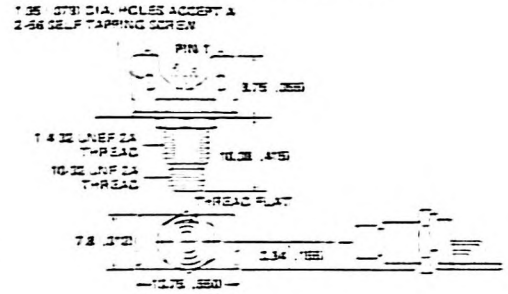
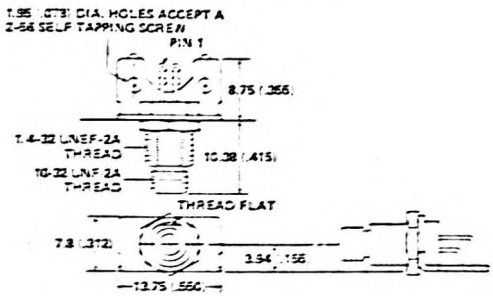


Figure 12.

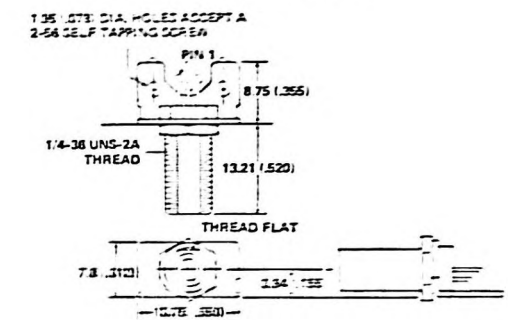
HFBR-1201 TRANSMITTER



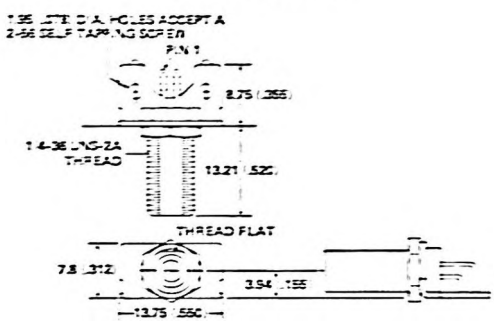
HFBR-2201 RECEIVER



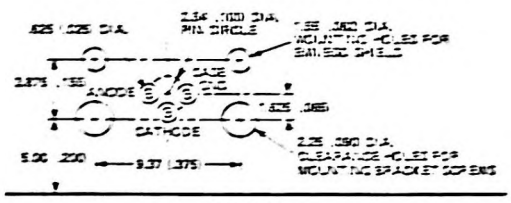
HFBR-1202 TRANSMITTER



HFBR-2202 RECEIVER



TRANSMITTER PCB LAYOUT DIMENSIONS



RECEIVER PCB LAYOUT DIMENSIONS

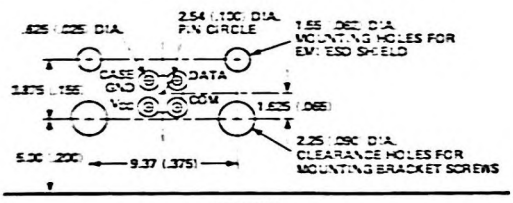


Figure 13. Mounting Dimensions
DIMENSIONS IN MILLIMETRES (INCHES).

Ordering Guide

Transmitter: HFBR-1201 HP Connector Compatible
HFBR-1202 SMA Connector Compatible

Receiver: HFBR-2201 (HP Connector Compatible)
HFBR-2202 (SMA Connector Compatible)

Mounting Hardware: HFBR-4201 HP Connector Compatible
HFBR-4202 SMA Connector Compatible

HFBR-0200 Kit:

HFBR-1201 Transmitter
HFBR-2201 Receiver
HFBR-4201 Mounting Hardware (2 sets)
HFBR-3000 10 Metre Cable/Connector Assembly
Technical Literature

Fiber Optic Cable — see data sheets

HFBR-3000	Single Channel Connectored — Custom Lengths
HFBR-3100	Dual Channel Connectored — Custom Lengths

Note: Option 001 specifies HFBR-4000 connector and Option 002 specifies SMA connectors.

HFBR-3001	Single Channel Connectored — 10 metres (HFBR-4000 connectors)
HFBR-3021	Single Channel Connectored — 10 metres (SMA connectors)
HFBR-3200	Unconnectored Single Channel — Custom Lengths
HFBR-3300	Unconnectored Dual Channel — Custom Lengths

HEWLETT PACKARD

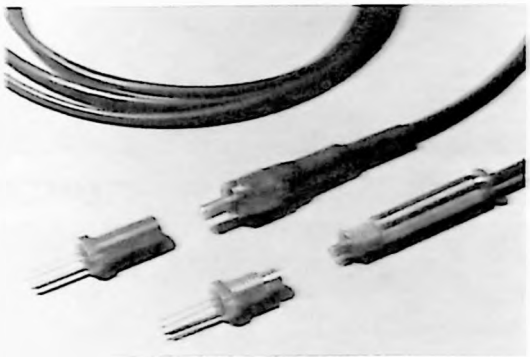
HIGH EFFICIENCY FIBER OPTIC TRANSMITTER

HFBR-1203
HFBR-1204

TECHNICAL DATA JANUARY 1984

Features

- OPTICAL POWER COUPLED INTO 100/140 μm FIBER CABLE
  —9.3 dBm Guaranteed at 25° C
  —7.4 dBm Typical
- FACTORY ALIGNED OPTICS
- RUGGED MINIATURE PACKAGE
- COMPATIBLE WITH HP OR SMA STYLE CONNECTORS



Description

The HFBR-1203/-1204 Fiber Optic Transmitter contains an etched-well 820 nm GaAlAs emitter capable of coupling greater than −10 dBm of optical power into 100/140 μm HFBR-3000 Fiber Cable/Connector Assemblies. This high power level is useful for fiber lengths greater than 1 km, or systems where star couplers, taps, or in-line connectors create large fixed losses.

Consistent coupling efficiency is assured by factory alignment of the LED with the mechanical axis of the package connector port. Power coupled into the fiber varies less than 5 dB from part to part at a given drive current and temperature. The benefit of this is reduced dynamic range requirements on the receiver.

High coupling efficiency allows the emitters to be driven at low current levels resulting in low power consumption and increased reliability of the transmitter. Another advantage of the high coupling efficiency is that a significant amount of power can still be launched into smaller fiber such as 50/125 μm (−19.1 dBm typ.).

The HFBR-1203/-1204 transmitter is housed in a rugged miniature package. The lens is suspended to avoid mechanical contact with the active devices. This assures improved reliability by eliminating mechanical stress on the die due to the lens. For increased ESD protection and design flexibility, both the anode and cathode are insulated from the case.

HFBR-1203 is compatible with HFBR-4000 connectors, and HFBR-1204 is compatible with SMA style connectors. The low profile package is designed for direct mounting on printed circuit boards or through panels without additional heat sinking. A complete mounting hardware package (HFBR-4201/-4202) is available for horizontal mounting on PCBs, including a snap-on metal shield for harsh EMI/ESD environments.

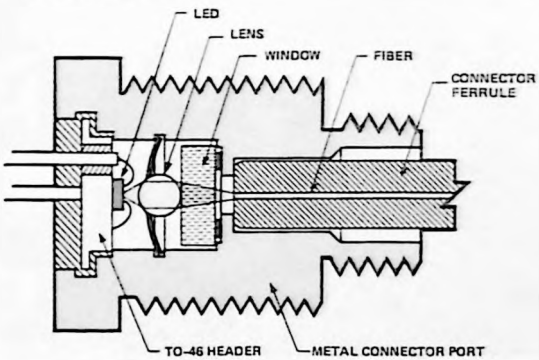
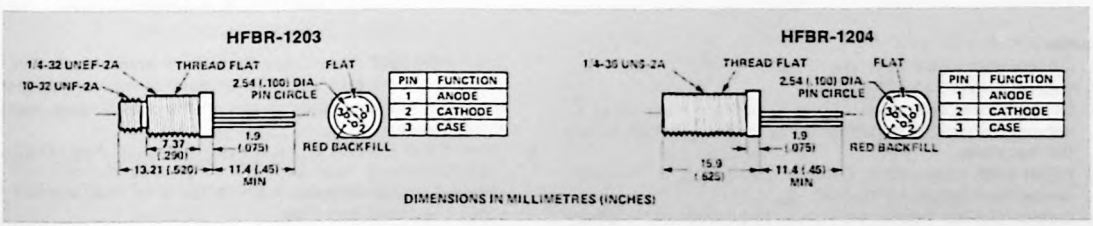


Figure 1. Cross Sectional View

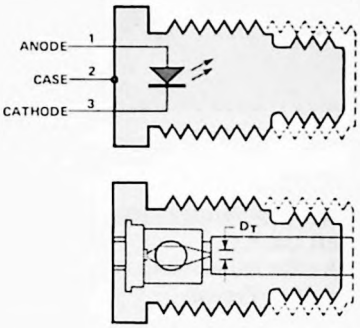
Mechanical Dimensions



FIBER OPTICS

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Unit	Reference
Storage Temperature		T_S	-55	+85	°C	
Operating Temperature		T_A	-40	+85	°C	Note 4
Lead Soldering Cycle	Temp.			+260	°C	Note 1
	Time			10	sec	
Forward Input Current	Peak	$I_{F,PK}$		100	mA	
	Average	$I_{F,AV}$		100	mA	
Reverse Input Voltage		V_R		1.0	V	
Voltage, Case-to-Junction		V_C		25	V	



Electrical/Optical Characteristics -40°C to +85°C unless otherwise specified

Parameter	Symbol	Min.	Typ.[2]	Max.	Units	Conditions	Reference
Forward Voltage	V_F	1.44	1.72	1.94	V	I_F = 100 mA	Fig. 2
Forward Voltage Temperature Coefficient	$\Delta V_F/\Delta T$		-0.54		mV/°C	I_F = 100 mA	Fig. 2
Reverse Breakdown Voltage	V_{BR}	1.0	3.1		V	I_R = 100 μA	
Numerical Aperture	NA		0.38				
Optical Port Diameter	D_T		250		μm		Note 3
Peak Emission Wavelength	λ_P		820		nm		Fig. 5
Output Optical Power Coupled into HFBR-3000 Fiber Cable/ Connector Assembly, 100/140 μm Fiber	P_T	-9.8	-7.4	-5.0	dBm	I_F = 100 mA	Fig. 3, 4 Notes 4, 5, 6, 8
		105	182	316	μW	T_A = 25°C	
		-11.2		-4.2	dBm	I_F = 100 mA	
		76		380	μW	-40°C < T_A < 85°C	
Output Optical Power Coupled into 50/125 μm Fiber	P_T		-19.1		dBm	I_F = 100 mA	Fig. 3, 4 Note 7
			12		μW	T_A = 25°C	
Optical Power Temperature Coefficient	$\Delta P_T/\Delta T$		-0.014		dB/°C	I_F = 100 mA	Fig. 3
Case Isolation Resistance (Case to Pins 1 or 2)	R_{CASE}	1			MΩ	V_{CASE} = 25 V	
Thermal Resistance	Θ_{JC}		90		°C/W		Note 9
Rise Time, Fall Time (10 to 90%)	t_r, t_f		11		nsec		Fig. 6 Note 10

WARNING: OBSERVING THE TRANSMITTER OUTPUT POWER UNDER MAGNIFICATION MAY CAUSE INJURY TO THE EYE. When viewed with the unaided eye, the infrared output is radiologically safe; however, when viewed under magnification, precaution should be taken to avoid exceeding the limits recommended in ANSI Z136.1-1981.

Notes:

1. 2.0 mm from where leads enter case.
2. Typical data at T_A = 25°C.
3. D_T is measured at the plane of the fiber face and defines a diameter where the optical power density is within 10 dB of the maximum.
4. HFBR-3000 series Fiber Cable is specified at a narrower temperature range, -20°C to 85°C.
5. Output Optical Power into connectored fiber cable other than HFBR-3000 Fiber Optic Cable/Connector Assemblies may be different than specified because of mechanical tolerances of the connector, quality of the fiber surface, and other variables.
6. Measured at the end of 1.0 metre HFBR-3000 Fiber Optic Cable/Connector Assembly with large area detector and cladding modes stripped (NA = 0.28). This fiber approximates a Standard Test Fiber.

7. Measured at the end of 1.0 metre 50/125 μm fiber with large area detector and cladding modes stripped (NA = 0.22). This fiber approximates a Standard Test Fiber. The test fiber is terminated with an SMA style connector.
8. When changing microwatts to dBm, the optical power is referenced to 1 milliwatt (1000 μW).
   Optical Power, P (dBm) = 10 log P (μW)/1000 μW
9. Thermal resistance is measured with the transmitter coupled to a connector assembly and mounted on a printed circuit board with the HFBR-4201 mounting hardware.
10. Measured with a 1 mA pre-bias current and terminated into a 50 ohm load.

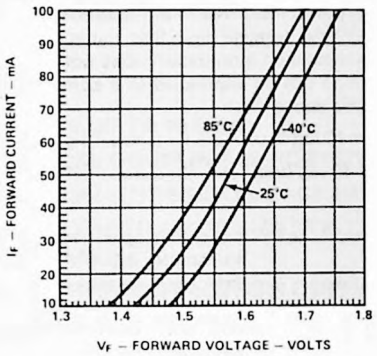


Figure 2. Forward Voltage and Current Characteristics

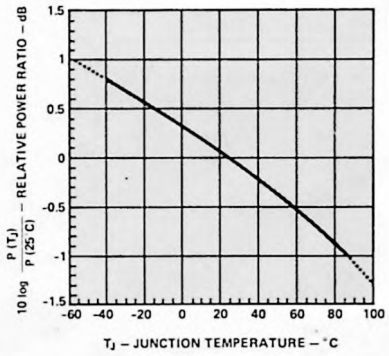


Figure 3. Normalized Thermal Effects in Transmitter Output

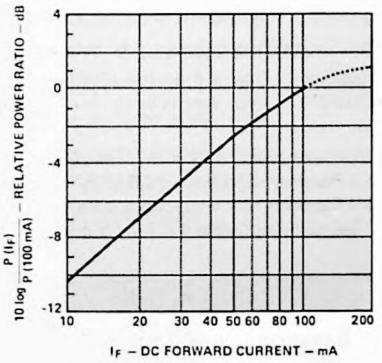


Figure 4. Normalized Transmitter Output vs. DC Forward Current

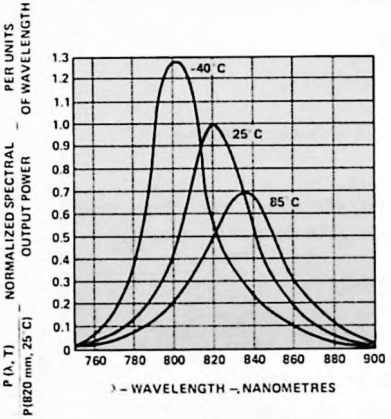


Figure 5. Transmitter Spectrum Normalized to the Peak at 25°C

Ordering Guide

Transmitter: HFBR-1203 (HP Connector Compatible)
HFBR-1204 (SMA Connector Compatible)

Receiver: HFBR-2201 (5 MBaud, HP Connector)
HFBR-2202 (5 MBaud, SMA Connector)
HFBR-2203 (40 MBaud, HP Connector Compatible)
HFBR-2204 (40 Mbaud, SMA Connector Compatible)

Mounting Hardware: HFBR-4201 (HP Connector Compatible)
HFBR-4202 (SMA Connector Compatible)

Fiber Optic Cable — see data sheets

HFBR-3000 Single Channel Connectored — Custom Lengths

HFBR-3100 Dual Channel Connectored — Custom Lengths

Note: Option 001 specifies HFBR-4000 HP connector and Option 002 specifies SMA connectors.

HFBR-3001 Single Channel Connectored — 10 metres (HFBR-4000 connectors)

HFBR-3021 Single Channel Connectored — 10 metres (SMA connectors)

HFBR-3200 Unconnectored Single Channel — Custom Lengths

HFBR-3300 Unconnectored Dual Channel — Custom Lengths

High Speed Operation

Rise and fall times can be improved by using a pre-bias current and "speed-up" capacitor. A 1 mA pre-bias current will significantly reduce the junction capacitance and will couple less than −34 dBm of optical power into the fiber cable. The TTL compatible circuit in Figure 7 using a speed-up capacitor will provide typical rise and fall times of 10 ns.

$$I_{PEAK} = 100\ mA = \frac{V_{CC} - V_F}{34.9\Omega}$$

$$I_{AVG} = 78\ mA = \frac{V_{CC} - V_F}{34.9 + 10\Omega}$$

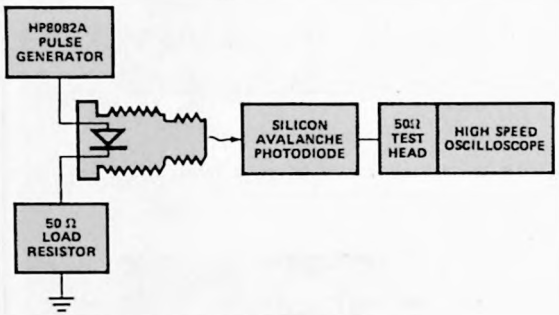


Figure 6. Test Circuit for Measuring t_r, t_f

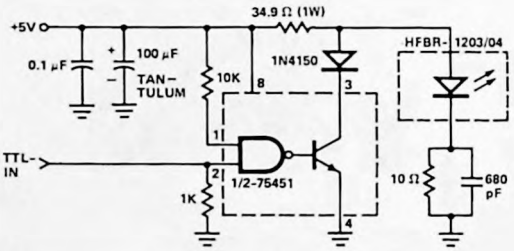


Figure 7. High Speed TTL Circuit

Link Design

With transmitter performance specified as power in dBm into a fiber of particular properties (core size, NA, and index profile), and receiver performance given in terms of the power in dBm radiated from the same kind of fiber, then the link design equation is simply:

(1) $P_T - \ell \cdot \alpha_O = P_R$

where

P_T = transmitter power into fiber (dBm)
ℓ = fiber (cable) length (km)
α_O = fiber attenuation (dB/km)
P_R = receiver power, from fiber, (dBm)

For transmitter input current in the range from 10 to 100 mA, the power varies approximately linearly:

(2) $P_T = P_O + 10 \log (I/I_O)$

where

P_O = transmitter power specification (dBm) at I_O
I_O = specified transmitter current (100 mA)
I = selected transmitter current (mA)

To allow for the dynamic range limits of proper receiver performance, it is necessary that a link with maximum transmitter power and minimum attenuation does not OVERDRIVE the receiver and that minimum transmitter power with maximum attenuation does not UNDERDRIVE it. These limits can be expressed in a combination of the two equations above:

(3) $P_{O\ MAX} + 10 \log (I_{MAX}/I_O) - \ell \cdot \alpha_{OMIN} < P_{R\ MAX}$

(4) $P_{O\ MIN} + 10 \log (I_{MIN}/I_O) - \ell \cdot \alpha_{OMAX} > P_{R\ MIN}$

where

$P_{O\ MAX}$, $P_{O\ MIN}$ = max., min. specified power from transmitter (dBm) at $I = I_O$
I_{MAX}, I_{MIN} = max., min. selected transmitter operating current (mA)
$P_{R\ MAX}$, $P_{R\ MIN}$ = max., min. specified power at receiver (dBm)
α_{OMAX}, α_{OMIN} = max., min. attenuation (dB/km)

A more useful form of these equations comes from solving them for the current ratio, expressed in dB:

(5) $10 \log (I_{MAX}/I_O) < P_{R\ MAX} - P_{O\ MAX} + \ell \cdot \alpha_{OMIN}$

(6) $10 \log (I_{MIN}/I_O) > P_{R\ MIN} - P_{O\ MIN} + \ell \cdot \alpha_{OMAX}$

These are plotted in Figure 8 as the OVERDRIVE LINE, and UNDERDRIVE LINE, respectively for the following components:

HFBR-1203/4 Transmitter $-11.2 < P_T < -4$ dBm
HFBR-2203/4 Receiver (25 MHz) $-28.5 < P_R < -12.6$ dBm
HFBR-2203/4 Receiver (2.5 MHz) $-35.5 < P_R < -12.6$ dBm
HFBR-3000 Series Fiber Cable $4 < \alpha_O < 8$ dB/km

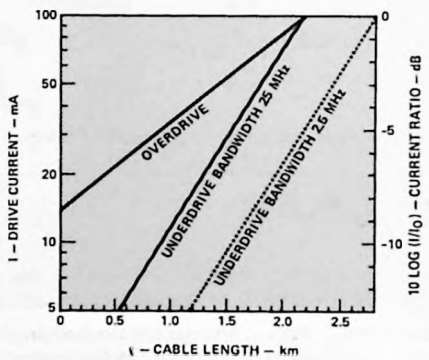


Figure 8. Link Design Limits.

These design equations take account only of the power loss due to attenuation. The specifications for the receiver and transmitter include loss effects in end connectors. If the system has other fixed losses, such as from directional couplers or additional in-line connectors, the effect is to shift both OVERDRIVE and UNDERDRIVE lines upward by the amount of the additional loss ratio.

HEWLETT PACKARD

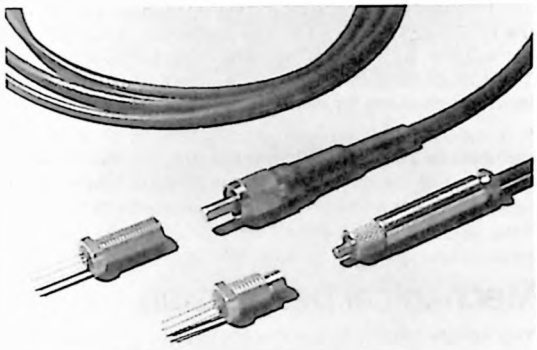
40 MBd MINIATURE FIBER OPTIC RECEIVERS

HFBR-2203
HFBR-2204

TECHNICAL DATA JANUARY 1984

Features

- DATA RATES UP TO 40 MBd
- HIGH OPTICAL COUPLING EFFICIENCY
- RUGGED, MINIATURE METAL PACKAGE
- COMPATIBLE WITH HP OR SMA STYLE CONNECTORS
- VERSATILE ANALOG RECEIVER OUTPUT
- 25 MHz ANALOG BANDWIDTH



Applications

- DATA ACQUISITION AND PROCESS CONTROL
- SECURE DATA COMMUNICATION
- EMC REGULATED SYSTEMS (FCC/VDE)
- EXPLOSION PROOF SYSTEMS
- WEIGHT SENSITIVE SYSTEMS (e.g., AVIONICS, MOBILE STATIONS)
- VIDEO TRANSMISSION

Description

The HFBR-2203/04 Receiver is capable of data rates up to 40 MBd at distances greater than 1 km when used with HFBR-3000 series cable and HFBR-1201/2/3/4 Transmitters. The HFBR-2203/04 Receivers contain a discrete PIN photodiode and preamplifier IC.

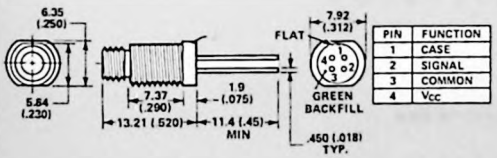
The signal from this simple analog receiver can be optimized for a variety of transmission requirements. For example the HFBR-0221/02/03/04 transceivers add low-cost external components to achieve logic compatible signal levels optimized for various data formats and data rates.

Each of these fiber optic components uses the same rugged, lensed, miniature package. This package assures a consistent, efficient optical coupling between the active devices and the optical fiber.

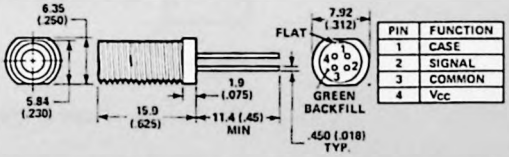
The HFBR-2203 Receiver is compatible with the HFBR-4000 Connector and HFBR-3000 series, Option 001 connectored cable. The HFBR-2204 Receiver is compatible with SMA style connectors, types A and B (see Figure 11), and HFBR-3000 series, Option 002 connectored cable. HFBR-3000 series cable can be ordered with or without connectors. The HFBR-0100 connector assembly kit is available if field installation of HFBR-4000 connectors is desired.

Mechanical Dimensions

HFBR-2203 RECEIVER



HFBR-2204 RECEIVER



DIMENSIONS IN MILLIMETRES (INCHES)
UNLESS OTHERWISE SPECIFIED, THE TOLERANCES ARE:
.X ± .51 mm (.XX ± .02 IN)
.XX ± .13 mm (.XXX ± .005 IN)

FIBER OPTICS

Electrical Description

The HFBR-2203/04 Fiber Optic Receiver contains a PIN photodiode and low noise transimpedance pre-amplifier hybrid circuit with an inverting output (see note 10). The HFBR-2203/04 receives an optical signal and converts it to an analog voltage. The output is a buffered emitter-follower. Because the signal amplitude from the HFBR-2203/04 Receiver is much larger than from a simple PIN photodiode, it is less susceptible to EMI, especially at high signal rates.

The frequency response is typically dc to 25 MHz. Although the HFBR-2203/04 is an analog receiver, it is easily made compatible with digital systems (see HFBR-0221/2/3/4 Transceiver data sheet). Separate case and signal ground leads are provided for maximum design flexibility.

It is essential that a bypass capacitor (0.01 μF to 0.1 μF ceramic) be connected from Pin 4 (V_{CC}) to Pin 3 (circuit common) of the receiver. Total lead length between both ends of the capacitor and the pins should be less than 20 mm.

Mechanical Description

The HFBR-2203/04 Fiber Optic Receiver is housed in a miniature package intended for use with HFBR-3000 Fiber Optic Cable/Connector Assemblies. This package has important performance advantages:

1. Precision mechanical design and assembly procedures assure the user of consistent high efficiency optical coupling.
2. The lens is suspended to avoid contact with the active devices, thereby assuring improved reliability.
3. The versatile miniature package is easy to mount. This low profile package is designed for direct mounting on printed circuit boards or through panels without additional heat sinking.

   A complete mounting hardware package is available for horizontal PCB applications, including a snap-on metal shield for harsh EMI/ESD environments.

   Good system performance requires clean port optics and cable ferrules to avoid obstructing the optical path. Clean compressed air often is sufficient to remove particles of dirt; Methanol or Freon on a cotton swab also works well.

   Note:
   When installing connectored cable on the optical port, do not use excessive force to tighten the nut. Finger tightening is sufficient to ensure connectoring integrity, while use of a wrench may cause damage to the connector or the optics.

System Design Considerations

For additional information, see the product data sheet for the HFBR-0221/2/3/4 Fiber Optic Transceivers.

OPTICAL POWER BUDGETING

The HFBR-2203/04 Fiber Optic Receivers when used with the HFBR-1201/02 Fiber Optic Transmitters can be operated at a signalling rate of more than 40 MBd over a distance greater than 1000 metres (assuming 8 dB/km cable attenuation). For shorter transmission distances, power consumption can be reduced by decreasing Transmitter drive current. At a lower data rate, the transmission distance may be increased by applying bandwidth-filtering at the

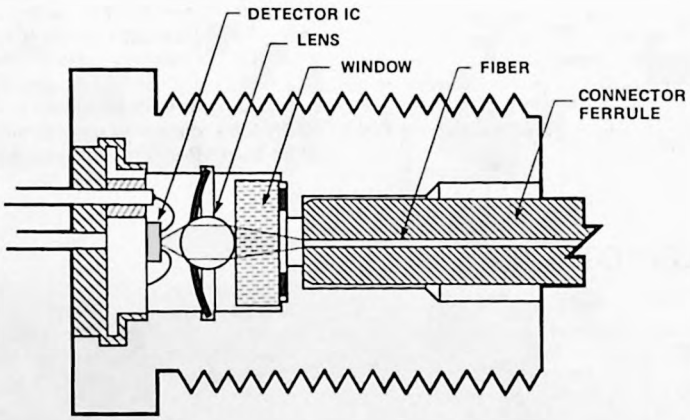


Figure 1. Cross Sectional View

output of the HFBR-2203/04 Receiver; since noise is reduced as the square root of the bandwidth, the sensitivity of the circuit is proportionately improved provided these two conditions are met:

a. input-referred noise of the follow on circuit is well below the filtered noise of the Receiver
b. logic comparator threshold is reduced in the same proportion as the noise reduction

As an example, consider a link with a maximum data rate of 10 MBd (e.g., 5 Mb/s Manchester); this requires a 3 dB bandwidth of only 5 MHz. For this example, the input-referred rms noise voltage of the follow-on circuit is 0.03 mV. The equivalent optical noise power of the complete receiver (P_{NO}) is given by:

$$P_{NO} = [(V_{NO})^2 (B/Bo) + (V_{NI})^2]^{0.5} / R_P$$

V_{NO} = rms output noise voltage of the HFBR-2203/04 with no bandwidth filtering
V_{NI} = input-referred rms noise voltage of the follow-on circuit
B = filtered 3 dB bandwidth
Bo = Unfiltered 3dB bandwidth of the HFBR-2203/04 (25 MHz)
R_P = optical-to-electrical responsivity (mV/μW) of the HFBR-2203/04

Note that noise adds in an rms fashion, and that the square of the rms noise voltage of the HFBR-2203/04 is reduced by the bandwidth ratio, B/Bo.

From the receiver data (Electrical/Optical Characteristics) taking worst-case values, and applying NO bandwidth filtering (B/Bo = 1):

$P_{NO} = [((0.43)^2 + (0.03)^2)^{0.5}]$ mV / 4.6 mV/μW = 0.094 μW or -40.3 dBm

To ensure a bit error rate less than 10^{-9} requires the signal power to be 12 times larger (+11 dB) than the rms noise as referred to the Receiver input. The minimum Receiver input power is then:

$$P_{RMIN} = P_{NO} + 11 \text{ dB} = -29.3 \text{ dBm}$$

With the application of a 5 MHz low-pass filter, the bandwidth ratio becomes:

$$B_{Bo} = 5 \text{ MHz} / 25 \text{ MHz} = 0.2$$

Note that 25 MHz should be used for the total noise bandwidth of the HFBR-2203/04. Inserting this value of the bandwidth ratio in the expressions for P_{NO} and P_{RMIN} above yields the results:

P_{NO} = 0.042 μW or -43.8 dBm and P_{RMIN} = -32.8 dBm

Given the HFBR-1201/2 Transmitter optical power P_T = -18 dBm at I_F = 40 mA, and allowing a 3 dB margin, a minimum optical power budget of 11.8 is obtained:

$$[-18 \text{ dBm} - 3 \text{ dB} - (-32.8 \text{ dBm})] = 11.8 \text{ dB}$$

Using 8 dB/km optical fiber, this translates into a minimum link length of 1475 metres (typical link power budget for this configuration is approximately 17.2 dB or 3130 metres with 5.5 dB/km fiber).

BANDWIDTH

The bandwidth of the HFBR-2203/04 is typically 25 MHz. Over the entire temperature range of -40° C to +85° C, the rise and fall times vary in an approximately linear fashion with temperature. Under worst case conditions, t_r and t_f may reach a maximum of 26 ns, which translates to a 3 dB bandwidth of:

$$f_{3dB} \approx \frac{.35}{t_r} = \frac{.35}{26 \text{ ns}} = 13.5 \text{ MHz}$$

The receiver response is essentially that of a single-pole system, rolling off at 6 dB/octave. In order for the receiver to operate up to 40 MBd even though its worst case 3 dB bandwidth is 13.5 MHz, the received optical power must be increased by 3 dB to compensate for the restricted receiver transmission bandwidth.

PRINTED CIRCUIT BOARD LAYOUT

When operating at data rates above 10 MBd, standard PC board precautions should be taken. Lead lengths greater than 20 mm should be avoided whenever possible and a ground plane should be used. Although transmission line techniques are not required, wire wrap and plug boards are not recommended.

OPERATION WITH HEWLETT-PACKARD TRANSISTORS

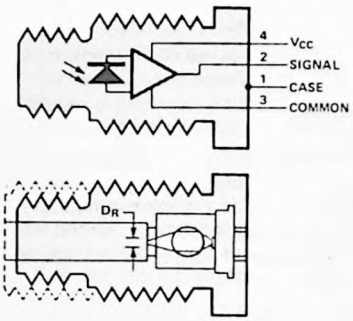
Hewlett-Packard offers two transmitters compatible with the HFBR-2203/4. Link performance with each transmitter is shown below for 25° C operation with HFBR-3000 series glass fiber cable. See product data sheets for further information.

	HFBR-1201/2 -17 dBm Coupled Optical Power	HFBR-1203/4 -9.5 dBm Coupled Optical Power
HFBR-2203/4 -27 dBm Sensitivity	1200 m 40 MBd	2100 m 40 MBd
HFBR-2203/4 -32 dBm Sensitivity	1800 M 10 MBd	2800 M 10 MBd

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Unit	Reference
Storage Temperature		T_S	-55	85	°C	
Operating Temperature		T_A	-40	85	°C	Note 9
Lead Soldering Cycle	Temp.			260	°C	Note 1
	Time			10	sec	
Case Voltage		V_{CASE}		25	V	
Signal Pin Voltage		V_{SIGNAL}	-0.5	1	V	
Supply Voltage		V_{CC}	-0.5	7.0	V	

HFBR-2203/2204 RECEIVER



Electrical/Optical Characteristics

-40° C to +85° C; $4.75 \le V_{CC} \le 5.25$; $R_{LOAD} = 511\Omega$ unless otherwise specified

Parameter	Symbol	Min.	Typ.[4]	Max.	Unit	Conditions	Reference
Responsivitity	R_P	5.1	7	10.9	mV/μW	T_A = 25° C at 820 nm	Note 10 Figure 3
		4.6		12.3	mV/μW	-40 ≤ T_A ≤ +85° C	
RMS Output Noise Voltage	V_{NO}		.30	.36	mV	T_A = 25° C, P_{IN} = 0μW	Figures 4, 7
				.43	mV	-40 ≤ T_A ≤85° C, P_{IN}= 0 μW	
Input Power	P_R			-12.6	dBm	T_A = 25° C	Note 2
				55	μW		
				-14	dBm	-40 ≤ T_A ≤ 85° C	
				-40	μW		
Output Impedance	Z_O		20		Ω	Test Frequency = 20 MHz	
DC Output Voltage	V_{odc}		.7		V	P_{IN} = 0 μW	
Power Supply Current	I_{CC}		3.4	6.0	mA	R_{LOAD} = ∞	
Equivalent N.A.	NA		.35				
Equivalent Diameter	D_R		250		μm		Note 3
Equivalent Optical Noise Input Power	P_N		-43.7	-40.3	dBm		
			.042	.094	μW		

Dynamic Characteristics

-40° C to +85° C; $4.75 \le V_{CC} \le 5.25$; $R_{LOAD} = 511\Omega$, C_{LOAD} = 13 pF unless otherwise specified

Parameter	Symbol	Min.	Typ.[7]	Max.	Units	Conditions	Reference
Rise/Fall Time, 10% to 90%	t_r, t_f		14	19.5	ns	T_A = 25° C P_{IN} = 10 μW Peak	Note 5
				26	ns	-40 ≤ T_A ≤ 85° C	Figures 8, 9
Pulse Width Distortion	$t_{phl} - t_{plh}$			2	ns	P_{IN} = 40 μW Peak	Figure 9
Overshoot			4		%	T_A = 25° C	Note 6 Figures 8, 9
Bandwidth			25		MHz		
Power Supply Rejection Ratio (Referred to Output)	PSRR		50		dB	at 2 MHz	Note 7 Figures 5, 6

Notes:
1. 2.0 mm from where leads enter case.
2. If $P_{in} > 40$ μW, then pulse width distortion may increase. At $P_{in} = 60$ μW and T_A = 85° C, some units have exhibited as much as 100 ns pulse width distortion.

Notes (cont.):

3. D_R is the effective diameter of the detector image on the plane of the fiber face. The numerical value is the product of the actual detector diameter and the lens magnification.
4. Typical specifications are for operation at $T_A = 25°C$ and $V_{CC} = 5.0V$.
5. Input optical signal is assumed to have 10% — 90% rise and fall times of less than 6 ns.
6. Percent overshoot is defined as:
$$\frac{V_{PK} - V_{100\%}}{V_{100\%}} \times 100\%$$ See Figure 16.
7. Output referred P.S.R.R. is defined as
$$20 \log \left(\frac{V_{OUT - RIPPLE}}{V_{POWER\ SUPPLY - RIPPLE}} \right)$$
8. It is essential that a bypass capacitor (0.01 μF to 0.1 μF ceramic) be connected from pin 4 (V_{CC}) to pin 3 (circuit common) of the receiver. Total lead length between both ends of the capacitor and the pins should be less than 20 mm.
9. HFBR-3000 series Fiber Cable is specified at a narrower temperature range, -20°C to 85°C.
10. $V_{OUT} = V_{ODC} - (R_P \times P_{IN})$.

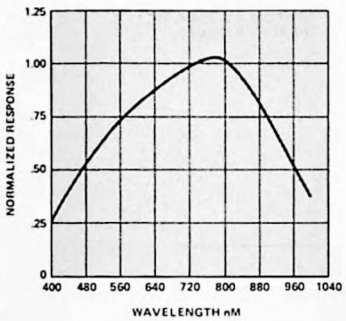


Figure 3. Receiver Spectral Response Normalized to 820 nm

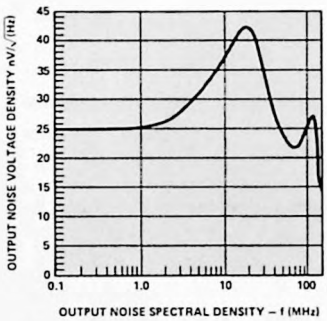


Figure 4. Receiver Noise Spectral Density

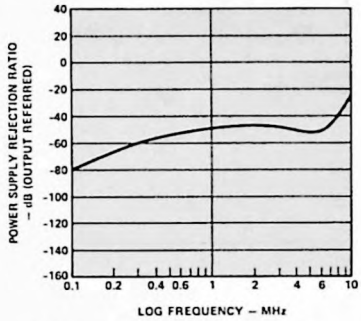


Figure 5. Receiver Power Supply Rej. vs. Freq.

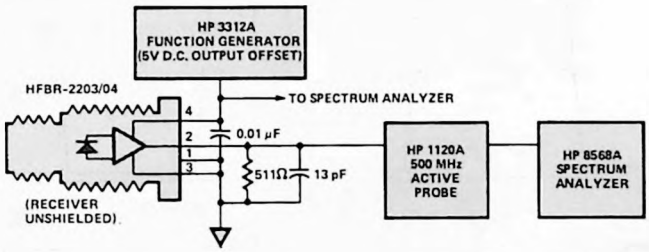


Figure 6. Power Supply Rejection Test Circuit

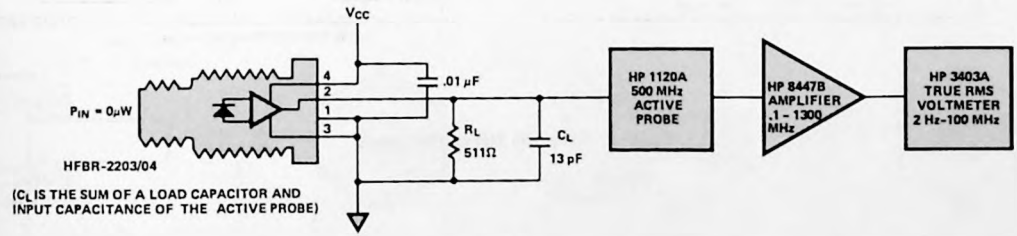


Figure 7. RMS Output Noise Voltage Test Circuit

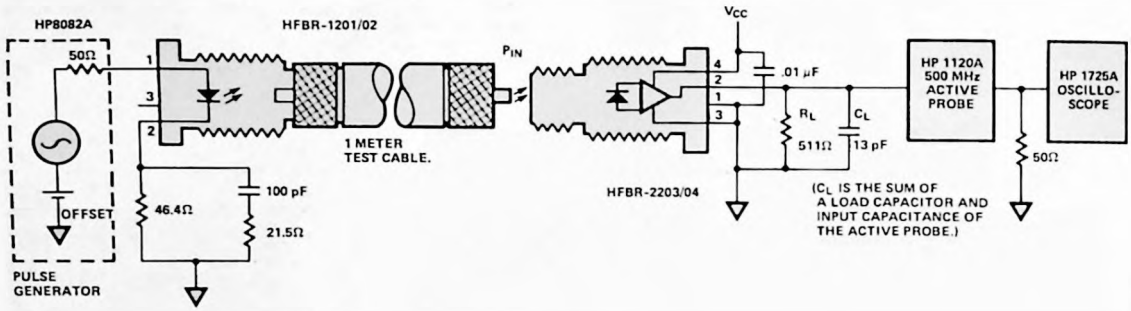


Figure 8. Rise and Fall Time Test Circuit

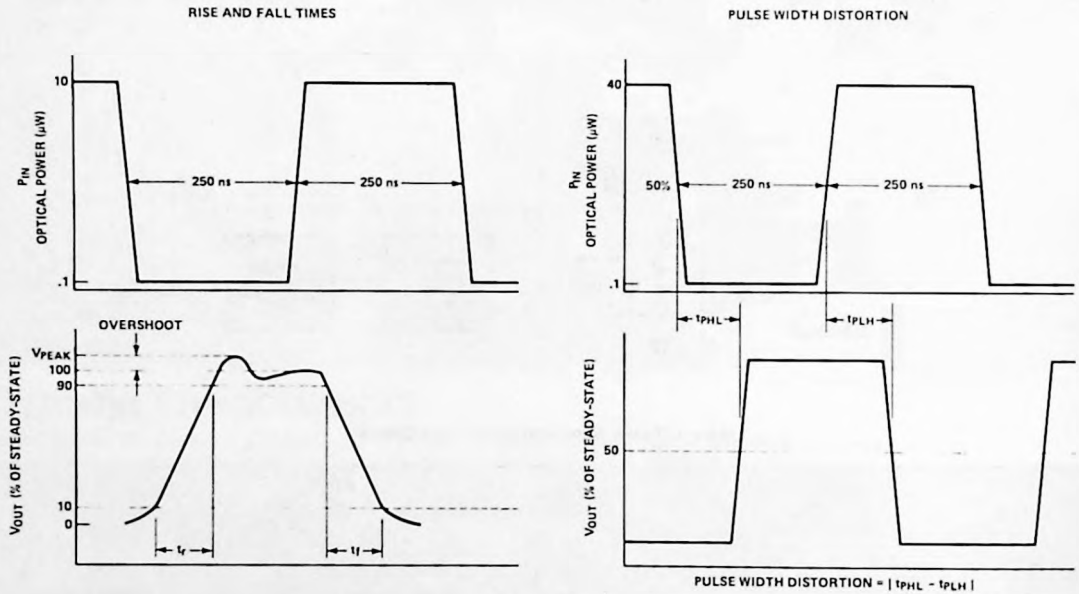


Figure 9. Waveform Timing Definitions

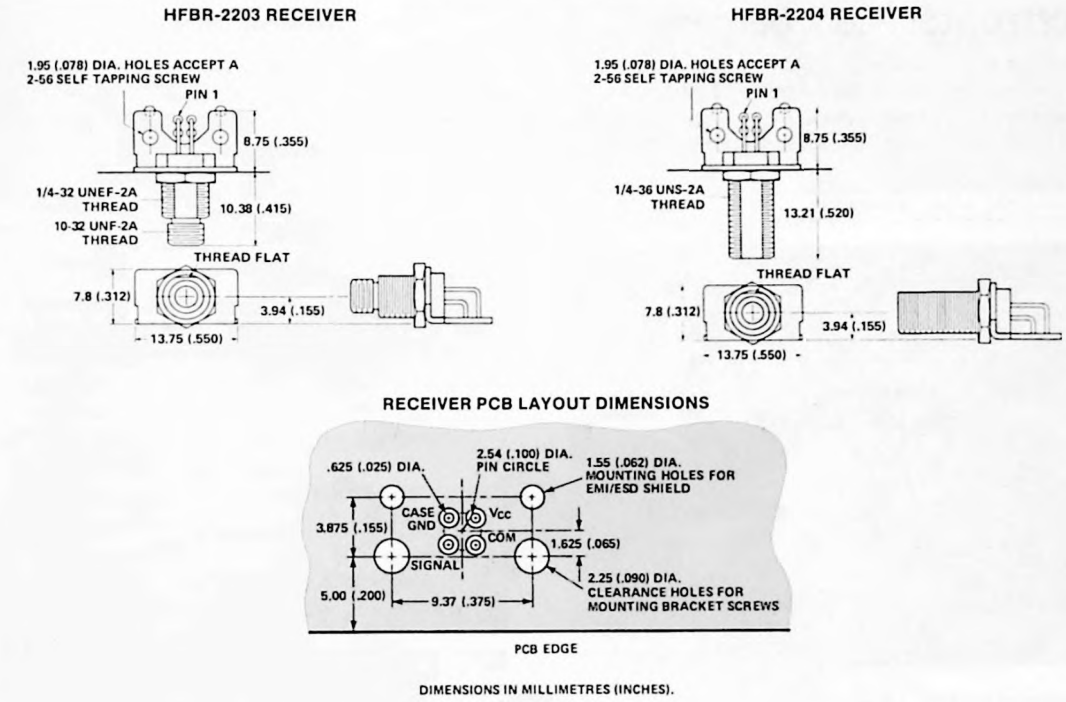
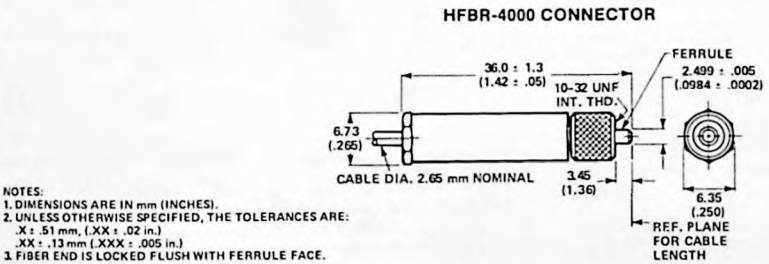


Figure 10. Mounting Dimensions

HEWLETT-PACKARD STYLE CONNECTOR (Used in HFBR-3000/3100, Option 001 Cable Assemblies).



SMA STYLE CONNECTORS

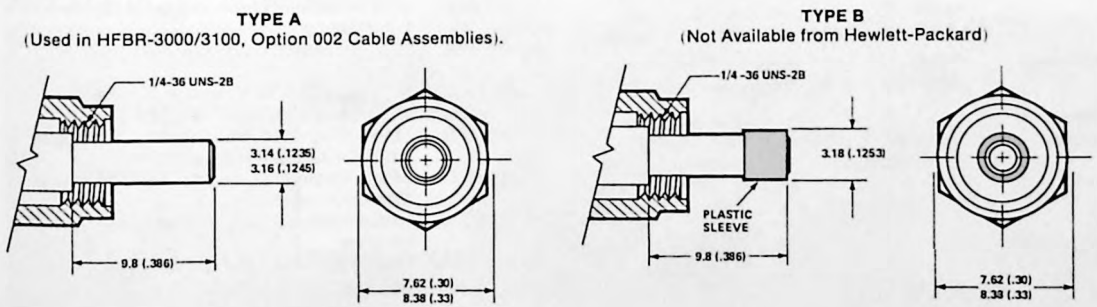


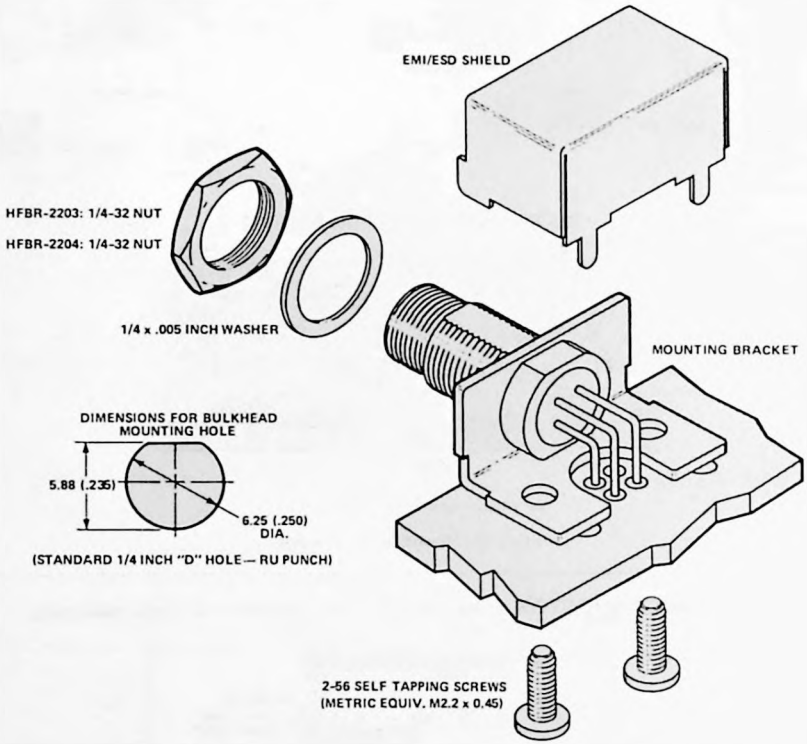
Figure 11. Fiber Optic Connector Styles

Horizontal PCB Mounting

Mounting at the edge of a printed circuit board with the lock nut overhanging the edge is recommended.

When bending the leads, avoid sharp bends right where the lead enters the backfill. Use needle nose pliers to support the leads at the base of the package and bend the leads as desired.

When soldering, it is advisable to leave the protective cap on the unit to keep the optics clean.



MOUNTING HARDWARE: HFBR-4201 (HFBR-2203)
- 1 EMI/ESD SHIELD
- 1 1/4-32 NUT
- 1 1/4 x .005 INCH WASHER
- 2 2-56 SELF TAPPING SCREWS
- 1 MOUNTING BRACKET

MOUNTING HARDWARE: HFBR-4202 (HFBR-2204)
- 1 EMI/ESD SHIELD
- 1 1/4-36 NUT
- 1 1/4 x .005 INCH WASHER
- 2 2-56 SELF TAPPING SCREWS
- 1 MOUNTING BRACKET

Ordering Guide

Transmitter:	HFBR-1201 (HP Connector Compatible)
	HFBR-1202 (SMA Connector Compatible)
	HFBR-1203 (HP Connector Compatible)
	HFBR-1204 (SMA Connector Compatible)
Receiver:	HFBR-2203 (HP Connector Compatible)
	HFBR-2204 (SMA Connector Compatible)
Mounting Hardware:	HFBR-4201 (HP Connector Compatible)
	HFBR-4202 (SMA Connector Compatible)

Fiber Optic Cable — see data sheets

HFBR-3000	Single Channel Connectored — Custom Lengths
HFBR-3100	Dual Channel Connectored — Custom Lengths

Note: Option 001 specifies HFBR-4000 connector and Option 002 specifies SMA connectors.

HFBR-3001	Single Channel Connectored — 10 metres (HFBR-4000 connectors)
HFBR-3021	Single Channel Connectored — 10 metres (SMA connectors)
HFBR-3200	Unconnectored Single Channel — Custom Lengths
HFBR-3300	Unconnectored Dual Channel — Custom Lengths

HEWLETT PACKARD

HIGH SPEED FIBER OPTIC TRANSCEIVERS

HFBR-0221
HFBR-0222
HFBR-0223
HFBR-0224

TECHNICAL DATA JANUARY 1984

Features

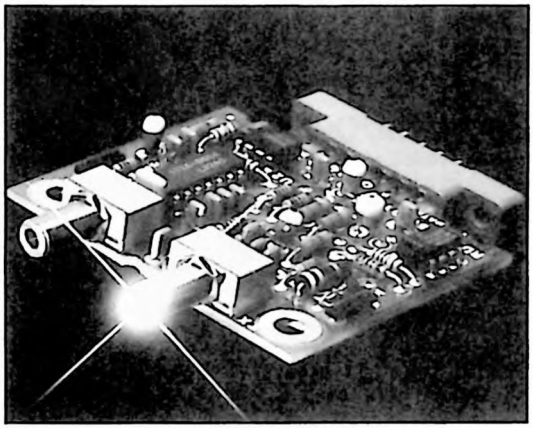
- GUARANTEED LINK PERFORMANCE
- DISTANCE/DATA RATE TRADEOFF ALLOWS INCREASED OPTICAL POWER BUDGET AT LOWER DATA RATES
- TTL I/O
- 20 MBAUD DATA RATE (CAN BE MODIFIED FOR 40 MBd OPERATION)
- COMPATIBLE WITH MOST DATA FORMATS
- AVAILABLE WITH HP OR SMA STYLE CONNECTORS
- LINK LENGTHS TYPICALLY GREATER THAN 1 km AT 20 MBd

Applications

- DESIGN AID FOR HIGH SPEED FIBER OPTIC COMPONENTS
- DATA ACQUISITION AND PROCESS CONTROL
- SECURE DATA COMMUNICATION
- EMC REGULATED SYSTEMS (FCC/VDE)
- EXPLOSION PROOF SYSTEMS
- WEIGHT SENSITIVE SYSTEMS (e.g. AVIONICS, MOBILE STATIONS)

Description

The HFBR-0221/2/3/4 High Speed Fiber Optic Transceivers are printed circuit board assemblies containing HFBR-1201/-1202 Transmitters, HFBR-2203/-2204 Receivers and support circuitry to provide TTL input and complementary TTL outputs. The performance of these transceivers at 20 MBd has been characterized over 0° C to 70° C and total link performance with HFBR-3000 Fiber Cable/Connector Assembly is guaranteed.

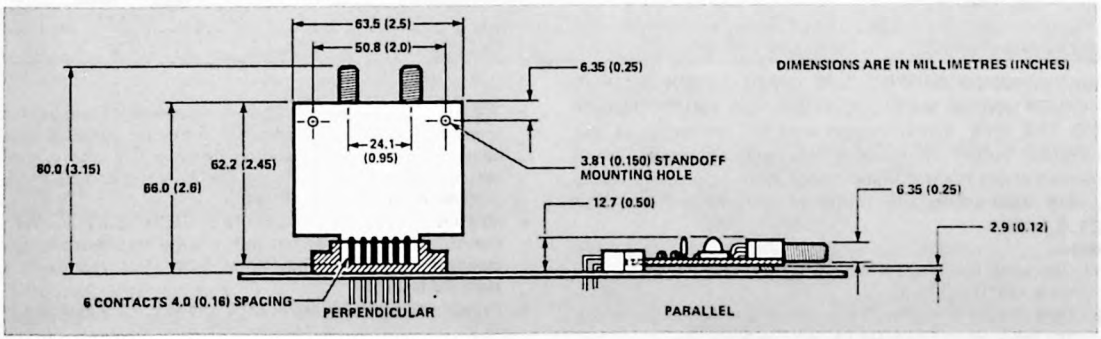


These transceivers are optimized for 20 MBd operation. However, the support circuitry on the printed circuit board can be optimized for other data rates. Recommendations for component values and anticipated performance for operation at 1 MBd, 5 MBd and 40 MBd are included in the "Application Information" section.

There are two transceiver designs (available with HP or SMA style connector ports) which accommodate various data formats. The HFBR-0221/0222 transceivers are optimized for data formats which have 50 percent duty factors such as Manchester and biphase. The HFBR-0223/-0224 transceivers are designed for arbitrary data formats including most NRZ schemes (see "Circuit Description" for details).

The transceivers can be mounted via an edge card connector, either parallel or perpendicular to a reference printed circuit board. A right angle edge card connector is included with each transceiver for parallel mounting.

Mechanical Dimensions



FIBER OPTICS

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Applied Voltage Data, $\overline{\text{Data}}$ +Vcc, Data In		−0.5	5.25	V
−Vcc		−6.5	+0.5	V
Storage Temperature[1]	Ts	−55	85	°C

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	+Vcc	4.75	5.25	V
	−Vcc	−4.5	−6.5	
Operating Temperature	TA	0	70	°C
Duty Factor HFBR-0221/22	DF	33	67	%
HFBR-0223/24		5	95	
Data Rate Range		0.01	20	MBd

Electrical/Optical Characteristics

(Recommended operating conditions for transceiver optimized for 20 MBd apply, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.[5]	Max.	Units
Optical Power Budget HFBR-0221/2	OPB	When used with HFBR-3000 Fiber Cable/Connectors, Data Rate = 20 MBd BER = 10^{-9}	9	15.5		dB
HFBR-0223/4			5	11		
Pulse Distortion HFBR-0221/2	$t_{PLH} - t_{PHL}$			7	12.5	ns
HFBR-0223/4				2	12.5	
Data Output Response Time[2]	t_r			7		ns
	t_f			5		
Transceiver Propagation Delay[3]	t_{PLH}, t_{PHL}			70		ns
Power Consumption +Vcc				750		mW
−Vcc				125		
Transmitter Output Optical Power[4]	PT	Data In is high, $T_A = 25°C$	−18	−16.5		dBm
Power coupled into HFBR-3000 Fiber Cable/ Connector Assembly			15.8	22.4		μW
		$0 < T_A < 70°C$ Data In is high	−19			dBm
			12.6			μW
Optical Rise and Fall Times	$t_{r,o}$ $t_{f,o}$	10% to 90%		10		ns
Receiver Optical Sensitivity HFBR-0221/2	PR	Data Rate = 20 MBd BER = 10^{-9}	−28	−32		dBm
			1.6	0.6		μW
HFBR-0223/4			−24	−27.5		dBm
			4	1.8		μW
TTL Gate Fanout			4			

WARNING: OBSERVING THE TRANSMITTER OUTPUT POWER UNDER MAGNIFICATION MAY CAUSE INJURY TO THE EYE. When viewed with the unaided eye, the infrared output is radiologically safe: however, when viewed under magnification, precaution should be taken to avoid exceeding the limits recommended in ANSI Z136.1-1981.

Notes:

1. Operating temperature of HFBR-3000 Fiber Cable/Connector is −20° C to +70° C.
2. Data Output Response Time is the 10% to 90% electrical rise and fall time on PIN 6 (DATA) and PIN 5 ($\overline{\text{DATA}}$).
3. Transceiver propagation delay is measured by looping the transmitter back on the receiver with one metre of fiber cable. Transceiver propagation delay is the time interval between a signal applied to the DATA IN pad and the signal received at the DATA OUT pad.
4. Measured at the end of one metre of HFBR-3000 Fiber Optic Connector/Cable Assembly with a large area detector and cladding modes stripped (NA = 0.28). This represents a standard test fiber.
5. Typical specifications are at 25° C and Vcc = 5 V and −Vcc = −5 V.

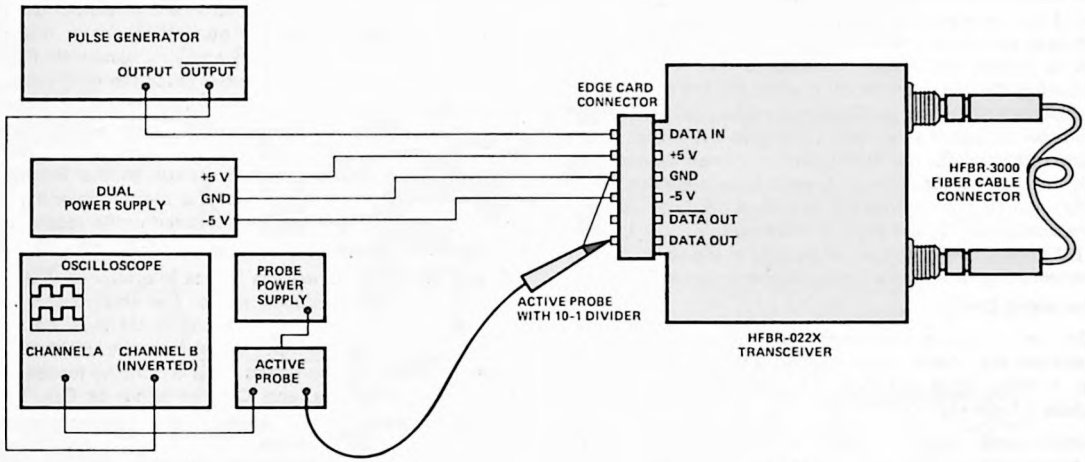
Test Set-Up

Equipment Needed

1. Dual power supply (HP 623613)
2. 100 MHz oscilloscope (HP 1725A)
3. Active oscilloscope probe and probe tip (HP 1120A/1122A)
4. 10:1 divider for oscilloscope probe (HP 10241A)
5. 50 MHz pulse generator (HP 8082A)
6. Miscellaneous cables and connectors

Procedure

1. Connect fiber cable and edge card conector to the transceiver board.
2. Adjust the power supply to +5 V and −5 V. Then connect to the transceiver board as shown below. Take care not to exceed the recommended operating voltage.
3. Adjust the pulse generator for TTL level square wave (+3 V) with a 5 nsec, edge transition time and then connect to the transceiver board.
4. Use the oscilloscope with the active probe and 10:1 divider to observe the input and output waveforms.



Notes:
1. The data out observed through the active probe exhibits overshoot at the rising edge. This overshoot will disappear if the output is loaded to drive a TTL input.
2. Oscilloscope inputs should be terminated into 50 ohms.
3. The active probe should be set on DC for observation of lower data rates. The offset on the active probe should be off.
4. The active probe is used to avoid reflection in the observed signal through impedance matching.
5. If necessary clean the optical port of the fiber connectors with Acetone before connecting them to the transceivers.

Ordering Information

	Connector Style	Data Format
HFBR-0221	HP	33 to 67% Duty Factor (For use with code schemes such as Manchester and Biphase)
HFBR-0222	SMA	
HFBR-0223	HP	5 to 95% Duty Factor (For use with code schemes such as NRZ and NRZI)
HFBR-0224	SMA	

Fiber Optic Cable (See Data Sheets)

HFBR-3000 Single Channel Connectored — Custom Lengths

HFBR-3100 Dual Channel Connectored — Custom Lengths

NOTE: Option 001 specifies HFBR-4000 (HP) connector and Option 002 specifies SMA style connectors.

HFBR-3001 Single Channel Connectored — 10 metres (HFBR-4000 connectors)

HFBR-3021 Single Channel Connectored — 10 metres (SMA connectors)

HFBR-3200 Unconnectored Single Channel — Custom Lengths

HFBR-3300 Unconnectored Dual Channel — Custom Lengths

Application Information

TRANSCEIVER CIRCUIT DESCRIPTION

There are separate transmitting and receiving circuits that function independently so data may be simultaneously sent and received without mutual interference.

Transmitting Circuit

On the transmitter side, the DATA IN terminal operates from TTL-level signals; the HFBR-1201/2 Transmitter is off ($P_T = 0$) with DATA IN low, and is on with DATA IN high. R_{12} holds the input low in the absence of anything connected. In this condition, the output transistor of U3 is on, and the current from R_2 is taken to ground through CR_1, making the voltage at the anode of the HFBR-1201/2 transmitter low enough to hold the LED off, yet allow it to be slightly forward biased (by the forward voltage on CR_1) so it can be turned on with little delay. With insignificant forward current in the LED, C_3 is discharged. When DATA IN is raised, the output transistor of U3 is turned off, allowing the current from R2 to enter the LED; there is an initial rush of current as C3 charges, thus peaking the LED turn-on. In steady state "on", LED current is limited by the sum of R_2 and R_3, but during turn-on current is limited by R_2 only, so the peak-to-dc current ratio is approximately $(R_2 + R_3)/R_2$. During turn-off, until C_3 is partly discharged, the voltage on C_3 will apply a small reverse voltage to the LED, thus peaking its turn-off as long as the voltage on C_3 remains higher than the voltage at the anode of CR_1.

Receiving Circuit

On the receiving side there is a similar relationship between the optical power and the TTL-level signals; that is, a rising input optical power excursion will normally cause a logic high DATA OUT.

Under steady-state conditions of optical input, both the positive and negative inputs of U1 are at ground potential, so the output of U1 is near zero and therefore capable of excursions either up or down in response to changes at its input. U2 is a comparator; when connected as shown it has positive feedback from DATA OUT when DATA OUT is high, and from $\overline{\text{DATA}}$ OUT when DATA OUT is low. This positive feedback makes it operate as a Schmitt circuit, the hysteresis thresholds being established by the voltage division ratios in R_{11}, R_9 when DATA OUT is high and in R_{10}, R_8 when DATA OUT is low.

Under dynamic conditions, a rise in optical input power causes the voltage at pin 2 of the HFBR-2203/-2204 to fall. This fall is ac-coupled by C_{11} to the input, pin 1, of U1, where it is amplified and converted to a balanced output signal, rising at pin 8 and falling at pin 7. The falling signal coupled by C_{13} to U2 will, if the amplitude exceeds the hysteresis threshold, cause U2 to latch a logic high at DATA OUT. Similarly, a drop in optical input power will cause U2 to latch a logic high at $\overline{\text{DATA}}$ OUT (low at DATA OUT).

After a change in optical input power, the U1 amplifier circuit may return to steady-state conditions, but U2 holds the logic state until an opposite excursion occurs unless there is a noise-voltage excursion that causes logic reversal. Consequently, the threshold set at U2 must be high enough that neither electromagnetic interference coupled from elsewhere on the circuit board, nor Receiver noise amplified through U1 can cause a false change. On the other hand, if the threshold is set too high, the Receiver would require inappropriately large changes in optical input power in order to make U2 change state properly.

Within the limits of its dynamic range, U1 operates linearly, so the threshold at U2 can be referred to the input of U1 as an equivalent threshold voltage (i.e., divided by the gain of U1). Similarly, the HFBR-2203/-2204 Receiver makes a linear conversion of optical input to voltage output (typically 7 mV per μW), so the U2 threshold can be referred to the optical input as an equivalent optical power level. Consequently, changes of either the gain of U1 or the threshold at U2 affect the threshold-equivalent input power.

Likewise, the rms noise voltage at the input of U1 can be referred to the optical input as noise-equivalent input power.

Sensitivity is defined relative to noise and threshold, as the optical input power excursion needed to obtain reliable operation. It can be improved by applying bandwidth filtering to reduce the noise amplitude. Since the HFBR-2203/-2204 Receiver is well shielded, its output noise is due only to shot and thermal noise, for which the amplitude varies as the square root of the bandwidth. Consequently, applying bandwidth filtering at the output of the Receiver reduces the noise in the rest of the circuit. How this is done and with what benefit is discussed in the section on "Sensitivity Improvement with Data Rate Reduction".

Bandwidth filtering is useless unless interference (EMI) is less than the filter-reduced noise. For this reason the impedances to ground at the inputs of U1 must be balanced, even though the input signal from the HFBR-2203/-2204 Receiver is single-ended. This is done by making R_5 the same value as R_6, and C_{11} the same as C_{12}. This makes the impedances balanced because the internal impedance of the Receiver's output is very low, and only low values of R_{13} are used for bandwidth filtering. Further neutralization of EMI is achieved by making the traces connecting to the inputs of U1 of approximately the same length and located as close together as possible.

DESIGN DIFFERENCES

(HFBR-0221/-0222 and HFBR-0223/-0224)

The two versions of the Transceiver are designed with different data-handling objectives. The HFBR-0221/-0222 is intended for use with signals having a nearly 50% duty factor (such as Biphase or Manchester coded signals). The HFBR-0223/-0224 is intended for use as an edge detector (differentiator); with a very short time constant at C_{13} and C_{14}, the voltage levels are restored so rapidly that response time is virtually unaffected by the time differences between transitions in optical power, and for this reason it is capable of dealing with an arbitrary data format, such as NRZ and NRZI coded signals.

The difference in response modes is shown in Figure 1. It is clear that for the HFBR-0223/-0224 version, the edge timing is restricted only at the low end (minimum edge spacing or maximum signalling rate), where encroachment of one pulse might affect the next. For the HFBR-0221/-0222 version, a duty factor much more or much less than 50% would reduce the signal-to-noise ratio and also add propagation delay distortion.

Circuit adjustments to realize these differences in performance are mainly in the receiving side. Obviously, for the

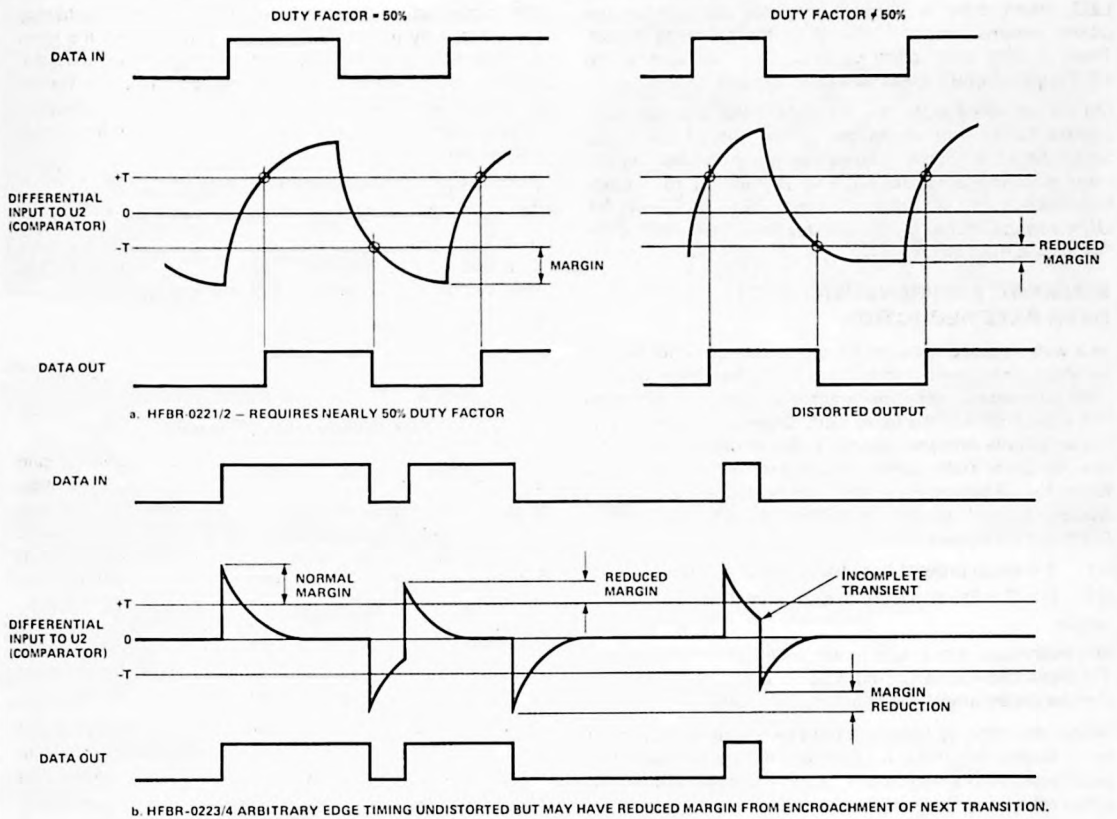


Figure 1. Transceiver Response Waveforms

HFBR-0221/-0222 version it is necessary only to make the time constants of C_{13} and C_{14} long enough to couple a rectangular waveform to the inputs of U2, then set U1 for high gain and make the thresholds at U2 the value which provides a threshold-to-noise ratio greater than six. For the HFBR-0221/-0222 version the time constant of C_{13}, C_{14} must be less than a third of the shortest time desired between successive edges. The peak amplitude of pulses reaching U2 will be limited by the short time constant, a situation which can be remedied somewhat by lowering the gain of U1 (thus raising its bandwidth). This, in turn will require reduction of the threshold at U2.

There is a limit to how far the U2 threshold can be reduced without making it too vulnerable to EMI from the transmitting side. Because of these design constraints, the accommodation of arbitrary data format is obtained at the expense of sensitivity; that is, the HFBR-0223/-0224 version requires excursions of optical input power slightly higher than the excursions required by the HFBR-0221/-0222 version.

There is also a limit to how much gain adjustment is possible at U1. The maximum possible gain is 400 with $R_7 = 0$, so the gain increase that is available is approximately 6 dB (i.e. x4 because of the linear relationship to input power). Raising the gain by a factor of four permits sensitivity improvement by the same ratio if the noise bandwidth is reduced by sixteen times.

On the transmitting side the difference is very small. Both versions are operated at the same steady-state input current to the HFBR-1201/-1202 Transmitter LED, but they have different peak-to-dc current ratios. The purpose of the peaking is mainly to charge the LED and stray capacitances, so the 2:1 peak-to-dc current ratio in the HFBR-0221/-0222 version does not overstress the LED even though the 80 mA peak exceeds the 40 mA data sheet specification for that part. In the HFBR-0223/-0224 version, the peaking is slightly reduced to make sure the trailing edge of the peak will not be sensed by the receiving circuit as a negative data transition.

CIRCUIT LAYOUT CONSIDERATIONS

In so far as possible, given the limited space, the sensitive portions of the receiving circuit are spaced away from the parts of the transmitting circuit that have large excursions of current and voltage. Components that have no signal function (power supply decoupling elements) are placed in the space between the receiving and transmitting circuits to further enhance the shielding. Traces connecting to balanced inputs are made as nearly as possible the same length and closely spaced. Of course, a ground-plane style of PC board layout is used, and the EMI/ESD Shields in the HFBR-4201/-4202 Mounting Hardware are installed.

The transmitting side requires only a single +5 V power supply. Because of the large excursion currents in the

LED, shunt drive is used to minimize reaction on the power supply, which is shared by the receiving circuit. There is also decoupling by L_1,C_1,C_2 in addition to the +5 V supply input bypass, C_{15},C_{16}.

On the receiving side, the −5 V supply has only the input bypass C_6,C_7 and single decoupling for U1 by L_2,C_8. Since the +5 V supply is shared with the transmitting circuit, considerable decoupling is needed to reduce interference. For U2 there is the first stage, L_4, C_4, C_5; for U1 a second stage, L_3,C_9; and for the HFBR-2203/-2204 Receiver a third stage, R_4,C_{10}.

SENSITIVITY IMPROVEMENT WITH DATA RATE REDUCTION

In a well-shielded receiver circuit, sensitivity is not limited by electro magnetic interference (EMI), but rather by random (Gaussian) noise for which the amplitude varies as the square root of the bandwidth. Sensitivity is defined as the amplitude of signal power needed to obtain sufficiently low Bit-Error Rate (BER), also known as Probability of Error, P_e. Obtaining $P_e < 10^{-9}$ in an ac-coupled circuit with hysteresis, such as used in HFBR-0221/-0222 and HFBR-0223/-0224, requires

a) $T > 6N$ to prevent false transition of output

b) $P > (T + 6N)$ to assure desired transition,

where

N = noise-equivalent input power (μW)
T = threshold-equivalent input power (μW)
P = excursion amplitude of input power (μW)

Noise reduction by filtering allows sensitivity improvement by reducing the noise amplitude. The filtered noise has amplitude, N in a bandwidth, B and the filtered/unfiltered noise ratio is:

$N/N_O = [B/B_O]^{0.5}$ as described above,

where

N_O = reference noise in a bandwidth, B_O

B_O = 25 MHz, the unfiltered 3-dB bandwidth of the HFBR-2203/4 Receiver

With noise reduced by the factor N/N_O, the threshold may be reduced by the same factor, and this allows the input excursion power to be reduced by N/N_O, while still obtaining $P_e < 10^{-9}$. If the noise is reduced by filtering, but no threshold adjustment is made, there is still some sensitivity improvement, but the improvement factor may be considerably less:

$P/P_O = N/N_O$ for threshold adjustment: $T/T_O = N/N_O$

$P/P_O = (1 + N/N_O)/2$ for no threshold adjustment

Bandwidth reduction is accomplished by lengthening the time constant at the output of the HFBR-2203/-2204 Receiver. The bandwidth, B, obtained by doing this is:

$B = 1/[(2 <\pi>) (Req) (C_{17})]$

where

Req = equivalent resistance of R_5 and R_{13} in parallel = $1/(1/R_5 + 1/R_{13})$

C_{17} = capacitance added in parallel with R_5

Threshold reduction can be done either by raising the gain of U1 or lowering the hysteresis set at U2, or by a combination. The simpler of the two is raising the gain of U1, since that requires changing the value of only one resistor, R_7; lowering R_7 raises the gain. The hysteresis setting at U2 should be kept balanced, so its reduction requires lowering R_8 and R_9 or raising R_{10} and R_{11}. It may even be necessary to change all four, since their values affect the time constant with C_{13} and C_{14}. The HFBR-0221/-0222 requires a long time constant, while the HFBR-0223/-0224 requires the time constant be kept short.

Bandwidth reduction will, or course, reduce the speed of response, and therefore the signalling rate will be reduced. A good rule for relating signalling rate to bandwidth is the ratio: two baud per hertz; that is, a 2 MHz bandwidth allows 4 MBd signalling.

A set of recommended component values and the anticipated result of such selection is listed in Table 1.

Table 1. Recommended Component Values and Typical Transceiver Performance (0° C to 70° C)

For HFBR-0221/-0222: (0.33 < Duty Factor < 0.67)

	1 MBd	5 MBd	20 MBd	40 MBd
R_{13} (ohms)	100	100	zero	zero
C_{17} (pF)	3300	680	100	100
R_7 (ohms)	zero	20	110	402
R_8 and R_9 (ohms)	1.0 k	1.0 k	1.0 k	1.0 k
R_{10} and R_{11} (ohms)	26.1 k	14.7 k	14.7 k	14.7 k

Minimum Power Budget (dB)

For Cabling Loss	17.5	14.0	9.0	6.0

Cable Length (metres)

@ 5.5 dB/km	3100	2500	1600	1000

Table 1. Recommended Component Values and Typical Transceiver Performance (0° C to 70° C) (cont.)

For HFBR-0223/-0224: (0.05 < Duty Factor < 0.95)

	1 MBd	5 MBd	20 MBd
R_{13} (ohms)	100	100	zero
C_{17} (pF)	3300	680	100
R_7 (ohms)	82.5	402	1620
C_{13} and C_{14} (pF)	1000	220	68
R_8 and R_9 (ohms)	0.215k	0.215k	0.215k
R_{10} and R_{11} (ohms)	8.25 k	8.25 k	8.25 k

Minimum Power Budget (dB)

For Cabling Loss	13.5	10.0	5.0

Cable Length (metres)

@ 5.5 dB/km	2400	1800	900

Schematic

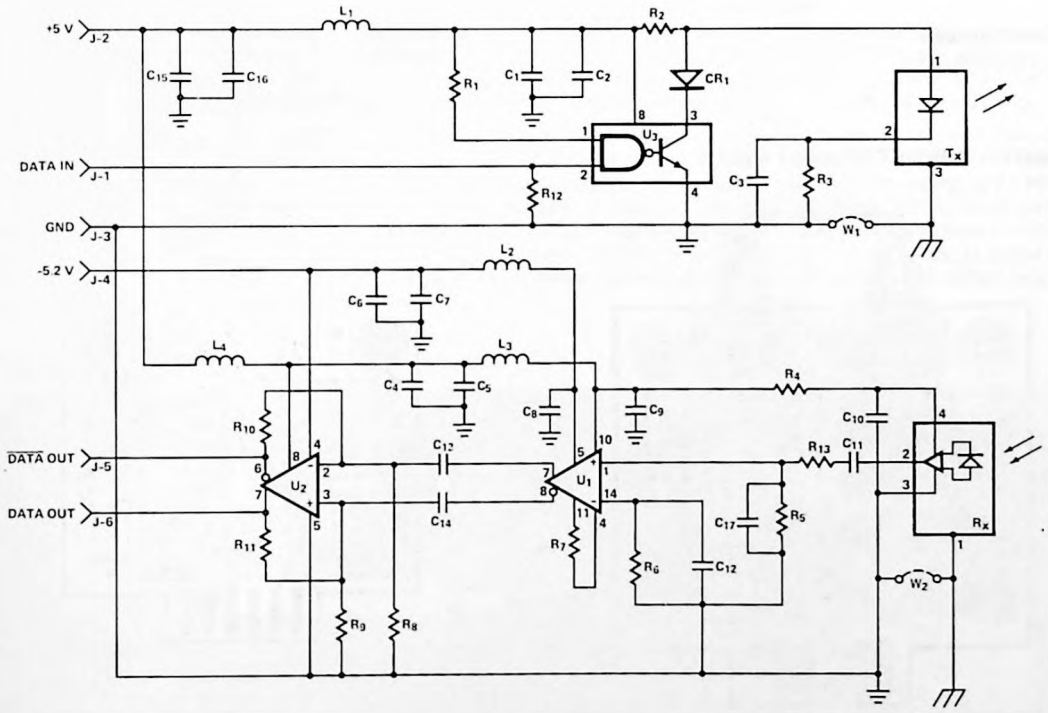


Figure 2.

COMPONENTS LIST

Common Components

Resistors	Part Description
R_1	10K Ω; 1%; 1/8W
R_4	51.1 Ω; 1%; 1/8W
$R_{5,6,12}$	1K Ω; 1% 1/8W
R_{13}	0 Ω (same as W_3)
Capacitors	
$C_{1,5,6,8,9,11,12,16}$	0.1 μF ceramic
C_2	47 μF tantalum
$C_{3,17}$	100 pF
$C_{4,7,15}$	4.7 μF tantalum
C_{10}	1 μF ceramic
Inductors	
$L_{1,2,3,4}$	2.7 μH ± 10%; Q = 40 @ 7.9 MHz dc res. = 0.55 ohms
Diode	
CR_1	1N3064
Integrated Circuits	
U1	LM-733C
U2	LM-360N
U3	MC-75451
Optional Jumpers	
$W_{1,2,3}$ ($W_3 = R_{13}$)	

PRODUCT SPECIFIC COMPONENTS

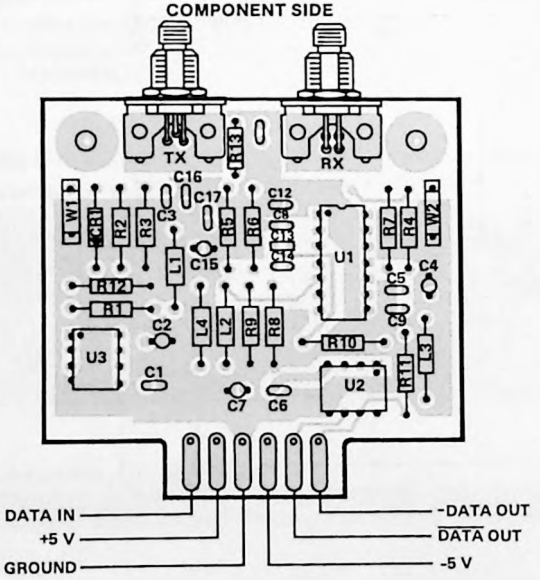
	HFBR-0221/-0222	HFBR-0223/-0224
Resistors		
R_2	43.0 Ω; 1%; 1/2W	51.0 Ω; 5%; 1/2W
R_3	42.2 Ω; 1%; 1/8W	31.6 Ω; 1%; 1/8W
R_7	110 Ω; 1%; 1/8W	1.62K Ω; 1%; 1/8W
$R_{8,9}$	1K Ω; 1%; 1/8W	215 Ω; 1%; 1/8W
$R_{10,11}$	14.7K Ω; 1%; 1/8W	8.25K Ω; 1%; 1/8W
Capacitors		
$C_{13,14}$	0.1 μF ceramic	68 pF

FIBER OPTIC COMPONENTS

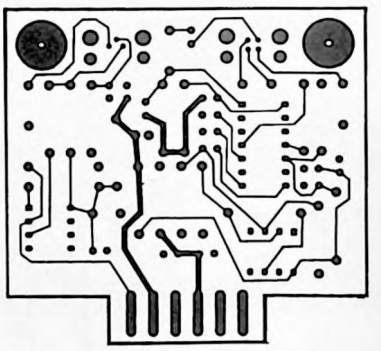
	HFBR-0221/-0223	HFBR-0222/-0224
T_X	HFBR-1201	HFBR-1202
R_X	HFBR-2203	HFBR-2204
Mounting Hardware	HFBR-4201	HFBR-4202

PRINTED CIRCUIT BOARD LAYOUT

COMPONENT SIDE



CIRCUIT SIDE



HEWLETT PACKARD

FIBER OPTIC 100m HIGH PERFORMANCE TRANSMITTER MODULE

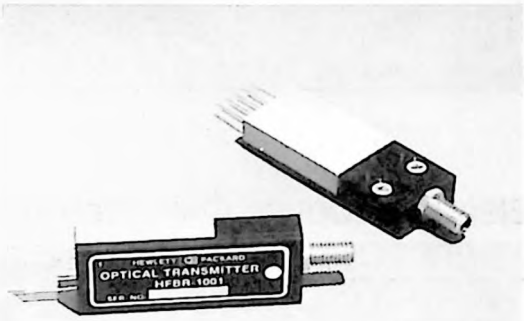
HFBR-1001

TECHNICAL DATA JANUARY 1984

Features

- **TRANSMISSION LENGTH: 100 METRES***
- **DATA RATE: DC TO 10 Mbaud***
- **NO DATA ENCODING REQUIRED***
- **TTL INPUT LEVELS**
- **FUNCTIONAL LINK MONITORING***
- **SINGLE +5V SUPPLY**
- **PCB MOUNTABLE, LOW PROFILE**
- **INTEGRAL, HIGH QUALITY OPTICAL CONNECTOR**
- **LOW POWER CONSUMPTION**

*When used with HFBR-2001 Receiver and any Hewlett Packard HFBR-3000/-3100 Series Cable/Connector Assembly.

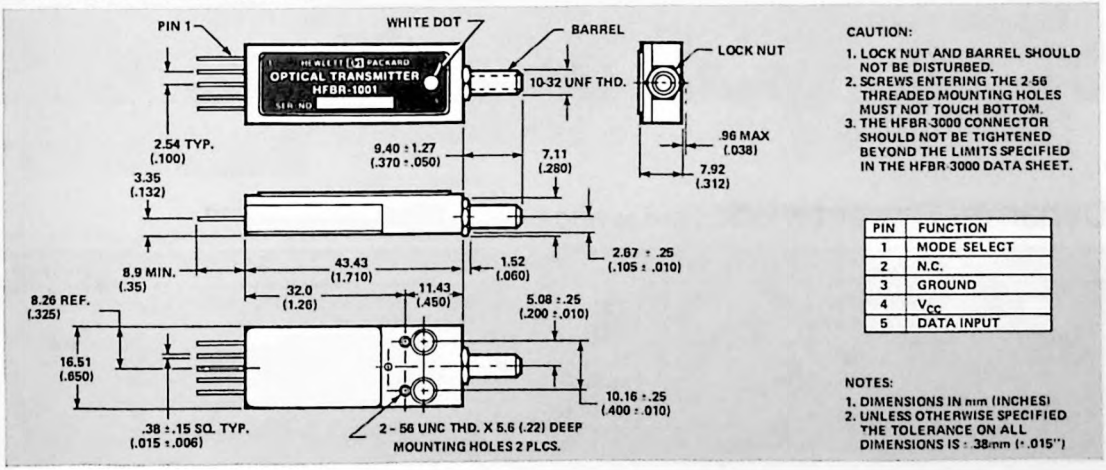


Description

The HFBR-1001 fiber optic transmitter is an integrated electrical to optical transducer designed for digital data transmission over single fiber channels. A bipolar integrated circuit and a GaAsP LED convert TTL level inputs to optical pulses at data rates from dc to 10Mb/s NRZ. An integral optical connector on the module allows easy interfacing without problems of source/fiber alignment. The low profile package is designed for direct printed circuit board mounting without additional heat sinking.

The HFBR-1001 is intended for use with HFBR-3000 fiber optic cable/connector assemblies, and the HFBR-2001 fiber optic receiver for transmission distances up to 100 metres. The HFBR-1001 generates optical signals in either of two externally selectable modes. The internally-coded mode produces a 3-level coded optical signal for reception and decoding by the HFBR-2001 receiver. This feature provides data format independence over the data rate range of dc to 10Mb/s NRZ while allowing for wide dynamic range and high sensitivity at the receiver. The externally-coded mode produces a 2-level optical signal which is a digital replica of the data input waveform. Used in this mode with the HFBR-2001 receiver, the user must provide proper data formatting (explained in the HFBR-2001 data sheet) to insure proper receiver operation. In either mode, the radiant output is radiologically safe (per ANSI Z136.1-1981).

Package Dimensions



CAUTION:

1. LOCK NUT AND BARREL SHOULD NOT BE DISTURBED.
2. SCREWS ENTERING THE 2-56 THREADED MOUNTING HOLES MUST NOT TOUCH BOTTOM.
3. THE HFBR-3000 CONNECTOR SHOULD NOT BE TIGHTENED BEYOND THE LIMITS SPECIFIED IN THE HFBR-3000 DATA SHEET.

PIN	FUNCTION
1	MODE SELECT
2	N.C.
3	GROUND
4	V_{CC}
5	DATA INPUT

NOTES:

1. DIMENSIONS IN mm (INCHES)
2. UNLESS OTHERWISE SPECIFIED THE TOLERANCE ON ALL DIMENSIONS IS ± .38mm (± .015")

FIBER OPTICS

Absolute Maximum Ratings

Parameter		Symbol	Min	Max	Units	Note
Storage Temperature		T_S	-55	+85	°C	
Operating Temperature		T_A	0	70	°C	
Lead Soldering	Temperature			260	°C	3
	Time			10	s	
Supply Voltage		V_{CC}	-0.5	6	V	
Mode Select or Data Input Voltage		V_I	-0.5	5.5	V	

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Units	Note
Ambient Temperature	T_A	0	70	°C	
Supply Voltage	V_{CC}	4.75	5.25	V	4
High Level Input Voltage, Mode Select or Data Input	V_{IH}	2.0	V_{CC}	V	
Low Level Input Voltage, Mode Select or Data Input	V_{IL}	0	0.8	V	
Data Input Voltage Pulse Duration (high or low)	t_H, t_L	100		ns	

Electrical/Optical Characteristics 0°C to 70°C Unless Otherwise Specified

Parameter		Symbol	Min	Typ(6)	Max	Units	Conditions		Fig.	Note
High Level Input Current	Mode Select	I_{IH}			100	µA	V_{CC} = 5.25V, V_I = 2.4V		2	
	Data Input				20					
Low Level Input Current	Mode Select	I_{IL}			-1.6	mA	V_{CC} = 5.25V, V_I = 0.4V			
	Data Input				-0.6					
Supply Current	Externally-Coded Mode	I_{CC}			170	mA	Mode Select High	Data Input High V_{CC} = 5.25V	1, 2	5
			40					Data Input Low V_{CC} = 4.75V		
	Internally-Coded Mode		68	95	125		Mode Select Low	Data Input High or Low V_{CC} = 5.25V		
Optical Power	High Level	P_H		67		µW	Mode Select High	Data Input High	1, 2, 3	
	Low Level	P_L		3				Data Input Low		
	Mid Level (average)	P_M		35			Mode Select Low	Data Input		
	Excursion $\left(\frac{\text{peak-to-peak}}{2}\right)$	ΔP	22	32			Mode Select High	Square Wave at 500 kHz		9
Amplitude Symmetry, Flux Excursion Ratio		k	0.8		1.2	—	Mode Select Low		1	7
Exit Numerical Aperture		N.A.		0.5		—			3	
Optical Port (fiber optic core) Diam.		D_C		200		µm				
Coupling Loss	from area mismatch	α_A		6.0		dB	with HFBR-3000 Cable/Connector Assembly			
	from numerical aperture mismatch	$\alpha_{N.A.}$		4.0						
Peak Emission Wavelength		λ_P		700		nm			4	

Dynamic Characteristics 0°C to 70°C Unless Otherwise Specified

Parameter		Symbol	Min	Typ(6)	Max	Units	Conditions	Fig.	Note
Propagation Delay	High-to-Low Data Input Voltage Step	t_{PHL}		31		ns	V_{CC} = 4.75 V	1	8
	Low-to-High Data Input Voltage Step	t_{PLH}		35		ns			
Refresh Pulse Internally-Coded Mode	Duration	t_p		60		ns	V_{CC} = 5.00 V, Mode Select Low	1	8
	Repetition Rate	f_R		400		kHz			

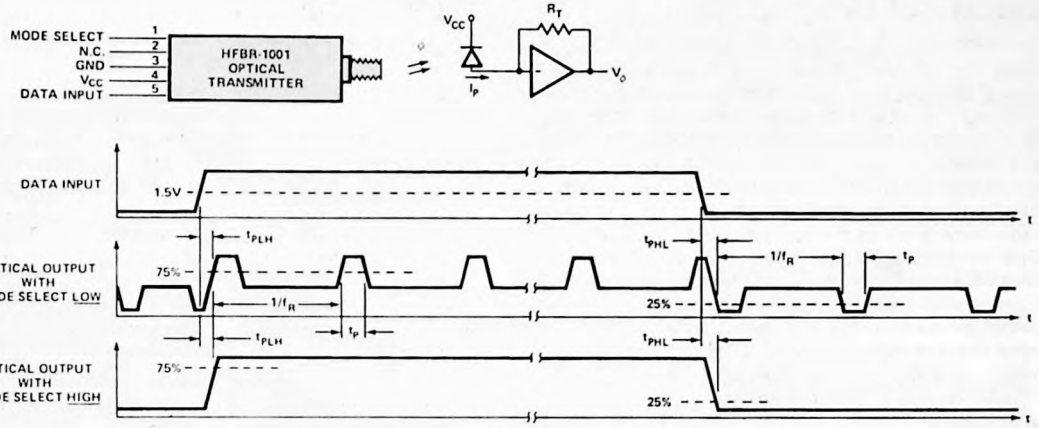


Figure 1. Optical Power Coding and Timing Diagram.

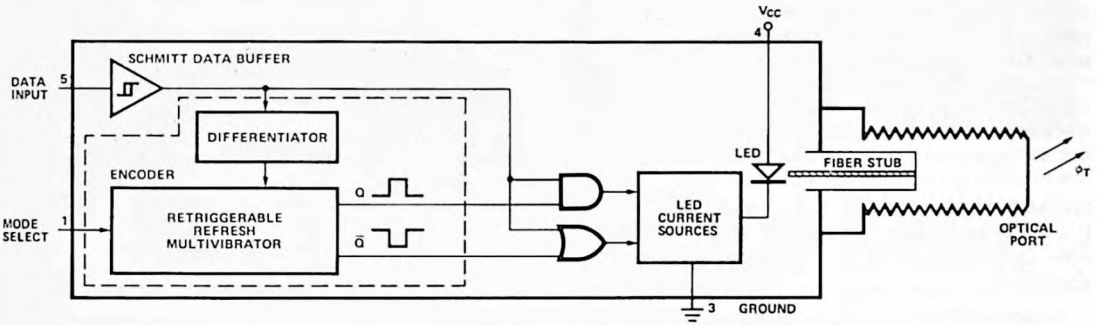


Figure 2. Schematic Diagram.

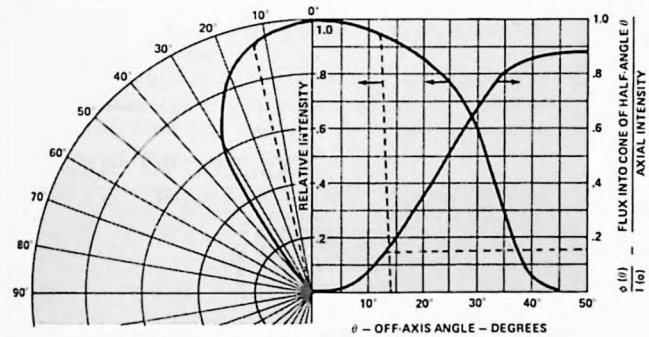


Figure 3. Radiation Pattern.*

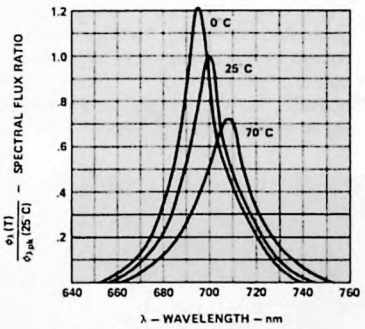


Figure 4. Emission Spectrum.

*The optical fiber is recessed within the barrel at a distance of approximately 7mm. Solid line represents radiation pattern from fiber stub without obscuration by connector barrel. Dashed line represents radiation pattern as seen from outside of connector.

Notes (cont'd):

3. Measured at a point 2mm (.079 in.) from where lead enters package.
4. A supply decoupling network of 2.2μH with 60μF is recommended.
5. Average currents for steady-state conditions at Data Input.
6. For typical values, V_{CC} = 5.00V and T_A = 25°C.
7. Optical power excursion ratio, k, is the ratio of optical power excursion above mid level to optical power excursion below mid level.
$$k = \frac{P_H - P_M}{P_M - P_L}$$
8. The refresh pulse is interrupted (abbreviated) if Data Input changes state during the refresh pulse. MAX propagation delay is for Data Input changing state during the maximum excursion of the refresh pulse.
9. Optical power excursion
$\Delta P = 0.5\,(P_H - P_L)$, or $\Delta P = 0.5\,(P_M - P_L) \bullet (1+k)$.

Notice that under the conditions specified for ΔP, the **average** flux is $(\Delta P + P_L)$.

Electrical Description

The HFBR-1001 has two modes of operation: Internally-Coded mode and Externally-Coded mode. These are selected by making the Mode Select input "low" for Internally-Coded mode and "high" for Externally-Coded mode. With Mode Select "low," the optical signal generator in the HFBR-1001 produces a "mid-level" optical power which has positive or negative excursions, depending on whether Data Input is "high" or "low." In this Internally-Coded mode, a train of positive excursions is initiated when Data Input goes "high;" when Data Input goes "low," a train of negative excursions is initiated. These excursions are pulses of approximately 60ns duration with a 400 kHz repetition rate. Each initiation of a pulse train starts with a full-duration pulse, but when Data Input changes state, the train is terminated — even at mid-pulse — as a new train of opposite-polarity pulses is initiated. With this coding scheme and the low duty factor, the average optical power is always near the mid-level, regardless of the data rate or duration in either state. This coding scheme is designed to operate the HFBR 2001 Fiber Optic Receiver most effectively; the mid-level flux operates the Receiver's dc-restorer and the "refresh" pulses of either polarity keep the Receiver's ALC voltage at the proper level, allowing low propagation delay for any change of state at Data Input. The Internally-Coded mode permits transmission of analog information, e.g., by means of Pulse Width Modulation. Another advantage of the 3-level Internally-Coded mode is that supply current is nearly the same for either logic state, this reducing transients on the power supply line.

With Mode Select "high," the optical signal is at full maximum (~2 X mid level) when Data Input is "high," and nearly zero when Data Input is "low." This mode provides for these three applications:

1. Steady state turn-on of the photo-emitter at maximum flux level (e.g., for system diagnosis).
2. Stand-by mode (e.g., when the system is not in use).
3. Transmission of 2-level optical signals from externally generated code (e.g., Manchester) for receivers not configured for the 3-level code. With Mode Select "high," the output is either P_H, or P_L. Direct analog operation is not possible due to hysteresis in the response of the optical signal to the Data Input signal.

Mechanical and Thermal Considerations

Typical power consumption is less than 500mW so the transmitter can be mounted without consideration for external heat sinking. The optical port is an optical fiber stub centered in a metallic ferrule. This ferrule supports a split-wall cylindrical spring sleeve which aligns the ferrule in the Transmitter with the ferrule in the HFBR-3000 Fiber Optic Cable/Connector. The connection procedure is to FIRST start the Connector ferrule into the sleeve; THEN screw the coupling ring on the barrel. The barrel performs no alignment function; its purpose is to hold the ferrule faces together when the coupling ring is tightened as specified in the HFBR-3000 Fiber Optic Cable/Connector data sheet.

The HFBR-1001 should be mounted so that the lock nut at the optical port is not disturbed. Moving the lock nut can cause misalignment of the optical fiber stub inside the module resulting in a reduction of power output. Mounting at the edge of a printed circuit board with the lock nut overhanging the edge is recommended.

Good system performance requires clean ferrule faces to avoid obstructing the optical path. Clean compressed air often is sufficient to remove particles of dirt; methanol or Freon™ on a cotton swab also works well. If it is absolutely necessary to remove the threaded barrel and lock nut to clean the transmitter ferrule face, refer to the section "Installation Measurement and Maintenance" in Hewlett-Packard Application Note 1000.

HEWLETT PACKARD

FIBER OPTIC 1250m HIGH PERFORMANCE TRANSMITTER MODULE

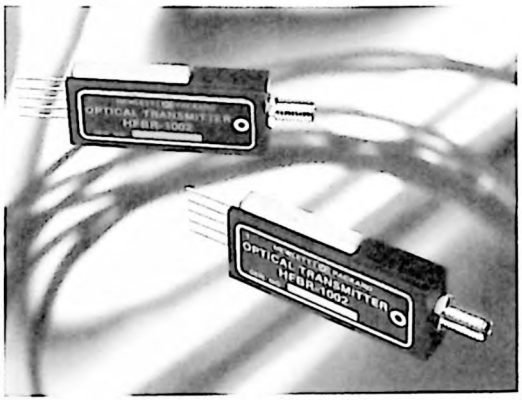
HFBR-1002

TECHNICAL DATA JANUARY 1984

Features

- **PIN COMPATIBLE WITH HFBR-1001 TRANSMITTER**
- **TRANSMISSION LENGTH: 1250 METRES***
- **DATA RATE: DC TO 10 Mbaud***
- **NO DATA ENCODING REQUIRED***
- **TTL INPUT LEVELS**
- **FUNCTIONAL LINK MONITORING***
- **SINGLE +5V SUPPLY**
- **PCB MOUNTABLE, LOW PROFILE**
- **INTEGRAL, HIGH QUALITY OPTICAL CONNECTOR**
- **LOW POWER CONSUMPTION**

*When used with HFBR-2001 Receiver and any Hewlett Packard HFBR-3000/-3100 Series Cable/Connector Assembly.



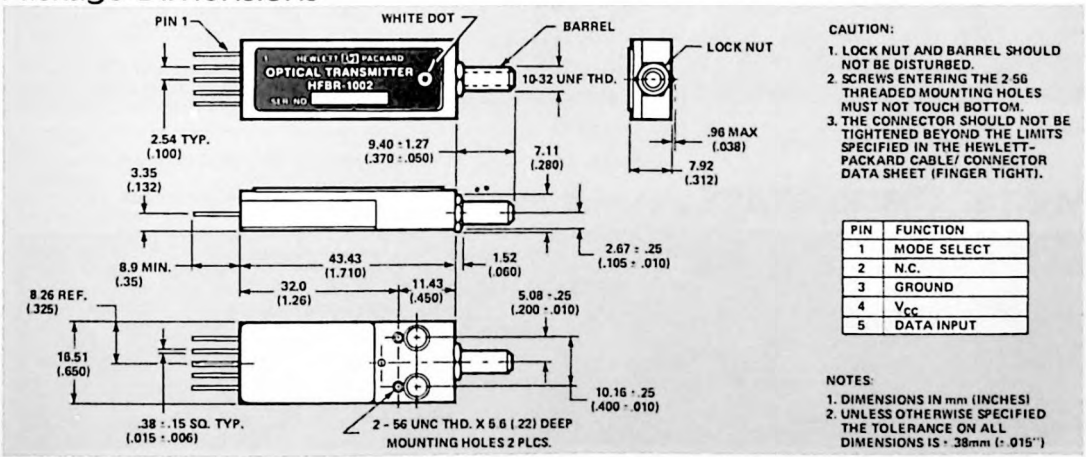
Description

The HFBR-1002 fiber optic transmitter is an integrated electrical to optical transducer designed for digital data transmission over single optical fiber channels. A bipolar integrated circuit and a high efficiency GaAlAs LED convert TTL level inputs to optical pulses at data rates from dc to 10 Mbaud (see note 5). An integral optical connector on the module allows easy interfacing without problems of fiber alignment. The low profile rugged industrial package is designed for direct circuit board mounting without additional heat sinking on printed circuit boards with 12.7 mm (0.5") card rack spacing.

The HFBR-1002 is intended for use with Hewlett-Packard fiber optic cable/connector assemblies, and the HFBR-2001 fiber optic receiver for transmission distances to 1250 metres. It is a direct replacement for extending links currently using the HFBR-1001 (100 metre) transmitter to give 1250 metre capability. The HFBR-1002 generates optical signals in either of two externally selectable modes. True dc response (data high or low for arbitrary time interval) is available when using the Internally-Coded mode.

WARNING: OBSERVING THE TRANSMITTER OUTPUT FLUX UNDER MAGNIFICATION MAY CAUSE INJURY TO THE EYE. When viewed with the unaided eye, the near IR output flux is radiologically safe; however, when viewed under magnification, precaution should be taken to avoid exceeding the limits recommended in ANSI Z136.1-1981.

Package Dimensions



CAUTION:

1. LOCK NUT AND BARREL SHOULD NOT BE DISTURBED.
2. SCREWS ENTERING THE 2-56 THREADED MOUNTING HOLES MUST NOT TOUCH BOTTOM.
3. THE CONNECTOR SHOULD NOT BE TIGHTENED BEYOND THE LIMITS SPECIFIED IN THE HEWLETT-PACKARD CABLE/ CONNECTOR DATA SHEET (FINGER TIGHT).

PIN	FUNCTION
1	MODE SELECT
2	N.C.
3	GROUND
4	V_{CC}
5	DATA INPUT

NOTES:

1. DIMENSIONS IN mm (INCHES)
2. UNLESS OTHERWISE SPECIFIED THE TOLERANCE ON ALL DIMENSIONS IS ± .38mm (± .015")

FIBER OPTICS

Absolute Maximum Ratings

Parameter		Symbol	Min	Max	Units	Note
Storage Temperature		T_S	-55	+85	°C	
Operating Temperature		T_A	0	+70	°C	
Lead Soldering	Temperature			260	°C	3
	Time			10	s	
Supply Voltage		V_{CC}	-0.5	6	V	
Mode Select or Data Input Voltage		V_I	-0.5	5.5	V	

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Units	Note
Ambient Temperature	T_A	0	+70	°C	
Supply Voltage	V_{CC}	4.75	5.25	V	4
High Level Input Voltage, Mode Select or Data Input	V_{IH}	2.0	V_{CC}	V	
Low Level Input Voltage, Mode Select or Data Input	V_{IL}	0	0.8	V	
Data Input Voltage Pulse Duration (high or low)	t_H, t_L	100		ns	5
Transmission Distance	ℓ		1250	m	6

Electrical/Optical Characteristics 0°C to+ 70°C Unless Otherwise Specified

Parameter		Symbol	Min	Typ[7]	Max	Units	Conditions		Fig.	Note
Optical Power	Transmitter Output $\left(\frac{\text{peak-to-peak}}{2}\right)$	P_O	-13	-11		dBm	Mode Select High	Data Input Square Wave at 500 kHz	1, 2,	8
			50	80		μW				
	High Level	P_H		165		μW	Mode Select High	Data Input High	3, 5	
	Low Level	P_L		5				Data Input Low		
	Mid Level	P_M		85			Mode Select Low	Data Input Square Wave at 500 kHz		
Fixed Coupling Loss		α_F		1.5	5.4	dB	with HFBR-3000/3100 $\ell > 300M$			12
Output Optical Power		P_T		-21		dBm	50/125 μm Fiber N.A. = 0.21, g = 2			13
				-12.5		dBm	HFBR-3000/3100 100/140 μm Fiber N.A. = 0.28, g = 2			
Amplitude Symmetry, Flux Excursion Ratio		k	0.8		1.2	—	Mode Select Low		1	9
Exit Numerical Aperture		N.A.		0.3		—			3	
Optical Port (fiber optic core) Diam.		D_C		100		μm				
Peak Emission Wavelength		λ_{PK}		820		nm			4	
High Level Input Current	Mode Select	I_{IH}			100	μA	V_{CC} = 5.25V, V_I = 2.4V		2	
	Data Input				20					
Low Level Input Current	Mode Select	I_{IL}			-1.6	mA	V_{CC} = 5.25V, V_I = 0.4V			
	Data Input				-0.6					
Supply Current	Externally-Coded Mode	I_{CC}			170	mA	Mode Select High	Data Input High V_{CC} = 5.25V	1, 2	10
			40					Data Input Low V_{CC} = 4.75V		
	Internally-Coded Mode		68	95	125		Mode Select Low	Data Input High or Low, V_{CC} = 5.25V		

Dynamic Characteristics 0°C to 70°C Unless Otherwise Specified

Parameter		Symbol	Min	Typ[7]	Max	Units	Conditions	Fig.	Note
Propagation Delay	High-to-Low Data Input Voltage Step	t_{PHL}		34		ns	V_{CC} = 4.75 V Data Input Square Wave at 500 kHz	1	11
	Low-to-High Data Input Voltage Step	t_{PLH}		32		ns			
Refresh Pulse Internally-Coded Mode	Duration	t_p		40		ns	V_{CC} = 5.00 V, Mode Select Low	1	11
	Repetition Rate	f_R		400		kHz			

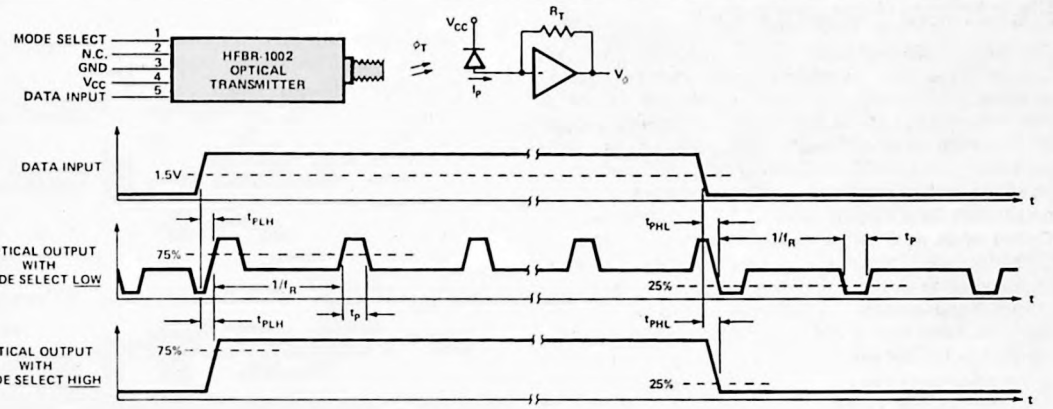


Figure 1. Flux Coding and Timing Diagram.

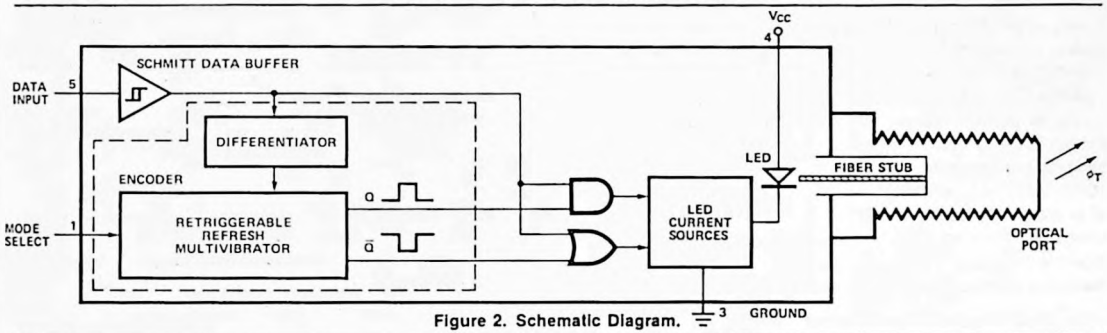


Figure 2. Schematic Diagram.

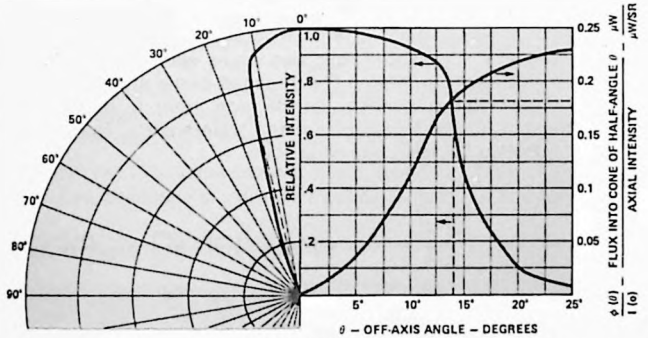


Figure 3. Radiation Pattern.*

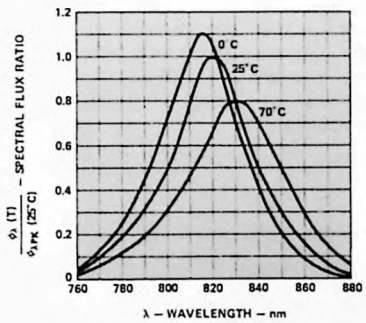


Figure 4. Emission Spectrum.

*The optical fiber is recessed within the barrel at a distance of approximately 7mm. Solid line represents radiation pattern from fiber stub without obscuration by connector barrel. Dashed line represents radiation pattern as seen from outside of connector.

Notes (cont'd):

3. Measured at a point 2mm (.079 in.) from where lead enters package.
4. A supply decoupling network of 2.2μH with 60μF is recommended.
5. With NRZ data, 10 Mbaud corresponds to a data rate of 10 Mbits/second. With other codes, the data rate is the baud rate divided by the number of code intervals per bit interval. Self-clocking code (e.g., Manchester) usually has two code intervals per bit interval giving 5 Mbits/second at 10 Mbaud.
6. With Hewlett-Packard HFBR-2001 and HFBR-3000 Series Cable/Connector Assembly.
7. For typical values, V_{CC} = 5.00V and T_A = 25°C.
8. The transmitter output, P_T, equals the optical power excursion, $\Delta P = (P_H - P_L)/2$. Notice that under the conditions specified for ΔP, the average optical power is $(P_H + P_L)/2$.
9. Optical power excursion ratio, k, is the ratio of optical power excursion above mid level to optical power excursion below mid level.

$$k = \frac{P_H - P_M}{P_M - P_L}$$

10. Average currents for steady-state conditions at Data Input.
11. The refresh pulse is interrupted (abbreviated) if Data Input changes state during the refresh pulse. MAX propagation delay is for Data Input changing state during the maximum excursion of the refresh pulse.
12. When used with the HFBR-3000/3100 cable assemblies, the total insertion loss (α_T) is calculated as follows:

    $\alpha_T = 8.4$ dB; $\ell \leq 300$m

    $\alpha_T = \alpha_F + \alpha_O \cdot \ell/1000$; $\ell > 300$m

    Where α_O = Cable attenuation at 820 nm; ℓ = cable length (metres).
13. Measured at the end of 1.0 meter of fiber optic cable with large area detector and cladding modes stripped.

FIBER OPTICS

Electrical Description

The HFBR-1002 has two modes of operation: Internally-Coded mode and Externally-Coded mode. These are selected by making the Mode Select input "low" for Internally-Coded mode and "high" for Externally-Coded mode. With Mode Select "low," the optical signal generator in the HFBR-1002 produces a "mid-level" optical power which has positive or negative excursions, depending on whether Data Input is "high" or "low". In this Internally-Coded mode, a train of positive excursions is initiated when Data Input goes "high," when Data Input goes "low", a train of negative excursions is initiated. These excursions are pulses of approximately 40ns duration with a 400kHz repetition rate. Each initiation of a pulse train starts with a full-duration pulse, but when Data Input changes state, the train is terminated — even at mid-pulse — as a new train of opposite-polarity pulses is initiated. With this coding scheme and the low duty factor, the average optical power is always near the mid-level, regardless of the data rate or duration in either state. This coding scheme, which is transparent to the user, is designed to operate the HFBR-2001 Fiber Optic Receiver most effectively; the mid-level flux operates the Receiver's dc-restorer and the "refresh" pulses of either polarity keep the Receiver's ALC voltage at the proper level, providing data format independence (no data encoding required) over the data rate range of dc to 10Mbaud. The Internally-Coded mode permits transmission of analog information, e.g., by means of Pulse Width Modulation. Another advantage of the 3-level Internally-Coded mode is that supply current is nearly the same for either logic state, thus reducing transients on the power supply line.

With Mode Select "high," the optical signal is at full maximum (~2 X mid-level) when Data Input is "high," and nearly zero when Data Input is "low." Used in this mode with the HFBR-2001 Receiver, the user must provide proper data formatting (e.g., Manchester or Bi-Phase coding, explained in HFBR-2001 data sheet) to ensure proper receiver operation. This mode provides for these three applications:

1. Steady state turn-on of the photo-emitter at maximum flux level (e.g., for system diagnosis).
2. Stand-by mode (e.g., when the system is not in use).
3. Transmission of 2-level optical signals from externally generated code (e.g., Manchester) for receivers not configured for the 3-level code. With Mode Select "high," the output is either P_H, or P_L. Direct analog operation is not possible due to hysteresis in the response of the optical signal to the Data Input signal.

Mechanical and Thermal Considerations

Typical power consumption is less than 500mW so the transmitter can be mounted without consideration for external heat sinking. The optical port is an optical fiber stub centered in a metallic ferrule. This ferrule supports a split-wall cylindrical spring sleeve which aligns the ferrule in the Transmitter with the ferrule in the Hewlett-Packard Fiber Optic Cable/Connector Assembly. The threaded barrel performs no alignment function; its purpose is to hold the ferrule faces together when the coupling ring is tightened finger-tight as specified in the Hewlett-Packard Fiber Optic Cable/Connector data sheet.

The HFBR-1002 should be mounted so that the lock nut at the optical port is not disturbed. Moving the lock nut can cause misalignment of the optical fiber stub inside the module resulting in a reduction of power output. Mounting at the edge of a printed circuit board with the lock nut overhanging the edge is recommended.

Good system performance requires clean ferrule faces to avoid obstructing the optical path. Clean compressed air often is sufficient to remove particles of dirt; methanol or Freon™ on a cotton swab also works well. If it is absolutely necessary to remove the threaded barrel and lock nut to clean the transmitter ferrule face, refer to the section "Installation Measurement and Maintenance" in Hewlett-Packard Application Note 1000.

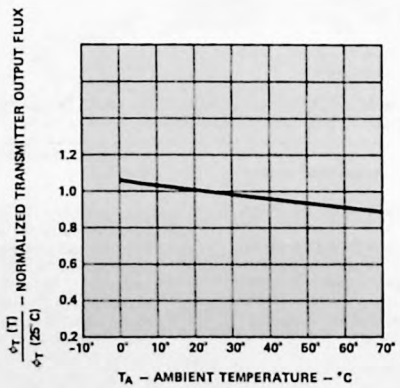


Figure 5. Normalized Transmitter Output Flux vs. Temperature.

HEWLETT PACKARD

FIBER OPTIC HIGH PERFORMANCE RECEIVER MODULE

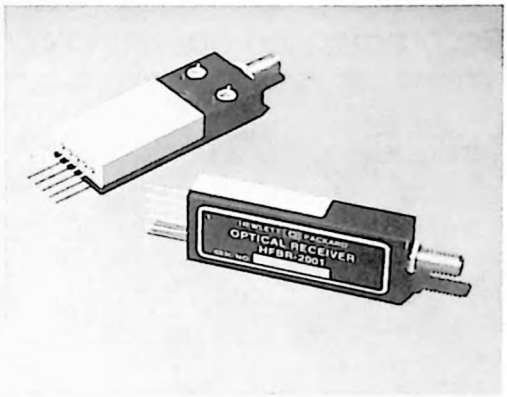
HFBR-2001

TECHNICAL DATA JANUARY 1984

Features

- DATA RATE: DC TO 10 Mbaud*
- LOW NOISE: 10^{-9} BER WITH 0.8 μ W INPUT*
- NO DATA ENCODING REQUIRED*
- TTL OUTPUT LEVELS
- FUNCTIONAL LINK MONITORING*
- OPTICAL POWER INPUT INDICATION
- SINGLE +5V SUPPLY
- PCB MOUNTABLE, LOW PROFILE
- INTEGRAL, HIGH QUALITY OPTICAL CONNECTOR.

*When used with HFBR-1001/-1002 Transmitters and any Hewlett Packard HFBR-3000/-3100 Series Cable/Connector Assembly.



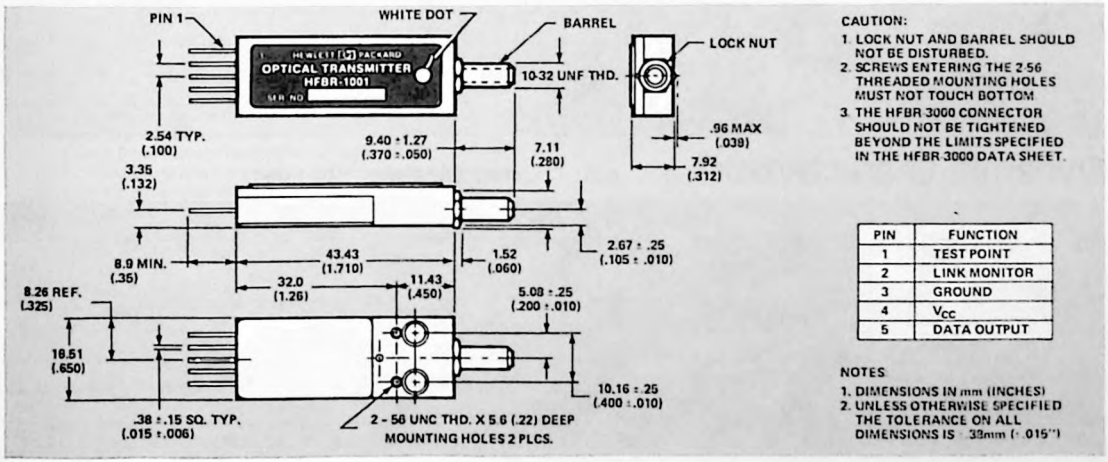
Description

HFBR-2001 fiber optic receiver is an integrated optical to electrical transducer designed for reception of digital data over single fiber channels. A silicon PIN photodetector and a bipolar integrated circuit convert optical pulses to TTL level outputs with an optical sensitivity of .8 μW, and data rates to 10 Mb/s NRZ. An integral optical connector on the module allows easy interfacing without problems of fiber/detector alignment. The low profile package is designed for direct printed circuit board mounting without additional heat sinking.

The HFBR-2001 is intended for use with HFBR-3000 fiber optic cable/connector assemblies and the HFBR-1001/1002 fiber optic transmitters. In order to provide wide dynamic range, dc response, and high sensitivity, the receiver must periodically extract information from the optical waveform. When operating with a transmitter in the internally-coded mode, this information is automatically provided by the transmitter. When operating in the externally-coded mode, or with another transmission source, the user must provide proper data formatting to insure proper receiver operation.

An additional TTL output called Link Monitor (LM), provides a digital indication of link continuity independent of the presence of data. Link continuity is indicated by a logical high output state.

Package Dimensions



CAUTION:

1. LOCK NUT AND BARREL SHOULD NOT BE DISTURBED.
2. SCREWS ENTERING THE 2-56 THREADED MOUNTING HOLES MUST NOT TOUCH BOTTOM.
3. THE HFBR-3000 CONNECTOR SHOULD NOT BE TIGHTENED BEYOND THE LIMITS SPECIFIED IN THE HFBR-3000 DATA SHEET.

PIN	FUNCTION
1	TEST POINT
2	LINK MONITOR
3	GROUND
4	V_{CC}
5	DATA OUTPUT

NOTES:

1. DIMENSIONS IN mm (INCHES).
2. UNLESS OTHERWISE SPECIFIED THE TOLERANCE ON ALL DIMENSIONS IS ± .33mm (± .015").

FIBER OPTICS

Absolute Maximum Ratings

Parameter		Symbol	Min	Max	Units	Note
Storage Temperature		T_S	-55	85	°C	
Operating Temperature		T_A	0	70	°C	
Lead Soldering Cycle	Temperature			260	°C	3
	Time			10	s	
Supply Voltage		V_{CC}	-0.5	6.0	V	
Output Voltage (High State)		V_{OH}		6.0	V	

Recommended Operating Conditions

Parameter			Symbol	Min	Max	Units	Note
Ambient Temperature			T_A	0	70	°C	
Supply Voltage			V_{CC}	4.75	5.25	V	
Supply Ripple (Peak-to-Peak)			ΔV_{CC}		250	mV	4
High Level Output Current	Link Monitor		I_{OH}		-100	μA	
	Data Output				-400		
Low Level Output Current			I_{OL}		8	mA	
Average Input Optical Power			P_M	0.8	70	μW	6
Peak-to-Peak Input Optical Power			P_H-P_L	1.6	140	μW	
Optical Input Pulse Duration and Timing	2-Level Code	High Level	t_H	100	5000	ns	
		Low Level	t_L				
	Flux Excursion Ratio		k	0.75	1.25		7
	3-Level Code	High Level	t_H	50		ns	8
		Low Level	t_L				
		Mid Level	t_M	0.05	6.7	μs	
	Refresh Repetition Rate		f_R	150		kHz	
	Refresh Duty Factor		$f_R t_H$, $f_R t_L$		0.04		

Electrical/Optical Characteristics 0°C to 70°C Unless Otherwise Specified

Parameter			Symbol	Min	Typ[5]	Max	Units	Conditions		Fig.	Note
Output Voltage	High State	Data Output	V_{OH}	2.4	2.85		V	$P = (P_M + 0.8\ \mu W)$, $I_o = -400\ \mu A$	V_{CC} = 4.75 V	1, 2	7, 9
		Link Monitor						$\Delta P = 0.8\ \mu W$, $I_o = -100\ \mu A$			
	Low State	Data Output	V_{OL}		0.35	0.5	V	$P = (P_M - 0.8\ \mu W)$	I_o = 8 mA, V_{CC} = 4.75 V		
		Link Monitor			0.2	0.4		$\Delta P = 0$			
Test Point Voltage			V_T		0		V	$P_M = 100\ \mu W$			10
					1.3			$P_M = 0$			
Supply Current			I_{CC}		77	100	mA	V_{CC} = 5.25 V			
				60	77			V_{CC} = 4.75 V			
Optical Port (fiber optic core) Diameter			D_c		200		μm				
Numerical Aperture			N.A.		0.5					3	
Peak Responsivity Wavelength			λ_p		770		nm			4	

Dynamic Characteristics 0°C to 70°C Unless Otherwise Specified

Parameter			Symbol	Min	Typ[5]	Max	Units	Conditions	Fig.	Note
Propagation Delay	High to Low	3-Level Code	t_{PHL}		29		ns	V_{CC} = 4.75 V, k = 1, Link Monitor High	1	11
		2-Level Code			37					
	Low to High	3-Level Code	t_{PLH}		37		ns			12
		2-Level Code			45					
Link Monitor Response Time	Low-to-High		t_{MH}		20		ms	V_{CC} = 4.75 V, Δp = 0.8 μW		13
	High-to-Low		t_{ML}		1000			I_{OL} = 8 mA, Peak-to-Peak		14
Bit Error Rate at 10 M baud			BER			10^{-9}		k = 1, $\Delta p \geq 0.8\ \mu W$		15

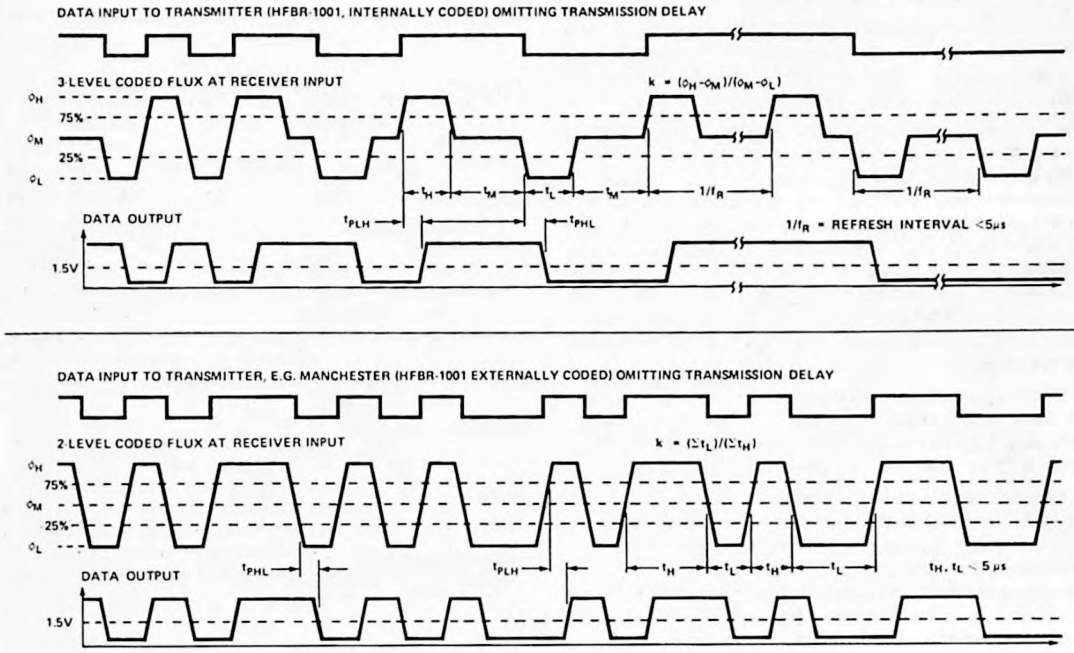


Figure 1. Optical Input Timing Requirements.

Notes (cont'd):

3. Measured at a point 2mm (.079") from where the lead enters the package.
4. If ripple exceeds the specified limit, the regulator shown in Figure 5 should be used. The LC filter shown in Figure 5 is recommended whether the regulator is used or not.
5. For typical values, V_{CC} = 5.00V and T_A = 25°C.
6. Optical power is average over an interval of at least 50 μs. Optical power values specified are for the equivalent of a monochromatic source between 700nm and 820nm.
7. For either 2-level or 3-level code, $k = (P_H - P_M)/(P_M - P_L)$.
8. For the HFBR-2001, a *3-Level Code* is defined as having a mid-level, with equal-amplitude and pulse width excursions to high-level or to low-level.
9. Link Monitor provides a check of link continuity. A low Link Monitor output indicates that the optical signal path has been interrupted. For example, it might indicate a broken cable or a loose, dirty, or damaged connector. The link may still be operational with Link Monitor low, but it should be checked to determine the cause of the low indication. When the source of optical power is an Internally-Coded HFBR-1001/1002 Fiber Optic Transmitter, Link Monitor high will be a valid indication of link continuity whether or not data is being transmitted. An optical input with excursions (ΔP) greater than or equal to 0.8μW is sufficient to hold Link Monitor high.
10. When observing V_T, use a voltmeter with at least 10MΩ input resistance. With zero input optical power, V_T is at its maximum value, $V_{T,MAX}$. Then when flux is being received, whether modulated or not:
    $(V_{T,MAX} - V_T) = (25k\Omega)(I_P) = (25k\Omega)(R_P P_M)$
    where I_P = average photodiode photocurrent
    $R_P \approx 0.4A/W$ = photodiode responsivity
    P_M = average flux being received
11. Measured from the time at which optical input crosses the 25% level until DATA OUTPUT = 1.5V in HL transition.
12. Measured from the time at which optical input crosses the 75% level until DATA OUTPUT = 1.5V in LH transition.

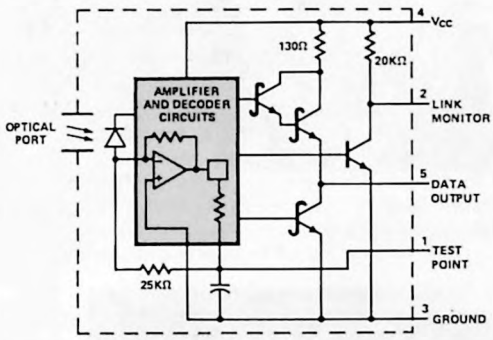


Figure 2. Schematic Diagram.

13. Measured from the time at which optical input fluctuation begins until LINK MONITOR rises to 1.5V.
14. Measured from the time at which optical input fluctuation ceases until LINK MONITOR falls to 1.5V.
15. With NRZ data, 10Mbaud corresponds to a data rate of 10Mb/s. With other codes, the data rate is the baud rate divided by the number of code intervals per bit interval—self-clocking code (e.g., Manchester) usually has two code intervals per bit interval giving 5Mb/s at 10Mbaud.

Electrical Description

Flux enters the HFBR-2001 via an optical fiber stub where a PIN photodiode converts it to a photocurrent. This photocurrent goes to an I-V (current-to-voltage) amplifier which utilizes both dc feedback and ALC (automatic level control).

The function of dc feedback is to keep the average value of the signal centered in the linear range of the amplifier. The dc feedback amplifier has a high impedance output to establish a long time constant on a capacitor at its output. (The voltage on the capacitor is observable at the test point). As seen in the schematic diagram, the voltage on this capacitor extracts the *average* component of photocurrent from the input of the I-V amplifier so its *average* output is at a *fixed level*. Optical flux excursions above and below the average cause voltage excursion above and below the fixed level at the output of the I-V amplifier.

The voltage excursions operate a flip-flop whose output drives the Data Output amplifier; an excursion above the average level sets the data output high, where it remains until an excursion below the average level resets the flip-flop.

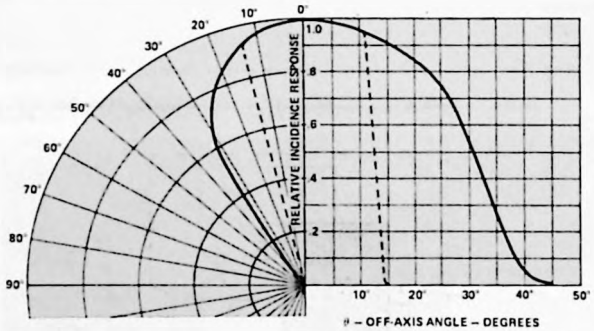
To prevent overdrive, an ALC circuit, responding to excursions *either above or below* the average level, controls the gain of the I-V amplifier. Gain is then determined by *whichever polarity* of excursion is the *greater*. If these excursions are too far from being balanced, the gain limitation imposed by the larger excursion may cause the smaller (opposite polarity) excursion to be too small to operate the flip-flop.

The Link Monitor output is driven by an amplifier which responds to the ALC voltage. The Link Monitor is high when the flux excursions are greater than or equal to 0.8μW.

Mechanical and Thermal Considerations

Typical power consumption is less than 500mW so the Receiver can be mounted without consideration for additional heat sinking. The optical port is an optical fiber stub centered in a metallic ferrule. This ferrule supports a split-wall cylindrical spring sleeve which aligns the ferrule in the Receiver with the ferrule in the HFBR-3000 Fiber Optic Cable/Connector. The connection procedure is to FIRST start the Connector ferrule into the sleeve, THEN screw the coupling ring on the barrel. The barrel performs no alignment function; its purpose is to hold the ferrule faces together when the coupling ring is tightened as specified in the HFBR-3000 Fiber Optic Cable/Connector data sheet.

Good system performance requires clean ferrule faces to avoid obstructing the optical path. Clean compressed air often is sufficient to remove particles of dirt; methanol or Freon™ on a cotton swab also works well. If it is absolutely necessary to remove the threaded barrel and lock nut to clean the Receiver ferrule face, refer to the section "Installation Measurement and Maintenance" in Hewlett-Packard Application Note 1000.



*The optical fiber is recessed within the barrel at a distance of approximately 7mm. Solid line represents reception pattern at fiber stub without obscuration by connector barrel. Dashed line represents reception pattern as seen from outside of connector.

Figure 3. Reception Pattern.*

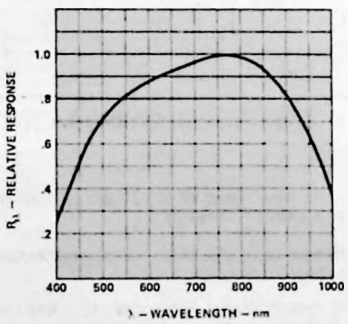


Figure 4. Spectral Response.

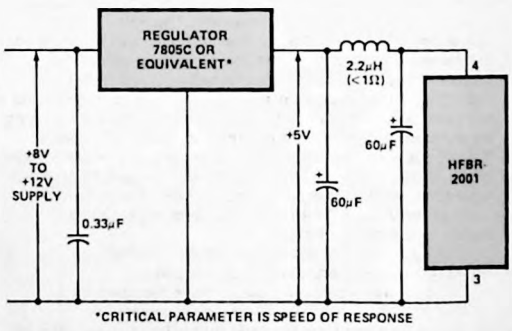


Figure 5. Power Supply Transient Filter Recommendation.

HEWLETT PACKARD

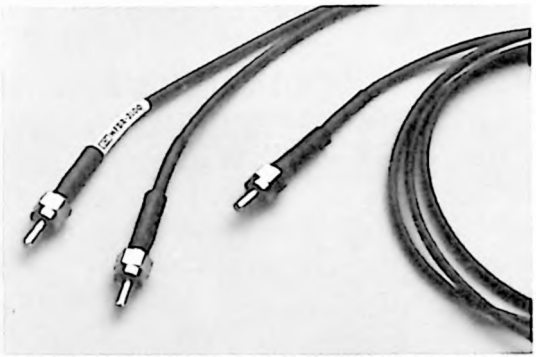
FIBER OPTIC CABLE/CONNECTOR ASSEMBLIES

HFBR-3000
HFBR-3100
HFBR-3001
HFBR-3021

TECHNICAL DATA JANUARY 1984

Features

- HFBR-4000 OR SMA STYLE CONNECTORS
- CONNECTORS FACTORY INSTALLED AND TESTED
- SIMPLEX OR DUPLEX CABLE
- USER SPECIFIED CABLE LENGTHS
- UL RECOGNIZED COMPONENT PASSES UL VW1 FLAME RETARDANCY SPECIFICATION*
- STANDARD 100/140 μm GLASS FIBER
- RUGGED TIGHT JACKET CONSTRUCTION
- PARAMETERS OPTIMIZED FOR LOCAL DATA COMMUNICATIONS
- BANDWIDTH: 40 MHz AT 1 km



Description

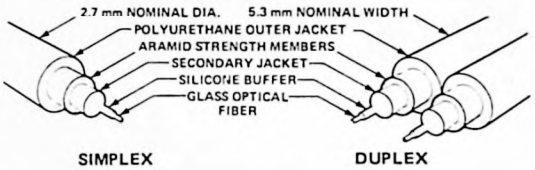
The HFBR-3000 Simplex Fiber Optic Cable/Connector assemblies and HFBR-3100 Duplex Fiber Optic Cable/Connector assemblies are intended for use with HP's High Performance Modules (HFBR-1001/2, HFBR-2001) and the Miniature Link series of transmitters and receivers (HFBR-12XX, HFBR-22XX) and 39301A RS-232 to Fiber Optic Multiplexer. These cable assemblies are available with either HFBR-4000 connectors (OPT 001) or SMA style connectors (OPT 002).

The HFBR-3000 Simplex cable is constructed of a single graded index glass fiber surrounded by a silicone buffer, secondary jacket, and aramid strength members. The combination is covered with a scuff resistant polyurethane outer jacket.

The HFBR-3100 Duplex cable has two glass fibers each in a cable of construction similar to the simplex cable, joined with a web. The individual channels are identified by a marking on one channel of the cable.

*UL File Number E84364

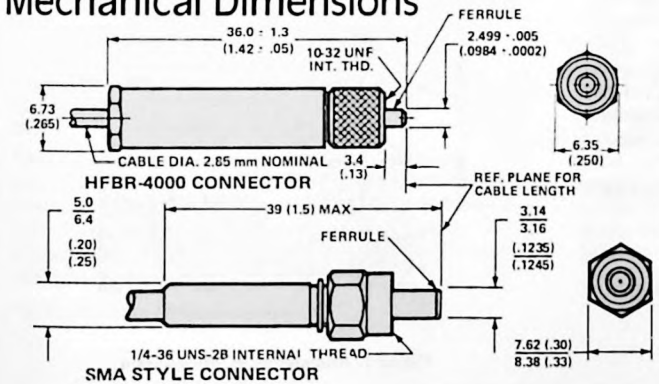
Fiber Optic Cable Construction



The HFBR-3001 is a ten metre Simplex Cable assembly terminated with HFBR-4000 connectors. The HFBR-3021 is a ten metre Simplex Cable assembly terminated with SMA style connectors.

The cable's resistance to mechanical abuse, safety in flammable environments, and absence of electromagnetic interference effects may make the use of conduit unnecessary. However, the light weight and high strength of the cables allows them to be drawn through most electrical conduits. The connectors must be protected during installation by a pulling grip such as Kellems 033-29-003.

Mechanical Dimensions



CABLE LENGTH TOLERANCE

Cable Length (Metres)	Tolerance
1-10	+10/-0 %
11-100	+1/-0 Metre
> 100	+1/-0 %

NOTES:
1. DIMENSIONS ARE IN mm (INCHES).
2. FIBER END IS LOCKED FLUSH WITH FERRULE FACE.

CAUTION:
1. COUPLING NUT SHOULD NOT BE OVERTIGHTENED: TORQUE 0.05 TO 0.1 UNITS N·m OVER TIGHTENING MAY CAUSE EXCESSIVE FIBER MISALIGNMENT OR PERMANENT DAMAGE.
2. GOOD SYSTEM PERFORMANCE REQUIRES CLEAN FERRULE FACES TO AVOID OBSTRUCTING THE OPTICAL PATH. CLEAN COMPRESSED AIR OFTEN IS SUFFICIENT TO REMOVE PARTICLES. A COTTON SWAB SOAKED IN METHANOL OR FREON * MAY ALSO BE USED.

FIBER OPTICS

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Relative Humidity at $T_A = 70°C$			95	%	
Storage Temp.	T_S	-40	+85	°C	
Operating Temp.	T_A	-20	+85		
Bend Radius, No Load	r	20		mm	9, 10
Flexing		50K		Cycles	1

Parameter		Symbol	Min.	Max.	Units	Note
Crush Load		F_C		200	N	2, 8
Impact		m		1.5	kg	3
		h		0.15	m	
Tensile Force	on Cable	F_T		300	N	9, 8
	on Connector/Cable			100		

Mechanical/Optical Characteristics

-20° C to +85° C Unless Otherwise Specified.

Parameter		Symbol	Min.	Typ.[6]	Max.	Units	Conditions	Fig.	Note
Exit Numerical Aperture		N.A.		0.3		—	λ = 820 nm, ≥ 300m		4
Attenuation		α_o		5.5	8	dB/Km	λ = 820 nm	1	7, 12
Bandwidth @ 1 km		BW		40		MHz	λ = 820 nm (LED)		5
Travel Time Constant		I/V		5		ns/m	λ = 820 nm		11
Optical Fiber Core Diameter		D_C		100		μm			
Cladding Outside Diameter		D_{CL}		140					
Index Grading Coefficient		g		2		—			
Cable Structural Strength		F_C		1800		N			8
Mass per Unit Length	Single Channel	m/ℓ		6		kg/km			
	Dual Channel			12					
Cable Leakage Current		I_L		30		nA	50KV, ℓ = 0.3m		

Notes:

1. 180° bending at minimum bend radius, with 10N tensile load.
2. Force applied on 2.5 mm diameter mandrel laid across the cable on a flat surface, for 100 hours, followed by flexure test.
3. Tested at 1 impact according to DOD-STD-1678, Method 2030, Procedure 1.
4. Exit N.A. is defined as the sine of the angle at which the off-axis radiant intensity is 10% of the axial radiant intensity.
5. Bandwidth is measured with a pulsed LED source (λ = 820 nm), and varies as $\ell^{-0.65}$, where ℓ is the length of the fiber (km). Pulse dispersion and bandwidth are approximately inversely related.
6. Typical values are at $T_A = 25°C$.
7. Fixed losses (length independent) are included in Transmitter/Receiver optical specifications.
8. One Newton equals approximately 0.225 pounds force.
9. Short term, ≤ 1 hr.
10. The probability of a fiber weak point occurring at a point of maximum bend is small, consequently the risk of fiber breakage from exceeding the maximum curvature is extremely low.
11. Travel time constant is the reciprocal of the group velocity for propagation of optical power. Group velocity, V = λ/n where λ = velocity of light in space = 3 x 10^8m/s and n = effective core index of refraction.
12. For lower attenuation cable consult local sales office.

Cable Assembly-Ordering Guide

HFBR-3000/HFBR-3100 defines fiber optic cables with factory installed connectors of user specified length. The cable length must be specified in metres and can be any length in one metre increments from 1 to 1000 metres (longer cables available upon request). Option 001 specifies that the cable is terminated with HFBR-4000 connectors and Option 002 specifies that the cable is terminated with SMA style connectors. Either OPT 001 or OPT 002 must be specified.

Examples:

A. To order one Duplex Cable assembly 125 metres long, with SMA style connectors, specify:
   HFBR-3100 Quantity 125
   OPT 002 Quantity 1

B. To order four Simplex Cable assemblies, 150 metres each, with HFBR-4000 connectors, specify:
   HFBR-3000 Quantity 600
   OPT 001 Quantity 4

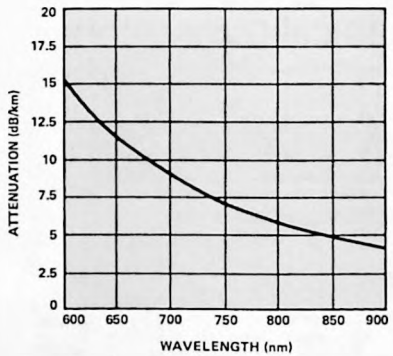


Figure 1. Attenuation vs. Wavelength

HEWLETT PACKARD

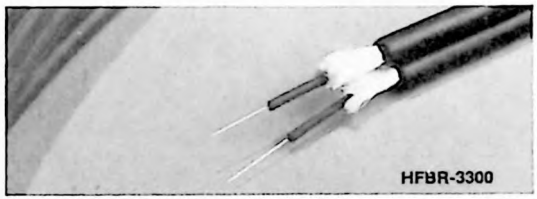
FIBER OPTIC CABLE

HFBR-3200
HFBR-3300

TECHNICAL DATA JANUARY 1984

Features

- SIMPLEX OR DUPLEX CABLE
- USER SPECIFIED CABLE LENGTHS
- UL RECOGNIZED COMPONENT, PASSES UL VW1 FLAME RETARDANCY SPECIFICATION*
- STANDARD 100/140 μm GLASS FIBER
- RUGGED TIGHT JACKET CONSTRUCTION
- PARAMETERS OPTIMIZED FOR LOCAL DATA COMMUNICATION
- BANDWIDTH: 40 MHz AT 1 km



Description

The HFBR-3200 Simplex Fiber Optic Cables and HFBR-3300 Duplex Fiber Optic Cables are intended for use with HP's High Performance Modules (HFBR-1001/2, HFBR-2001) and the Miniature Link series of transmitters and receivers (HFBR-12XX, HFBR-22XX).

The HFBR-3200 Simplex Fiber Optic Cable is constructed of a single graded index glass fiber surrounded by a silicone buffer, secondary jacket, and aramid strength members. The combination is covered with a scuff resistant polyurethane outer jacket.

The HFBR-3300 Duplex Fiber Optic cable has two glass fibers, each in a cable of construction similar to the Simplex cable, joined with a web. The individual channels are identified by a marking on one channel of the cable.

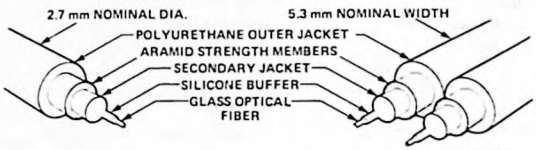
The optical waveguide is a fused silica glass, graded index fiber, which gives low attenuation and wide bandwidth. The silicone buffer and secondary jacket protect the fiber from being scratched and provide a base for the helically wrapped aramid strength members.

The HFBR-3200 and HFBR-3300 cables can be terminated with HFBR-4000 connectors using the HFBR-0100 Connector Assembly Tooling Kit. Information on cables with factory installed connectors is available in the HFBR-3000/HFBR-3100 data sheet.

The cable's resistance to mechanical abuse, safety in flammable environments, and immunity from electromagnetic interference effects may make the use of conduit unnecessary. However, the light weight and high strength of the cables allows them to be drawn through most electrical conduits.

*UL File Number E84364

Fiber Optic Cable Construction



SIMPLEX DUPLEX

CABLE LENGTH TOLERANCE

Cable Length (Metres)	Tolerance
1-10	+10/-0 %
11-100	+1/-0 Metre
> 100	+1/-0 %

Installation

Hewlett-Packard Fiber Optic cable is designed so that when pulled through conduit, accepted wire pulling methods and tools, such as a cable grip, can be used. However, a few precautions for optical cable are necessary: the cable must not be bent tighter than its minimum bend radius; the tensile strength of the cable should not be exceeded (a cable lubricant can be used to minimize the drawing force); tensile load should be applied only to the cable and not the connector.

FIBER OPTICS

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Relative Humidity at $T_A = 70°C$			95	%	
Storage Temp.	T_S	-40	+85	°C	
Operating Temp.	T_A	-20	+85		
Bend Radius, No Load	r	20		mm	8, 9
Flexing		50K		Cycles	1

Parameter	Symbol	Min.	Max.	Units	Note
Crush Load	F_C		200	N	2, 7
Impact	m		1.5	kg	3
	h		0.15	m	
Tensile Force Per Cable Channel	F_T		300	N	7, 8

Mechanical/Optical Characteristics -20° C to +85° C Unless Otherwise Specified.

Parameter		Symbol	Min.	Typ.[6]	Max.	Units	Conditions	Fig.	Note
Exit Numerical Aperture		N.A.		0.3		—	$\lambda = 820$ nm, $\ell \geq 300$m		4
Attenuation		α_o		5.5	8	dB/km	$\lambda = 820$ nm	1	11
Bandwidth @ 1 km		BW		40		MHz	$\lambda = 820$ nm (LED)		5
Travel Time Constant		I/V		5		ns/m	$\lambda = 820$ nm		10
Optical Fiber Core Diameter		D_C		100		μm			
Cladding Outside Diameter		D_{CL}		140					
Index Grading Coefficient		g		2		—			
Cable Structural Strength		F_C		1800		N			7
Mass per Unit Length	Single Channel	m/ℓ		6		kg/km			
	Dual Channel			12					
Cable Leakage Current		I_L		30		nA	50 kV, $\ell = 0.3$m		

Notes:

1. 180° bending at minimum bend radius, with 10N tensile load.
2. Force applied on 2.5 mm diameter mandrel laid across the cable on a flat surface, for 100 hours, followed by flexure test.
3. Tested at 1 impact according to DOD-STD-1678, Method 2030, Procedure 1.
4. Exit N.A. is defined as the sine of the angle at which the off-axis radiant intensity is 10% of the axial radiant intensity.
5. Bandwidth is measured with a pulsed LED source ($\lambda = 820$ nm), and varies as $\ell^{-0.65}$, where ℓ is the length of the fiber (km). Pulse dispersion and bandwidth are approximately inversely related.
6. Typical values are at $T_A = 25°C$.
7. One Newton equals approximately 0.225 pounds force.
8. Short term, ≤ 1 hr.
9. The probability of a fiber weak point occurring at a point of maximum bend is small, consequently the risk of fiber breakage from exceeding the maximum curvature is extremely low.
10. Travel time constant is the reciprocal of the group velocity for propagation of optical power. Group velocity, $V = \lambda/n$ where λ = velocity of light in space = 3×10^8 m/s, n = effective core index of refraction.
11. For lower attenuation cable consult your local sales office.

Cable Ordering Guide

HFBR-3200/HFBR-3300 defines fiber optic cables of user specified length. The cable length must be specified in metres and can be any length in one metre increments from 1 to 1000 metres (longer cables available upon request). Option 001 specifies the number of equal length cables ordered.

Examples:

A. To order one Duplex Cable 150 metres long specify:

HFBR-3300	Quantity 150
OPT 001	Quantity 1

B. To order five Simplex Cables, 100 metres each, specify:

HFBR-3200	Quantity 500
OPT 001	Quantity 5

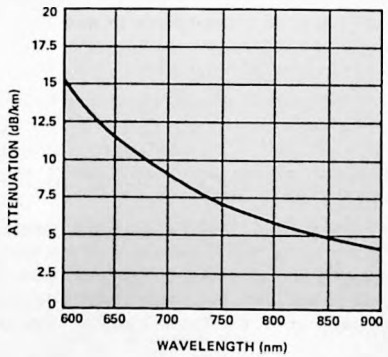


Figure 1. Typical Cable Attenuation vs. Wavelength

HEWLETT PACKARD

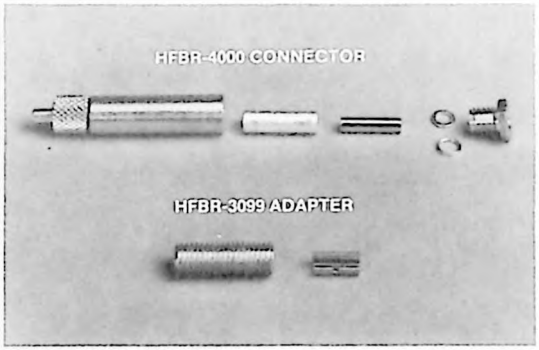
FIBER OPTIC CONNECTOR

HFBR-4000
CONNECTOR
HFBR-3099
ADAPTER

TECHNICAL DATA JANUARY 1984

Features

- **TERMINATES HEWLETT-PACKARD 100/140 μm FIBER OPTIC CABLE**
- **TYPICAL INSERTION LOSS 1.5 dB**
- **ALL METAL PIECE-PARTS**
- **SIMPLE, RAPID ASSEMBLY**
- **STANDARD 2.50 mm FERRULE**
- **WIDE OPERATING TEMPERATURE RANGE**
- **SMALL DIAMETER**



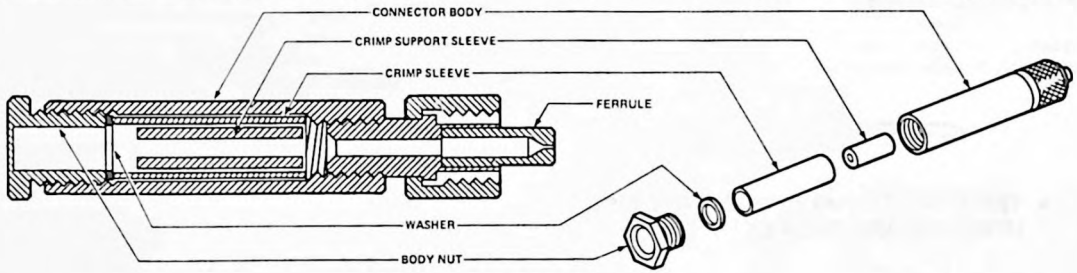
Description

The HFBR-4000 Fiber Optic Connector is constructed of all metal piece-parts and has been designed to use a high performance epoxy to stake the optical fiber. The standard, 2.50 mm connector ferrule is prepared with a polished optical surface giving the assembly a uniformly repeatable low insertion-loss of typically 1.5 dB.

The connector can be assembled in less than 20 minutes by an experienced user with suitable tooling, such as provided in the Hewlett-Packard HFBR-0100 Connector Assembly Tooling Kit. When properly assembled, the connector has excellent strength and repeatable performance over a wide temperature range.

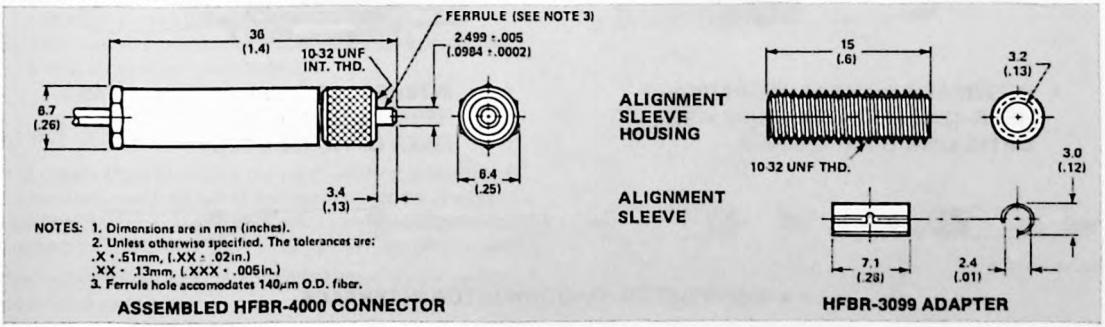
The connector is compatible with Hewlett-Packard HFBR-3200/3300 Fiber Optic Cables.

The HFBR-3099 adapter is used for making an aligned, easily disassembled, connector-to-connector junction.



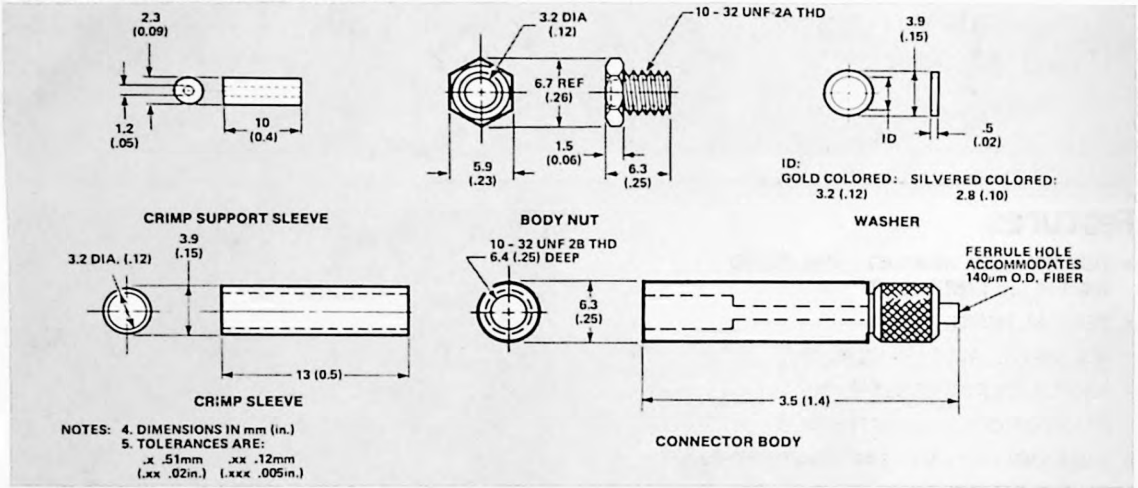
CONNECTOR ASSEMBLY

Mechanical Details



FIBER OPTICS

Connector Piece-Parts



Absolute Maximum Ratings

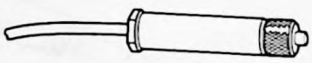
Parameter	Symbol	Min.	Max.	Units	Note
Storage Temp.	T_S	-40	+85	°C	7
Operating Temp.	T_A	-20	+70	°C	7
Tensile Force	F_T		100	N	7

6. αcc, connector-to-connector loss; measured steady state.
7. When assembled with Hewlett-Packard HFBR-0100 procedure and HFBR-3000 series glass fiber cable.
8. 100 connection cycles.

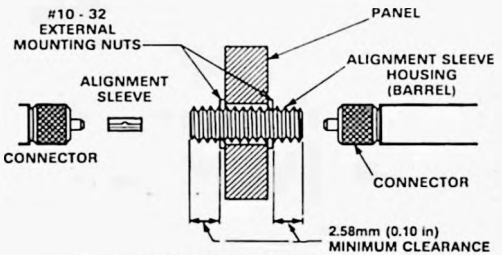
Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Note
Insertion Loss	αcc		1.5		dB	6,7
Insertion Loss Repeatability	Δαcc		0.2		dB	8

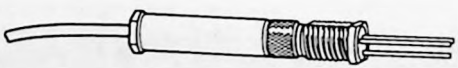
Applications



- **TERMINATION FOR HEWLETT-PACKARD HFBR-3200/3300 FIBER OPTIC CABLE**

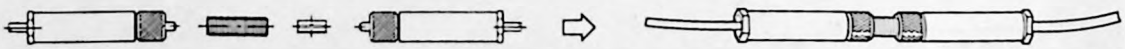


- **BULKHEAD OR PANEL MOUNTING OF HFBR-4000 CONNECTORS**



- **INTERFACE TO HEWLETT-PACKARD HFBR-12XX/22XX MINIATURE FIBER OPTIC LINK COMPONENTS**

- **INTERFACE TO HEWLETT-PACKARD HFBR-1001/1002/2001 FIBER OPTIC MODULES**



- **CONNECTOR-TO-CONNECTOR INTERFACE**

HEWLETT PACKARD

FIBER OPTIC CONNECTOR ASSEMBLY TOOLING KIT

HFBR-0100 TOOLING KIT

HFBR-0101 CONSUMABLES KIT

HFBR-0102 CUSTOM TOOLS

TECHNICAL DATA JANUARY 1984

Features

- AIDS IN THE ASSEMBLY AND REPAIR OF HEWLETT-PACKARD 100/140 μm FIBER OPTIC CABLE WITH HEWLETT-PACKARD CONNECTORS
- INCLUDES AN ILLUSTRATED, STEP-BY-STEP TUTORIAL USER'S MANUAL
- PRODUCES FACTORY-QUALITY CONNECTIONS; 1.5 dB Typical Insertion Loss
- COMPLETE — INCLUDES ALL TOOLS, MATERIALS AND CONNECTOR PARTS REQUIRED TO ASSEMBLE 10 CONNECTORS
- RAPID, LESS THAN 20 MINUTE CONNECTOR ASSEMBLY TIME WITH EXPERIENCE
- PACKAGED IN A RUGGED CASE

Description

The HFBR-0100 Fiber Optic Connector Assembly Tooling Kit is a complete kit designed for quick field installation of Hewlett-Packard HFBR-4000 connectors onto Hewlett-Packard HFBR-3200/3000 Fiber Optic Cable. The kit is packaged in a rugged case, supplying the user with everything required for terminating the fiber optic cable. The contents are:

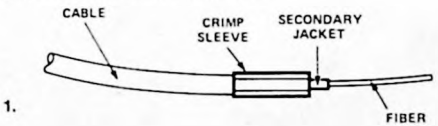
1. A set of common connectoring tools
2. A consumables kit containing sufficient material to assemble ten fiber optic connectors (available separately as HFBR-0101).
3. A set of custom tools (available separately as HFBR-0102).
4. A set of connector piece-parts for terminating ten connector ends, and adapters for making connector-to-connector junctions (the individual unassembled connectors are available as HFBR-4000; the adapter is available as HFBR-3099).
5. An illustrated user's manual presenting the procedure in a step by step, tutorial fashion.

User's Manual Outline

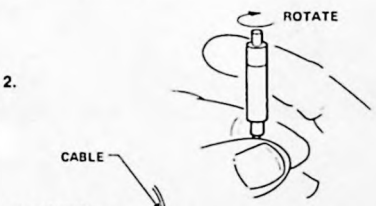
The User's Manual details the connectoring procedure for the first time user, allowing an inexperienced technician to construct factory-quality fiber optic connectors. Numerous photographs and diagrams simplify the assembly process.

The User's Manual is composed of three major sections, described as follows:

1. CABLE PREPARATION: The fiber optic cable is stripped of its jackets, and the strength members are terminated by the installation of crimp hardware.
2. CONNECTOR ASSEMBLY: The prepared cable end is assembled into the connector body using a high performance epoxy to stake the optical fiber. The epoxy is cured in ten minutes using the supplied heater.
3. CONNECTOR POLISHING: The fiber end is ground to an optically flat finish and inspected with a microscope comparing the finish with the detailed photomicrographs in the User's Manual.



1.



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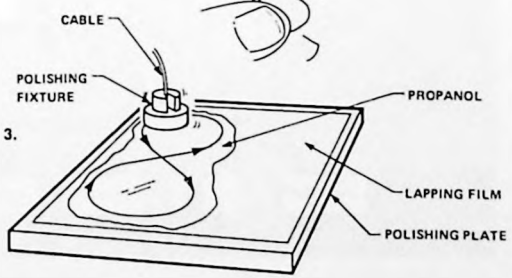


3.

FIBER OPTICS

HFBR-0100 Materials List

1. COMMON CONNECTORING TOOLS WITH CASE
   - Diagonal Cutters
   - No-Nik™ Strippers
   - Scissors
   - 50X Microscope
   - Safety Glasses
   - 16 AWG Wire Strippers
   - Crimping Tool
   - Polishing Plate
   - Heater:
     (option 001) 100-120 VAC 50/60 Hz
     (option 2XX) 200-240 VAC 50/60 Hz
2. TEN HFBR-4000 CONNECTORS WITH SIX HFBR-3099 ADAPTERS
3. HFBR-0101 CONSUMABLES KIT
   - Hysol™ 1C Epoxy
   - Propanol/Acetone swabs
   - Loctite™ 495 Adhesive
   - Stirring Sticks
   - Syringes with Flat-tipped Needles
   - Hand Towels
   - Propanol
   - Lapping Film:
     — Coarse grit, 12 micron
     — Medium grit, 3 micron
     — Fine grit, 0.5 micron
   - Bottle Spout
   - Mixing Pads
4. HFBR-0102 CUSTOM TOOLS
   - Slotted Vise
   - Polishing Weight
   - Polishing Assembly
5. USER'S MANUAL

Specifications

Parameter		Value	Units
Weight	Net	7.3 (16)	kg (lbs)
	Shipping	8.2 (18)	
Size	Height	356 (14)	mm (in.)
	Width	457 (18)	
	Depth	229 (9)	
Heater Wattage	Opt 001	600	W
	Opt 2XX	80	

Ordering Guide

The HFBR-0100 Connector Assembly Tooling Kit is designed to be sold as a complete unit, ready for use. Common connectoring tools, consumables, custom tools, connector piece-parts, and the user's manual are included.

The kit is ordered by specifying both the base product number (HFBR-0100) and a heater option. The heater option specifies either a 110 VAC (option 001) or a 220 VAC (option 2XX) heater with the appropriate power cord.

Both the Consumables Kit (HFBR-0101) and the Custom Tools (HFBR-0102) are available separately for restocking the kit. The unassembled connectors (HFBR-4000), adapters (HFBR-3099) and fiber optic cable (HFBR-3200/3300) are also available.

Order Examples:

1. Three Connector Assembly Tooling Kits — specify;
   HFBR-0100 Fiber Optic Connector Assembly Tooling Kit — Quantity 3
   Option 202: European Continent Plug, 220 VAC
2. One Consumables Kit replacement — specify;
   HFBR-0101 Consumables Kit — Quantity 1

POWER CORD (MALE PLUG) OPTIONS

OPTION NO.	PLUG* CONFIGURATION	COUNTRY
001		USA, CANADA (120V) JAPAN
200		U.K.
201		AUSTRALIA, NEW ZEALAND
202		EUROPEAN CONTINENT
206		SWITZERLAND
212		DENMARK

*VIEW OF PLUG FACE

E – EARTH OR SAFETY GROUND
N – NEUTRAL OR IDENTIFIED CONDUCTOR
L – LINE OR ACTIVE CONDUCTOR

HEWLETT PACKARD

RS-232-C/ V.24 TO FIBER OPTIC MULTIPLEXER

39301A

TECHNICAL DATA JANUARY 1984

Features

- EXTEND UP TO 16 RS-232-C/V.24 CHANNELS TO 1.25 km STANDARD, 2.5 km WITH SELECTED CABLE
- DATA UP TO 19.2 kbps ON EACH OF 16 CHANNELS SIMULTANEOUSLY
- SYSTEM IMMUNITY TO EMI SOURCES SUCH AS LIGHTNING STRIKES
- SECURE DATA TRANSMISSION
- ELIMINATION OF SPARK HAZARDS IN VOLATILE ATMOSPHERES
- BUILT-IN FAULT ISOLATION CAPABILITY
- LOW INSTALLATION COSTS DUE TO LIGHTWEIGHT FIBER OPTIC CABLE

Description

A pair of HP 39301A Multiplexers interconnected with Hewlett-Packard HFBR-3000 Series Fiber Optic Cable, may be used to extend up to 16 full duplex RS-232-C/V.24 channels up to 2.5 km (8200 ft.). Figure 1 shows a typical link configuration between a host CPU and a cluster of 16 terminal devices.

This link provides an easy way to incorporate the advantages of fiber optic links into local area terminal communications. These advantages include immunity to electromagnetic interference of all types, from lightning strikes to noisy electric motors, and freedom from static discharge and crosstalk. The fiber optic cable also provides security for data as it will not radiate electromagnetic signals. In volatile atmospheres, there is no need for special cable

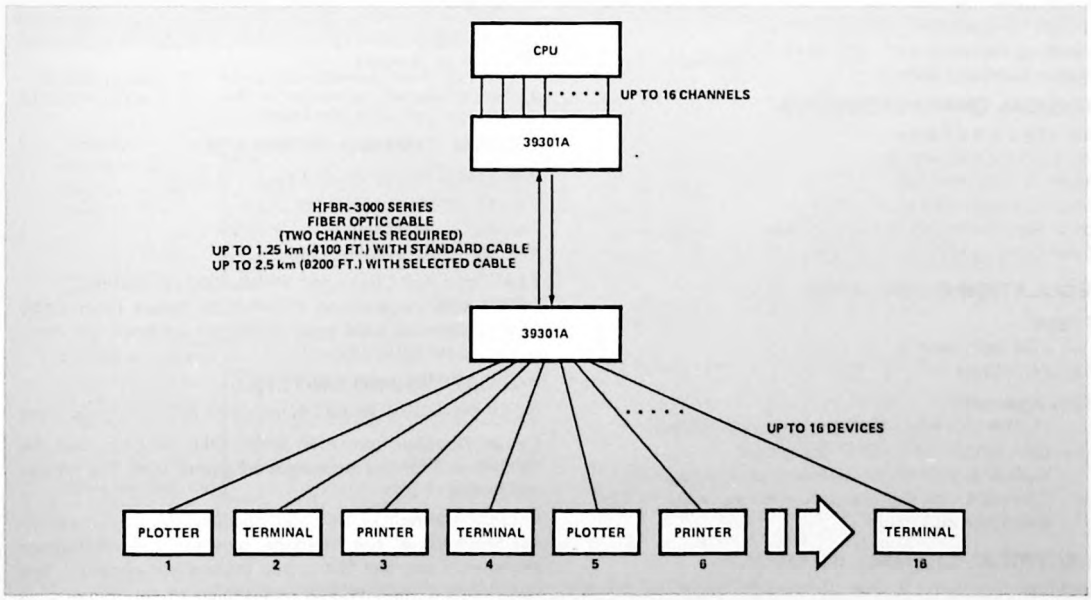


Figure 1. Typical Link Configuration

shielding because no sparks can be generated by this totally dielectric medium.

Each 39301A Multiplexer has eight RS-232-C/V.24 connectors. Each connector has both the Primary and Secondary Data channels available. This provides for a variety of possible configurations. These configurations include: sixteen independent asynchronous channels, eight independent asynchronous channels with handshake control lines, or eight independent synchronous channels with Data Terminal Equipment (DTE) supplied clock signals. The cables required to accomplish any combination of these connections are described in the Typical Configurations Section of this Data Sheet.

Each of the Primary and Secondary Data channels may operate any asynchronous protocol up to 19200 bps. Each channel may be used independently with different protocols and data rates without adjustments to the Multiplexer. This is possible because the 39301A operates as a time division multiplexer, sampling each of the 16 data channels at a 200 kHz rate. This sampled data is serialized and transmitted in real time at a rate of 7 Mbaud over the interconnecting HFBR-3000 Series Fiber Optic Cable to the companion 39301A. This serial data is then reconverted to 16 parallel channels and distributed to the respective Primary or Secondary Data channels.

Specifications

SYSTEM PERFORMANCE

A system consists of two or more 39301A's interconnected by fiber optic cable assemblies.

Transmission Distance: The usable distance between 39301A's is determined by the optical fiber and connectors used.

Typical Fiber Specifications Size, α_o, N.A.	Connector Mfr./Model	Distance Max.	Distance Typ.
Local Communication Fiber 100/140 μm, 5.5 dB/km, 0.28	HP/HFBR-4000 Amphenol/ 906-120-5000	1.25 km Note 1, 2	2.5 km
Telecommunication Fiber 50/125 μm, 4 dB/km, 0.21	Amphenol/ 906-120-5001	Note 2	1.5 km

NOTES:
1. Guaranteed with HFBR-3000 Series cable assemblies.
2. Contact HP Sales Office for expected performance of specific fiber and connectors used.

System Bit Error Rate: One error in 10^9 bits typical.

ENVIRONMENTAL

Storage Temperature: -40°C to +75°C
Operating Temperature: 0°C to +55°C
Relative Humidity: 95%

PHYSICAL CHARACTERISTICS

Size: 42.5 x 8.9 x 7.2 cm
(16.75 x 3.5 x 2.85 inches)
Weight: 2.2 kg (4.75 lbs)
Shipping Weight: 3.4 kg (7.5 lbs)
Power Requirements: 18 VA Maximum
Power Cord Length: 2.3 m (7.5 ft.)

REGULATION COMPLIANCE

RFI/EMI:
- — VDE 0871 level A
- — FCC Class A

Safety Approvals:
- — UL478, UL114 for EDP and office equipment
- — CSA C22.2-154 for EDP equipment
- — VDE 0730 part 2P for EDP and office equipment
- — Complies with IEC standard #380 and #435 for EDP and office equipment

ELECTRICAL CHANNEL INTERFACE

Electrical: Conforms to EIA standard RS-232-C Section 2 (CCITT V.24) for the assigned pins.

Pulse Width Distortion: +/- 6 μs maximum at data rates to 19.2 kbps
(Operated with RS-232-C load of 3K ohms and 2500 pF).

Electrical Connector: Female 25 pin subminiature "D"

PIN ASSIGNMENTS

Pin No.	EIA RS-232-C		CCITT V.24		Notes
1	Protective Ground	AA	Earth Common	101	1
2	Transmitted Data (Primary)	BA	Transmitted Data	103	3
3	Received Data (Primary)	BB	Received Data	104	4
6	Data Set Ready	CC	Data Set Ready	107	2
7	Signal Ground	AB	Signal Ground	102	1
14	Secondary Transmitted Data	SBA	Transmitted Backward Channel Data	118	3
16	Secondary Received Data	SBB	Received Backward Channel Data	119	4

Notes:
1. Pins 1 and 7 are internally connected.
2. Pin 6 is internally hardwired "on" to +12V through a 316 ohm resistor.
3. Data to 39301A.
4. Data from 39301A.

OPTICAL CHANNEL INTERFACE

Transmitter Optical Output Flux: −13 dBm
(50 μW) minimum at 820 nm

Receiver Optical Input Flux: -31 dBm
(0.8 μW) minimum at 820 nm

Fiber Optic Port Connector: HFBR-4000 compatible.
(HFBR-4000 installed on HFBR-3000 Series Fiber Optic Cables. Optional SMA style connector adapters are available from HP sales offices.)

INDICATORS AND SWITCHES

AC Line Indicator: When ON indicates that AC power is on.

Carrier Received Indicator: When ON, indicates that the 39301A is receiving a modulated signal from the remote transmitter.

Loopback Switch: In the TEST position, enables an electrical loopback at the interface between the multiplexer electronics and the fiber optic transceiver circuitry. The "Carrier Received Indicator" is disabled when this switch is in the TEST position.

DTE Interface Configurations

Each RS-232-C/V.24 connector on the 39301A Multiplexer can be interfaced to a variety of Data Terminal Equipment (DTE) by use of properly configured interconnecting RS-232-C/V.24 data cables. Each connector provides two independent full duplex asynchronous channels on the Primary and Secondary Data lines. Therefore, 16 total channels are available on any 39301A link. The following figures will describe the cable configurations for four typical DTE connections. Only one end of the full 39301A link is shown in each figure. The opposite end will be a mirror image in all cases, therefore, two of the illustrated RS-232-C/V.24 data cables will be required to complete each link. Shielded RS-232-C/V.24 cables are recommended in all cases to minimize radio frequency emissions. Any of the DTE configurations described may be intermixed and connected to a 39301A link simultaneously with the only limitation being that no more than 16 full duplex channels are available.

ASYNCHRONOUS DATA ONLY DTE

It is possible to connect one or two "Data Only" DTEs to each connector on the 39301A. Figure 2 shows the configuration for a single DTE connection utilizing the Primary Transmitted/Received Data pins on the 39301A connector. Figure 3 shows the configuration of HP's 8120-3569 Dual Channel RS-232-C/V.24 Adapter Cable. This 8120-3569 Cable can be used to separately access both the Primary and Secondary Data channels on each 39301A connector. Then two of the cables shown in Figure 2 can be used to extend these channels out to two separate "data only" DTEs. This 8120-3569 Cable will enable up to 16 "data only" DTEs to be connected to each 39301A link.

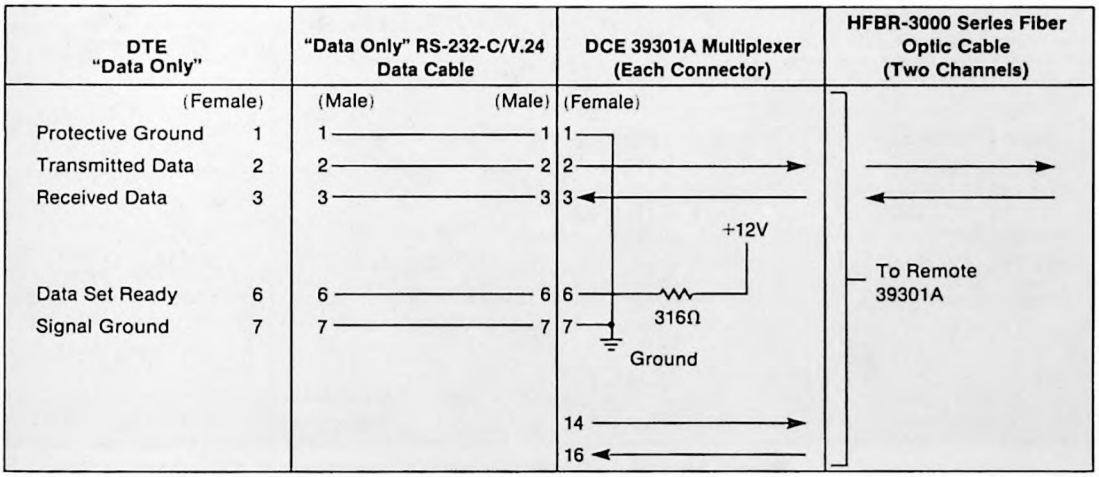


Figure 2. Asynchronous Data Only Configuration

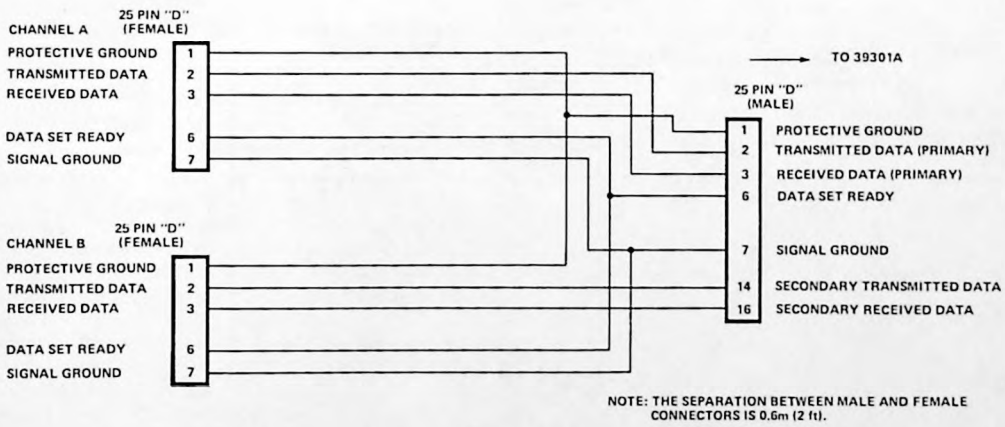


Figure 3. 8120-3569: Dual Channel RS-232-C/V.24 Adapter Cable

ASYNCHRONOUS DATA PLUS HANDSHAKE DTE

If a DTE requires that normal modem handshake lines be active for control purposes, the Secondary Data channel on each 39301A connector can be used to establish this connection between the host CPU and the remote terminal. Figure 4 shows one possible cable configuration using the Secondary Data channel to interconnect the DTE's Request to Send/Clear to Send handshake lines. Up to eight DTEs with handshake lines may be connected to a 39301A link in this way.

Note that pin 6, Data Set Ready, on each 39301A connector is hardwired "on" to +12V through a 316 ohm resistor. If the connected DTE does not require this signal, it may be eliminated from the RS-232-C/V.24 data cable.

SYNCHRONOUS DATA WITH DTE SUPPLIED CLOCK

Although the 39301A does not provide a clock for synchronous data transmission, synchronous DTE may be interconnected by the 39301A link if the DTE can supply the necessary clock signal. Figure 5 illustrates the use of a 39301A connector's Secondary Data channel to accomplish this type of DTE connection. Up to eight synchronous data DTEs with their own clock lines may be connected to a 39301A link.

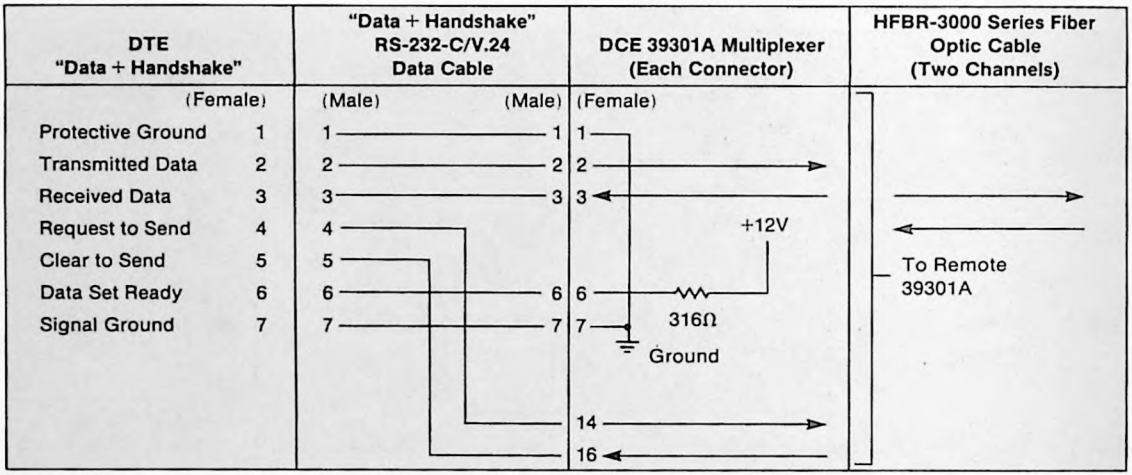


Figure 4. Asynchronous Data Plus Handshake Configuration

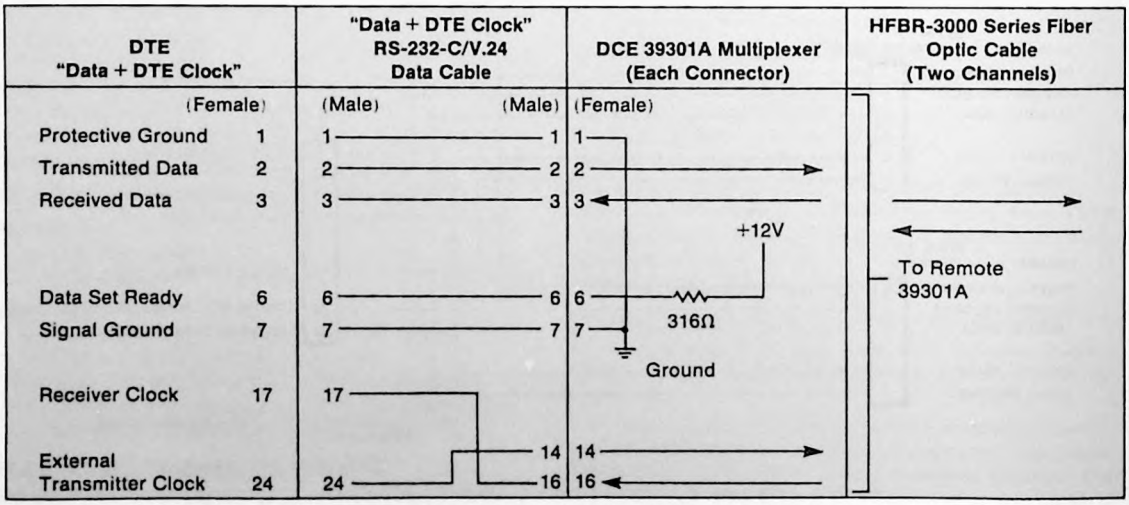


Figure 5. Synchronous Data with DTE Supplied Clock Configuration.

System Configurations

Point-to-Point: See Figure 1
The 39301A's can be configured in a normal point-to-point fashion utilizing a two channel fiber optic cable assembly to interconnect them.

Multiple Node Loop:
Several 39301A's can be interconnected in a simple closed loop configuration using single channel fiber optic cable assemblies to interconnect the transmitter of each 39301A to the receiver of the subsequent 39301A. This configuration allows one multiplexer at the computer center to address several different groups of terminals at different locations in a local facility. A maximum of 16 asynchronous "Data Only" DTE connections can be made around the loop. The unused channels at each multiplexer must be externally looped back on the 25 pin connectors, (i.e., tie pins 2 to 3 and 14 to 16). The maximum data rate of any channel in the loop is determined by the number of multiplexers in the loop and the amount of distortion that the interconnected DTE's can tolerate.

Number of 39301A's	Maximum Channel Data Rate
Up to 3	19.2 Kbps
Up to 6	9.6 Kbps
Up to 15	4.8 Kbps

This data rate limit is due to the accumulated distortion thru the loop. The accumulated distortion will be within the 25% limits of EIA Standard RS-404, Standard for Start-Stop Signal Quality Between Data Terminal Equipment and Non-Synchronous Data Communications Equipment.

Installation

The 39301A Multiplexer and the interconnecting HFBR-3000 Series Fiber Optic Cable is designed for easy installation. Complete details are provided in the Installation, Operating, and Service Manual supplied with each 39301A.

It is recommended that the 39301A Multiplexer be securely mounted to protect the attached data cables. The 39301A is designed for surface or EIA standard 19 inch width rack mounting. Standard Rack/Surface Mounting Hardware supplied with each 39301A allows installation in a standard open rack or flush mounting on any convenient flat surface. Optional Recessed Rack Mounting Hardware (Option 001) allows mounting inside standard racks with closed doors without damage to the attached cables.

The HFBR-3000 Series Fiber Optic Cable required to interconnect the 39301A Multiplexers is available in several configurations. These configurations are detailed in the Support Products Section of this Data Sheet. Two channels of this cable are required to operate the link. This cable is suitable for installation in cable trays, conduits and ducts. The cable will operate in environments from -20°C to +70°C and 95% Relative Humidity. Standard cable installation techniques and equipment may be used with the minor precautions stated in the 39301A Installation, Operating, and Service Manual. The precautions include maintaining the minimum bend radius of 25mm (1 in.) and maximum tensile load of 300N (67 lb) per channel during installation.

If junction box or bulkhead splices are required in a cable run, or a link is reconfigured to a longer distance requiring additional fiber optic cable to be added to the original installation, HFBR-3099 Cable Coupling Hardware may be used to splice these cables together. The HFBR-3099 is supplied with each factory connectored HFBR-3000 Series Cable or may be ordered separately. Each in-line HFBR-3099 Coupler produces a 2 dB optical power loss in the cable run. This loss will affect the maximum separation between 39301A's by the distance equal to 2 dB ÷ cable attenuation in dB/km. For example, if standard HFBR-3000 series cable is used the maximum link length will be reduced by 2 dB ÷ 8 dB/km = 250 m for each intermediate HFBR-3099 used.

The RS-232-C/V.24 data cables required for connection to various Data Terminal Equipment are detailed in the Typical Configurations Section of this Data Sheet. It is recommended that shielded cables are used for these connections for maximum suppression of radio frequency emissions. These cables should be no longer than 15m (50 ft.) for compliance with the EIA and CCITT Standards, unless low capacitance cable is used.

Service

The 39301A is designed with easy-to-use link fault isolation facilities. Loopback techniques utilizing the built-in loopback switch and fiber optic loopback cable supplied with each 39301A Multiplexer are used to quickly isolate link failures to either 39301A Multiplexer, the HFBR-3000 Series Fiber Optic Cable, or the interconnected Data Terminal Equipment. These procedures are described in the Installation, Operating, and Service Manual supplied with each 39301A. 39301A Multiplexers or HFBR-3000 Series Fiber Optic Cables may be self-serviced by the customer or returned to the nearest Hewlett-Packard Sales Office for service.

Customer self-service may be accomplished for the Multiplexer by following the procedures outlined in the Installation, Operating and Service Manual to identify the failed subassembly. Replacement subassemblies are available through HP Sales Offices. HFBR-3000 Series Fiber Optic Cables may be repaired by using the HP HFBR-0100 Connector Assembly Tool kit to splice or reconnector a damaged cable.

Hewlett-Packard service is available for the 39301A by returning the Multiplexer to the nearest HP Sales Office. This service is available either on Monthly Contract basis or for a Time and Materials charge. The HFBR-3000 Series Cable will be repaired on a Time and Materials basis upon return to the nearest HP Sales Office.

Support Products for the 39301A

39301A MOUNTING HARDWARE

Rack/Surface Mounting Hardware:
Supplied standard with each 39301A. Available separately as part 1600-1090.

Recessed Rack Mounting Hardware:
Supplied as Option 001 to the 39301A. Available separately as part 1600-1092.

39301A FIBER OPTIC LOOPBACK CABLE

Supplied standard with each 39301A. Available separately as part 5061-2694.

39301A INSTALLATION, OPERATING, AND SERVICE MANUAL

Supplied standard with each 39301A. Extra copies available as part 39301-90001.

8120-3569 DUAL CHANNEL RS-232-C/V.24 ADAPTER CABLE

Enables two Data Terminal Equipment devices to be connected to each 39301A RS-232-C/V.24 connector port. A wiring diagram is shown in Figure 3 of this Data Sheet. The length is 0.6m (2 ft.)

HFBR-3000* SERIES FIBER OPTIC CABLE

	Single Channel (Two Req.)	OR	Dual Channel (One Req.)
With Factory Installed HFBR-4000 Fiber Optic Connectors	HFBR-3000* or 39200A*		HFBR-3100* or 39200B*
Without Factory Installed Connectors	HFBR-3200*		HFBR-3300*

Two channels of HFBR-3000 Series Fiber Optic Cable are required to interconnect the HP 39301A Multiplexers. This cable is available in several forms as shown in the table above. It may be ordered in any length in one metre increments up to 1000 metres (3280 ft.)

*Detailed specifications for these products are available from HP sales offices.

HFBR-0100* CONNECTOR ASSEMBLY TOOLING KIT

This kit allows the installation of HFBR-4000 Fiber Optic Connectors onto HFBR-3000 Series Fiber Optic Cables in the field. It is used for system installation purposes if HFBR-3200/3300 unconnectored cables are used. It may also be used for field repair of HFBR-3000 Series Fiber Optic Cables.

HFBR-4000* FIBER OPTIC CONNECTORS

These connectors are compatible with the HFBR-3000 Series Fiber Optic Cable and the fiber optic ports on the 39301A.

HFBR-3099* FIBER OPTIC CABLE COUPLING HARDWARE

This hardware enables two cables with HFBR-4000 connectors to be coupled together for link extension or repair splices. See Installation Section of this Data Sheet for limitations on use of the HFBR-3099.

Ordering Information

HP 39301A: RS-232-C/V.24 TO FIBER OPTIC MULTIPLEXER

Two are required per link. Each 39301A is supplied with standard Rack/Surface Mounting Hardware, a Fiber Optic Loopback Cable and an Installation, Operating, and Service Manual.

Option 001: Recessed Rack Mounting Hardware

Required Power Supply Option: One required per 39301A

Option 210: 100V 50/60Hz Operation
Option 212: 120V 50/60Hz Operation
Option 222: 220V 50/60Hz Operation
Option 224: 240V 50/60Hz Operation

8120-3569: DUAL CHANNEL RS-232-C/V.24 ADAPTER CABLE

This cable may be used to separately access both Primary and Secondary Data channels on each 39301A connector. Eight of these cables will enable up to 16 "data only" DTE to be connected to each 39301A.

HFBR-3000 SERIES FIBER OPTIC INTERCONNECTING CABLE

Two channels are required per link.

See Support Products Section of this Data Sheet for product choices.

HEWLETT PACKARD

PIN PHOTODIODES

5082-4200 SERIES

TECHNICAL DATA JANUARY 1984

Features

- HIGH SENSITIVITY (NEP <-108 dBm)
- WIDE DYNAMIC RANGE (1% LINEARITY OVER 100 dB)
- BROAD SPECTRAL RESPONSE
- HIGH SPEED (T_r, T_f, EQUALS 1.5 ns TYP.)
- STABILITY SUITABLE FOR PHOTOMETRY/ RADIOMETRY
- HIGH RELIABILITY
- FLOATING, SHIELDED CONSTRUCTION
- LOW CAPACITANCE
- LOW NOISE
- HERMETIC PACKAGE

Active area: 1mm Diam — 5082-4207 — Tall (TO-18)

0.5mm Diam — 5082-4203, 5082-4204 — Tall (TO-18)

0.5mm Diam — 5082-4220 — Short (TO-46)

0.25mm Magnified 2.5x — 5082-4205 — Subminiature

Description

The HP silicon planar PIN photodiodes are ultra-fast light detectors for visible and near infrared radiation. Their response to blue and violet is unusually good for low dark current silicon photodiodes.

These devices are suitable for applications such as high speed tachometry, optical distance measurement, star tracking, densitometry, radiometry, and fiber-optic termination.

The low dark current of these planar diodes enables detection of very low light levels. The quantum detection efficiency is constant over ten decades of light intensity, providing a wide dynamic range.

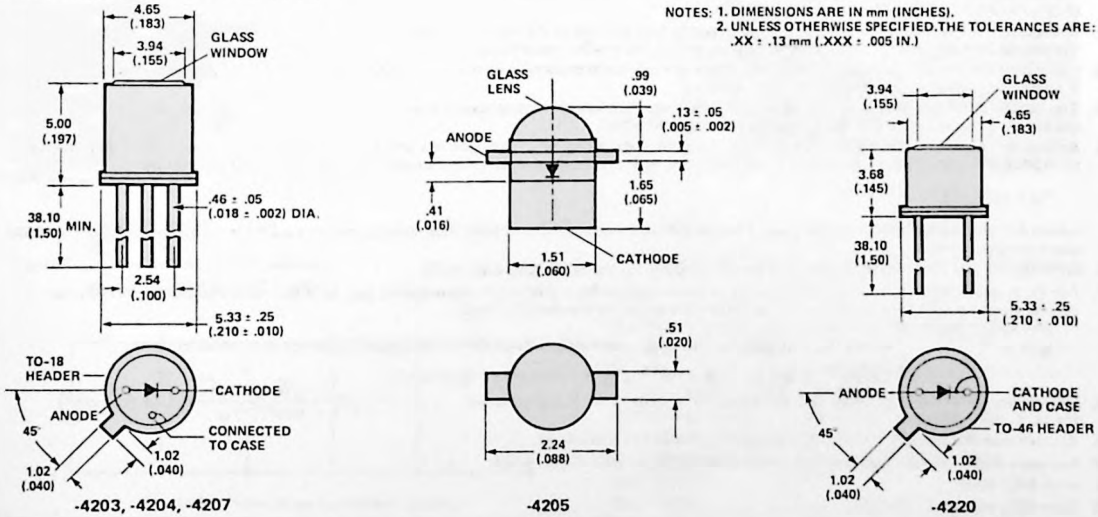
The 5082-4203, -4204, and -4207 are packaged on a standard TO-18 header with a flat glass window cap. For versatility of circuit connection, they are electrically insulated from the header. The light sensitive area of the 5082-4203 and -4204 is 0.508mm (0.020 inch) in diameter and is located 1.905mm (0.075 inch) behind the window. The light sensitive area of the 5082-4207 is 1.016mm (0.040 inch) in diameter and is also located 1.905mm (0.075 inch) behind the window.

The 5082-4205 is in a low capacitance Kovar and ceramic package of very small dimensions, with a hemispherical glass lens.

The 5082-4220 is packaged on a TO-46 header with the 0.508mm(0.020 inch) diameter sensitive area located 2.540mm (0.100 inch) behind a flat glass window.

Package Dimensions

NOTES: 1. DIMENSIONS ARE IN mm (INCHES).
2. UNLESS OTHERWISE SPECIFIED.THE TOLERANCES ARE: .XX ± .13 mm (.XXX ± .005 IN.)



FIBER OPTICS

Absolute Maximum Ratings Operating and Storage Temperature -55° to 125°C

Parameter	-4203	-4204	-4205	-4207	-4220	Units
P_{MAX} Power Dissipation [1]	100	100	50	100	100	mW
Steady Reverse Voltage[3]	50	20	50	20	50	volts

Electrical/Optical Characteristics at T_A=25°C

Symbol	Description	-4203			-4204			-4205			-4207			-4220			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
R_E, 0= R_ϕ * A	Axial Incidance Response at 820nm[4]		0.86			0.86			1.1			3.4			.74		$\frac{\mu A}{mW/cm^2}$
A	Active Area[4]		2 x 10^{-3}			2 x 10^{-3}			3 x 10^{-3}*			8 x 10^{-3}			2 x 10^{-3}		cm^2
R_ϕ	Flux Responsivity 820nm[5] (Fig. 1, 3)		0.43			0.43			.37			0.43			.37		$\frac{\mu A}{\mu W}$
I_D	Dark Current[6] (Fig. 4)			2.0			0.6			.15			2.5			5.0	nA
NEP	Noise Equivalent Power [7] (Fig. 8)		5.9 x 10^{-4}			3.2 x 10^{-14}			1.6 x 10^{-14}			6.6 x 10^{-14}			9.3 x 10^{-14}		$\frac{W}{\sqrt{Hz}}$
D*	Detectivity[8]		7.5 x 10^{11}			1.4 x 10^{12}			3.4 x 10^{12}			1.3 x 10^{12}			4.8 x 10^{11}		$\frac{cm\sqrt{Hz}}{W}$
C_j	Junction Capacitance[9] (Fig. 5)		1.5			2.0			0.7			5.5			2.0		pF
C_P	Package Capacitance [10]		2			2						2					pF
t_r, t_f	Zero Bias Speed (Rise, Fall Time) [11]		300			300			300			300			300		ns
t_r, t_f	Rev.-Bias Speed (Rise, Fall Time) [12]		1.5			1.5			1.5			1.5			1.5		ns
R_S	Series Resistance			50			50			50			50			50	Ω
V_{BR}	Breakdown Voltage	50			50			50			50			50			V

*see Note 4.

NOTES:

1. Peak Pulse Power

   When exposing the diode to high level incidance the following photocurrent limits must be observed:

   $$I_{p\ (avg\ MAX.)} < \frac{P_{MAX} - P_\phi}{E_c}$$; and in addition:

   $$I_{p(PEAK)} < \frac{1000\ A}{t\ (\mu sec)}$$ or <500mA or $< \frac{I_{p\ (avg\ MAX.)}}{f \times t}$

   whichever of the above three conditions is least.

   I_p - photocurrent (A) f - pulse repetion rate (MHz)
   E_c - supply voltage (V) P_ϕ - power input via photon flux
   t - pulse duration (μs) P_{MAX} - max dissipation (W)

   Power dissipation limits apply to the sum of both the optical power input to the device and the electrical power input from flow of photocurrent when reverse voltage is applied.
2. Exceeding the Peak Reverse Voltage will cause permanent damage to the diode. Forward current is harmless to the diode, within the power dissipation limit. For optimum performance, the diode should be reversed biased with E_c between 5 and 20 volts.
3. Exceeding the Steady Reverse Voltage may impair the low-noise properties of the photodiodes, an effect which is noticeable only if operation is diode-noise limited (see Figure 8).
4. The 5082-4205 has a lens with approximately 2.5x magnification; the actual junction area is 0.5 x 10^{-3} cm^2, corresponding to a diameter of 0.25mm (.010"). Specification includes lens effect.
5. At any particular wavelength and for the flux in a small spot falling entirely within the active area, responsivity is the ratio of incremental photodiode current to the incremental flux producing it. It is related to quantum efficiency, η_q in electrons per photon by:

   $$R_\phi = \eta_q \left(\frac{\lambda}{1240}\right)$$

   where λ is the wavelength in nanometers. Thus, at 820nm, a responsivity of 0.43 A/W corresponds to a quantum efficiency of 0.65 (or 65%) electrons per photon.
6. At -10V for the 5082-4204, -4205, and -4207; at -25V for the 5082-4203 and -4220.
7. For (λ, f, Δf) = 820nm, 100Hz, 6Hz) where f is the frequency for a spot noise measurement and Δf is the noise bandwidth, NEP is the optical flux required for unity signal/noise ratio normalized for bandwidth. Thus:

   $$NEP = \frac{I_N/\sqrt{\Delta f}}{R_\phi}$$ where $I_N/\sqrt{\Delta f}$ is the bandwidth – normalized noise current computed from the shot noise formula:

   $I_N/\sqrt{\Delta f} = \sqrt{2qI_D} = 17.9 \times 10^{-15} \sqrt{I_D}$ ($A/\sqrt{Hz}$) where I_D is in nA.
8. Detectivity, D*is the active-area-normalized signal to noise ratio. It is computed for (λ, f, Δf) = (820nm, 100Hz, 6Hz).

   $$D^* = \frac{\sqrt{A}}{NEP}\left(\frac{cm\sqrt{Hz}}{W}\right)$$ for A in cm^2,
9. At -10V for 5082-4204, -4205, -4207, -4220; at -25V for 5082-4203.
10. Between diode cathode lead and case – does not apply to 5082-4205, -4220.
11. With 50Ω load.
12. With 50Ω load and -20V bias.

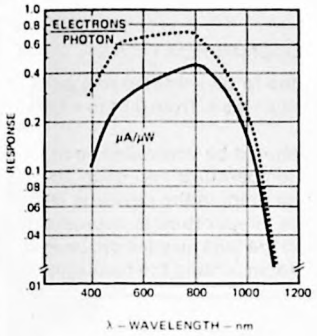


Figure 1. Spectral Response.

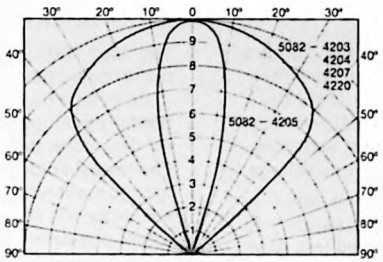


Figure 2. Relative Directional Sensitivity of the PIN Photodiodes.

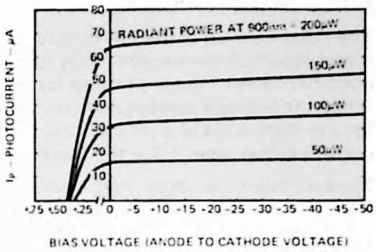


Figure 3. Typical Output Characteristics at λ = 900nm.

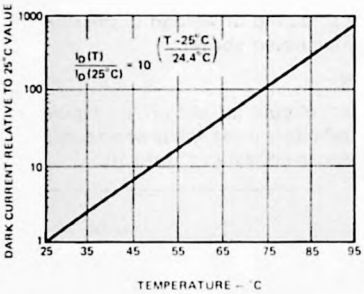


Figure 4. Dark Current at –10V Bias vs. Temperature.

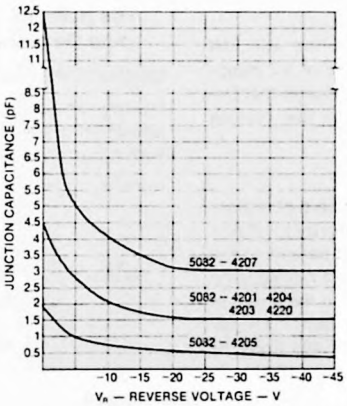


Figure 5. Typical Capacitance Variation With Applied Voltage.

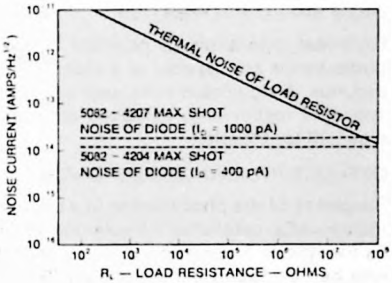


Figure 6. Noise vs. Load Resistance.

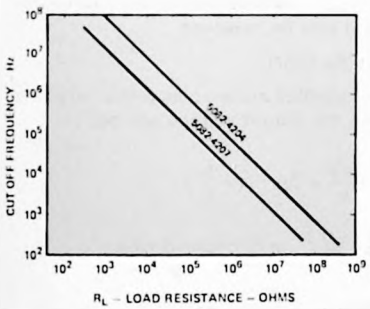


Figure 7. Photodiode Cut-Off Frequency vs. Load Resistance (C = 2pF).

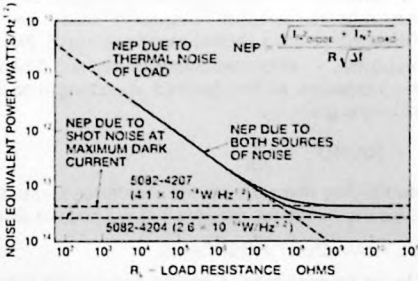


Figure 8. Noise Equivalent Power vs. Load Resistance.

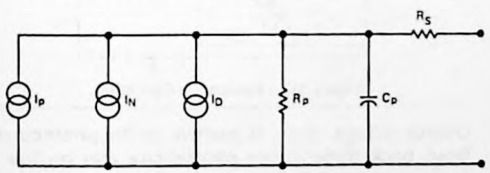


Figure 9. Photodiode Equivalent Circuit.

I_P = Signal current ≈ 0.43 μA/μW x flux input at 820 nm
I_N = Shot noise current
<1.2 x 10–14 amps/Hz1/2(5082-4204)
<4 x 10–14 amps/Hz1/2(5082-4207)
I_D = Dark current
<600 x 10–12 amps at –10 V dc (5082-4204)
<2500 x 10–12 amps at –10 V dc (5082-4207)
R_P = 1011Ω
R_S = <50Ω

FIBER OPTICS

Application Information

NOISE FREE PROPERTIES

The noise current of the PIN diodes is negligible. This is a direct result of the exceptionally low leakage current, in accordance with the shot noise formula $I_N = (2qI_R\Delta f)^{1/2}$. Since the leakage current does not exceed 600 picoamps for the 5082-4204 at a reverse bias of 10 volts, shot noise current is less than 1.4×10^{-14} amp $Hz^{-1/2}$ at this voltage.

Excess noise is also very low, appearing only at frequencies below 10 Hz, and varying approximately as 1/f. When the output of the diode is observed in a load, thermal noise of the load resistance (R_L) is 1.28×10^{-10} $(R_L)^{-1/2} \times (\Delta f)^{1/2}$ at 25°C, and far exceeds the diode shot noise for load resistance less than 100 megohms (see Figure 6). Thus in high frequency operation where low values of load resistance are required for high cut-off frequency, all PIN photodiodes contribute virtually no noise to the system (see Figures 6 and 7).

HIGH SPEED PROPERTIES

Ultra-fast operation is possible because the HP PIN photodiodes are capable of a response time of 1.5 nanoseconds. A significant advantage of this device is that the speed of response is exhibited at relatively low reverse bias (–10 to –20 volts).

OFF-AXIS INCIDANCE RESPONSE

Response of the photodiodes to a uniform field of radiant incidanceE_e, parallel to the polar axis is given by I = (RA) x E_e for 820nm. The response from a field not parallel to the axis can be found by multiplying (RA) by a normalizing factor obtained from the radiation pattern at the angle of operation. For example, the multiplying factor for the 5082-4207 with incidance E_e at an angle of 40° from the polar axis is 0.8. If $E_e = 1mW/cm^2$, then $I_p = k \times (RA) \times E_e$; $I_p = 0.8 \times 4.0 \times 1 = 3.2$ μamps.

SPECTRAL RESPONSE

To obtain the response at a wavelength other than 820nm, the relative spectral response must be considered. Referring to the spectral response curve, Figure 1, obtain response, X, at the wavelength desired. Then the ratio of the response at the desired wavelength to response at 820nm is given by:

$$\text{RATIO} = \frac{X}{.43}$$

Multiplying this ratio by the incidance response at 820nm gives the incidance response at the desired wavelength.

ULTRAVIOLET RESPONSE

Under reverse bias, a region around the outside edge of the nominal active area becomes responsive. The width of this annular region is approximately 25μm (0.001 inch) at –20V, and expands with higher reverse voltage. Responsivity in this edge region is higher than in the interior, particularly at shorter wavelengths; at 400nm the interior, responsivity is 0.1 A/W while edge responsivity is 0.35 A/W. At wavelengths shorter than 400nm, attenuation by the glass window affects response adversely. Speed of response for edge incidance is t_r, $t_f \approx 300$ns.

5082-4205 MOUNTING RECOMMENDATIONS

a. The 5082-4205 is intended to be soldered to a printed circuit board having a thickness of from 0.51 to 1.52mm (0.02 to 0.06 inch).
b. Soldering temperature should be controlled so that at no time does the case temperature approach 280°C. The lowest solder melting point in the device is 280°C (gold-tin eutectic). If this temperature is approached, the solder will soften, and the lens may fall off. Lead-tin solder is recommended for mounting the package, and should be applied with a small soldering iron, for the shortest possible time, to avoid the temperature approaching 280°C.
c. Contact to the lens end should be made by soldering to one or both of the tabs provided. Care should be exercised to prevent solder from coming in contact with the lens.
d. If printed circuit board mounting is not convenient, wire leads may be soldering or welded to the devices using the precautions noted above.

LINEAR OPERATION

Having an equivalent circuit as shown in Figure 9, operation of the photodiode is most linear when operated with a current amplifier as shown in Figure 10.

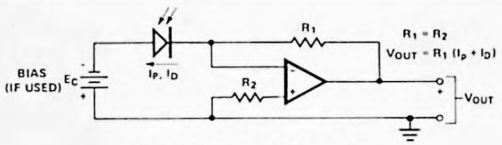


Figure 10. Linear Operation.

Lowest noise is obtained with $E_c = 0$, but higher speed and wider dynamic range are obtained if $5 < E_c < 20$ volts. The amplifier should have as high an input resistance as possible to permit high loop gain. If the photodiode is reversed, bias should also be reversed.

LOGARITHMIC OPERATION

If the photodiode is operated at zero bias with a very high impedance amplifier, the output voltage will be:

$$V_{OUT} = \left(1 + \frac{R_2}{R_1}\right) \cdot \frac{kT}{q} \cdot \ell n \left(1 + \frac{I_P}{I_S}\right)$$

where $I_S = I_F \left(e^{\frac{qV}{kT}} - 1\right)^{-1}$ at $0 < I_F < 0.1$mA

using a circuit as shown in Figure 11.

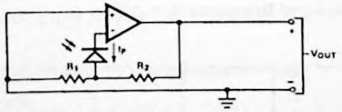
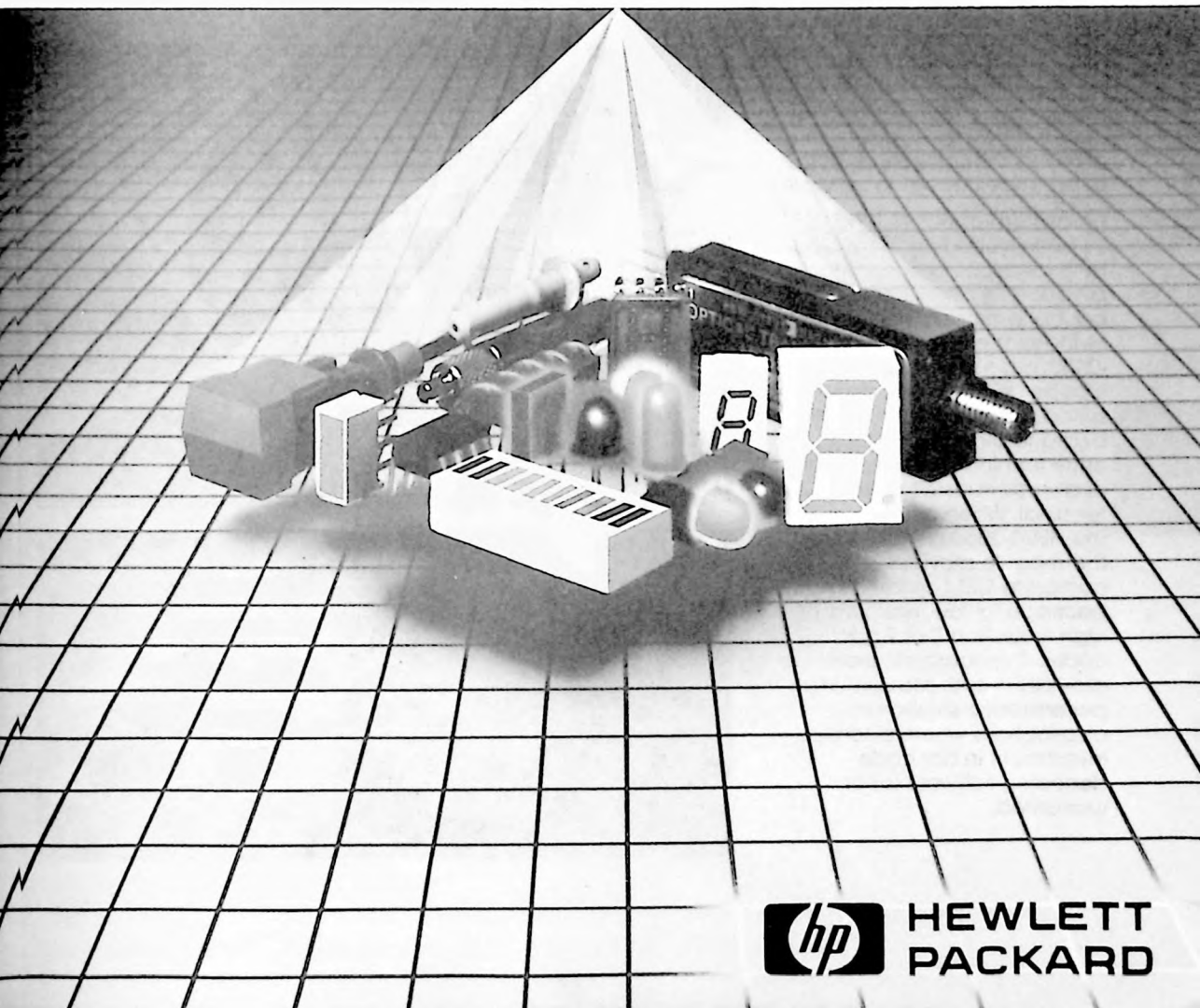


Figure 11. Logarithmic Operation.

Output voltage, V_{OUT}, is positive as the photocurrent, I_P, flows back through the photodiode making the anode positive.

7. Bar Code Products

- Digital Wands
- Decoder
- Readers
- Scanner



HEWLETT PACKARD

Bar Code Products

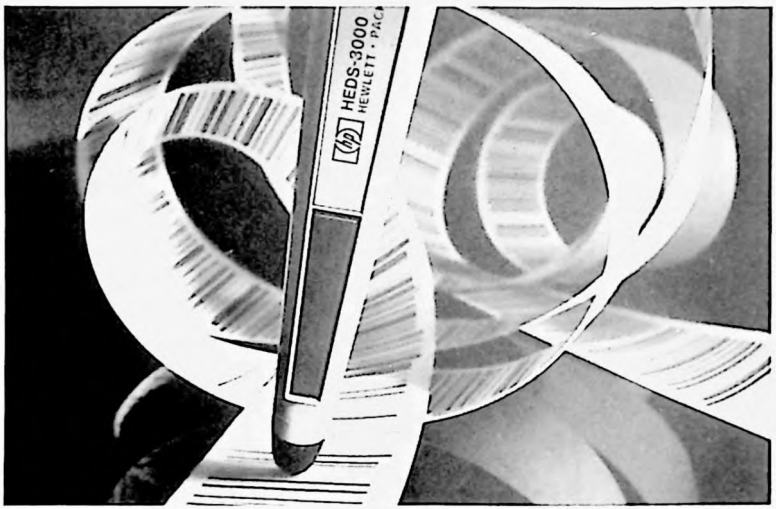
HP has taken years of experience in LED materials technology, bipolar photo IC processing, and precision lens design to develop the HEDS-3000 (medium resolution) and HEDS-3200 (high resolution) digital bar code wand families. HP wands are housed in attractive and rugged plastic cases designed to comfortably fit the human hand. The digital output is compatible with standard TTL and CMOS circuitry, thus providing an easy design interface and eliminating the design time, cost, and space otherwise required for an analog-to-digital interface. The performance of the HP digital wands is fully specified, allowing the software engineer to optimize decoding software.

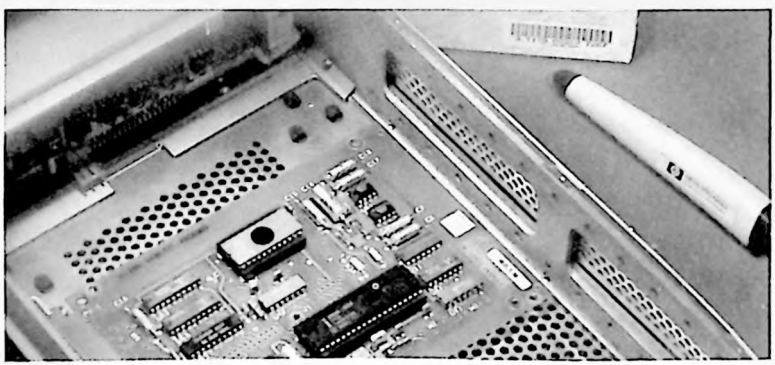
For customers not wishing to invest in decoding technology, HP is developing decoding products as an extension of its bar code product line. The first of these, the HEDS-0100/ -0150, is a fully integrated 3 of 9 code decoder board ideally suited to serve as a slave MPU board to almost any data entry terminal, or as the heart of a small transmit-only terminal. When combined with the HEDS-3050 or HEDS-3250, the module provides a complete OEM data entry package for low, medium, or high resolution 3 of 9 bar codes. This complete package provides a cost effective, high performance solution in applications where extensive investment in bar code decoding software is not warranted.

Two new bar code readers are being introduced this year, the 16800A programmable model and the 16801A non-programmable model. Both can be configured in a variety of ways and provide visual and audio operator feedback. Watch for more exciting products as HP grows as a supplier to the bar code data collection market.

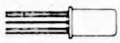
Advantages of Bar Code Data Entry:

- Faster than most other data entry techniques
- Greater accuracy due to built-in error checking and optional checksum characters
- Little operator training required
- Symbols easily produced on a wide variety of printers
- Cost competitive with other technologies

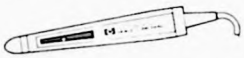
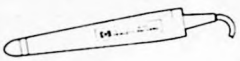
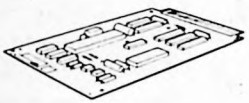




Detector Components

Package Outline Drawing	Part No.	Description	Features	Page No.
	HEDS-1000	High Resolution Optical Reflective Sensor	• Fully Specified and Guaranteed for Assured Performance • Visible Light Source can Detect Most Colors • Photo IC Detector Optimizes Speed and Response • Standard TO-5 Header	7-4

Bar Code Products

Package Outline Drawing	Part No.	Description	Features	Page No.
	HEDS-3000	Medium Resolution Digital Bar Code Wand (with Switch)	• Digital Output • Specified for 0.3 mm (0.012 in.) Narrow Element Width • Push-to-read Switch Available for Low Powered Applications • Internal Shielding Available for Improved Electrical Noise Rejection • Full Line of Options Available	*
	HEDS-3050	Medium Resolution Digital Bar Code Wand (Shielded, Non-Switched)		
	HEDS-3200 HEDS-3201	High Resolution Digital Bar Code Wand (with Switch)	• Digital Output • Specified for 0.19 mm (0.0075 in.) Narrow Element Width • Push-to-read Switch Available for Low Powered Applications • Internal Shielding Available for Improved Electrical Noise Rejection • Full Line of Options Available	*
	HEDS-3250 HEDS-3251	High Resolution Digital Bar Code Wand (Shielded, Non-Switched)		
	HEDS-0100 HEDS-0150	Bar Code Decoder Module	• Standard PC Board Designs • Decodes 3 of 9 Code • RS-232-C; 2400 Baud Standard, 1200, 4800, 9600 Baud Available • Parallel ASCII Interface	*
	16800A	Programmable Bar Code Reader	• Flexible Configuration • Computer Control Capability (16800A) • Wide Bar Code Selection • Choice of High Performance Wands • Meets HP Class B Environmental Specifications	*
	16801A	Non-Programmable Bar Code Reader		

*For more information regarding bar code products, please refer to the 1984 Bar Code Products Catalog. Contact your local Hewlett-Packard Sales Office or authorized distributor for a copy of this new catalog.

HEWLETT PACKARD

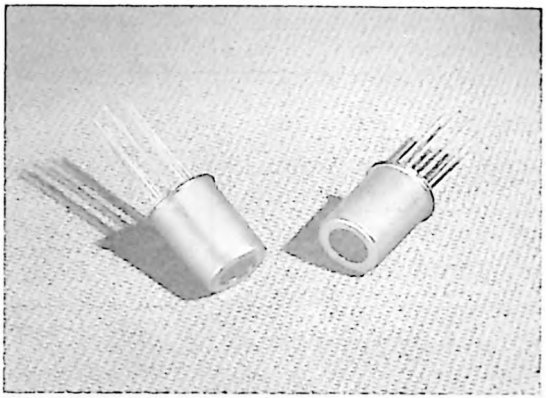
HIGH RESOLUTION OPTICAL REFLECTIVE SENSOR

HEDS-1000

TECHNICAL DATA JANUARY 1984

Features

- FOCUSED EMITTER AND DETECTOR IN A SINGLE PACKAGE
- HIGH RESOLUTION — .190mm SPOT SIZE
- 700nm VISIBLE EMITTER
- LENS FILTERED TO REJECT AMBIENT LIGHT
- TO-5 MINIATURE SEALED PACKAGE
- PHOTODIODE AND TRANSISTOR OUTPUT
- SOLID STATE RELIABILITY



Description

The HEDS-1000 is a fully integrated module designed for optical reflective sensing. The module contains a .178mm (.007 in.) diameter 700nm visible LED emitter and a matched I.C. photodetector. A bifurcated aspheric lens is used to image the active areas of the emitter and the detector to a single spot 4.27mm (0.168 in.) in front of the package. The reflected signal can be sensed directly from the photodiode or through an internal transistor that can be configured as a high gain amplifier.

Applications

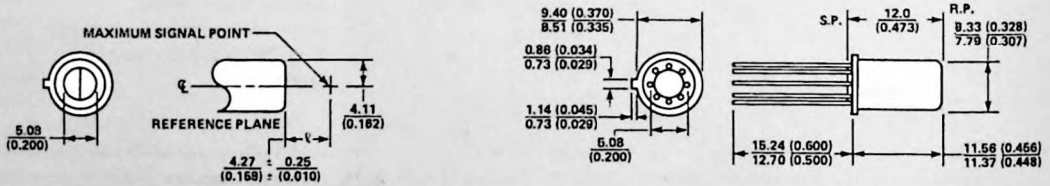
Applications include pattern recognition and verification, object sizing, optical limit switching, tachometry, textile thread counting and defect detection, dimensional monitoring, line locating, mark, and bar code scanning, and paper edge detection.

Mechanical Considerations

The HEDS-1000 is packaged in a high profile 8 pin TO-5 metal can with a glass window. The emitter and photodetector chips are mounted on the header at the base of the package. Positioned above these active elements is a bifurcated aspheric acrylic lens that focuses them to the same point.

The sensor can be rigidly secured by commercially available two piece TO-5 style heat sinks, such as Thermalloy 2205, or Aavid Engineering 3215. These fixtures provide a stable reference platform and their tapped mounting holes allow for ease of affixing this assembly to the circuit board.

Package Dimensions



NOTES:
1. ALL DIMENSIONS IN MILLIMETERS AND (INCHES).
2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
3. THE REFERENCE PLANE IS THE TOP SURFACE OF THE PACKAGE.
4. NICKEL CAN AND GOLD PLATED LEADS.
5. S.P. SEATING PLANE.
6. THE LEAD DIAMETER IS 0.45mm (0.018in.) TYP.

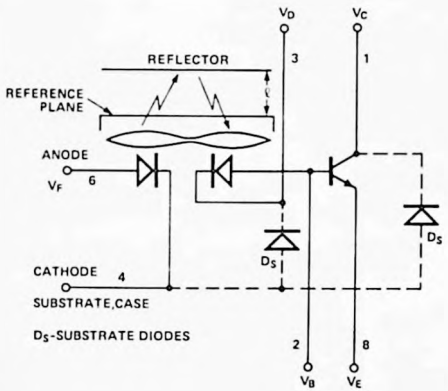
Electrical Operation

The detector section of the sensor can be connected as a single photodiode, or as a photodiode transistor amplifier. When photodiode operation is desired, it is recommended that the substrate diodes be defeated by connecting the collector of the transistor to the positive potential of the power supply and shorting the base-emitter junction of the transistor. Figure 15 shows photocurrent being supplied from the anode of the photodiode to an inverting input of the operational amplifier. The circuit is recommended to improve the reflected photocurrent to stray photocurrent ratio by keeping the substrate diodes from acting as photodiodes.

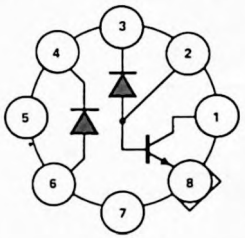
The cathode of the 700nm emitter is physically and electrically connected to the case-substrate of the device. Applications that require modulation or switching of the LED should be designed to have the cathode connected to the electrical ground of the system. This insures minimum capacitive coupling of the switching transients through the substrate diodes to the detector amplifier section.

The HEDS-1000 detector also includes an NPN transistor which can be used to increase the output current of the sensor. A current feedback amplifier as shown in Figure 6 provides moderate current gain and bias point stability.

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



TOP VIEW

PIN	FUNCTION
1	TRANSISTOR COLLECTOR
2	TRANSISTOR BASE, PHOTODIODE ANODE
3	PHOTODIODE CATHODE
4	LED CATHODE, SUBSTRATE, CASE
5	NC
6	LED ANODE
7	NC
8	TRANSISTOR EMITTER

Absolute Maximum Ratings at T_A=25°C

Parameter	Symbol	Min.	Max.	Units	Fig.	Notes
Storage Temperature	T_S	-40	+75	°C		
Operating Temperature	T_A	-20	+70	°C		
Lead Soldering Temperature 1.6mm from Seating Plane			260 for 10 sec.	°C		11
Average LED Forward Current	I_F		50	mA		2
Peak LED Forward Current	I_{FPK}		75	mA	1	1
Reverse LED Input Voltage	V_R		5	V		
Package Power Dissipation	P_P		120	mW		3
Collector Output Current	I_O		8	mA		
Supply and Output Voltage	V_D,V_C,V_E	-0.5	20	V		10
Transistor Base Current	I_B		5	mA		
Transistor Emitter Base Voltage	V_{EB}		.5	V		

CAUTION: The small junction sizes inherent to the design of this bipolar component increase the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be introduced by ESD.

System Electrical/Optical Characteristics at T_A=25°C

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Fig.	Note
Total Photocurrent (I_{PR}+I_{PS})	I_P			375	nA	T_A=-20°C		
		100	180	250		T_A=25°C, I_F=35mA, V_D=V_C=5V	2,3	4
		50				T_A=70°C	15	
Reflected Photocurrent (I_{PR}) to internal Stray Photocurrent (I_{PS})	$\frac{I_{PR}}{I_{PS}}$	4	8.5			I_F=35mA, V_C=V_D=5V	3	
Transistor DC Static Current Transfer Ratio	h_{FE}	50				T_A=-20°C, V_{CE}=5V, I_C=10μA	4,5	
		100	200			T_A=25°C		
Slew Rate			.08		V/μs	R_L=100K, I_{PK}=50mA, R_F= 10M, t_{ON}=100μs, Rate = 1kHz	6	
Image Diameter	d		.17		mm	I_F=35mA, ℓ=4.27mm (0.168in.)	8,10	8,9
Maximum Signal Point	ℓ	4.02	4.27	4.52	mm	Measured from Reference Plane	9	
50% Modulation Transfer Function	MTF		2.5		$I_{npr/mm}$	I_F=35mA, ℓ=4.27mm	10,11	5,7
Depth of Focus	$\frac{\Delta\ell}{FWHM}$		1.2		mm	50% of I_P at ℓ=4.27mm	9	5
Effective Numerical Aperature	N.A.		.3					
Image Location	D		.51		mm	Diameter Reference to Centerline ℓ=4.27mm		6
Thermal Resistance	θ_{JC}		85		°C/W			

Detector Electrical/Optical Characteristics at T_A=25°C

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Fig.	Note
Dark Current	I_{PD}		5	120	pA	T_A=25°C, I_F=0, V_D=5V; Reflection=0%		
				10	nA	T_A=70°C		
Capacitance	C_D		45		pF	V_D=0V, I_P=0, f=1MHz		
Flux Responsivity	R_ϕ		.22		$\frac{A}{W}$	λ=700nm, V_D=5V	12	
Detector Area	A_D		.160		mm^2	Square, with Length=.4mm/Side		

Emitter Electrical/Optical Characteristics at T_A=25°C

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Fig.	Note
Forward Voltage	V_F		1.6	1.8	V	I_F=35mA	13	
Reverse Breakdown Voltage	BV_R	5			V	I_R=100μA		
Radiant Flux	ϕ_E	5	9.0		μW	I_F=35mA, λ=700nm	14	
Peak Wavelength	λ_p	680	700	720	nm	I_F=35mA	14	
Thermal Resistance	θ_{JC}		150		°C/W			
Temperature Coefficient of V_F	$\Delta V_F/\Delta T$		-1.2		mV/°C	I_F=35mA		

Transistor Electrical Characteristics at T_A=25°C

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Fig.	Note
Collector-Emitter Leakage	I_{CEO}		1		pA	V_{CE}=5V		
Base-Emitter Voltage	V_{BE}		.6		V	I_C=10μA, I_B=70nA		
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$		.4		V	I_B=1μA, I_E=10μA		
Collector-Base Capacitance	C_{CB}		.3		pF	f=1MHz, V_{CB}=5V		
Base-Emitter Capacitance	C_{BE}		.4		pF	f=1MHz, V_{BE}=0V		
Thermal Resistance	θ_{JC}		200		°C/W			

NOTES:
1. 300μs pulse width, 1 kHz pulse rate.
2. Derate Maximum Average Current linearly from 65°C by 6mA/°C.
3. Without heat sinking from T_A = 65°C, derate Maximum Average Power linearly by 12mW/°C.
4. Measured from a reflector coated with a 99% reflective white paint (Kodak 6080) positioned 4.27mm (0.168 in.) from the reference plane.
5. Peak-to-Peak response to black and white bar patterns.
6. Center of maximum signal point image lies within a circle of diameter D relative to the center line of the package. A second emitter image (through the detector lens) is also visible. This image does not affect normal operation.
7. This measurement is made with the lens cusp parallel to the black-white transition.
8. Image size is defined as the distance for the 10%-90% response as the sensor moves over an abrupt black-white edge.
9. (+) indicates an increase in the distance from the reflector to the reference plane.
10. All voltages referenced to Pin 4.
11. CAUTION: The thermal constraints of the acrylic lens will not permit the use of conventional wave soldering procedures. The typical preheat and post cleaning temperatures and dwell times can subject the lens to thermal stresses beyond the absolute maximum ratings and can cause it to defocus.

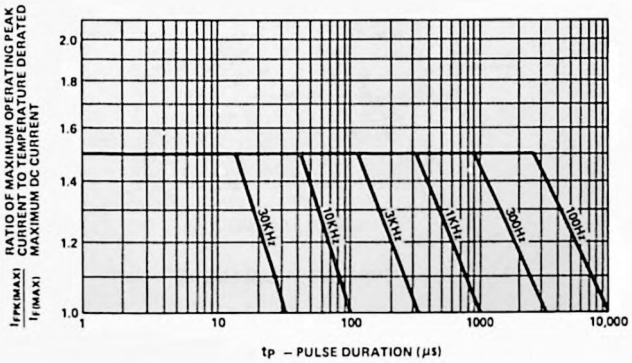


Figure 1. Maximum Tolerable Peak Current vs. Pulse Duration

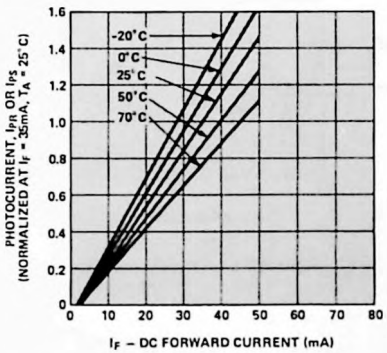


Figure 2. Relative Total Photocurrent vs. LED DC Forward Current

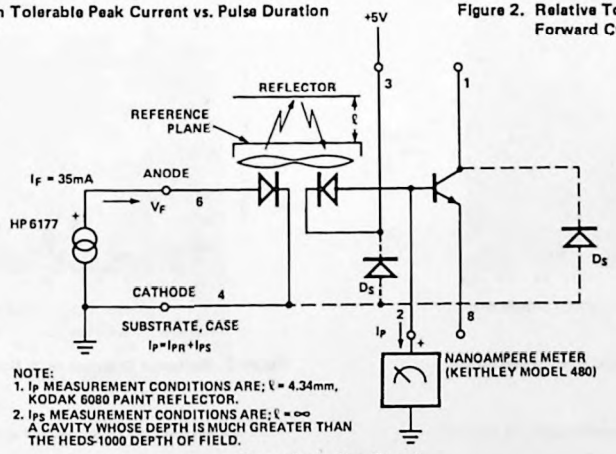


Figure 3. Ip Test Circuit

BAR CODE PRODUCTS

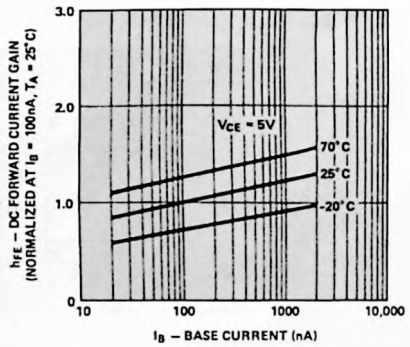


Figure 4. Normalized Transistor DC Forward Current Gain vs. Base Current at Temperature

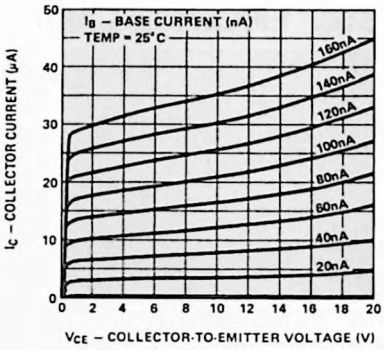


Figure 5. Common Emitter Collector Characteristics

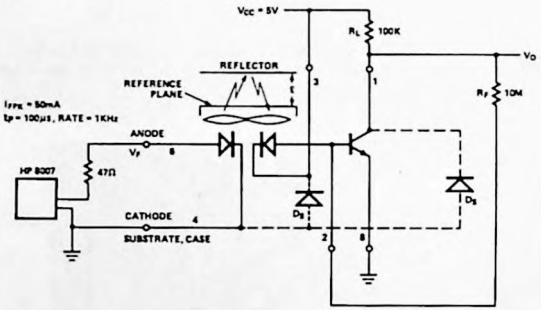


Figure 6. Slew Rate Measurement Circuit

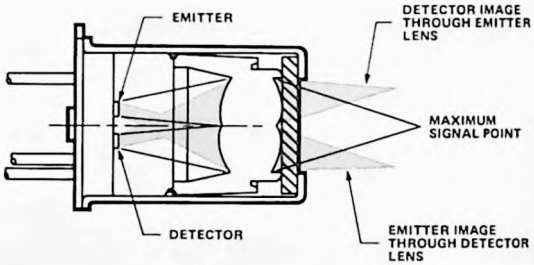


Figure 7. Image Location

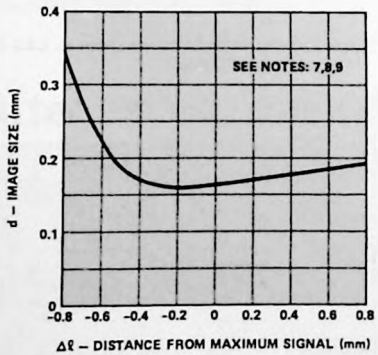


Figure 8. Image Size vs. Maximum Signal Point

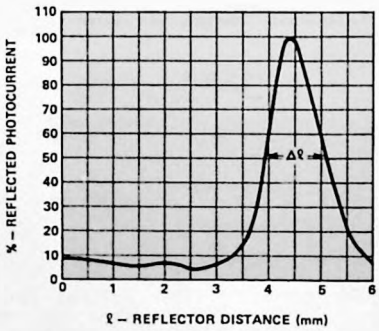


Figure 9. Reflector Distance vs. % Reflected Photocurrent

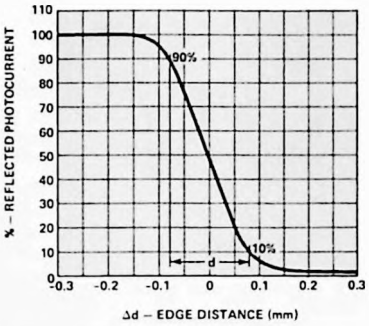


Figure 10. Step Edge Response

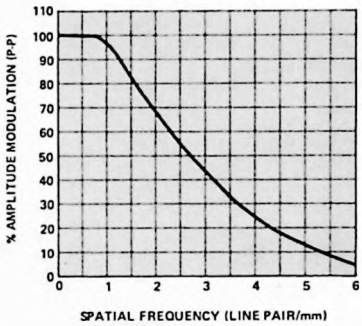


Figure 11. Modulation Transfer Function

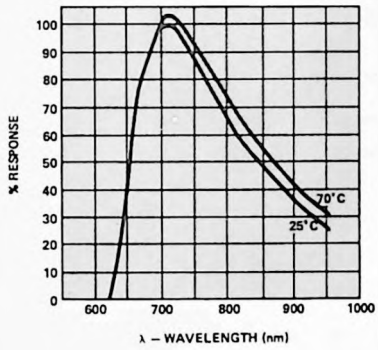


Figure 12. Detector Spectral Response

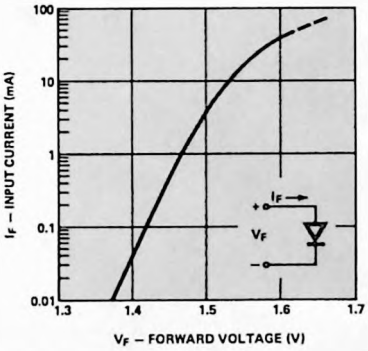


Figure 13. LED Forward Current vs. Forward Voltage Characteristics

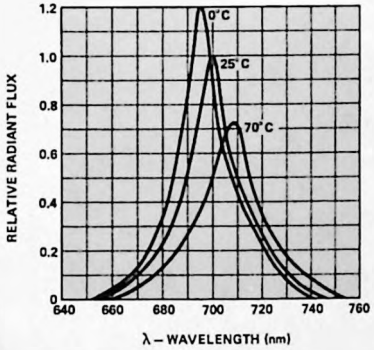


Figure 14. Relative Radiant Flux vs. Wavelength

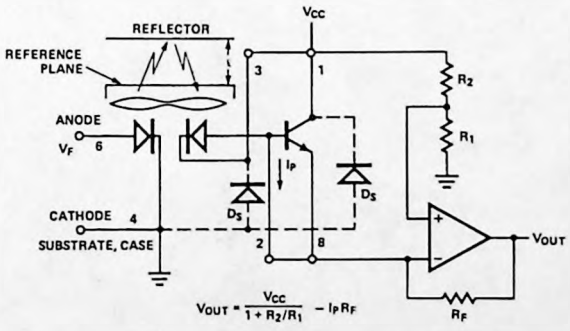
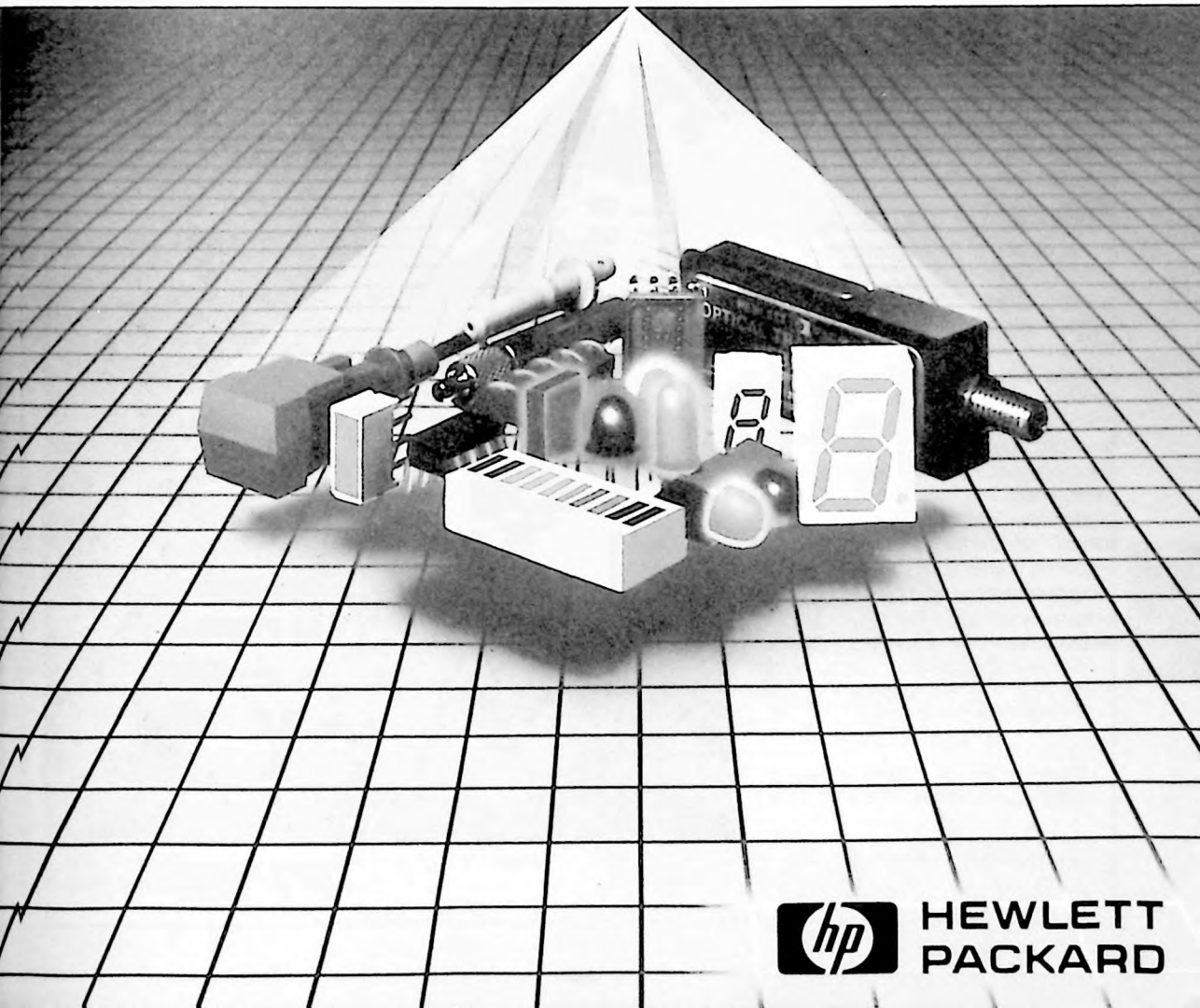


Figure 15. Photodiode Interconnection

8. High Reliability

- Testing Programs
- Selection Guide



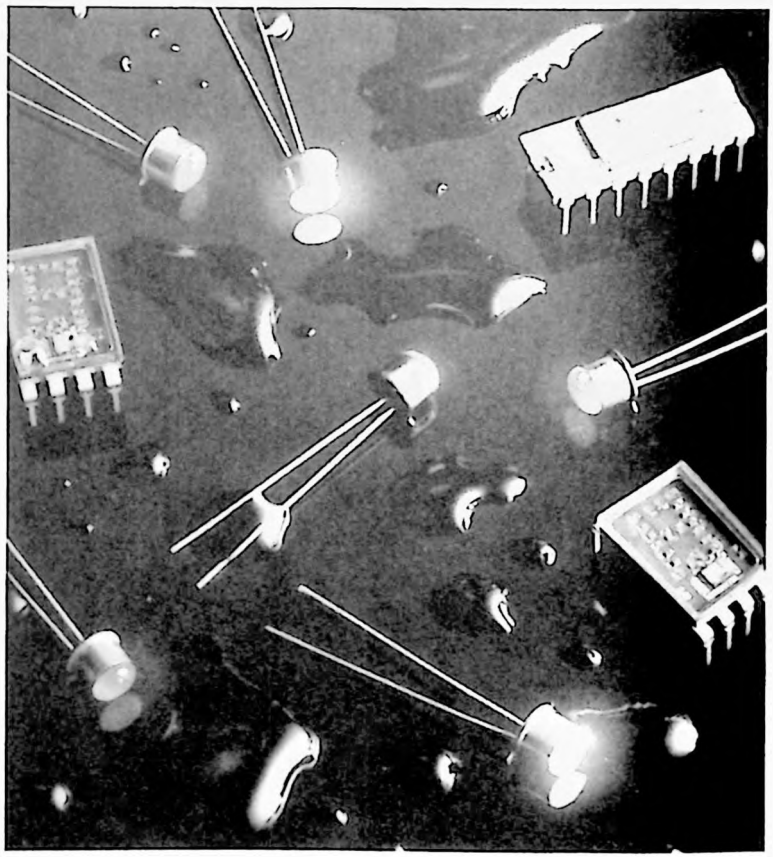
HEWLETT PACKARD

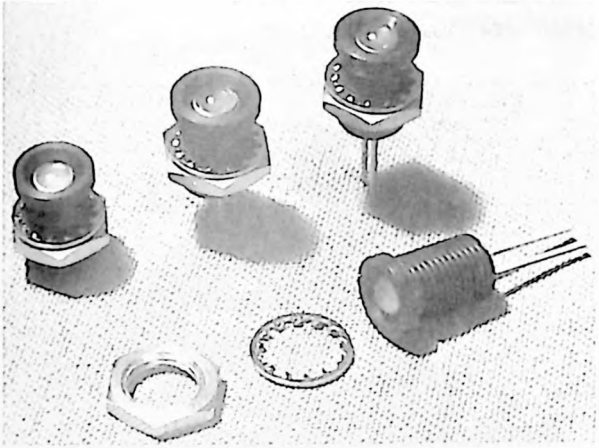
High Reliability

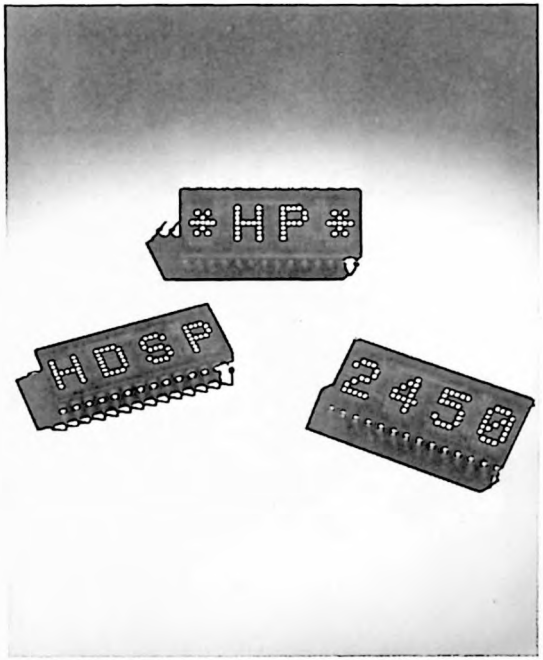
Hewlett-Packard has supplied specially tested high reliability optoelectronic products since 1968 for use in state-of-the-art commercial, military, and aerospace applications. To meet the requirements of high reliability, products must be designed with rugged capabilities to withstand severe levels of environmental stress and exposure without failure. We have accomplished this objective by designing a unique family of hermetic products including lamps, displays, and optocouplers which have proven their merits in numerous advanced space and defense programs in the international marketplace. These products receive reliability screening and qualification tests in accordance with appropriate reliability programs similar to those of MIL-S-19500, MIL-M-38510, and MIL-D-87157. HP supplies JAN and JANTX LED indicators, a DESC drawing for an optocoupler, and HP standard military equivalent screening programs for optocouplers (MIL-M-38510) and displays (MIL-D-87157). Reliability programs are also performed to individual customer control drawings and specifications when needed. Some of these special testing programs are very complex and may include Class S requirements for microcircuits.

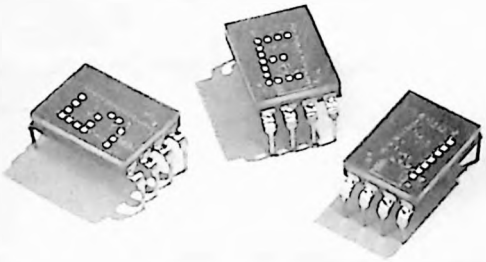
HP's optoelectronic epoxy encapsulated products are designed for long life applications where non-man rated or ground support requirements allow their use. As with hermetic products, the capabilities of epoxy parts can be enhanced by 100% screening and conditioning tests. Lot capabilities can be confirmed by acceptance qualification test programs. MIL-D-87157 is used to define the military requirements for plastic LED indicators and displays.

All testing is done by experienced Hewlett-Packard employees using facilities which are approved by DESC for JAN products and by customer inspection for special programs. Environmental equipment capabilities and operating methods of the test laboratory meet MIL-STD-750 or MIL-STD-883 procedures.









Visible Product Qualification

Two military documents are presently in use to qualify visible products. MIL-S-19500 establishes the standard JAN and JANTX test programs for hermetic lamps. Four hermetic lamps are listed on the Qualified Parts List (QPL) of MIL-S-19500. Descriptions of the individual devices are given in detail specifications called slash sheets. The lamp section of this catalog gives more information on these products.

1N5765	MIL-S-19500/467	Standard Red
1N6092	MIL-S-19500/519	High Efficiency Red
1N6093	MIL-S-19500/520	Yellow
1N6094	MIL-S-19500/521	Green

The second military document governing the qualification of visible products is MIL-D-87157. This general specification was dated August 26, 1981, and covers solid state, light emitting diode displays. This specification may be used to cover all display products including lamps not covered in MIL-S-19500. This specification has provisions for four different quality levels as follows:

Level A	Hermetically sealed displays with 100% screening tests
Level B	Hermetically sealed displays without 100% screening tests
Level C	Non-hermetic displays with 100% screening tests
Level D	Non-hermetic displays without 100% screening tests

Displays meeting the hermeticity requirements of MIL-D-87157 include the dot matrix family; 4N51, 4N52, 4N53, 4N54, and the alphanumeric families; HDSP-2010 and HDSP-2450, 2451, 2452, 2453. These devices may be purchased to Level A of MIL-D-87157 by adding the suffix TXVB to the part number. If only the 100% screening tests are required, the suffix TXV is added.

Detailed testing programs for hermetic products are given in the individual data sheets which follow the general program for quality Level A.

The general program for quality Level C non-hermetic displays from MIL-D-87157 is given below.

TABLE I. 100% SCREEN FORMAT FOR QUALITY LEVEL C

Test Screen	MIL-STD-750 Method	Level C
1. Precap Visual[1]	2072	When specified
2. High Temperature Storage[1]	1032	100%
3. Temperature Cycling[1]	1051	100%
4. Constant Acceleration[1,2]	2006	When specified
5. Fine Leak[1]	1071	N/A
6. Gross Leak[1]	1071	N/A
7. Interim Electrical/Optical Tests[1]	—	When specified
8. Burn-In[1,3]	1015	100%
9. Final Electrical/Optical Tests	—	100%
10. Delta Determinations[1]	—	When specified
11. External Visual[3]	2009	100%

Notes:
1. These tests are design dependent. The conditions and limits shall be specified in the detail specification when these tests are applicable.
2. Applicable to cavity type displays only.
3. MIL-STD-883 test method applies.

TABLE II. GROUP A ELECTRICAL TESTS[1]

Subgroups	LTPD
Subgroup 1 DC Electrical Tests at 25°C	5
Subgroup 2 Selected DC Electrical Tests at High Temperatures	7
Subgroup 3 Selected DC Electrical Tests at Low Temperatures	7
Subgroup 4 Dynamic Electrical Tests at $T_A = 25°C$	5
Subgroup 5 Dynamic Electrical Tests at High Temperatures	7
Subgroup 6 Dynamic Electrical Tests at Low Temperatures	7
Subgroup 7 Optical and Functional Tests at 25°C	5
Subgroup 8 External Visual	7

Notes:
1. The specific parameters to be included for tests in each subgroup shall be as specified in the applicable detail specification.

TABLE IIIb. GROUP B ENVIRONMENTAL TESTS (CLASS C AND D DISPLAYS ONLY)

Test	MIL-STD-750 Method	Sampling Plan
Subgroup 1		
Resistance to Solvents[1]	1022	4 Devices/ 0 Failures
Internal Visual and Mechanical[2,5]	2014	1 Device/ 0 Failures
Subgroup 2[3,4]		
Solderability[1]	2026	LTPD = 15
Electrical/Optical Endpoints[1]		
Subgroup 3		
Thermal Shock[1] (Temperature Cycling)	1051	LTPD = 15
Moisture Resistance[1]	1021	
Electrical/Optical Endpoints[1]		
Subgroup 4		
Operating Life Test (340 Hours)[1]	1027	LTPD = 10
Electrical/Optical Endpoints[1]		
Subgroup 5		
Non-Operating (Storage) Life Test (340 Hours)[1]	1032	LTPD = 10
Electrical/Optical Endpoints[1]		

Notes:
1. Test method or conditions in accordance with detail specification.
2. Not required for solid encapsulated displays.
3. The LTPD applies to the number of leads inspected except in no case shall less than three displays be used to provide the number of leads required.
4. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
5. MIL-STD-883 test method applies.

TABLE IVb. GROUP C PERIODIC TESTS (CLASS C AND D DISPLAYS ONLY)

Test	MIL-STD-750 Method	Sampling Plan
Subgroup 1[1]		
Physical Dimensions	2066	2 Devices/ 0 Failures
Subgroup 2[1]		
Lead Integrity[6]	2004	LTPD = 15
Subgroup 3		
Shock[2]	2016	LTPD = 15
Vibration, Variable Frequency[2]	2056	
Constant Acceleration[2]	2006	
External Visual[3]	1001 or 1011	
Electrical/Optical Endpoints[4]		
Subgroup 4		
Operating Life Test[4,5]	1026	$\lambda = 10$
Electrical/Optical Endpoints[4]		
Subgroup 5		
Temperature Cycling (25 cycles min.)[4]	1051	LTPD = 20
Electrical/Optical Endpoints[4]		

Notes
1. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used.
2. Not required for solid encapsulated displays.
3. Visual requirements shall be as specified in MIL-STD-883, method 1010 or 1011.
4. Test method or conditions in accordance with detail specification.
5. If a given inspection lot undergoing Group B inspection has been selected to satisfy Group C inspection requirements, the 340 hour life tests may be continued on test to 1000 hours in order to satisfy the Group C life test requirements. In such cases, either the 340 hour endpoint measurements shall be made as a basis for Group B lot acceptance or the 1000 hours endpoint measurements shall be used as the basis for both Group B and C acceptance.
6. MIL-STD-883 test method applies.

Hermetic Optocoupler Product Qualification

Hewlett-Packard hermetically sealed optocouplers are hybrid microcircuits which are tested to Class B requirements of MIL-STD-883. Devices which meet these stringent conditions are the 4N55, 6N134, and 6N140 optocouplers. With certain clarifications of their new testing conditions given in the individual data sheets, these products are now available in compliance with the 100% screening program in Method 5004 and the Quality Conformance testing in Method 5005 of MIL-STD-883 Class B. The new military compliant products are: 4N55/883B, 6N140/883B, and 8102801EC (selected item drawing number assigned to the DESC approved 6N134 optocoupler.) Complete details of this testing program are given below and in the individual device data sheets. These parts are preferred units for use in military, high reliability applications.

100% Screening

MIL-STD-883, METHOD 5004 (CLASS B DEVICES)

Test Screen	Method	Conditions
1. Precap Internal Visual	2010	Condition B
2. High Temperature Storage	1008	Condition C, T_A = 150°C, Time = 24 Hours minimum
3. Temperature Cycling	1010	Condition C, -65°C to +150°C, 10 cycles
4. Constant Acceleration	2001	Condition A, 5K G's, Y_1 axis only
5. Fine Leak	1014	Condition A
6. Gross Leak	1014	Condition C
7. Interim Electrical Test	—	Group A, Subgroup 1, except $I_{I/O}$ (optional)
8. Burn-In	1015	Condition B, Time = 160 Hours minimum 6N134: T_A = +125°C, V_{CC} = 5.5V, I_F = 13 mA, I_O = 25 mA 6N140: T_A = +100°C, V_{CC} = 18V, I_F = 5 mA, I_O = 10 mA 4N55: T_A = +125°C, V_{CC} = 5.5V, I_F = 20 mA, V_{OC} = 3.5V, R_L = 270Ω
9. Final Electrical Test Electrical Test Electrical Test Electrical Test	—	Group A, Subgroup 1 Group A, Subgroup 2 Group A, Subgroup 3 Group A, Subgroup 9
10. External Visual	2009	

GROUP A TESTING MIL-STD-883, METHOD 5005 (CLASS B DEVICES)

	LTPD
Subgroup 1 Static tests at T_A = 25°C, I_{OH}, BV_R, I_{CCL}, I_{CCH}, CTR, V_F, I_{OH1} and I_{I-O}.	5
Subgroup 2 Static tests at T_A = +125°C, I_{OH}, BV_R, I_{CCL}, I_{CCH}, CTR V_F and I_{OH1}	7
Subgroup 3 Static tests at T_A = −55°C, I_{OH}, BV_R, I_{CCL}, I_{CCH}, CTR V_F and I_{OH1}	7
Subgroups 4, 5, 6, 7 and 8 These subgroups are non-applicable to this device type	
Subgroup 9 Switching tests at T_A = 25°C, t_{PLH} and t_{PHL}	7
Subgroup 10 Switching tests at T_A = +125°C, t_{PLH} and t_{PHL}	10
Subgroup 11 Switching tests at T_A = -55°C, t_{PLH} and t_{PHL}	10

Qualification/Quality Conformance

Group A electrical tests are product dependent and are given in the individual device data sheets. Group B testing is performed on each manufactured lot.

GROUP B TESTING MIL-STD-883, METHOD 5005 (CLASS B DEVICES)

Test	Method	Conditions	LTPD
Subgroup 1 Physical Dimensions (Not required if Group D is to be performed)	2016		2 Devices/ 0 Failures
Subgroup 2 Resistance to Solvents	2015		4 Devices/ 0 Failures
Subgroup 3 Solderability (LTPD applies to number of leads inspected — no fewer than 3 devices shall be used.)	2003	Soldering Temperature of 260 ± 10°C for 10 seconds	15 (3 Devices)
Subgroup 4 Internal Visual and Mechanical (may be performed at precap)	2014		1 Device/ 0 Failures
Subgroup 5 Bond Strength (1) Thermocompression (performed at precap, prior to seal. LTPD applies to number of bond pulls from a minimum of 4 devices).	2011	(1) Test Condition D	15 (4 Devices)
Subgroup 6 Internal water vapor content (Not applicable — per footnote of MIL-STD)	—		—
Subgroup 7 Fine Leak Gross Leak (Not applicable — per footnote of MIL-STD)	—		—
Subgroup 8* Electrical Test Electrostatic Discharge Sensitivity Electrical Test	3015	Group A, Subgroup 1, except I_{I-O} Group A, Subgroup 1	15

*(To be performed at initial qualification only)

Group C testing is performed on a periodic basis from current manufacturing every 3 months.

GROUP C TESTING MIL-STD-883, METHOD 5005 (CLASS B DEVICES)

Test	Method	Conditions	LTPD
Subgroup 1			
Steady State Life Test	1005	Condition B, Time = 1000 Hours Total 6N134: T_A = +125°C, V_{CC} = 5.5V, I_F = 13 mA, I_O = 25 mA 6N140: T_A = +100°C, V_{CC} = 18V, I_F = 5 mA, I_O = 10 mA 4N55: T_A = +125°C, V_{CC} = 5.5V, I_F = 20 mA, V_{OC} = 3.5V, R_L = 270Ω	5
Endpoint Electricals at 168 hours and 504 hours		Group A, Subgroup 1, except I_{I-O}	
Endpoint Electricals at 1000 hours		Group A, Subgroup 1	
Subgroup 2			
Temperature Cycling	1010	Condition C, -65°C to +150°C, 10 cycles	15
Constant Acceleration	2001	Condition A, 5KG's, Y_1 axis only	
Fine Leak	1014	Condition A	
Gross Leak	1014	Condition C	
Visual Examination	1010	Per visual criteria of Method 1010	
Endpoint Electricals		Group A, Subgroup 1	

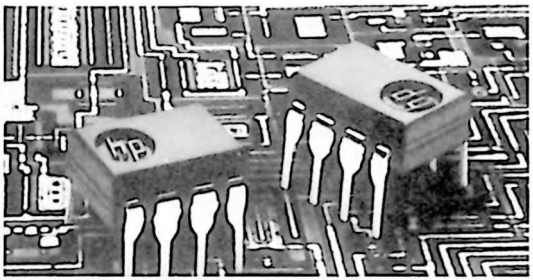
Group D testing is performed on a periodic basis from current manufacturing every 6 months.

GROUP D TESTING MIL-STD-883, METHOD 5005 (CLASS B DEVICES)

Test	Method	Conditions	LTPD
Subgroup 1			
Physical Dimensions	2016		15
Subgroup 2			
Lead Integrity	2004	Test Condition B2, lead fatigue	15
Fine Leak	1014	Condition A	
Gross Leak	1014	Condition C	
Lid Torque*	2024		
* Not applicable per footnote of MIL-STD			
Subgroup 3			
Thermal Shock	1011	Condition B, -55°C to +125°C, 15 cycles min.	15
Temperature Cycling	1010	Condition C, -65°C to +150°C, 100 cycles min.	
Moisture Resistance	1004		
Fine Leak	1014	Condition A	
Gross Leak	1014	Condition C	
Visual Examination		Per visual criteria of Method 1004	
Endpoint Electricals		Group A, Subgroup 1	
Subgroup 4			
Mechanical Shock	2002	Condition B, 1500G, t = 0.5 ms, 5 blows in each orientation	15
Vibration Variable Frequency	2007	Condition A	
Constant Acceleration	2001	Condition A, 5 KG's, Y_1 axis only	
Fine Leak	1014	Condition A	
Gross Leak	1014	Condition C	
Visual Examination	1010	Per visual criteria of Method 1010	
Endpoint Electricals		Group A, Subgroup 1	
Subgroup 5			
Salt Atmosphere	1009	Condition A min.	15
Fine Leak	1014	Condition A	
Gross Leak	1014	Condition C	
Visual Examination	1009	Per visual criteria of Method 1009	
Subgroup 6			
Internal Water Vapor Content exception being taken	1018		—
Subgroup 7			
Adhesion of lead finish	2025		15

Plastic Optocouplers

Hewlett-Packard supplies plastic optocouplers with high reliability testing for commercial/industrial applications requiring prolonged operational life. Two of the most frequently requested 100% preconditioning and screening programs are given. The first program has burn-in and electrical test only, the second program adds temperature storage and temperature cycling. Either program is available for HP's plastic optocouplers. Electrical testing is to catalog conditions and limits and will include 100% DC parameters, sample testing of input-output insulation leakage current and appropriate AC parameters. Contact your local field representative for pricing and availability of these programs.



PLASTIC OPTOCOUPLERS
PRECONDITIONING AND SCREENING 100%

COMMERCIAL BURN-IN**

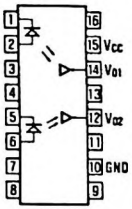
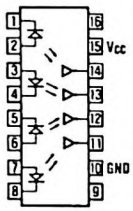
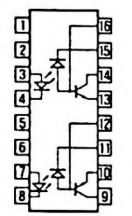
Examinations or Tests	MIL-STD-883 Methods	Conditions
1. Commercial Burn-in	1015	T_A = 70°C, 160 hours per designated circuit.
2. Electrical Test		Per specified conditions and min./max. limits at T_A = 25°C

SCREENING PROGRAM**

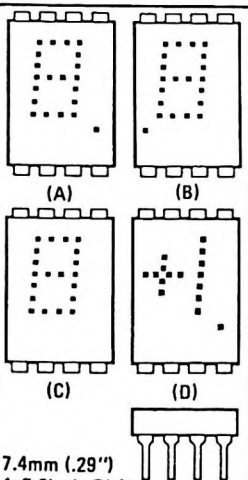
Examinations or Tests	MIL-STD-883 Methods	Conditions
1. High Temperature Storage	1008	24 hours at 125°C
2. Temperature Cycling	1010	10 cycles, -55°C to +125°C
3. Burn-in	1015	T_A = 70°C, 168 hours per designated circuit
4. Electrical Test		Per specified conditions and min./max. limits at T_A = 25°C
5. External Visual	2009	

**Contact your field salesman for details.

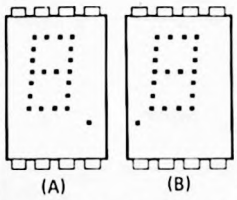
Hermetic Optocouplers

Device		Description	Application	Typical Data Rate (NRZ)	Current Transfer Ratio	Specified Input Current	Withstand Test Voltage	Page No.
	6N134	Dual Channel Hermetically Sealed Optically Coupled Logic Gate	Line Receiver, Ground Isolation High Reliability Systems	10M bit/s	400% Typ.	10 mA	1500 V dc	5-96
	8102801EC	DESC Approved 6N134	Military/High Reliability					5-99
	6N134TXV	TXV — Screened	Use 8102801EC in New Designs					5-96
	6N134TXVB	TXVB — Screened with Group B Data						
	6N140	Hermetically Sealed Package Containing 4 Low Input Current, High Gain Optocouplers	Line Receiver, Low Power Ground Isolation for High Reliabilty Systems	300k bit/s	300% Min.	0.5 mA	1500 V dc	5-103
	6N140/883B	MIL-STD-883 Class B Part	Military/High Reliability					
	6N140TXV	TXV — Hi-Rel Screened	Use 6N140/883B in New Designs					
	6N140TXVB	TXVB — Hi-Rel Screened with Group B Data						
	4N55	Dual Channel Hermetically Sealed Analog Optical Coupler	Line Receiver, Analog Signal Ground Isolaton, Switching Power Supply Feedback Element	700k bit/s	7% Min.	16 mA	1500 V dc	5-106
	4N55/883B	MIL-STD-883 Class B Part	Military/High Reliability					
	4N55TXV	TXV — Hi-Rel Screened	Use 4N55/883B in New Designs					
	4N55TXVB	TXVB — Hi-Rel Screened with Group B Data						

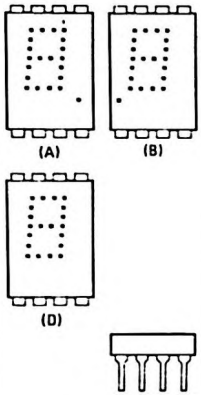
Hermetically Sealed Integrated LED Displays

Device		Description	Package	Application	Page No.
	4N51 (5082-7391) 4N51TXV 4N51TXVB (A)	Numeric RHDP Built in Decoder/Driver/Memory TXV — Hi Rel Screened TXVB — Hi Rel Screened with Group B data	8 Pin Hermetic 15.2mm (.6") DIP with gold plated leads	• Military High Reliability Applications • Avionics/Space Flight Systems • Fire Control Systems • Ground Support, Shipboard Equipment	3-136
	4N52 (5082-7392) 4N52TXV 4N52TXVB (B)	Numeric LHDP Built in Decoder/Driver/Memory TXV — Hi Rel Screened TXVB — Hi Rel Screened with Group B data			
	4N54 (5082-7395) 4N54TXV 4N54TXVB (C)	Hexadecimal Built in Decoder/Driver/Memory TXV — Hi Rel Screened TXVB — Hi Rel Screened with Group B data			
	4N53 (5082-7393) 4N53TXV 4N53TXVB (D)	Character Plus/Minus Sign TXV — Hi Rel Screened TXVB — Hi Rel Screened with Group B data			

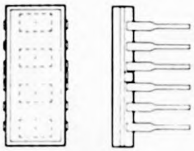
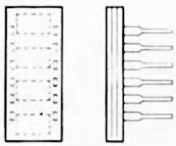
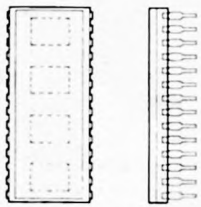
Military/Industrial Grade Displays

Device and Package		Description	Color	Application	Page No.
 (A) (B) (C) (D) 7.4 mm (.29") 4 x 7 Single Digit Package: 8 Pin Glass Ceramic 15.2 mm (.6") DIP	5082-7356 (A)	Numeric RHDP Built-in Decoder/Driver/Memory	Standard Red	• Medical Equipment • Industrial and Process Control Equipment • Computers • Where Ceramic Package IC's required • High Reliability Applications	437
	5082-7357 (B)	Numeric LHDP Built-in Decoder/Driver/Memory			
	5082-7359 (C)	Hexadecimal Built-in Decoder/Driver/Memory			
	5082-7358 (D)	Character Plus/Minus Sign			
	HDSP-0760 (A)	Numeric RHDP Built in Decoder/Driver/Memory	High Efficiency Red Low Power	• Military Equipment • Ground Support Equipment • Avionics • High Reliability • Applications	3-131
	HDSP-0761 (B)	Numeric LHDP Built in Decoder/Driver/Memory			
	HDSP-0762 (C)	Hexadecimal Built in Decoder/Driver/Memory			
	HDSP-0763 (D)	Over Range ± 1			
	HDSP-0770 (A)	Numeric RHDP Built in Decoder/Driver/Memory	High Efficiency Red High Brightness	• High Brightness Ambient Systems • Cockpit, Shipboard Equipment • High Reliability Applications	
	HDSP-0771 (B)	Numeric LHDP Built in Decoder/Driver/Memory			
	HDSP-0772 (C)	Hexadecimal Built in Decoder/Driver/Memory			
	HDSP-0763 (D)	Over Range ± 1			
	HDSP-0860 (A)	Numeric RHDP Built in Decoder/Driver/Memory	Yellow	• Business Machines • Fire Control Systems • Military Equipment • High Relaibility Applications	
	HDSP-0861 (B)	Numeric LHDP Built in Decoder/Driver/Memory			
	HDSP-0862 (C)	Hexadecimal Built in Decoder/Driver/Memory			
	HDSP-0863 (D)	Over Range ± 1			
	HDSP-0960 (A)	Numeric RHDP Built in Decoder/Driver/Memory	Green	• Business Machines • Fire Control Systems • Military Equipment • High Reliability Applications	
	HDSP-0961 (B)	Numeric LHDP Built in Decoder/Driver/Memory			
	HDSP-0962 (C)	Hexadecimal Built in Decoder/Driver/Memory			
	HDSP-0963 (D)	Over Range ± 1			

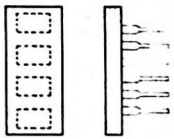
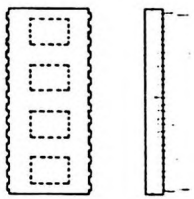
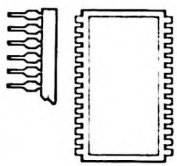
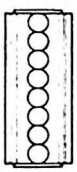
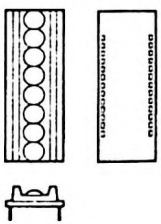
Military/Industrial Grade Displays (cont.)

Device		Description	Color	Application	Page No.
 (A) (B) (D) 7.4 mm (.29") 4 x 7 Single Digit	HDSP-0781 HDSP-0781 TXV HDSP-0781 TXVB	Numeric RHDP, Built-in Decoder/Driver Memory	High Efficiency Red, Low Power	• Ground, Airborne, Shipboard Equipment • Fire Control Systems • Space Flight Systems • Other High Reliability Uses	3-150
	HDSP-0782 HDSP-0782 TXV HDSP-0782 TXVB	Numeric LHDP, Built-in Decoder/Driver Memory			
	HDSP-0783 HDSP-0783 TXV HDSP-0783 TXVB	Overrange ±1			
	HDSP-0784 HDSP-0784 TXV HDSP-0784 TXVB	Hexadecimal, Built-in Decoder/Driver Memory			
	HDSP-0791 HDSP-0791 TXV HDSP-0791 TXVB	Numeric RHDP, Built-in Decoder/Driver Memory	High Efficiency Red, High Brightness	• Ground, Airborne, Shipboard Equipment • Fire Control Systems • Space Flight Systems • Other High Reliability Uses	
	HDSP-0792 HDSP-0792 TXV HDSP-0792 TXVB	Numeric LHDP, Built-in Decoder/Driver Memory			
	HDSP-0793 HDSP-0793 TXV HDSP-0793 TXVB	Overrange ±1			
	HDSP-0794 HDSP-0794 TXV HDSP-0794 TXVB	Hexadecimal, Built-in Decoder/Driver Memory			
	HDSP-0881 HDSP-0881 TXV HDSP-0881 TXVB	Numeric RHDP, Built-in Decoder/Driver Memory	Yellow	• Ground, Airborne, Shipboard Equipment • Fire Control Systems • Space Flight Systems • Other High Reliability Uses	
	HDSP-0882 HDSP-0882 TXV HDSP-0782 TXVB	Numeric LHDP, Built-in Decoder/Driver Memory			

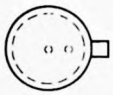
Alphanumeric LED Displays

Device		Description	Color	Application	Page No.
	HDSP-2000	3.7 mm (.15") 5 x 7 Four Character Alphanumeric	Red	• Computer Terminals • Business Machines • Medical Instruments • Portable, Hand-held or mobile data entry, read-out or communications For further information see Application Note 1016.	3-14
	HDSP-2001	12 Pin Ceramic 7.62 mm (.3") DIP with untinted glass lens	Yellow		
	HDSP-2002		High Eff. Red		
	HDSP-2003		High Performance Green		
	HDSP-2010 HDSP-2010 TXV HDSP-2010 TXVB	Extended Temperature to T_A = -40°C 3.7 mm (.15") 5 x 7 Four Character Alphanumeric TXV Hi Rel Screened TXVB Hi Rel Screened	Red, Red Glass Contrast Filter	• Extended temperature applications requiring high reliability. • I/O Terminals • Avionics For further information see Application Note 1016.	3-18
	HDSP-2300	4.87 mm (.19") 5 x 7 Four Character Alphanumeric, 12 Pin Ceramic 6.35 mm (.25") DIP/Low Power	Red	• Avionics • Ground Support, Cockpit, Shipboard systems • Medical Equipment • Industrial and Process control • Computer Peripherals and Terminals	3-124
	HDSP-2301		Yellow, High Brightness		
	HDSP-2302		High Eff. Red, High Brightness		
	HDSP-2303		High Performance Green, High Brightness		
	HDSP-2450 HDSP-2450 TXV HDSP-2450 TXVB	Hermetic Extended Temperature Range to T_A = -55°C 6.9 mm (.27") 5 x 7 Four Character Alphanumeric 28 Pin Ceramic 15.24 mm (.6") DIP	Red TXV — Hi Rel Screened TXVB — Hi Rel Screened to Level A MIL-D-87117	• Military Equipment • High Reliability Applications	3-41
	HDSP-2451 HDSP-2451 TXV HDSP-2451 TXVB		Yellow TXV — Hi Rel Screened TXVB — Hi Rel Screened to Level A MIL-D-87157		
	HDSP-2452 HDSP-2452 TXV HDSP-2452 TXVB		High Efficiency Red TXV — Hi Rel Screened TXVB — Hi Rel Screened to Level A MIL-D-87157		

Alphanumeric LED Displays (continued)

Device		Description	Color	Application	Page No.
	HDSP-2310	Hermetic Extended Temperature Range 5.0 mm (.20") 5 x 7 Alpha-numeric 12 Pin Ceramic	Standard Red	• Military Equipment • Avionics • High Rel Industrial Equipment	3-30
	HDSP-2310 TXV		TXV — High Rel Screened		
	HDSP-2310 TXVB		TXVB — High Rel Screened to Level A MIL-D-87157		
	HDSP-2311		Yellow		
	HDSP-2311 TXV		TXV — High Rel Screened		
	HDSP-2311 TXVB		TXVB — High Rel Screened to Level A MIL-D-87157		
	HDSP-2312		High Eff. Red		
	HDSP-2312 TXV		TXV — High Rel Screened		
	HDSP-2312 TXVB		TXVB — High Rel Screened to Level A MIL-D-87157		
	HDSP-2490	6.9 mm (.27") 5 x 7 Four Character Alphanumeric 28 Pin Ceramic 15.24 mm (.6") DIP	Red	• Computer Base Mobile Units • High Brightness Ambient Systems For further information see Application Note 1016.	3-37
	HDSP-2491		Yellow, High Brightness		
	HDSP-2492		High Eff. Red, High Brightness		
	HDSP-2493		High Performance Green, High Brightness		
	5082-7100	6.9 mm (.27") 5 x 7 Three Digit Alphanumeric 22 Pin Ceramic 15.2 mm (.6") DIP	Red Untinted Glass Lens	General Purpose Market • Business Machines • Calculators • Solid State CRT • High Reliability Applications For further information ask for Application Note 931 on Alpanumeric Displays.	3-48
	5082-7101	6.9 mm (.27") 5 x 7 Four Digit Alphanumeric 28 Pin Ceramic 15.2 mm (.6") DIP			
	5082-7102	6.9 mm (.27") 5 x 7 Five Digit Alphanumeric 36 Pin Ceramic 15.2 mm (.6") DIP			
	HDSP-6504	3.8 mm (.15") Sixteen Segment Four Character Alphanumeric 22 Pin 15.2 mm (.6") DIP	Red	• Computer Terminals • Hand Held Instruments • In-Plant Control Equipment • Diagnostic Equipment	3-152
	HDSP-6508	3.8 mm (.15") Sixteen Segment Eight Character Alphanumeric 26 Pin 15.2 mm (.6") DIP			
	HDSP-6300	3.56 mm (.14") Sixteen Segment Eight Character Alphanumeric 26 Pin 15.2 mm (.6") DIP	Red	• Computer Peripherals and Terminals • Computer Base Emergency Mobile Units • Automotive Instrument Panels • Desk Top Calculators • Hand-Held Instruments For further information ask for Application Note 931.	3-58

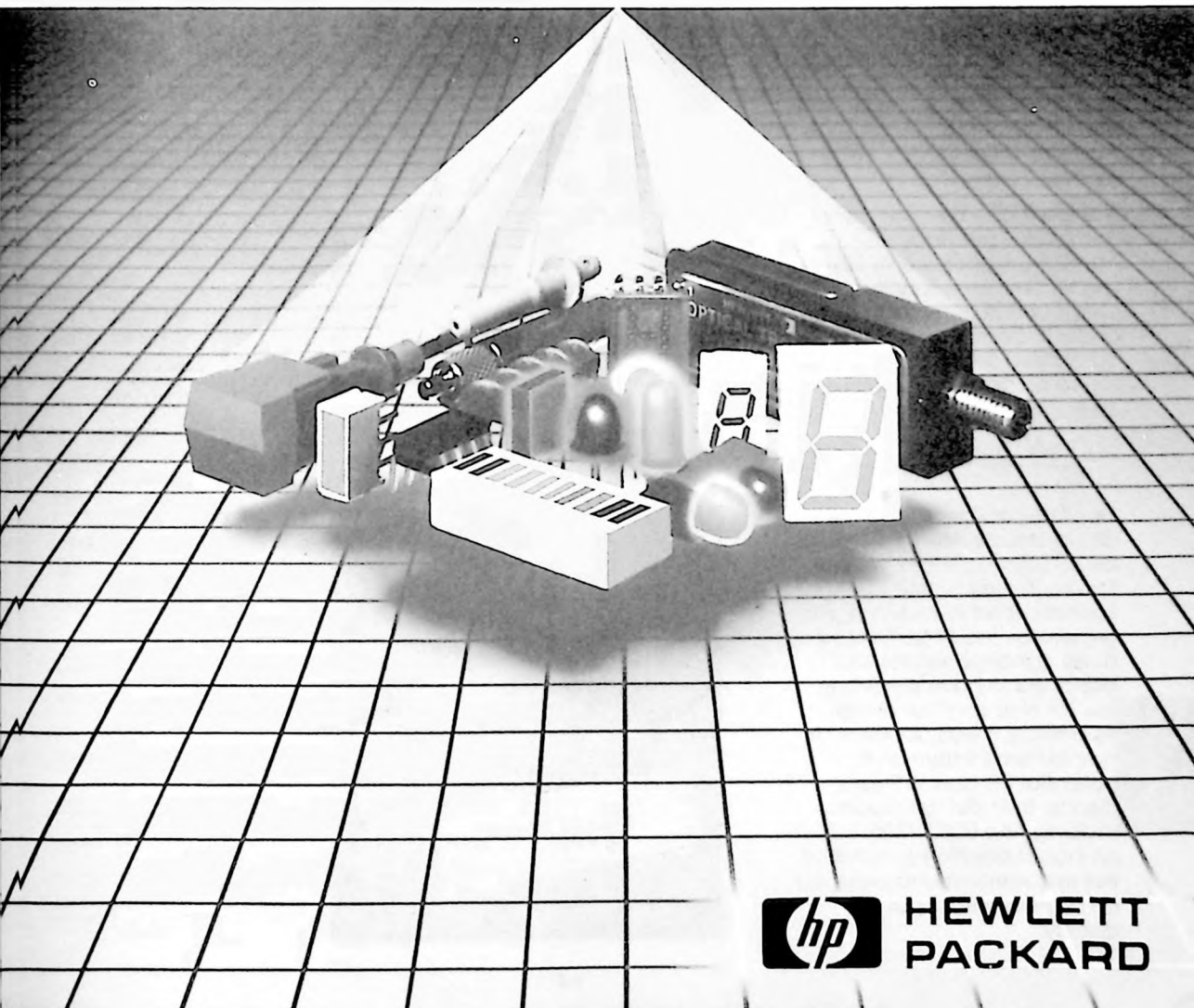
Hermetically Sealed and High Reliability LED Lamps

Device		Description			Typical Luminous Intensity	2θ 1/2[1]	Typical Forward Voltage	Page No.
Package Outline Drawing	Part No.	Color[2]	Package	Lens				
	1N5765 JAN1N5765[4] JANTX1N5765[4]	Red (640 nm)	Hermetic/ TO-46[3]	Red Diffused	0.5 mcd @ 20 mA	70°	1.6 V @ 20 mA	1-64
	1N6092 JAN1N6092[4] JANTX1N6092[4]	High Efficiency Red (626 nm)			1.0 mcd @ 20 mA		2.0 V @ 20 mA	
	1N6093 JAN1N6093[4] JANTX1N6093[4]	Yellow (585 nm)		Yellow Diffused				
	1N6094 JAN1N6094[4] JANTX1N6094[4]	Green (572 nm)		Green Diffused	0.8 mcd @ 25 mA		2.1 V @ 20 mA	
	5082-4787 HLMP-0930 HLMP-0931	Red (640 nm)	Panel Mount Version	Red Diffused	0.5 mcd @ 20 mA		1.6 V @ 20 mA	
	5082-4687 M19500/519-01[4] M19500/519-02[4]	High Efficiency Red (626 nm)			1.0 mcd @ 20 mA		2.0 V @ 20 mA	
	5082-4587 M19500/520-01[4] M19500/520-02[4]	Yellow (585 nm)		Yellow Diffused				
	5082-4987 M19500/521-01[4] M19500/521-02[4]	Green (572 nm)		Green Diffused	0.8 mcd @ 25 mA		2.1 V @ 20 mA	

NOTES:
1. θ1/2 is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. Peak Wavelength.
3. PC Board Mountable.
4. Military Approved and qualified for High Reliability Applications.

9. Applications

- Application Bulletins, Notes, and Manual Listings
- Abstracts
- Application Bulletins and Notes



HEWLETT PACKARD

Applications

(HPBK-2000) Optoelectronics/ Fiber Optics Applications Manual

A vastly expanded version of the original Optoelectronics Applications Manual published by McGraw-Hill in 1977, this new edition provides the electronic engineer with up to date design techniques on state-of-the-art optoelectronic products. Added to the original extensive coverage of LED's, Displays, and Optocouplers is a new wealth of information on Fiber Optics, Industrial Uses of Optocouplers, Back Lighting, Interfacing displays to Microprocessors, Sunlight Viewable displays, and Precision reflective optical position sensing.

This book can be purchased from a Hewlett-Packard franchised distributor or from the McGraw-Hill Publishing Company. A complete listing of all HP Components authorized distributors can be found on pages 10-2 through 10-4.

Hewlett-Packard's 5082-7300 dot matrix display was chosen by HP's Stanford Park division for use in their highly sophisticated low noise signal generator, the 8662. This low noise signal generator was designed to have extremely low RFI and spurious emission. As a result, it was necessary to pay extreme attention to potential RFI and to find a display that did not require strobing. The 5082-7300, with its on-board electronics, satisfied this requirement and provided an aesthetic front panel display.

Below is a complete listing of all of the Optoelectronic Applications Information available. For those items which were not included in this catalog, a brief abstract is shown. These are available in their entirety from your local HP Sales Office or nearest HP Components Franchised Distributor or Representative.

APPLICATION BULLETINS

Model Pub. No. (Date)	Description	Ref.
AB-1 5952-8378 (1/75)	Construction and Performance of High Efficiency Red, Yellow and Green LED Materials	Abstract
AB-3 5952-8380 (3/75)	Soldering Hewlett-Packard Silver Plated Lead Framed LED Devices	9-5
AB-4 5952-8381 (4/75)	Detection and Indication of Segment Failures in 7-Segment LED Displays	Abstract
AB-54 5953-0363 (7/77)	Mechanical Handling of Sub-miniature LED Lamps and Arrays	Abstract
AB-60 5953-9347 (4/83)	Applications Circuits for HCPL-3700 and HCPL-2601	9-9
AB-64 5953-9366 (9/83)	Mechanical and Optical Considerations for the 0.3" Microbright Seven-Segment Display	9-11
AB-65 5953-9370 (9/83)	Using 50/125 μm Optical Fiber with Hewlett-Packard Components	9-13
AB-69 5953-9384 (10/83)	CMOS Circuit Design using Hewlett-Packard Optocouplers	9-17

APPLICATION NOTES

Model Pub. No. (Date)	Description	Ref.
AN-915 5953-0431 (4/80)	Threshold Detection of Visible and Infrared Radiation with PIN Photodiodes	9-20
AN-934 5952-0337 (11/72)	5082-7300 Series Solid State Display Installation Techniques	Abstract
AN-939 5953-9368 (8/83)	High Speed Optocouplers	Abstract
AN-945 5952-0420 (10/73)	Photometry of Red LEDs	Abstract
AN-947 5953-7759 (6/82)	Digital Data Transmission Using Optically Coupled Isolators	Abstract
AN-948 5953-7716 (12/81)	Performance of the 6N135, 6N136 and 6N137 Optocouplers in Short to Moderate Length Digital Data Transmission Systems	9-26
AN-951-1 5953-7794 (10/82)	Applications for Low Input Current, High Gain Optocouplers	9-35
AN-951-2 5953-7730 (4/82)	Linear Applications of Optocouplers	9-39
AN-1000 5953-0463 (1/82)	Digital Data Transmission with the HP Fiber Optic System	9-43
AN-1002 5953-7799 (10/82)	Consideration of CTR Variations in Optically Coupled Isolator Circuit Designs	9-62
AN-1003 5953-0405 (9/79)	Interfacing 18-Segment Displays to Microprocessors	9-78

APPLICATION NOTES (Cont'd)

Model Pub. No. (Date)	Description	Ref.
AN-1004 5953-0406 (11/79)	Threshold Sensing for Industrial Control Systems with the HCPL-3700 Interface Optocoupler	9-98
AN-1005 5953-0419 (3/80)	Operational Considerations for LED Lamps and Display Devices	9-112
AN-1006 5953-0439 (7/80)	Seven Segment LED Display Applications	9-118
AN-1007 5953-0452 (1/81)	Bar Graph Array Applications	9-138
AN-1008 5953-0460 (12/80)	Optical Sensing with the HEDS-1000	9-146
AN-1011 5953-0482 (4/81)	Design and Operational Considerations for the HEDS-5000 Incremental Shaft Encoder	9-166
AN-1012 5953-0478 (2/81)	Methods of Legend Fabrication	9-186
AN-1015 5953-7788 (9/82)	Contrast Enhancement Techniques for LED Displays	9-192
AN-1016 5953-7787 (9/82)	Using the HDSP-2000 Alphanumeric Display Family	9-224
AN-1017 5953-7784 (9/82)	LED Solid State Reliability	9-256
AN-1018 5953-9359 (8/83)	Designing with HCPL-4100 and HCPL-4200 20 mA Optocouplers	9-263
AN-1019 5953-9369 (8/83)	Using the HLMP-4700/-1700/ -7000 Series Low Current Lamp	9-282

APPLICATIONS MANUAL

Model Pub. No. (Date)	Description	Ref.
HPBK-2000 McGraw-Hill (No. 93203815) (1981)	Optoelectronics/Fiber-Optics Applications Manual	9-2

Abstracts

APPLICATION BULLETIN 1
Construction and Performance of High Efficiency Red, Yellow and Green LED Materials

The high luminous efficiency of Hewlett-Packard's High Efficiency Red, Yellow and Green lamps and displays is made possible by a new kind of light emitting material utilizing a GaP transparent substrate. This application bulletin discusses the construction and performance of this material as compared to standard red GaAsP and red GaP materials.

APPLICATION BULLETIN 4
Detection and Indication of Segment Failures in Seven Segment LED Displays

The occurrence of a segment failure in certain applications of seven segment displays can have serious consequences if a resultant erroneous message is read by the viewer. This application bulletin discusses three techniques for detecting open segment lines and presenting this information to the viewer.

APPLICATION BULLETIN 54
Mechanical Handling of Subminiature LED Lamps and Arrays

The Need for Careful Mechanical Handling

Hewlett-Packard manufactures a series of individual LED lamps and lamp arrays that are very small epoxy encapsulated devices. These devices are classified as having a SUBMINIATURE package configuration. When carefully installed on a printed circuit board, these devices will reliably function with a long predictable operating life.

To obtain long operating life, these subminiature devices must be carefully installed on the printed circuit board in such a manner as to insure the integrity of the encapsulating epoxy. This will in turn maintain the integrity of the device by not permitting mechanical and thermal stresses to induce strains on the LED die attach and wire bonds which may cause failure.

This application bulletin describes the subminiature package assembly, the package's mechanical limitations and offers specific suggestions for proper installation.

APPLICATION NOTE 934
5082-7300 Series Solid State Display Installation Techniques

The 5082-7300 series Numeric/Hexadecimal indicators are an excellent solution to most standard display problems in commercial, industrial and military applications. The unit integrates the display character and associated drive electronics in a single package. This advantage allows for space, pin and labor cost reductions, at the same time improving overall reliability. The information presented in this note describes general methods of incorporating the -7300 into varied applications.

APPLICATION NOTE 939
High Speed Optocouplers

Often designers are faced with the problem of providing circuit isolation in order to prevent ground loops and common mode signals. Typical devices for doing this have been relays, transformers and line receivers. However, both relays and transformers are low speed devices, incompatible with modern logic circuits. Line receiver circuits are fast enough, but are limited to a common mode voltage of 3 volts.

In addition, they do not protect very well against ground loop signals. Now optocouplers are available which solve most isolation problems.

This Application Note contains a description of Hewlett-Packard's high speed optocouplers and discusses their applications in digital and analog systems.

APPLICATION NOTE 945
Photometry of Red LEDs

Nearly all LEDs are used either as discrete indicator lamps or as elements of a segmented or dot-matrix display. As such, they are viewed directly by human viewers, so the primary criteria for determining their performance is the judgement of a viewer. Equipment for measuring LED light output should, therefore, simulate human vision.

This Application Note will provide answers to these questions:

1. What to measure (definition of terms)
2. How to measure it (apparatus arrangement)
3. Whose equipment to use (criteria for selection)

APPLICATION NOTE 947
Digital Data Transmission Using Optically Coupled Isolators

Optically coupled isolators (optocouplers) make ideal line receivers for digital data transmission applications. They are especially useful for elimination of common mode interference between two isolated data transmission systems. This application note describes design considerations and circuit techniques with special emphasis on selection of line drivers, transmission lines, and line receiver termination for optimum data rate and common mode rejection. Both resistive and active terminations are described in detail. Specific techniques are described for multiplexing applications, and for common mode rejection and data rate enhancement.

HEWLETT PACKARD

APPLICATION BULLETIN 3

Soldering Hewlett-Packard Silver Plated Lead Frame LED Devices

INTRODUCTION

Since the price of gold has increased several times over past years, the cost of a gold plated lead frame has increased substantially above the cost of a silver plated lead frame. The impact of this increase in cost has been industry wide.

By using silver plating, no additional manufacturing process steps are required. Silver has excellent electrical conductivity. LED die attach and wire bonding to a silver lead frame is accomplished with the same reliability as with a gold lead frame. Also, soldering to a silver lead frame provides a reliable electrical and mechanical solder joint. Soldering silver plated lead frame LED devices into a printed circuit board is not more complicated than soldering LED devices with gold plated lead frames. This application bulletin offers some suggestions on how to solder HP silver plated lead frame LED devices.

THE SILVER PLATING

The silver plating process is performed as follows: The lead frame base metal is activated (cleaned) and then plated with a copper strike, nominally 50 microinches (0.00127mm) thick. Then a minimum 100 microinch (0.00381mm) thick plating of silver is added. A "brightener" is usually added to the silver plating bath to insure an optimum surface texture to the silver plating. The term "brightener" comes from the medium bright surface reflectance of the silver plate.

Since silver is porous with respect to oxygen, the copper strike acts as an oxygen barrier for the lead frame base metal. Thus, oxide compounds of the base metal are prevented from forming underneath the silver plating. Copper readily diffuses into silver forming a solution that has a low temperature eutectic point. The interdiffusion between the copper strike and the silver overplate improves the solderability of the overall plating system. If basic soldering time and temperature limits are not exceeded, a lead frame base metal-copper-silver-solder metallurgical bonding system will be obtained.

THE EFFECT OF TARNISH

Silver reacts chemically with sulfur to form the tarnish, silver sulfide (Ag_2S). The build-up of tarnish is the primary reason for poor solderability. However, the density of the tarnish and the kind of solder flux used actually determine the solderability. As the density of the tarnish increases, the more active the flux must be to penetrate and remove the tarnish layer. Some recommended fluxes and cleaner/surface conditions are discussed in the "Solder, Flux and Cleaners" section.

STORAGE AND HANDLING

The best technique for insuring good solderability of a silver plated lead frame device is to prevent the formation of tarnish. This is easily accomplished by preventing the leads from being exposed to sulfur and sulfur compounds. The two primary sources of sulfur are free air and most paper products such as paper sacks and cardboard containers. The best defense against the formation of tarnish is to keep silver lead frame devices in protective packaging until just prior to the soldering operation. One way to accomplish this is to store the LED devices unwrapped in their original packaging as received from HP. For example, Hewlett-Packard ships its seven segment display products in plastic tubes which are sealed air tight in polyethylene. It is best to leave the polyethylene intact during storage and open just prior to soldering.

Listed below are a few suggestions for storing silver lead frame devices.

1. Store the devices in the original wrapping unopened until just prior to soldering.
2. If only a portion of the devices from a single tube are to be used, tightly re-wrap the plastic tube containing the unused devices in the original or a new polyethylene sheet to keep out free air.
3. Loose devices may be stored in zip-lock or tightly sealed polyethylene bags.
4. For long term storage of parts, place one or two petroleum napthalene mothballs inside the plastic package containing the devices. The evaporating napthalene creates a vapor pressure inside the plastic package which keeps out free air.
5. Any silver lead frame device may be wrapped in "Silver Saver" paper for positive protection against the formation of tarnish. "Silver Saver" is manufactured by:

   The Orchard Corporation
   1154 Reco Avenue
   St. Louis, Missouri 63126 (312) 822-3888

6. To reduce shelf storage time, it will be worthwhile to use inventory control to insure that the devices first received will be the first devices to be used.

   One caution: The adhesives used on pressure sensitive tapes such as cellophane, electrical and masking tape can soak through silver protecting papers and may leave an adhesive film on the leads. This film reduces solderability and should be removed with freon T-P35, freon T-E35 or equivalent prior to soldering.

SOLDER, FLUX AND CLEANERS

The solder most widely used for soldering electronic components into printed circuit boards is Sn60 (60% tin and 40% lead) per federal standard QQ-S-571. Two alternates are the eutectic composition Sn63 and the 2% silver solder Sn62.

As the device leads pass through the solder wave of a flow solder process, the tin in the solder scavenges silver from the silver plating and forms one of two silver-tin intermetallics (Ag_6Sn or Ag_3Sn). This silver in the molten solder should not be considered a contaminant. As the silver content increases, the rate of scavenging decreases and the probability of obtaining the desired base metal-copper-silver-solder metallurgical system is improved. The result is that the silver content in solder, which reaches a maximum of 2-1/2% in Sn60 at 230°C, aids in producing reliable solder joints on silver plated lead frames.

Solder flux classifications per federal standard QQ-S-571, listed in order of increasing strength, are as follows:

Type R: Non-Activated Rosin Flux
Type RMA: Mildly Activated Rosin Flux
Type RA: Activated Rosin Flux
Type AC: Organic Acid Flux, Water Soluble

Suggested applications of these flux types with respect to various tarnish levels are as follows:

Silver plated lead frames that are clean, contaminant and tarnish free may be soldered using a Type R flux such as Alpha 100.

Minor Tarnish

Since some minor tarnish or other contaminant may be present on the leads, a type RMA flux such as Alpha 611 or 611 Foam, Kester 197 or equivalent is recommended. Minor tarnish may be identified by reduced reflectance of the ordinarily medium bright surface of the silver plating. Type RMA fluxes which meet MIL-F-14256 are used in the construction of telephone communication, military and aero space equipment.

Mild Tarnish

For a mild tarnish, a type RA flux such as Alpha 711-35, Alpha 809 foam, Kester 1544, Kester 1585 or equivalent should be used. A mild tarnish may be identified by a light yellow tint to the surface of the silver plating.

Moderate Tarnish

A type AC water soluable flux such as Alpha 830, Alpha 842, Kester 1429 or 1429 foam, Lonco 3355 or equivalent will give acceptable results on surface conditions up to a moderate tarnish. A moderate tarnish may be identified by a light yellow-tan color on the surface of the silver plating.

If a more severe tarnish is present, such as a heavy tarnish identified by a dark tan to black color, a cleaner/surface conditioner must be used. Some possible cleaner/surface conditioners are Alpha 140, Alpha 174, Kester 5560, and Lonco TL-1. The immersion time for each cleaner/surface conditioner will be just a few seconds and each is used at room temperature. For example, Alpha 140 will remove severe tarnish almost upon contact; therefore, the immersion time need not exceed 2 seconds. These cleaner/surface conditioners are acidic formulations. Therefore, thoroughly wash all devices which have been cleaned with a cleaner/surface conditioner in cold water. A hot water wash will cause undue etching of the surface of the silver plating. A post rinse in deionized water is advisable.

CAUTION: These cleaner/surface conditioners may etch exposed glass and may have a detrimental effect upon the glass filled encapsulating epoxies used in optoelectronic devices. Complete immersion of an optoelectronic device into a surface conditioner solution is NOT recommended. For best results, immerse only the tarnished leads and do not expose the encapsulating epoxy to the solutions.

The cleaning of printed circuit boards after soldering is important to remove ionic contaminants and increase circuit reliability. When a Type RMA or Type RA flux is used, vapor clean with an azeotrope of fluorocarbon F113 and approximately 15% alcohol by weight. Some equivalent products are Allied Chemical Genesolve DI-15/DE-15, Blaco-Tron DE-15/DI-15 and Arklone K. A Type RMA or Type RA flux is a mixture of basic Type R rosin flux and an organic acid. The fluorocarbon F113 removes the residual rosin and the alcohol removes the residual active ions. Room temperature cleaning may be accomplished by using Freon T-E35, T-P35 or equivalent. When a Type AC flux is used, wash thoroughly with water. Specific cleaning processes are suggested in the soldering process section.

SOLDERING PROCESS

Before the actual soldering begins, the printed circuit boards and components to be soldered should be free of dirt, oil, grease, finger prints and other contaminants. Fluorinated cleaners such as Freon T-P35 may be used to preclean both the printed circuit boards and LED devices. Operators may wear cotton gloves to prevent finger prints when loading components into the printed circuit boards.

If the silver lead frames have acquired an unacceptable layer of tarnish, remove this tarnish layer with a cleaner/surface conditioner just prior to soldering. Since a cleaner/surface conditioner does slightly etch the surface of the silver plating, the silver leads are now more susceptible to tarnish formation. Therefore, use a cleaner/surface conditioner only on those silver lead frame devices which will be soldered within a four hour time period. The effect of various tarnish levels on the choice of flux is discussed in the previous section.

Many of Hewlett-Packard's LED Lamps and Display products have a soldering specification of 230°C (446°F) for a maximum time period of 5 seconds. Therefore, in a flow solder operation adjust the solder temperature and belt speed to conform to this specification, or as is specified on the device data sheet. The flow solder operation may now proceed in a normal fashion. For best results, any one single lead should be immersed in molten solder for as short a time period as possible. At a solder

temperature of 230°C (446°F), Sn60 solder will dissolve silver at the rate of 60 microinches per second. Therefore, with an initial silver plating thickness of 100 microinches, an immersion time of 2 seconds will completely dissolve the silver plating. At a solder temperature of 260°C (500°F), Sn60 solder will dissolve silver at the rate of 80 microinches per second. These dissolving rates decrease as the silver content increases in the molten solder bath.

Post cleaning of soldered assemblies when a type RMA or Type RA flux has been used may be accomplished via a vapor cleaning process in a degreasing tank, using an azeotrope of fluorocarbon F113 and alcohol as the cleaning agent. A recommended method is a 15 second suspension in vapors, a 15 to 30 second spray wash in liquid cleaner, and finally a one minute suspension in the vapors. When a water soluable Type AC flux such as Alpha 830 or Kester 1429/1429F is used, the following post cleaning process is suggested: thoroughly wash with water, neutralize using Alpha 2441 or Kester 5760 or Kester 5761 foaming, then thoroughly wash with water and air dry.

CAUTION: The use of tetrachloro-di-fluoroethane (F112), acetone, trichloroethylene, MEK, carbon tetrachloride and similar solvents as cleaning agents is NOT recommended, as these cleaners will attack or dissolve the epoxies used in optoelectronic devices.

A WORD ABOUT PRINTED CIRCUIT BOARDS

Printed circuit boards, either single sided, double sided or multilayer, may be manufactured with plated through holes with a metal trace pad surrounding the hole on both sides of the printed circuit board. The plated through hole is desirable to provide a sufficient surface for the solder to wet, and thereby be pulled up by capillary attraction along the lead through the hole to the top of the printed circuit board. This provides the best possible solder connection between the printed circuit board and the leads of the LED device.

SOLDERED LEADS

Figure 1 illustrates an ideally soldered lead. The amount of solder which has flowed to the top of the printed circuit board is not critical. A sound electrical and mechanical joint is formed.

Figure 2 illustrates a soldered lead which is undesirable.

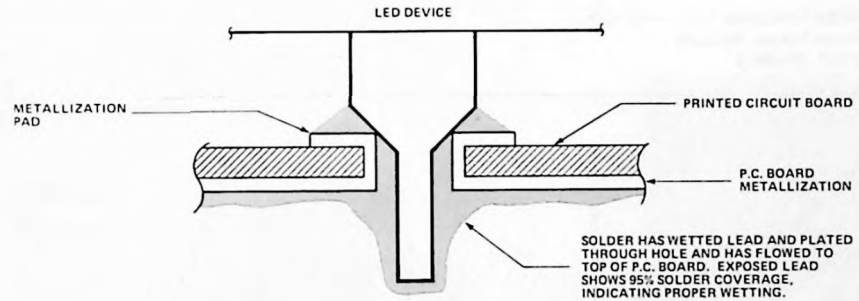


Figure 1. Ideally Soldered Lead

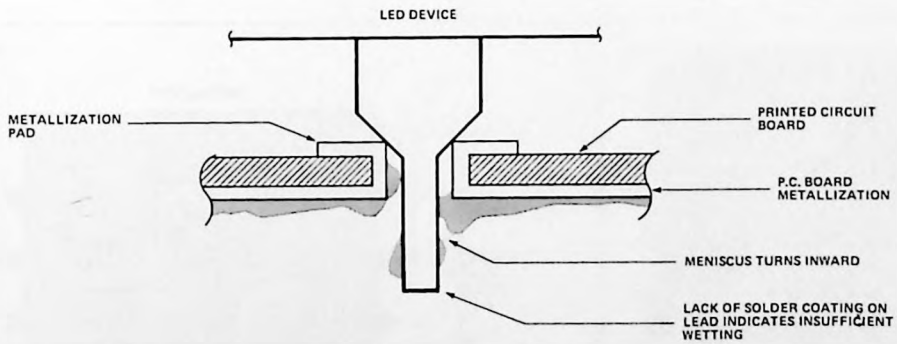


Figure 2. Undesirable Soldered Lead

LIST OF MANUFACTURERS

Alpha Metals, Inc.
56 G Water Street
Jersey City, New Jersey 07304
(302) 434-6778

London Chemical Co. (Lonco®)
240 G Foster
Bensenville, Illinois 60106
(312) 287-9477

E.I. DuPonte De Nemours & Co.
Freon Products Division
Wilminton, Delaware 19898
(302) 774-8341

Frank Curran Co. (Petroleum Napthalene Mothballs)
8101 South Lemont Road
Downers Grove, Illinois 60515
(312) 969-2200

Kester Solder Co.
4201 G Wrightwood Avenue
Chicago, Illinois 60639
(312) 235-1600

Allied Chemical Corporation
Speciality Chemicals Division
P.O. Box 1087R
Morristown, New Jersey 07960
(201) 455-5083

Baron-Blakeslee (Blaco-Tron)®
1620 S. Laramie Avenue
Chicago, Illinois 60650
(312) 656-7300

Imperial Chemical Industries, Ltd. (Arklone)®
Imperial Chemical House, Millbank
London SW1P3JF, England

REFERENCES

Manko, Howard H. *Solders and Soldering.* New York: McGraw-Hill, 1964.

Coombs, Clyde F. *Printed Circuits Handbook. New York: McGraw-Hill, 1964.*

Flaskerud, Paul and Rick Mann. "Silver Plated Lead Frames for Large Molded Packages," IEEE Catalog No. 74CH0839-1PHY (1974), pp. 211-222.

HEWLETT PACKARD

APPLICATION BULLETIN 60

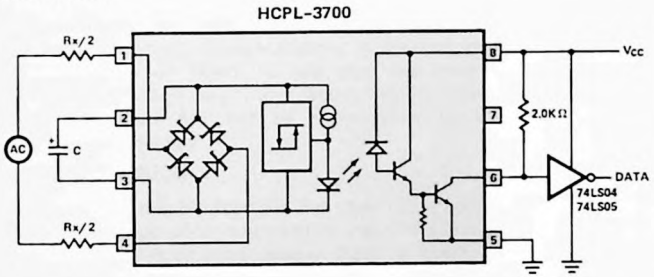
Applications Circuits for HCPL-3700 and HCPL-2601

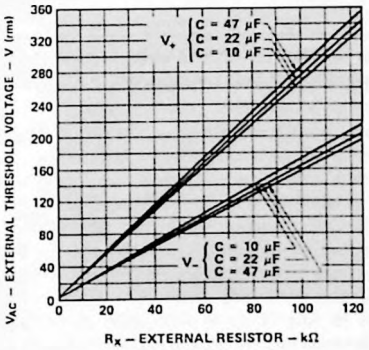
The HCPL-3700 and HCPL-2601 are versatile members of HP's High Performance Optocoupler family. The following circuits will help you start using HP Optocouplers.

THRESHOLD SENSING INTERFACE OPTOCOUPLER — HCPL-3700

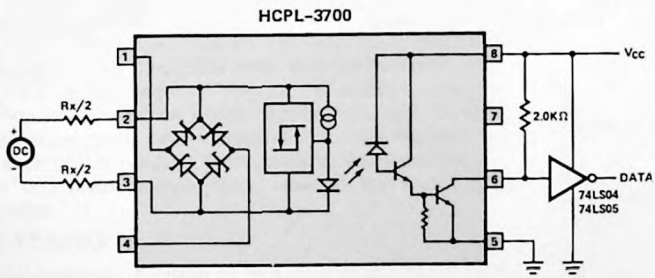
- Programmable Sense Voltage with Hysteresis
- LSTTL and CMOS Compatible Output
- AC or DC Input
- Recognized under the Components Program of Underwriters Laboratories, Inc. (File No. E55361)

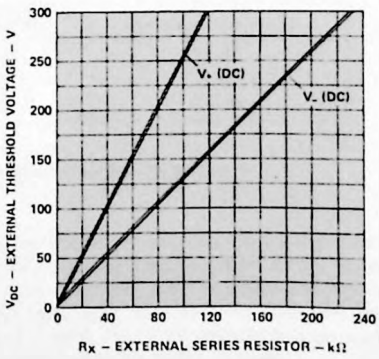
AC INPUT





DC INPUT



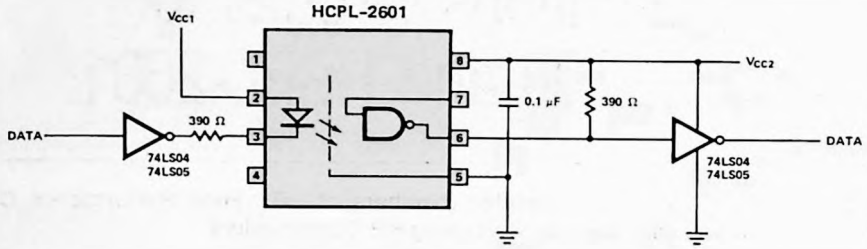


For additional information see HP Application Note 1004.

APPLICATIONS

LSTTL TO LSTTL OPTOCOUPLER INTERFACE — HCPL-2601

- **10 MBaud Speed Typical**
- **Shield provides 1 KV/μs Common Mode Noise Immunity**
- **Low Input Current Required: 5 mA**
- **Recognized under the Components Program of Underwriters Laboratories, Inc. (File No. E55361)**



Other HP single channel logic compatible optocouplers are 6N136, 6N137, 6N138, HCPL-2200, and HCPL-2503. Dual channel logic compatible optocouplers are HCPL-2531, HCPL-2630, and HCPL-2700.

For additional optocoupler applications consult the HP Optocoupler Selection Guide.

HEWLETT PACKARD

APPLICATION BULLETIN 64

Mechanical and Optical Considerations for the 0.3" Microbright Seven-Segment Display

INTRODUCTION

The need to conserve space in electronic instruments has increased drastically in the drive to design more compact, more portable equipment. Hewlett-Packard has facilitated the saving of space in the design of front panels with the introduction of the Microbright, Hewlett-Packard's new HDSP-7300/-7400/-7500/-7800 series compact 0.3" seven segment displays. Smaller than the conventional 0.3" device, the Microbright requires less space without sacrificing display height and is also Hewlett-Packard's most sunlight viewable seven segment display.

This application bulletin deals with several issues in the use of the Microbright. Optical filtering is covered, with recommendations on filters to use over the devices. Adjusting the package height and recommended sockets are also presented, followed by a discussion on the brightness of the display.

PACKAGE DESIGN

The package of the Microbright has been designed to optimize device operation and ease of use. The package requires a smaller front panel area of 0.300" x 0.500", as opposed to the 0.400" x 0.750" area of the conventional 0.3" device, so that it is ideal for applications with tight space constraints. The gray package yields higher color contrast between the package and the "on" segments and therefore provides a more visible display in sunlight viewable applications than red, yellow, or green colored packages. Moreover, mitered segments have made the character font compatible with Hewlett-Packard's 0.56" and 0.8" seven segment displays. In addition, the efficiency of the cavities which "stretch" the light to make each segment has been increased so that the light emitted by each LED is used more efficiently for a brighter display. For brightness comparisons, refer to the section on Sterance.

FILTERING

The Microbright is similar to HP's other stretched segment products; hence, recommended filtering techniques are the same. For indoor ambient lighting, refer to Application Note 1015, Table 2. For bright ambients, a 15-20% transmission filter is recommended, such as Gray 15 by Panelgraphic, or Plexiglas 2370 (Bronze) or 2538 (Gray), both by Rohm and Haas. Another alternative is a louvered filter, such as 3M's Louvered Light Control Film ND0220; however, the designer should remember that any louvered filter restricts viewing angle in the vertical direction. For more information, refer to Application Note 1015.

PACKAGE HEIGHT ADJUSTMENT

The package height to the seating plane of the Microbright is 6.09 mm (0.240 in.). This dimension is the same as that of the conventional 0.3" display to allow retrofits in existing designs. It also makes the Microbright compatible with other display elements, such as light bars and bar graph arrays. If a taller height is required to elevate the display to a position closer to the filter, spacers may be used to elevate the display. Bivar, Inc. manufactures plastic spacers which will fit the 0.200 inch row-to-row spacing to slip over two pins (one from each row) such that two spacers should be used for each digit, one at each end of the package. Figure 1 shows elevation height by part number.

Bivar Part No.	Elevation Height (In.)
360-200	0.030
361-200	0.060
362-200	0.090

Figure 1. Spacer Height vs. Part Number

In the event that the display must be elevated a significant distance, the user may find that the lead length is too short. In this case, the user may position the spacer between a socket (preferably wire-wrap for sufficient lead length) and the PC board. For recommendations on socketing, refer to Socketing section in this bulletin.

SOCKETING

Standard DIP sockets which have the 0.200" row-to-row spacing are available from a number of socket manufacturers. Circuit Assembly offers solder tail and wire-wrap bifurcated pin sockets with tin or gold plated finish. The base part number is CA-10S-TSD, which is a solder tail socket with tin-over-copper finish and phosphor bronze contacts. Three different wire-wrap lead lengths as well as heat-treated beryllium copper contacts are other offered features. These sockets are 0.300" high to the seating plane.

Another vendor, Aries Electronics, Inc., offers the same sockets with much the same options with either collet (P/N 10-2513-10) or bifurcated (P/N 10-2511-10) contacts. The collet contact version has a seating plane height of 0.17". In addition, Aries makes right angle sockets: use part number 10-2820-90 for bifurcated contacts; for collet contacts, add "C" to part number. Another option is to use strip sockets, which are made by most socket manufacturers.

STERANCE

The brightness perceived by the human eye may quantitatively be defined as luminous sterance, Lv. Sterance, unlike intensity, takes into account the area which radiates the light energy. Thus, sterance is basically the luminous intensity of the device, Iv, divided by the light-emitting area, A:

$$Lv\ (cd/m^2) = \frac{Iv\ (candela)}{A\ (metre^2)}$$

This means that given two identical light-emitting areas, the first with twice the intensity of that of the second, the first would appear twice as bright. Another approach is that for the same intensity, if the first has half the area of that of the second, the energy is distributed over a smaller area and therefore appears twice as bright.

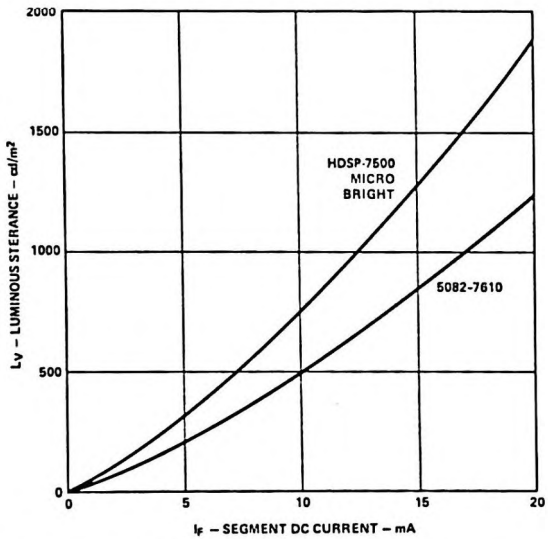


Figure 2. Typical Luminous Sterance vs. Forward DC Current

If the faces of both displays are studied, it can be observed that, due to the character design, the light-emitting area of the Microbright is 20% smaller than the area of the conventional 0.3" display. This means that a more visible display is obtained with the same amount of drive current, or that for the same intensity there is a savings in power required to drive the display.

Figure 2 shows typical luminous sterance as a function of DC forward current for both devices. From this graph it is obvious that the 20% reduction in area does not account for the observed sterance improvement of about 50%. Hewlett-Packard has improved the cavity efficiency of the Microbright to increase the light emitted from the display; this better cavity efficiency accounts for the additional 30% gain in sterance. The net result is that use of the Microbright yields a brighter, more readable display without additional power consumption.

VENDOR NAMES AND ADDRESSES

Spacers

Bivar, Inc.
4 Thomas
Irvine, CA 92714
(714) 951-8808

Sockets

Aries™ Electronics, Inc.
P.O. Box 130
Frenchtown, NJ 08825
(201) 996-6841

Circuit Assembly Corporation
3169 Red Hill Avenue
Costa Mesa, CA 92626
(714) 855-7887

Filters

Chequers Engraving, Ltd.
1-4 Christina Street
London EC2A 4PA
01-779-6964/5

Panelgraphic Corporation
10 Henderson Drive
West Caldwell, NJ 07006
(201) 227-1500

Rohm and Haas
Independence Mall West
Philadelphia, PA 19105
(215) 592-3000

3M Company
Industrial Optics
Carbonless/Related Products Division
225-35 3M Center
St. Paul, MN 55144
(612) 733-4403

HEWLETT PACKARD

APPLICATION BULLETIN 65

Using 50/125 μm Optical Fiber with Hewlett-Packard Components

INTRODUCTION

In some applications, 50/125 μm size optical fiber may be more advantageous to use than 100/140 μm size optical fiber. 100/140 μm fiber is used primarily in the local data communications area where link lengths typically run anywhere from 500 metres to 2000 metres. 100/140 μm fiber, having a larger core diameter, is easier to launch light into but the attenuation per unit length is higher than the 50/125 μm. The 50/125 μm fiber, having a lower attenuation per unit length, is used more in the telecommunications area where links typically run several kilometres.

Tests were made with three HP metal packaged fiber optic transmitters using 50/125 μm fiber, and this application bulletin documents those test results to aid in designing a fiber optic system using 50/125 μm fiber. Use of this bulletin in conjunction with the HP Optoelectronics Designers Catalog and Application Note 1000, "Digital Data Transmission with the HP Fiber Optic System", is suggested to help in understanding, in more detail, the design parameters required to determine typical transmission distance.

A fiber optic system is defined as a transmitter, receiver, cable and connectors as shown in Figure 1.

In constructing a system, there are optical and mechanical losses incurred at the transmitter to connector interface, the connector to receiver interface, and there is also the steady state cable attenuation which contributes to losses. In using 50/125 μm size fiber with HP components, as will be shown, most of the coupling losses occur at the transmitter to connector interface. This is where tests were made, to determine what the typical losses are. Using the data from these tests, a full system performance can be predicted.

In designing a fiber optic system, concern must be taken to ensure enough optical power will reach the receiver for it to operate correctly. The following equation is used to predict losses and an expected link length. The equation applies to any fiber optic system design.

THE OPTICAL POWER BUDGET

$$10 \text{ Log } \frac{\Phi T}{\Phi R} \geq \alpha_o \ell + \alpha_{TC} + \alpha_{CR} + \alpha_M \qquad (1)$$

The optical power ratio should be greater than or equal to the system losses.

ΦT = Optical power available from the transmitter (μW)

ΦR = Minimum optical power required by the receiver (μW)

$10 \text{ Log } \frac{\Phi T}{\Phi R}$ = Optical power ratio (dB)

System Losses:

- $\alpha_o \ell$ = Steady state fiber loss (dB/km · length)
- α_{TC} = Transmitter to connector coupling loss (dB)
- α_{CR} = Connector to receiver coupling loss (dB)
- α_M = Optical power margin (set by user, should be > 1 dB)

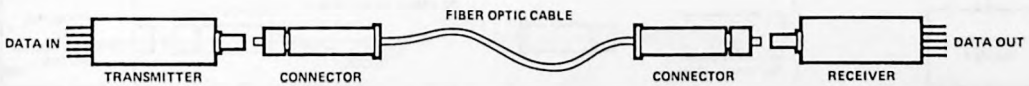
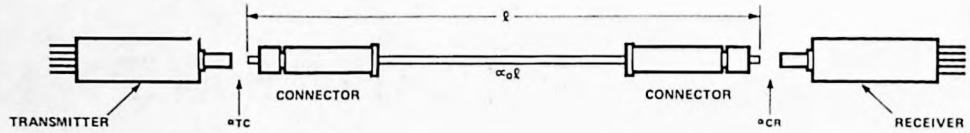


Figure 1. A Fiber Optic System

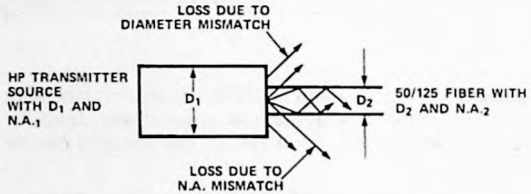
APPLICATIONS

WHERE THE LOSSES OCCUR



In a fiber optic link using HP transmitters/receivers and 50/125 μm fiber, all HP transmitters have a larger source area and larger N.A. than the 50/125 μm fiber. Therefore a large optical loss is obtained at the transmitter/connector interface.

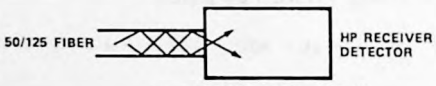
HP receivers have a larger detecting area and larger N.A. than the 50/125 μm fiber, therefore all light is accepted into the receiver and the only optical loss is due to Fresnel loss which is about 0.17 dB. The diagrams below illustrate the calculations required to predict the optical losses across each interface.



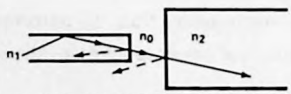
$$\alpha_{TC} = 20 \text{ Log } \frac{D_1}{D_2} + 20 \text{ Log } \frac{\text{N.A.}_1}{\text{N.A.}_2} + \text{Fresnel loss} \qquad (2)$$

Loss due to diameter mismatch (See Note 1).

Loss due to effective N.A. mismatch



α_{CR} = FRESNEL LOSS ≈ 0.17 dB



FRESNEL LOSS RESULTS FROM PARTIAL REFLECTION AT BOUNDARY OF CHANGE IN REFRACTIVE INDEX, n.

Note:
1. D_1, D_2, N.A.$_1$, N.A.$_2$ can be obtained from their respective data sheets.

Empirical tests were performed with the 50/125 μm fiber optic cable specified in Table 3. The cable was cut into two 1 metre lengths and connected on both ends with identical connectors listed in Table 1.

Table 1. Connectors Used in Test

Amphenol 906-120-5001	HP style thread
Amphenol 906-110-5017	SMA style thread

These connectors are commonly used for 50/125 μm optical fiber. The cable was connectored according to the procedures documented with each connector when purchased.

Upon connectoring, an epoxy having a greater index of refraction than the fiber cladding was used. This removed light from the cladding and allowed light to be measured within the core only (i.e. the fiber was mode stripped).

The links were connected to random samples of HP transmitters and optical power was measured at the end of the 1 m links while driving the transmitters at various currents. Figure 2 shows the test set up.

Before empirical tests were performed, theoretical data was calculated to determine losses, using data from the HP transmitter data sheets and data from the specific cable used.

Table 2 lists the HP transmitters used in the tests.

Table 2. HP Transmitters Tested

Transmitter
HFBR-1002
HFBR-1203
HFBR-1204

Table 3 lists the specifications of the 50/125 μm fiber used in the tests.

Table 3. Test Cable Specifications

Core Diameter	50 μm
Outside Cladding Diameter	125 μm
Numerical Aperture, N.A.,	0.21
Attenuation at λ = 820 nm, α_o,	4.09 dB/km
Index Grading Coefficient, g,	2

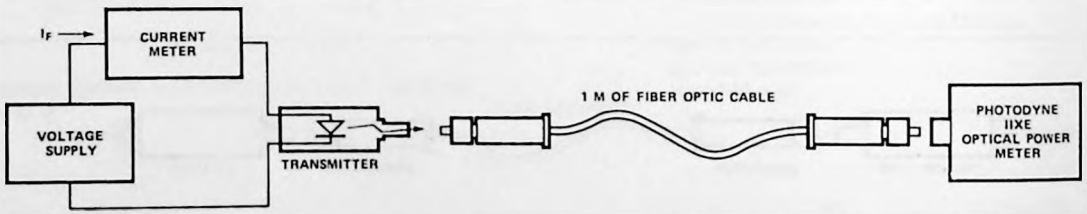


Figure 2. Test Set Up

An example theoretical calculation to determine optical power out of a 1 metre of cable is shown below using the HFBR-1002 transmitter and the 50/125 μm fiber. Optical power out of the transmitter (ΦT) minus the transmitter to connector coupling loss (α_{TC}) minus the attenuation of ℓ = 1 m of cable ($\alpha_o\ell$) equals the optical power out of 1 metre of cable (Φ1m).

$$\Phi 1m = \Phi T - \alpha_{TC} - \alpha_o \ell \quad (3)$$

ΦT = −12.5 dB

Typical, from HFBR-1002 data sheet (including 1.5 dB fixed coupling loss)

α_{TC} = 9 dB

$$= 20 \text{ Log } \frac{100}{50} + 20 \text{ Log } \frac{0.3}{0.21}$$

D_1 = 100 μm, N.A.$_1$ = 0.3 for HFBR-1002
D_2 = 50 μm, N.A.$_2$ = 0.21 for the 50/125 μm fiber
Fresnel loss is included in the 1.5 dB fixed coupling loss.

Φ1m = −12.5 dB - 9 dB - [4.09 dB/km (0.001 km)] = −21.5 dB

Knowing ΦR (from HFBR-2001 receiver data sheet) and using the equation below, a link length can be predicted.

$$\Phi 1m - \alpha_{CR} - \alpha_o \ell \geq \Phi R$$

$$\ell = (-\Phi R + \Phi 1m - \alpha_{CR})/\alpha_o \quad (4)$$

ΦR = −30.9 dB minimum from HFBR-2001 data sheet

α_{CR} = 0.17 dB

ℓ = (30.9 dB - 21.5 dB - 0.17 dB)/4.09 dB/km
ℓ = 2.25 km

Typical link lengths using each T/R pair can be obtained from Figures 4, 5, and 6.

For each transmitter, measured and typical data sheet values of Φ1m are listed in Table 4.

Included in the test results is information on the expected performance of each T/R pair using HP 100/140 μm size fiber.

A review of the data will confirm the following points when comparing the performance of HP T/R pairs with 100/140 μm and 50/125 μm size fibers:

- Φ1m is reduced by approximately 10 dB when using 50/125 μm fiber
- Link distance will be longer with 100/140 μm fiber

The graphs (Figures 4, 5, and 6) allow the designer to predict the optical power available from a given fiber at a specific length, for typical transmitters.

Typical links lengths can be obtained by noting where the slope of the fiber attenuation line crosses the receiver sensitivity and extrapolating down.

Table 4. Test Results

Transmitter	Cable/Connector [Note 2]	Φ1m (Measured)	Φ1m (Data Sheet Typical)	Link Length, m [Note 4]	Conditions [Note 3]
HFBR-1002	100/140 μm/ HFBR-4000	−10.5 dBm 89 μW	−12.5 dBm 56 μW	3.6 k	T = 25°C V_{CC} = 5 V I_F = 83.6 mA
	50/125 μm/ Amphenol 906-120-5001	−20.3 dBm 9.3 μW	−21.5 dBm 7.1 μW	2.5 k	
HFBR-1203	100/140 μm/ HFBR-4000	−8.6 dBm 138 μW	−7.4 dBm 182 μW	3.1 k	T = 25°C I_F = 100 mA
	50/125 μm/ Amphenol 906-120-5001	−19.0 dBm 12.6 μW	−19.3 dBm 11.7 μW	1.7 k	
HFBR-1204	100/140 μm/ OFT1 455B (SMA Style)	−8.5 dBm 141 μW	−7.4 dBm 182 μW	3.1 k	T = 25°C I_F = 100 mA
	50/125 μm/ Amphenol 906-110-5017	−17.2 dBm 19.3 μW	−19.3 dBm 11.7 μW	2.1 k	

Notes:
2. The attenuation of the 100/140 μm fiber used = 5.5 dB/km. The attenuation of the 50/125 μm fiber used = 4.09 dB/km.
3. Tests were made at ambient temperature of 25°C. For guaranteed operation at −40°C ≤ T ≤ 85°C, see HP Optoelectronics Designers Catalog for transmitter and receiver data sheets.
4. Link lengths are predicted using eq. 4, the measured value of Φ1m, and the appropriate HP receiver and cable. See Figures 4, 5, and 6 for graphical representation.

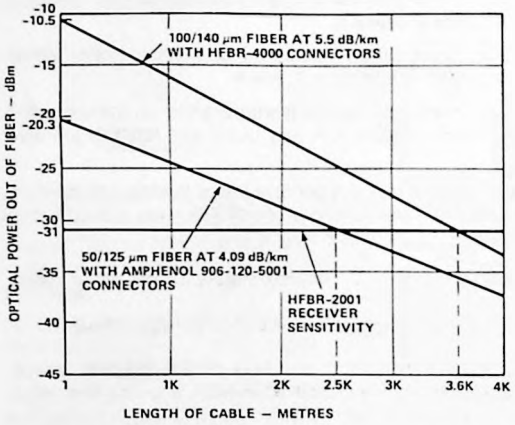


Figure 4. Expected Optical Power out of a Given Length of Cable Using the HFBR-1002 Transmitter

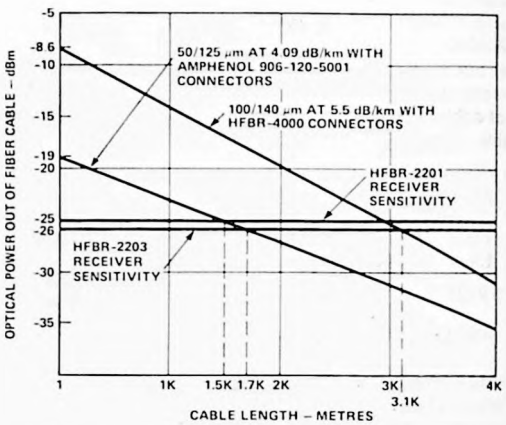


Figure 5. Expected Optical Power out of a Given Length of Cable Using the HFBR-1203 Transmitter

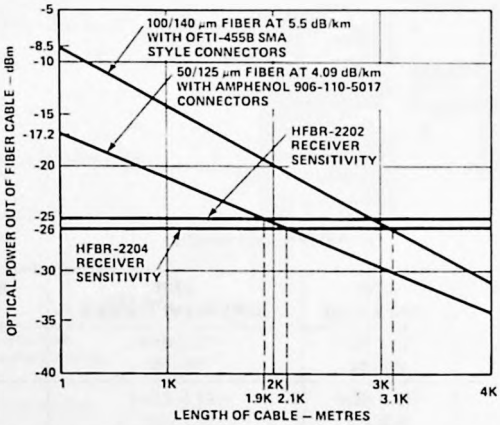


Figure 6. Expected Optical Power out of a Given Length of Cable Using the HFBR-1204 Transmitter

Note: All graphs are constructed from measured values.

HEWLETT PACKARD

APPLICATION BULLETIN 69

CMOS Circuit Design Using Hewlett-Packard Optocouplers

INTRODUCTION

The purpose of this bulletin is to provide the CMOS designer with a set of useful interface circuits incorporating Hewlett-Packard optocouplers. HP offers a wide variety of optocouplers suitable for use in the low current, low power CMOS design environment. Typical applications include logic system isolation, ground loop elimination, logic level translation, microprocessor system interface, computer-peripheral interface, and line receiver applications.

HEWLETT-PACKARD CMOS COMPATIBLE OPTOCOUPLERS

The HCPL-2300 optocoupler (Table 1, Figure 1) offers the unique combination of low LED operating drive current of 0.5 mA at a 5 MBd data rate. Power supply voltage is rated at +7 V max and the open collector output is rated at +18 volts. A 1K Ω internal pull-up resistor eliminates the need for an external pull-up resistor, if so desired. An internal shield, which shunts capacitively coupled common mode noise to ground, improves common mode transient immunity.

The HCPL-2200 optocoupler (Table 1, Figure 2) has +20 V maximum power supply and output voltage ratings. At a drive current of 1.6 mA, a 2.5 MBd data rate is achievable. The HCPL-2200 also features the internal shield to improve common mode transient immunity.

The 6N139 optocoupler (Table 1, Figure 3) has a low input drive current requirement of 0.5 mA, as well as +18 V power supply and output voltage capabilities. The data rate can be increased to 100 KBd by connecting a 51KΩ emitter-base bypass resistor between pins 5 and 7. This resistor provides an alternate path for output current to flow, which shortens transition times and effectively increases data rate capability.

The HCPL-2731 optocoupler (Table 1, Figure 4) performs as a dual channel version of the 6N139 and features an internal emitter-base bypass resistor. The power supply and output voltages are also rated at +18 V max.

RECOMMENDED CIRCUIT DESIGNS

The shunt drive interface circuit (Table 1, Figure 5) provides optimal speed performance, protection against leakage current through the LED, and reduced common mode influences associated with switching a floating LED. The diode, D1, is required for active devices to ensure that the drive current originates from the power supply and not the device output. The low forward voltage of the diode, D1, ensures that the LED remains off when the driver switches low. The capacitor, C_P, can be used with the HCPL-2300 to correct pulse width distortion by substantially delaying the turn-on time of the LED while leaving the turn-off time nearly the same.

The active CMOS series drive (Table 1, Figure 6) does not require a diode, thus saving the designer one component. The capacitor, C_P, functions as a peaking capacitor by effectively dumping charge to and from the HCPL-2300 LED when switching. This circuit, however, does not provide protection from leakage current and its switching action is slightly slower due to the total interruption of current rather than the re-direction of it as seen in the shunt drive circuit.

The open collector LSTTL/TTL series drive interface circuit (Table 1, Figure 7) also provides leakage current protection. The resistor, R_2, shunts up to 250 μA of leakage current away from the optocoupler input terminals, protecting the LED from undesired conduction when the driver output transistor is in the off state.

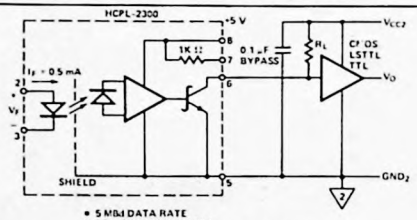
On the output side, a pull-up resistor is required for use with the open collector HCPL-2300, 6N139, and HCPL-2731. A pull-up resistor is recommended for use in CMOS designs with the HCPL-2200 to improve data rate, but is optional due to the device's three-state output.

The circuit parameters of Table 1 were obtained with low power dissipation as the main design objective, in keeping with CMOS characteristics. However, data rate capability can be improved with increased I_F and I_O. When R_I and R_L are decreased in value, the respective RC time constants which correspond to the input and output circuitry decrease to an optimum value. This yields faster transition times, lower pulse width distortion and higher data rate capability at the expense of greater power dissipation.

To choose an optocoupler and drive circuit suitable for a particular application, the designer should select the optocoupler which best matches the data rate and input current requirements. Then, a drive circuit can be chosen: shunt drive is recommended for speed and leakage current protection; series drive is recommended if the designer wants to minimize the number of components. The individual component values are then selected according to the power supply voltages indicated in Table 1.

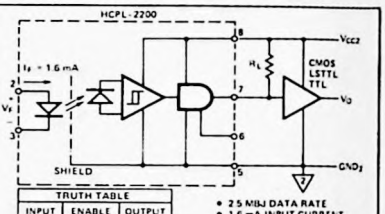
Table 1. Optocoupler Circuit Configurations for use in CMOS Circuit Design

OPTOCOUPLERS



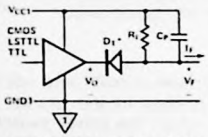
- 5 MBd DATA RATE
- 0.5 mA INPUT CURRENT
- INTERNAL SHIELD FOR GUARANTEED COMMON MODE REJECTION
- OPTIONAL INTEGRATED PULL-UP RESISTOR

Figure 1. HCPL-2300



- 2.5 MBd DATA RATE
- 1.6 mA INPUT CURRENT
- THREE STATE OUTPUT

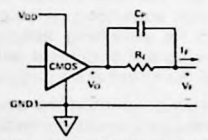
Figure 2. HCPL-2200



*DIODE D1 NOT REQUIRED FOR UNITS WITH OPEN-COLLECTOR OUTPUT

Figure 5. CMOS/LSTTL/TTL Shunt Drive Circuit

V_{CC1} (V dc)	R_I (KΩ)	C_P	D_1	V_{CC2} (V dc)	R_L (KΩ)	V_{CC1} (V dc)	R_I (KΩ)	D_1	V_{CC2} (V dc)	R_L (KΩ)
+5	6.19	20 pF	1N5711	+5	1.00 Internal	+5	2.15	1N916	+5	1.1
+10	14.7	20 pF	1N5711	+10	2.37	+10	5.11	1N916	+10	2.37
+15	21.5	20 pF	1N5711	+15	3.16	+15	8.25	1N916	+15	3.83



NOTE: USE OF THIS DRIVE CIRCUIT WILL REDUCE DATA RATE CAPABILITY BY APPROXIMATELY 20%

Figure 6. Active CMOS Series Drive Circuit

V_{DD} (V dc)	R_I (KΩ)	C_P	V_{CC2} (V dc)	R_L (KΩ)	V_{CC1} (V dc)	R_I (KΩ)	V_{CC2} (V dc)	R_L (KΩ)
+5	5.11	20 pF	+5	1.00 Internal			+5	1.1
+10	13.3	20 pF	+10	2.37			+10	2.37
+15	19.6	20 pF	+15	3.16	+15	7.5	+15	3.83

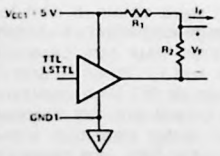


Figure 7. Open-Collector TTL/LSTTL Series Drive Circuit with Leakage Current Protection

V_{CC1} (V dc)	R_1 (KΩ)	R_2 (KΩ)	V_{CC2} (V dc)	R_L (KΩ)	V_{CC1} (V dc)	R_1 (KΩ)	R_2 (KΩ)	V_{CC2} (V dc)	R_L (KΩ)
+5	3.48	3.16	+5	1.0 Internal	+5	1.33	3.16	+5	1.1
			+10	2.37				+10	2.37
			+15	3.16				+15	3.83

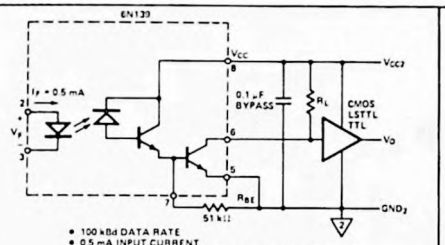


Figure 3. 6N139

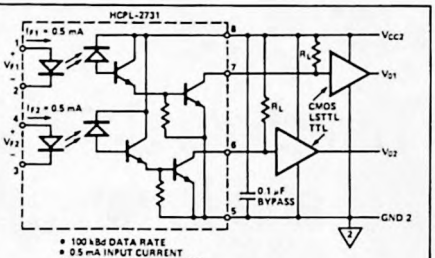


Figure 4. HCPL-2731

V_{CC1} (V dc)	R_I (KΩ)	D_1	R_{BE} (KΩ)	V_{CC2} (V dc)	R_L (KΩ)
+5	6.81	1N916	51.0	+5	1.1
+10	16.2	1N916	51.0	+10	2.37
+15	26.1	1N916	51.0	+15	3.83

V_{CC1} (V dc)	R_I (KΩ)	D_1	V_{CC2} (V dc)	R_L (KΩ)
+5	6.81	1N916	+5	1.1
+10	16.2	1N916	+10	2.37
+15	26.1	1N916	+15	3.83

V_{CC1} (V dc)	R_I (KΩ)	R_{BE} (KΩ)	V_{CC2} (KΩ)	R_L (KΩ)
+5	6.19	51.0	+5	1.1
+10	16.2	51.0	+10	2.37
+15	23.7	51.0	+15	3.83

V_{CC1} (V dc)	R_I (KΩ)	V_{CC2} (V dc)	R_L (KΩ)
+5	6.19	+5	1.1
+10	16.2	+10	2.37
+15	23.7	+15	3.83

V_{CC1} (V dc)	R_1 (KΩ)	R_2 (KΩ)	R_{BE} (KΩ)	V_{CC2} (V dc)	R_L (KΩ)
+5	3.16	3.16	51.0	+5	1.1
				+10	2.37
				+15	3.83

V_{CC1} (V dc)	R_1 (KΩ)	R_2 (KΩ)	V_{CC2} (V dc)	R_L (KΩ)
+5	3.16	3.16	+5	1.1
			+10	2.37
			+15	3.83

HEWLETT PACKARD

APPLICATION NOTE 915

Threshold Detection of Visible and Infrared Radiation with PIN Photodiodes

Traditionally, the detection and demodulation of extremely low level optical signals has been performed with multiplier phototubes. Because of this tradition, solid-state photodetectors are often overlooked even though they have a number of clear functional advantages and in some applications provide superior performance as well. Some of these advantages are summarized below and become even more apparent in the following discussion.

ADVANTAGES OF PIN PHOTODIODES VERSUS MULTIPLIER PHOTOTUBES

1. Size and weight:
   PIN photodiodes are approximately three orders of magnitude smaller and lighter. This greatly simplifies and reduces the cost of mounting.
2. Power Supply:
   Multiplier phototubes require more than 1000 volts, which must be precisely regulated and divided among the dynodes. By comparison, PIN photodiodes and associated amplifiers operate stably on less than 20 volts, which does not require precise regulation.
3. Cost:
   The cost, including that of the necessary amplifier, is lower for the PIN photodiode because of lower power supply requirements.
4. Spectral Response:
   Broad skirts of the PIN photodiode make it useful from the ultra-violet, through the visible, and well into the infrared region. This exceeds the range of any other device of comparable sensitivity.
5. Sensitivity:
   Noise equivalent power of the PIN photodiode is lower than that of any other type of photodetector. The signal levels are extremely low, however, and to achieve low level performance they require a high gain, high input resistance amplifier. Multiplier phototubes have built-in gain and do not require additional low-noise amplification. Moreover, the high input resistance needed for sensitive performance precludes fast response, whereas the response time of multiplier phototubes may be in the nanosecond region even in the sensitive mode.
6. Stability:
   The characteristics of noise, responsivity, and spectral response of the PIN photodiode are not dependent on time, temperature, or other environmental considerations. The same conditions may be hazardous to multiplier phototubes.
7. Overloading:
   In the presence of excessive signal, multiplier phototubes of comparable sensitivity are capable of destroying themselves as a result of excessive output current. The PIN photodiode is unaffected by exposure to room light or even direct sunlight.
8. Ruggedness:
   PIN photodiodes can tolerate exposure to extreme levels of shock and vibration. Typical shock capability is 1500 G's for 0.5 millisecond.
9. Magnetic Fields:
   Multiplier phototube gain is affected by fields as small as one gauss. If the interfering field is fluctuating, the output will be modulated by it. The PIN photodiode is insensitive to magnetic fields.
10. Precision:
    The responsivity of the PIN photodiode is inherently precise and repeatable. Within a given type, the characteristics agree (from unit to unit) within plus or minus 0.1 decade. Responsivity of multiplier phototubes may vary over more than a decade from one unit to another.
11. Sensitive Area:
    The small sensitive area of the PIN photodiode makes it unnecessary to establish an aperture which may be required for some applications. However, in some applications good optical alignment is imposed by the small area.

PIN PHOTODIODE DETECTORS

At the present time a variety of different types of solid-state photodetectors are available. Of these, the Silicon PIN Photodiode has the broadest applicability and is the subject of this note. The PIN photodiode's main advantages are: broad spectral response, a wide dynamic range, high speed, and extremely low noise. With appropriate terminal circuits it is well suited for many applications that require converting an optical signal to an electrical signal. The

present discussion, however, will be limited to the description of the PIN photodiode's threshold detection sensitivity and the design of suitable terminal circuits that will realize this capability.

PHOTODIODE DESCRIPTION

Construction

A brief description of the PIN photodiode will be helpful in understanding its performance and the principles for designing appropriate circuits to be used with it. Figure 1 shows a typical construction of the PIN photodiode. This figure is for the purpose of explanation only and is not to scale. The relative proportions have been deliberately distorted for the sake of clarity.

The PIN structure is produced by diffusion through an oxide (S_iO_2) mask which also serves to protect the surface. Since most metals are very opaque to optical radiation, especially at infrared wavelengths, the gold contact is deposited only around the perimeter of the P-layer, and the gold contact pattern provides for lead attachment a short distance away from the junction region, so the lead is not in the light path.

Mode of Operation

When a photon is absorbed by the silicon it produces a hole and an electron. If the absorption of the photon occurs in the I-layer, as shown in Figure 1, the hole and the electron are separated by the electric field in the I-layer. For the highest quantum conversion efficiency (electrons per photon) it is desirable to have the P-layer as thin as possible and the I-layer as thick as possible. The thickness of the P-layer also determines the value of the parasitic series resistance (R_S in Figure 2). The thinner the P-layer the higher the R_S. Since R_S affects high frequency performance there is therefore a design trade-off between quantum efficiency and bandwidth. Once the trade-off is settled, the desired thickness is then controlled during the diffusion process. The effective thickness of the I-layer is controlled partly by the manufacturing diffusion process and partly by the magnitude of the electric field applied to the diode—the higher the field, the thicker will be the effective I-layer. It is therefore desirable to operate the diode with an external reverse bias, as shown in Figure 2. As the reverse bias voltage is increased from zero, there are three beneficial effects: hole and electron transit time decreases; conversion efficiency increases slightly; and most importantly, the capacitance decreases sharply with bias up to about ten volts and continues to decrease slightly up to about twenty volts reverse bias.

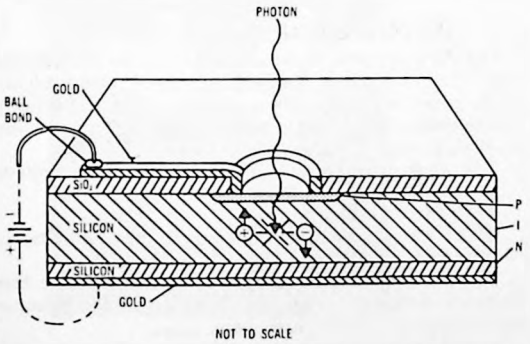


Figure 1. PIN Photodiode Cutaway View

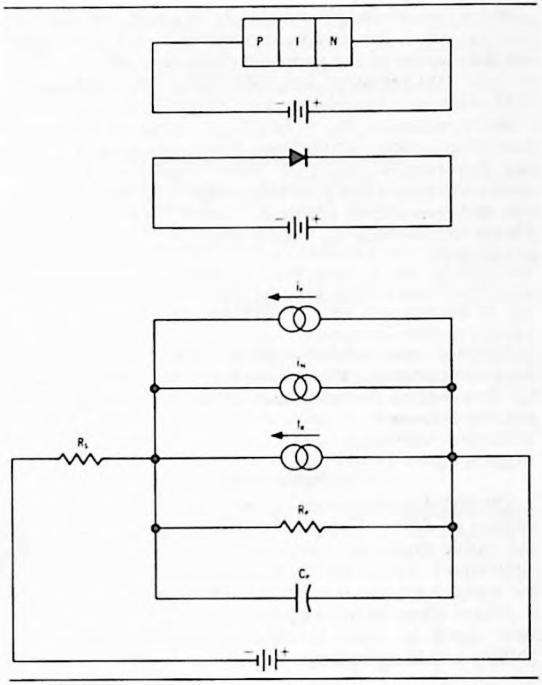


Figure 2. PIN Photodiode Schematic Symbol, and Equivalent Circuit

In the presence of optical signals there is a slight modulation of the shunt conductance as the presence of photon-produced holes and electrons in the I-layer modulate its conductivity. This effect can be quite significant at very high levels of illumination since the I-layer may become saturated, resulting in a decrease in quantum efficiency and an increase in rise time. Saturation can be prevented by applying a very high reverse bias voltage (up to 200 volts). However, such a high voltage, applied over a long period of time, may cause a degradation of the diode's leakage properties. Since our present concern is with threshold performance, reverse bias voltages greater than twenty volts need not be considered.

Equivalent Circuit

When properly biased, the PIN photodiode can be accurately represented by the equivalent circuit shown in Figure 2. Here i_p is the external current resulting when the diode is illuminated. It has a time constant of 10 picoseconds and a value of approximately 0.5 amp per watt of input at a wavelength of 8000 angstroms (800 nanometers). This corresponds to a quantum efficiency of 75%, that is, 0.75 electrons per photon. The quantum efficiency is constant from 500 nanometers to 800 nanometers (5,000 Å to 8,000 Å).

i_N is the noise current of the PIN photodiode. Since the diode is reverse biased, the shot noise formula is applicable, so that the noise current can be computed from:

$$\frac{i_N^2}{B} = 2qI_{dc} \qquad (1)$$

where B = system output bandwidth, Hz
q = electron charge, 1.6×10^{-19} coulombs
I_{dc} = dc current, Amp.

In the case of the photodiode, I_{dc} is simply the dark current, I_R, which has a value determined by the construction and dimensions of the particular diode type. Maximum values are: 100 picoamps for 5082-4204, 150 picoamps for 5082-4205 and 2 nanoamps for 5082-4203.

Shunt resistance, R_p, is very large, being usually greater than 10 gigaohms (10,000 megohms), and its noise current may therefore be neglected. Shunt capacitance, C_p, has a value from two to five picofarads, depending upon the diode type and reverse bias. For high frequency operation it is important to minimize C_p because the cutoff frequency is determined by:

$$f_c = \frac{1}{2\pi R_s C_\mu} \qquad (2)$$

Although our present concern is with low frequency threshold operation, there is another reason for minimizing C_p. This will be discussed later, when circuit design principles are presented.

Performance

Threshold performance can and has been specified in a number of different ways. The most commonly understood and usable expression takes the form of a noise equivalent input signal. This is the input signal which produces an output signal level that is equal in value to the noise level that is present when no input signal is applied. The noise equivalent input in watts is called Noise Equivalent Power (NEP) and is defined by:

$$\text{NEP} = \frac{\text{NOISE CURRENT (amps per root hertz)}}{\text{CURRENT RESPONSIVITY (amps per watt)}} \qquad (3)$$

which has the units of watts per root hertz. Devices for photo-detection could then be compared on the basis of NEP. The lower the NEP the more sensitive is the device.

Another method of defining threshold sensitivity is on the basis of signal-to-noise ratio for given input signal power levels. Taking a power level of one picowatt, for example, the signal-to-noise ratio at the output can be obtained from:

$$\text{SNR} = \frac{\text{RESPONSIVITY } \left(\frac{\text{amps}}{\text{watts}}\right) \times \text{INPUT (watts)}}{\text{NOISE CURRENT (amps)}} \qquad (4)$$

This is a ratio of currents. To express it in dB we would take twenty times its log to base ten, even though the expression converts linearly to a power ratio. This is because the devices respond *linearly* to input *power*.

Figure 3 shows spectral sensitivity characteristics of several PIN photodiodes and multiplier phototubes. Sensitivity is given in terms of SNR and NEP. The latter is in terms of dBm. Several interesting features are evident in Figure 3. Although the quantum efficiency for PIN photodiodes is constant from 500 to 800 nanometers, the sensitivity curve is not. This is due to the fact that the energy per quantum (photon) of radiant energy varies with wavelength.

The curves for the three different PIN photodiodes also show the dependence of sensitivity on leakage current. Here the highest sensitivity is obtained with the 5082-4204 which has a maximum leakage current of 100 picoamps. Next is the 5082-4205 with 150 picoamps and finally the 5082-4203 with maximum leakage of 2 nanoamps. The three curves are in effect displaced by the magnitude of the noise current difference because quantum efficiency is equal for all. These curves also show the inherent broad response of PIN photodiodes with respect to multiplier phototubes. Therefore, the power responsivity of the PIN photodiode

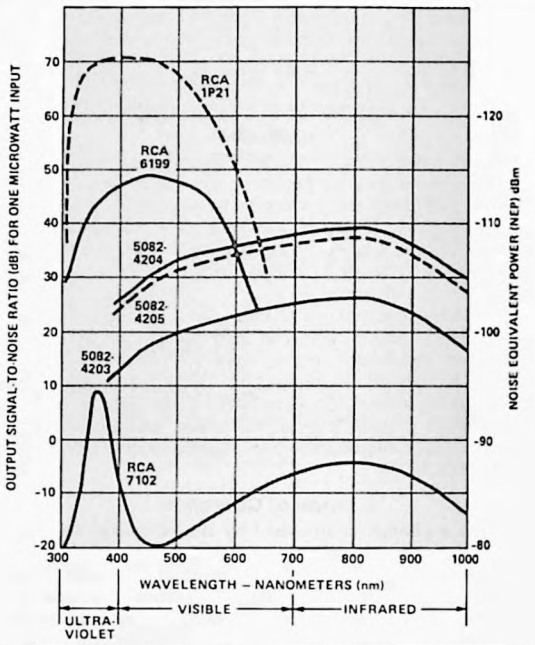


Figure 3. Spectral Sensitivity Comparisons of Photodetectors

has a corresponding slope. Notice how the inherently broad response of silicon, enhanced by the thick I-layer construction, extends the range of useful performance over the response ranges of two types of photocathodes.

Although the threshold sensitivity of multiplier phototubes is superior in the visible region, nevertheless for many applications the advantage is not significant enough to outweigh the disadvantages of generally unstable and temperature-sensitive gain, large size and weight, and the need of very high and stable power supply voltages. On the other hand, the superior red and infrared threshold performance of the PIN photodiode does not necessarily mean it is better in any application, because one must take into account its small sensitive area and low signal levels. Realization of the performance capability described in Figure 3 also requires fairly careful attention to the design of the terminal circuits into which the PIN photodiode operates.

TERMINAL CIRCUIT DESIGN PRINCIPLES

The design of the terminal amplifier must consider the usual design objectives of low noise, broad band, wide dynamic range, etc. In addition, there are two fundamental considerations which are dictated by the PIN photodiode:

1. High Reverse Voltage:
   The diode must be operated at ten to twenty volts of reverse bias to reduce shunt capacitance.
2. High Input Resistance:
   This is a fundamental consideration in the sensitivity/rise time trade-off.

The effects of reverse voltage on capacitance have been discussed earlier. However, the effect is sufficiently important to deserve a re-emphasis here.

A high input resistance is necessary in order to maintain a high signal-to-noise ratio. Since the output signal from the photodiode is a current, and its own internal noise is repre-

sented by a current, it is appropriate to represent the noise of the terminal amplifier as an equivalent noise current at the input. The smallest value of resistor which may be connected to the input is then limited by its noise current according to the formula for thermal noise:

$$\frac{i_N^2 \text{ (thermal)}}{B} = \frac{4kT}{R} \qquad (5)$$

By comparing eq(1), relating diode noise current to leakage current, with eq(5), relating resistor noise current to its resistance value, it is clear that there is some value of resistance below which the NEP of the system, i.e., threshold sensitivity, would be degraded at the rate of 5 dB per decade of decreasing resistance. For example, in the case of the 5082-4203, assuming a maximum leakage current of 2 nanoamps, the value of resistance should be greater than 25 megohms, to avoid degrading the threshold sensitivity.

TRANSISTOR AMPLIFIER

In addition to keeping the input noise current low by using large values of input resistance, it is also important to keep other sources of noise in the amplifier at a minimum. Using ordinary transistors (PNP or NPN) it is not possible to approach the ultimate sensitivity of which the PIN photodiode alone is capable, even when low-noise transistors, such as the 2N2484, are used. However, in those applications where it is possible to sacrifice sensitivity for simplicity, transistors may be used. A typical transistor circuit is shown in Figure 4. With this circuit, a sensitivity corresponding to an NEP of — 95 dBm was obtained. In this case, Q1 was operated at the lowest possible collector current which would still give adequate gain. A high loop gain was desired in order to compensate, with negative feedback, for the long open-loop rise time produced by the high input resistance. A resistance higher than 10 megohms was not necessary here, since the transistor itself sets the fundamental noise limitation. A PNP transistor was selected for Q2 in order to balance out most of the base-to-emitter voltage of Q1, so that the output would tend to be near zero without any zero adjustment. A slight zero adjustment, provided by R2 and R3, gives the necessary range without appreciably attenuating the feedback current. As the photocurrent, I_2, increases, the amplifier causes the voltage at the emitter of Q3 to decrease, which causes a current in R1 to flow out of the node (base of Q1) into which I_2 flows.

Basic Amplifier Arrangements

For linear operation, the photodiode should be operated with as small a load resistance as possible. Figure 5 shows the recommended amplifier arrangement. The negative-going input is at virtual ground; the dynamic resistance seen there by the photodiode is R_1 divided by loop gain. If the op-amp has extremely high input resistance, loop gain is very nearly the forward gain of the op-amp. R_2 can be omitted if the photocurrent is reasonably high — its purpose is only to balance off the effect of offset current. As shown, the output voltage will rise in response to the optical signal. If it is preferable to have the output drop in response to optical input, then *both* the photodiode *and* E_C should be reversed. E_C may, of course, be zero. Speed of response is usually limited by the time constant of R_1 with its own capacitance, so it is improved by using a string of two or more resistors in place of a single R_1.

Logarithmic operation requires the highest possible load resistance — at least 10GΩ. With an FET-input op-amp, this is

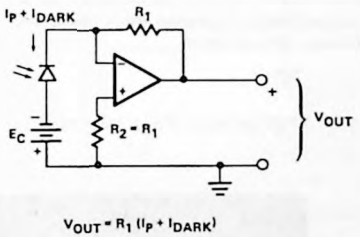
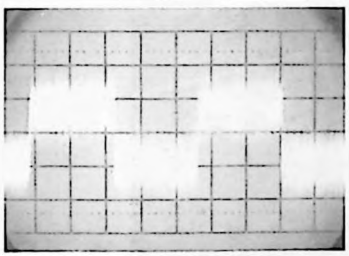
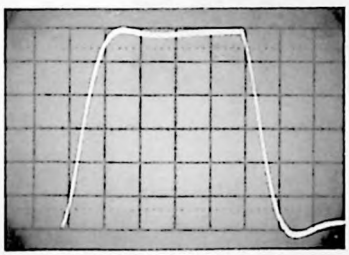


Figure 5. Linear Response; Photodiode and Amplifier Circuit Arrangement





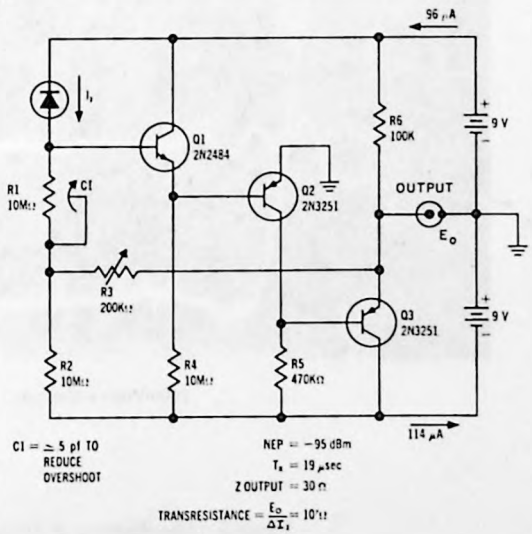


Figure 4. Transistor Photodiode Amplifier Schematic

APPLICATIONS

easily achieved as in Figure 6. If the offset current of the amplifier poses a problem, a resistor can be added between the positive- and negative-going inputs. Its value should not be less than 10GΩ divided by loop gain. If the amplifier has a very high input resistance, loop gain is equal to the forward gain of the amplifier divided by (1 + R / R1) so making $R_2 = 0$ allows the smallest possible resistance between the inputs. The speed of response of this amplifier will be very low, with a time constant $\tau \approx 0.1$s. If high speed logarithmic operation is required, it is best to use the linear amplifier of Figure 5 followed by a logarithmic converter.

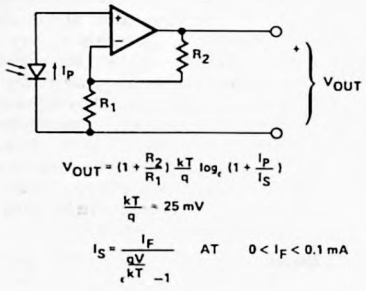


Figure 6. Logarithmic Response; Photodiode and Amplifier Circuit Arrangement

High Speed Photodiode Amplifier

Applications that call for high speed data signaling, such as CRT light pens, require amplifiers that have a wider bandwidth than the circuit shown in Figure 5.

Using a five transistor array (RCA CA3127E) it is possible to construct a high speed, high gain photodiode amplifier. This circuit is shown in Figure 8. It is configured as a two stage amplifier. The first stage is composed of transistors Q1-Q3, where Q1 is an input emitter follower with feedback obtained from the emitter of Q3. Q2 functions as an inverting amplifier interconnecting Q1 to Q3. The second stage consists of Q4 and Q5 which provide additional gain and output buffering, of the first stage. These two stages provide an equivalent transresistance of 420K ohms. This means that the output voltage Vo is equal to the photocurrent, Ip, times 420K ohms.

When high speed circuit layout techniques are used it is possible to obtain the rise and fall time performance shown in Figure 7. This speed is equivalent to a bandwidth of 9.5MHz with an input flux of 1.9μW. This flux level can be obtained from a HEMT-6000 700nm High Intensity Subminiature Emitter when it is operated at 10mA, at a distance of 1cm from the 5082-4207 PIN photodiode.

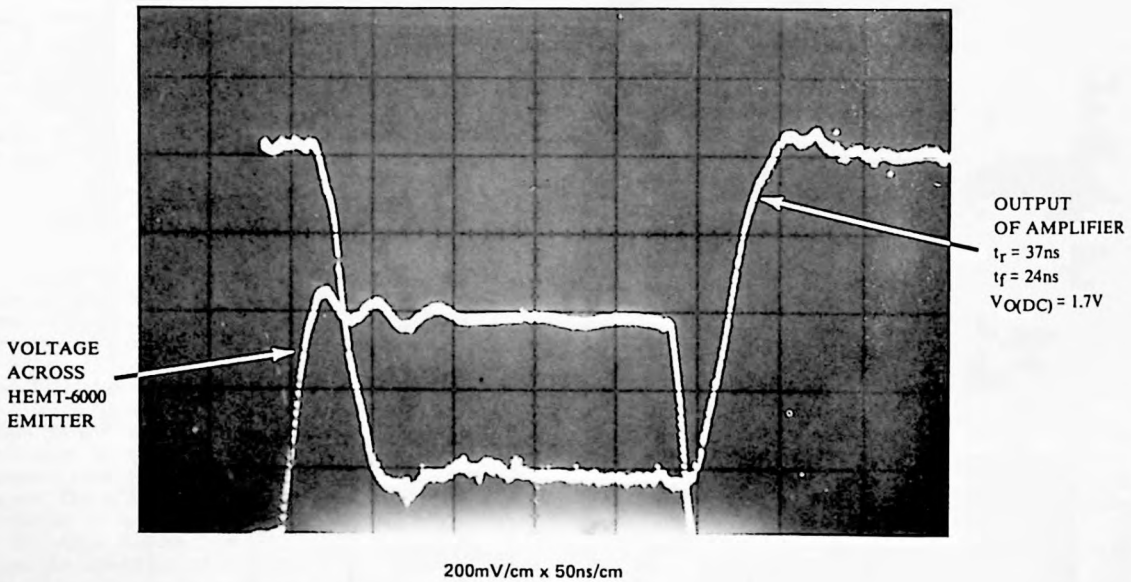
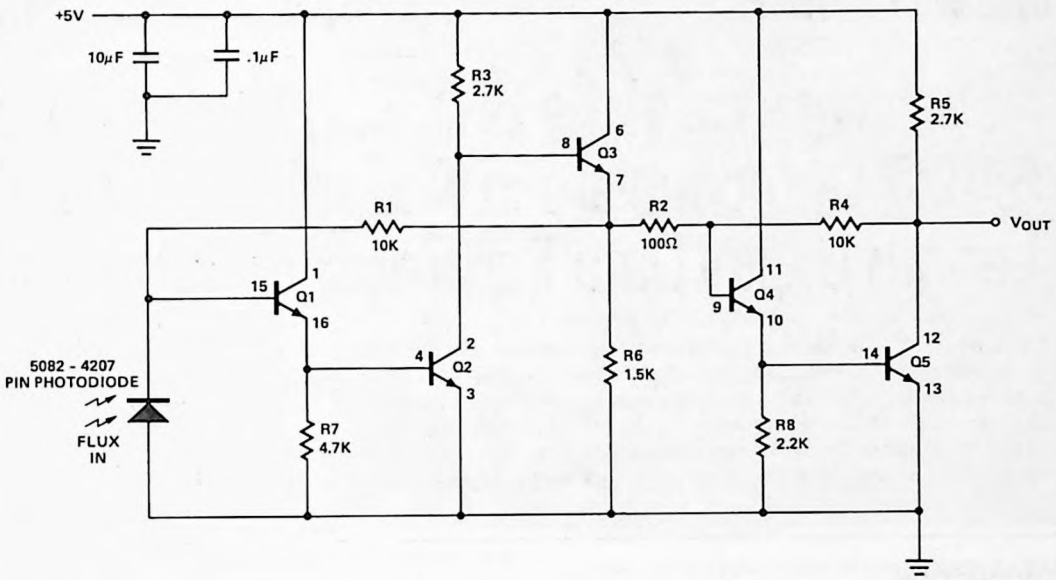


Figure 7. Pulse Response of Photodiode Amplifier



NOTES: TRANSISTORS ARE SINGLE PACKAGE, CA3127E. PINS LABELED FOR EACH. PIN 5 IS SUBSTRATE.

Figure 8. High Speed, High Gain Photodiode Amplifier

HEWLETT PACKARD

APPLICATION NOTE 948

Performance of the 6N135, 6N136 and 6N137 Optocouplers in Short To Moderate Length Digital Data Transmission Systems

This application note assists system designers by describing the performance to be expected from the use of HP 6N135-6N137 optocouplers as a line receiver in a TTL-TTL compatible NRZ[1] data transmission link. It describes several useful total systems including line driver, cable, terminations and TTL compatible connections. The systems described utilize inexpensive cable and operate satisfactorily over the range of transmission distances from 1 ft. to 300 ft. Over this range of distances, the data rate varies from 0.6 megabits per second to 19 megabits per second largely limited by coupler performance at short distances, and cable losses at longer distances.

[1] Non-return to zero

INTRODUCTION

Optocouplers can function as excellent alternatives to integrated circuit line receivers in digital data transmission applications. Their major advantages consist of superior common-mode noise rejection and true ground isolation between the two subsystems. For example, a conventional line receiver is limited to a ±20V common-mode noise rejection at best from DC over its operating frequency range, while an optocoupler can achieve rejections of ±2.5kV at 60Hz.

A conventional optocoupler that utilizes a photo-transistor is limited in its minimum total switching time. At the higher data rates, above 200-500 kbits/s, these delay times can become very significant. The HP 6N135 and 6N136 utilize an integrated photo-diode and transistor to produce lower total switching time. The HP 6N137 adds an integrated amplifier within its package to decrease these delay times still further. All three units can produce data rates well in excess of 500 kbits/s, while the 6N137 can couple an isolated 9.5MHz (19M bits/s) clock from its input to its output. These data rates are achieved with common-mode noise voltage rejection in excess of that provided by most types of line receivers at all frequencies.

The information contained in this application note covers the performance of optocoupler line receiver circuits; however, it does not describe design details. These details are covered in Application Note 947 "Digital Data Transmission Using Optically Coupled Isolators".

This application note describes the basic design elements of a data transmission link and presents several examples of total systems that will be useful to systems designers at distances that range from 1 ft. to 300 ft. and have a moderate overall cost. First, a few measures of performance are defined to allow systems to be compared with one another. Second, the elements of an optocoupler data transmission system are discussed. Third, circuit examples and demonstrated performance of a selected set of systems are presented for the various transmission distances. This presentation includes schematics, representative waveforms at intermediate circuit points, and a summary performance table. It compares the results of passive (resistive) terminations with active terminations that improve overall performance at the longer transmission distances. Fourth, the trade-offs that were made to arrive at the selected system components are described. Along with the trade-offs, there is a discussion of approaches to increase performance by selection of other circuit components or by "peaking" a given length system.

DEFINITIONS OF PERFORMANCE

In data transmission systems that utilize optocouplers, there are no standardized definitions that allow performance capability to be specified. The major performance parameters that are of interest are data rate capability, usually specified in bits per second; and immunity to common mode noise at the coupler input, usually specified as AC or DC common mode voltage rejection in volts, or transient voltage noise rejection in volts/microsecond.

To arrive at a definition of maximum data rate capability requires that the total system be specified including all components, and in addition, data modulation and demodulation techniques. In order to compare the various systems presented in the application note, it is necessary to define some useful terms.

One commonly used modulation technique for digital data data transmission is NRZ, or non-return-to-zero transmission. In the most common form of this technique, a twisted pair transmission line is driven by a balanced driver with an alternating plus or minus voltage signal. A number of integrated circuits are available to provide the drive signals and create a straightforward design.

One potential measure of system performance for NRZ, and potentially other modulation techniques as well, is the measurement of the maximum 50% duty cycle clock frequency that the system will pass. Since a clock represents a total 1/0 and 0/1 transition each full cycle, this square wave provides two bits of data for each cycle. As the upper clock frequency limit of a system using couplers is reached, the duty cycle will change from 50%. The MAXIMUM CLOCK DATA RATE is found by observing the system output as a function of a square wave input until the output distorts to a 10% duty cycle and multiplying this frequency by two (two bits/cycle). At this input frequency, the system data rate is very close to its absolute maximum and any potential recovery of a signal at a higher data rate is impractical. A more detailed definition of this term appears in the glossary.

Another parameter indicative of the performance of a system is to measure the system transient response in its worst case condition. The step response of a transmission system using isolators is a function of the duty cycle and repetition rate. For NRZ, if this term is properly defined, it can indicate a worst case maximum data rate that the system will faithfully transmit, regardless of the combination of ones and zeroes in the data bit stream. This step response term will be referred to as the STEP TRANSIENT DATA RATE MAXIMUM. It assumes that the pulse propagation delay down the transmission line is essentially constant, and defines a data rate maximum at which a single bit of data in a stream of all zeroes and a one, or all ones and a zero may be successfully sent through the system. This is simulated by placing a very low frequency square wave input into the line. Then the circuit delay time from a pulse received at the *end* of the line until the system output makes a transition is measured. This delay time is a function of the cable output risetime and the delays experienced in the coupler and its associated circuitry. The specific delay times are called t_{PHL} and t_{PLH}, indicating delay times for a 1/0 and 0/1 transition respectively. The STEP TRANSIENT DATA RATE MAXIMUM is defined as the inverse of t_{PLH} or t_{PHL}, whichever is longer. In general, this data rate will be lower than the MAXIMUM CLOCK DATA RATE. A more exact definition of t_{PHL}, t_{PLH} and STEP TRANSIENT DATA RATE appears in the glossary.

The parameters used to define worst-case common mode noise immunity are measured for the coupler and associated circuitry without the transmission cable. The common mode voltage rejection is a function of frequency and indicates the maximum AC steady state signal voltage common to both inputs and output ground that will not create an error in the output. This rejection reaches a minimum at some frequency. The transient voltage noise immunity is a measure of the maximum rate of rise (or fall) that can be placed across the common input terminals and output ground without producing an error voltage in the output. This term is a function of the input pulse magnitude and rate of rise for an optocoupler and is stated as a dv/dt minimum in volts per microsecond. Further definitions of these terms appear in the glossary. It should be noted that common mode characteristics of such systems are largely determined by the point at which the noise enters the transmission system. Common mode rejection for a total system would be expected to improve with increasing distance between the common mode insertion point and the input to optocoupler.

ELEMENTS OF AN OPTOCOUPLER DATA TRANSMISSION SYSTEM

The basic elements of an optocoupler transmission system are:

- ☐ Line Driver
- ☐ Transmission Cable
- ☐ Line Termination Circuit
- ☐ Optocoupler
- ☐ TTL Interface Circuit

In order that the performance of systems using the 6N135-6N137 optocouplers might be demonstrated, component elements had to be defined for several systems. These elements are chosen to be TTL compatible at the input and the output. They are also chosen to produce high performance, be moderate in cost, and work over a range of distances of one foot to 300 feet. This can then maximize the utility to systems designers of the circuits demonstrated, thus allowing them to be used without change in a variety of specific applications to produce a known level of performance.

CIRCUIT EXAMPLES AND DEMONSTRATED PERFORMANCE

To reduce the number of complete systems upon which performance is demonstrated to a practical number, a basic representative set of elements must be selected or designed. This includes a single line driver and cable type with performance measurements taken at three transmission distances — 1 ft., 100 ft., and 300 ft. It also includes two termination types, active and passive, and three types of couplers with companion TTL interface circuits. This produces six total data transmission systems upon which data rate performance can be observed at the three transmission distances. Figure 1 illustrates the line driver and cable combination selected. Figure 2 illustrates the pulse response of this driver/cable combination. Figures 3 through 8 indicate the line termination, coupler, and TTL interface circuitry for the various terminations. Included are representative waveforms measured on the three passive termination systems at the 300 ft. transmission distance. Table 1 outlines the critical parameters of the cable used and Tables 2, 3, and 4 summarize the performance demonstrated on all of the transmission systems.

The performance tabulated for the 1 ft. transmission length is indicative of that which might be achieved by a system with negligible performance degradation in the cable. The performance at 100 ft. and 300 ft. indicates the decrease in data rate due to cable losses as the transmission distance increases. This decrease is the most critical data rate limitation and is indicative of the change in performance of systems using low cost cable. Clearly evident in the tables is the increase in performance of the active termination at the 300 ft. transmission distance. Note also that the data rate of the system utilizing the 6N137 at short transmission distances is less with the active than with the passive termination. This decrease is due to the additional delay added by the active termination.

These performance tables can be used to select a design suitable for an application required by a system designer. For example, assume it is desired to design a data transmission system of variable lengths up to 100 ft. and data rates of up to 1.6 Mbits/s. The circuit shown in Figure 4 and the line driver and cable shown in Figure 1 could be selected to assure this level of performance.

SELECTION OF DEMONSTRATION CIRCUIT ELEMENTS

The foregoing systems exemplify achievable performance and incorporate a number of design decisions which are discussed in this section.

LINE DRIVER

Line Drivers generate the signal that is sent down the transmission line. They have limits as to voltage swing, output impedance, and switching time. A good compromise is provided by National Semiconductor's DM 8830. Any similar device with a low output impedance such as the Fairchild 9614 would operate satisfactorily. These devices are TTL input compatible, require no external components, are relatively inexpensive and readily available. They provide adequate performance and produce directly a dual rail (inverting and non-inverting) output.

For systems requiring higher data rates, more sophisticated and expensive drivers can be selected or designed. Figure 9 illustrates a circuit that has a higher current output and produces a higher data rate than an integrated driver. It uses several components, but does not require a supply voltage above the standard TTL 5 volts. To obtain still higher data rates, the driver line voltage output must be increased. This in turn requires a supply voltage above 5 volts. The National Semiconductor LH 0002C is an example of an integrated circuit that can be used to produce directly a higher line voltage. Numerous other discrete circuits could be designed.

TRANSMISSION CABLE

Transmission cables are very critical in the overall system. They can decrease the effect of extraneous noise voltages on system performance by providing shielding. They also greatly affect the signal losses as the transmission length increases. By controlling these losses, cables can permit a single set of system elements to function adequately for both long and short transmission distances. The critical performance parameters of a transmission cable include cost, transmission length, line series resistance (DC losses), high frequency losses, type and amount of shielding and characteristic impedance.

The Belden type 8777 is representative of a relatively well-shielded, inexpensive cable with typical transmission loss. The important characteristics of this cable are summarized in Table 1.

If it is desired to attain higher performance, the line cost becomes considerably more expensive and tends to dominate system costs. These higher performance cables utilize a large conductor size to lower DC losses, and provide considerably lower losses at high frequencies. Examples of such a cable would be Belden 9269 (IBM 32392), Belden 9250 or their equivalents.

The pulse response of the DM 8830 and the Belden 8777 illustrates the waveform degradation of signals sent down this driver/transmission line pair, regardless of the line receiver employed. Figure 1 illustrates this circuit combination, and Figure 2 illustrates the pulse waveform degradation at 1 ft., 100 ft., and 300 ft. into a 68Ω equivalent load.

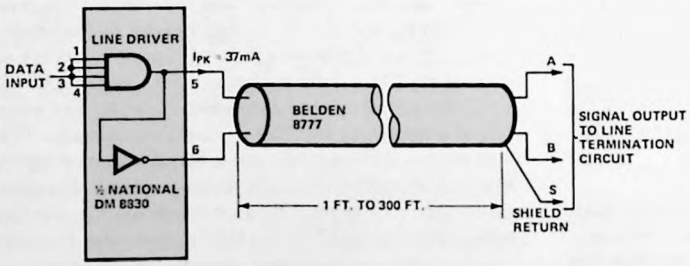


Figure 1. Line Driver and Cable Combination Selected for Use on All Six Systems to Indicate Their Performance.

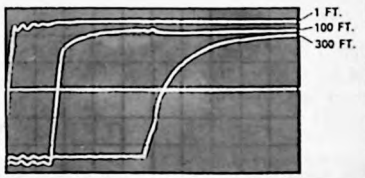


Figure 2. Pulse Characteristics of the Selected Line Driver and Cable. Measurement Observed with a 68Ω Equivalent Termination at One, 100, and 300' Distances. All Waveforms are Line to Line Voltage, Time Referenced to zero feet. Note Time Delay and Waveform Degradation.

LINE TERMINATION CIRCUIT

The line termination circuit converts the voltage arriving at the end of the line to a current impulse to drive the coupler emitter diode. In these system examples, performance of both passive and active circuits was measured.

A passive circuit consists of a set of resistors to match the line to its characteristic impedance and to convert the line voltage to a current. The circuits illustrated here were designed to provide good performance at 300 ft., while not exceeding the coupler input drive current maximum at the 1 ft. line length condition. With this design criterion, these circuits are useful over this *range* of transmission cable lengths. These design characteristics required that two resistive line termination circuits be designed for the three isolators. They are illustrated in Figures 3, 4, and 5.

An improvement in the performance of a resistive termination can be obtained by peaking the line to operate at a specific length as shown in Figure 10. This technique allows the coupler to operate from the peak to peak voltage at the end of the line. To avoid overdriving the coupler, the peaking capacitor value must be minimized. It is chosen by observing the circuit delay time t_{PLH} and selecting the smallest value of capacitor that significantly decreases this delay. With this technique, performance can be expected to improve by as much as 20-30% or more, but the values of peaking capacitor tend to vary with many of the characteristics of components in all of the elements of the system. These include driver output voltage, line length, line losses, coupler delay, etc. This in turn requires each individual system to have a selected value of peaking capacitor.

An active termination utilizes a transistor to act as a line voltage to coupler input current regulator. This technique ignores any attempt to match the line, but instead converts any incoming voltage to a suitable current, once the circuit threshold voltage is exceeded. This tends to decrease circuit sensitivity to line length and other line voltage variations. The delay of an active circuit can limit the maximum system data rate, especially for short transmission distances. But, in general, their use can improve the maximum data rate at the longer distances. In the system examples, two active termination circuits were designed and are illustrated in Figures 6, 7 and 8.

Improving the performance of the active circuit consists of finding transistors and circuit designs to perform the voltage to input current regulation function without limiting overall system performance.

OUTPUT TO TTL INTERFACE

The 6N136 and 6N137 have sufficiently high input to output coupling efficiency (CTR) that the only component required to interface the optocoupler to a TTL input gate is a pull-up resistor. The 6N135 has a somewhat lower CTR and requires an external transistor and resistor to interface with a TTL gate input. The actual circuit configuration and values required for these interface circuits are illustrated in Figures 3 through 8. The circuits illustrate, in general, the optimum interface for a TTL-TTL compatible circuit. Performance could be improved through the use of lower pull-up resistor values in the coupler output collectors and high speed TTL compatible comparators.

Table 1

IMPORTANT LINE CHARACTERISTICS OF BELDEN 8777

- Three sets of two conductor, twisted and individually foil shielded, 22 gauge wire
- Z_0 (Measured Characteristic Impedance)—68Ω line to line
- Line-to-line capacitance — 30pF/ft.
- Line Resistance — 3.2Ω/100 ft. (per conductor pair)
- Attenuation at 10MHz ≃ 4 dB/100 ft.
- Delay ≃ 1.5 nsec/ft.
- Cost ≈ 5¢/ft./Transmission Pair

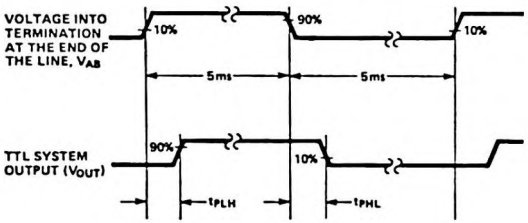
GLOSSARY

1. DATA RATE – This term is typically stated in bits per second and has no standardized definition when used in reference to optocouplers. It is related to the minimum pulse transition time that will be passed by the system and detected. This in turn is related to the distortion or change in duration the pulse experiences upon passing through the system.

2. STEP TRANSIENT DATA RATE MAXIMUM – This term, stated in bits per second, is a function of the maximum delay experienced by a 0/1 or a 1/0 transition in passing through the optocoupler. The step transient data rate maximum is defined as:

$$\text{STEP TRANSIENT DATA RATE (MAX)} = \frac{1}{t_{PHL}} \text{ or } \frac{1}{t_{PLH}}$$

whichever is smaller. Where t_{PLH} and t_{PHL} are measured at the coupler termination input (end of the line) and the TTL output and are defined as follows:

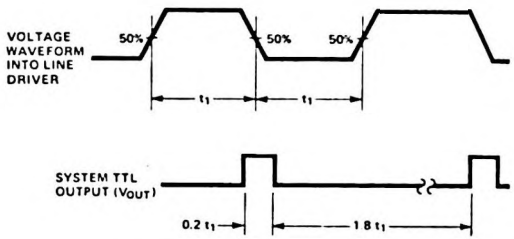


The t_{PHL} and t_{PLH} measured under these conditions approach the maximum delay that will be experienced by data sent through the isolator.

3. MAXIMUM CLOCK DATA RATE – This term defines the maximum data rate at which a 50% duty cycle square wave (clock) will be distorted to a 90%/10% pulse. It is very close to the maximum alternating 1/0 and 0/1 transition that can be passed by the system. It is defined mathematically as:

$$\text{MAXIMUM CLOCK DATA RATE} = \frac{1}{t_1}$$

where t_1 is defined as:



4. COMMON MODE REJECTION VOLTAGE – This term is defined as the maximum sinusoidal voltage at a given frequency that can be applied *simultaneously* to both inputs with respect to output ground and not produce an error signal in the system output. In optocouplers, the value of this voltage is very high at low frequencies and decreases with increasing frequency until it reaches a minimum. The effect is caused by the effective intercircuit capacitance of the emitter and detector chips, and the detector gain and bandwidth. (See Figure 11.)

5. COMMON MODE dv/dt REJECTION MINIMUM – This term is defined as the maximum rate of change of voltage that can be applied to both inputs *simultaneously* with respect to output ground and not produce an error in the system output. Note that this parameter is a function of the duration of the change, or equivalently the pulse amplitude. The stated values in this application note are for a 10V step pulse amplitude generated by a source having a controlled risetime and falltime (e.g., HP 8007B). (See Figure 11.)

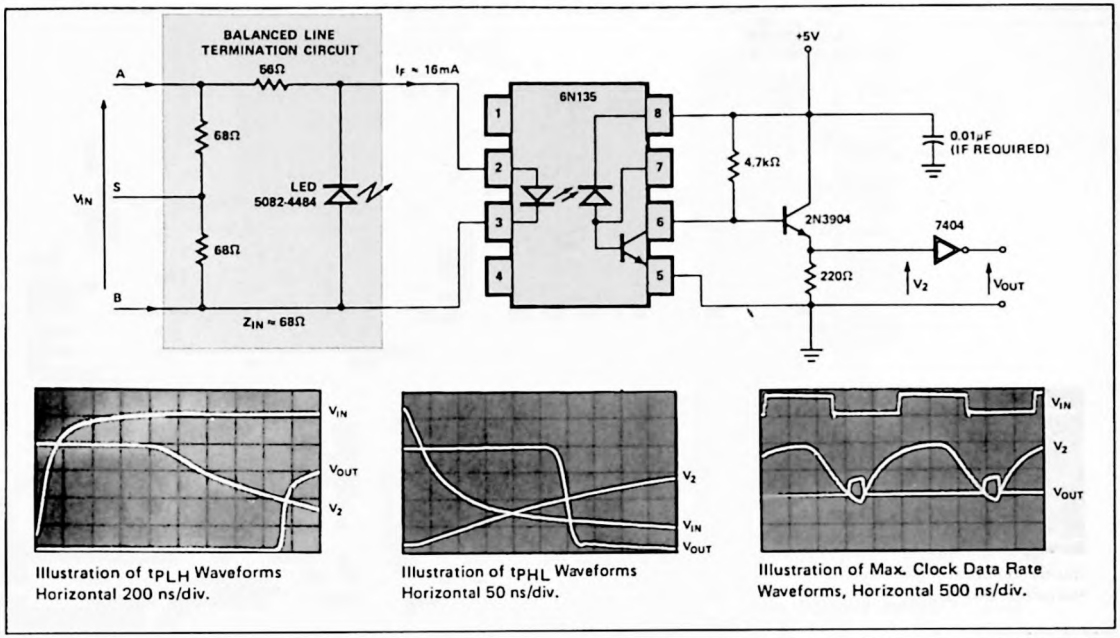


Illustration of t_{PLH} Waveforms
Horizontal 200 ns/div.

Illustration of t_{PHL} Waveforms
Horizontal 50 ns/div.

Illustration of Max. Clock Data Rate
Waveforms, Horizontal 500 ns/div.

Figure 3. TTL Compatible Passive (Resistive) Termination for the 6N135 and Photographs Indicating Measured Performance at the End of the 300 Ft. Transmission Cable.

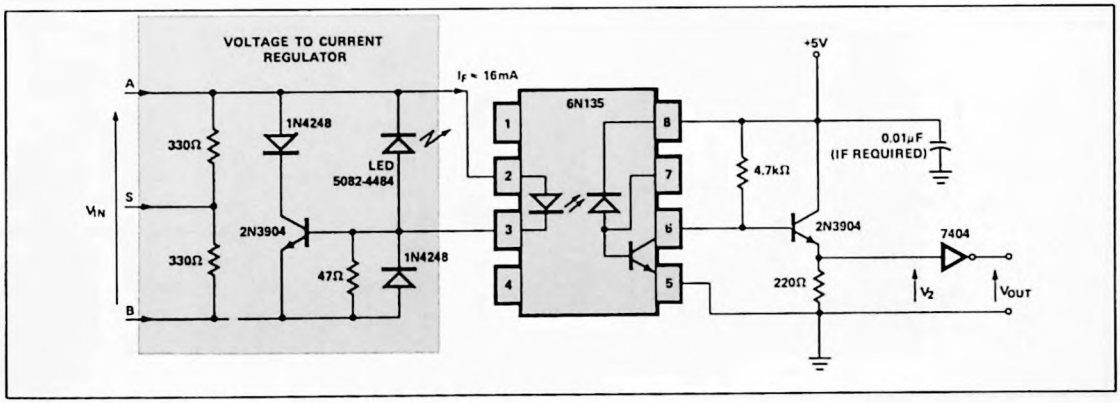


Figure 6. TTL Compatible Active Termination for the 6N135.

Table 2. Summary of Performance of 6N135 Data Transmission Systems at 1, 100, and 300 ft.

Termination	Transmission Distance (ft)	t_{PLH} (ns)	t_{PHL} (ns)	Step Transient Data Rate Max. (Mbits/s)	Clock Data Rate Max. (Mbits/s)	Worst Case Common Mode Noise Rejection	
						Sinusoidal	dV/dt
RESISTIVE (PASSIVE)	1	475	500	2.0	11.2	<10kHz: 5.0kV pk-pk	250V/μs min.
	100	900	425	1.1	3.0		
Fig. 3	300	1700	300	0.6	0.8	1MHz: 84V pk-pk min.	
ACTIVE	1	500	330	2.0	5.3		
Fig. 6	100	580	270	1.7	4.0		
	300	875	330	1.1	1.6		

APPLICATIONS

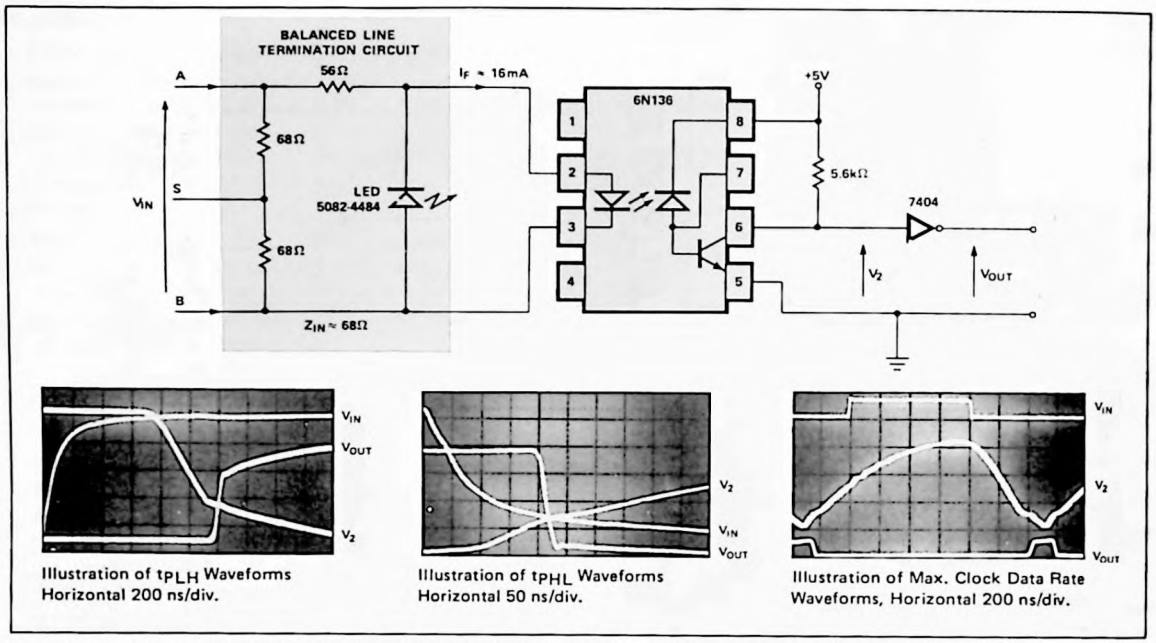


Figure 4. TTL Compatible Passive (Resistive) Termination for the 6N136 and Photographs Indicating Measured Performance at the End of the 300 Ft Cable.

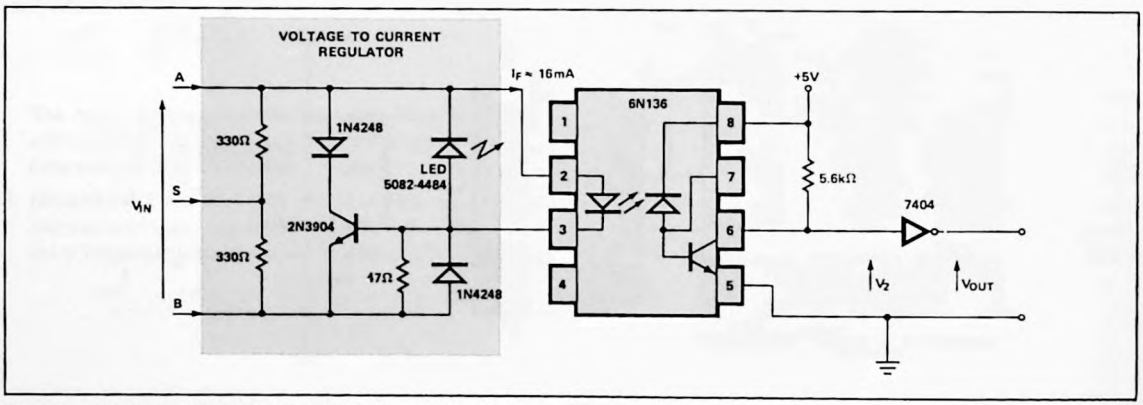


Figure 7. TTL Compatible Active Termination for the 6N136.

Table 3. Summary of Performance of 6N136 Data Transmission Systems at 1, 100, and 300 ft.

	Transmission Distance (ft)	t_{PLH} (ns)	t_{PHL} (ns)	Step Transient Data Rate Max. (Mbits/s)	Clock Data Rate Max. (Mbits/s)	Worst Case Common Mode Noise Rejection	
						Sinusoidal	dV/dt
RESISTIVE (PASSIVE)	1	320	270	2.7	10.0	<10kHz: 5.0kV pk-pk 1MHz: 84V pk-pk min.	250V/μs min.
	100	640	265	1.6	4.0		
Fig. 4	300	1200	220	0.8	1.2		
ACTIVE	1	375	250	2.7	6.6		
Fig. 7	100	440	250	2.3	5.0		
	300	700	250	1.4	2.4		

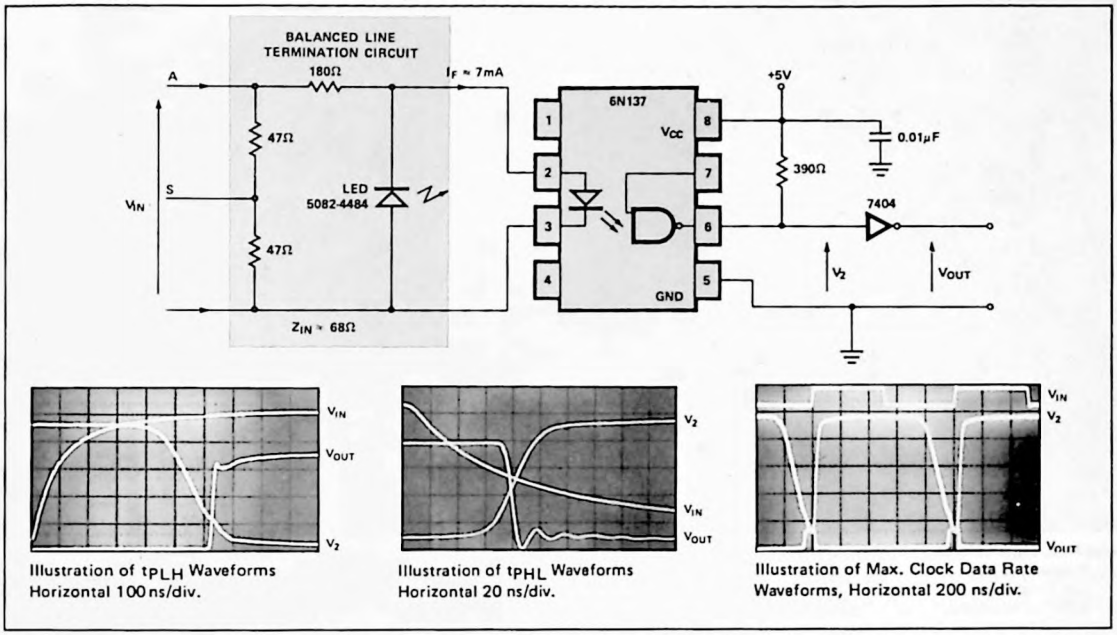


Illustration of t_{PLH} Waveforms
Horizontal 100 ns/div.

Illustration of t_{PHL} Waveforms
Horizontal 20 ns/div.

Illustration of Max. Clock Data Rate
Waveforms, Horizontal 200 ns/div.

Figure 5. TTL Compatible Passive (Resistive) Termination for the 6N137 and Photographs Indicating Measured Performance at the End of the 300 Ft. Transmission Cable.

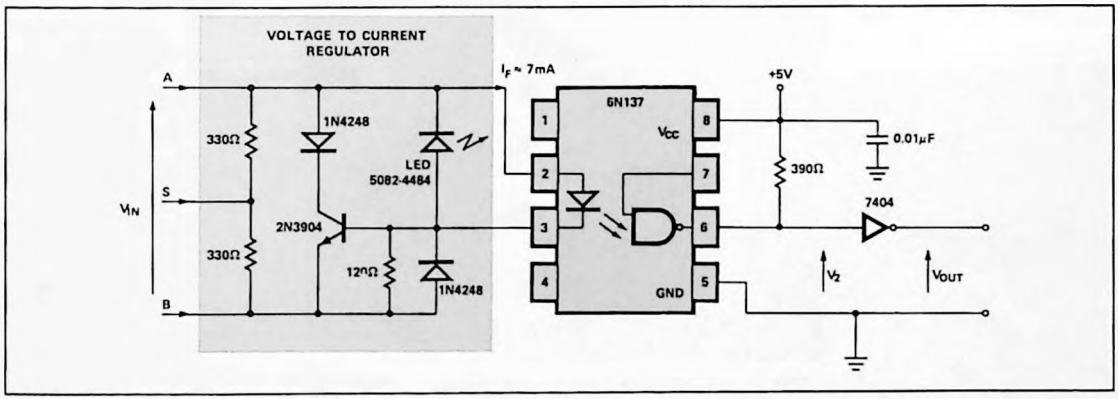


Figure 8. TTL Compatible Active Termination for the 6N137.

Table 4. Summary of Performance of 6N137 Data Transmission Systems at 1, 100, and 300 ft.

	Transmission Distance (ft)	t_{PLH} (ns)	t_{PHL} (ns)	Step Transient Data Rate Max. (Mbits/s)	Clock Data Rate Max. (Mbits/s)	Worst Case Common Mode Noise Rejection	
						Sinusoidal	dV/dt
RESISTIVE (PASSIVE)	1	105	70	9.5	19.0	≤10kHz: 5.0kV pk-pk 8MHz: 22V pk-pk min.	40V/μs min.
	100	170	70	5.8	8.0		
	300	625	70	1.6	2.0		
ACTIVE	1	190	65	5.3	11.0		
	100	190	70	5.3	13.2		
	300	275	80	3.9	8.2		

APPLICATIONS

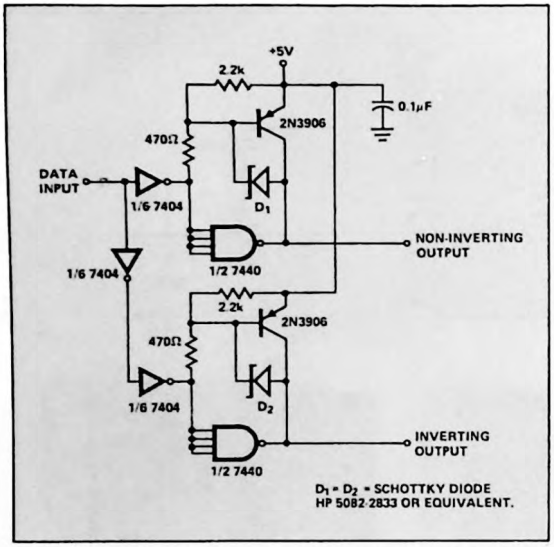


Figure 9. High Output Voltage Swing, High Current, Wide Bandwidth Line Driver that Operates From a 5 Volt Supply and Produces a >8.5V Pk to Pk Pulse into 300 Ft. of Belden 8777 at 10 MHz.

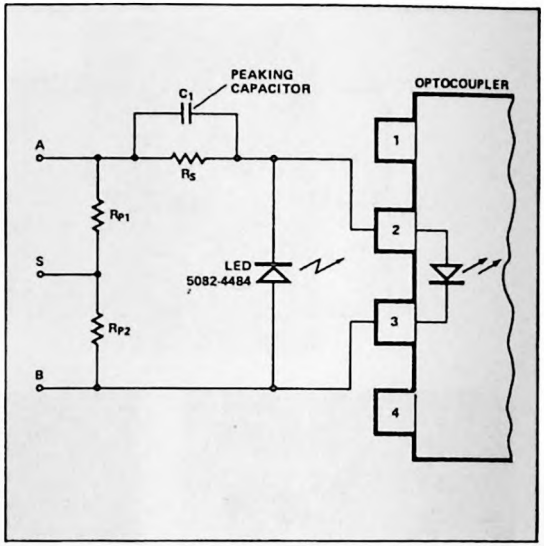


Figure 10. An Example of Circuit Peaking to Improve the Performance of the Passive Termination. C_1 is Chosen for the Minimum Value that Significantly Reduces Input to Output Delay Time. In General, C_1 Must be Selected Individually For Each System.

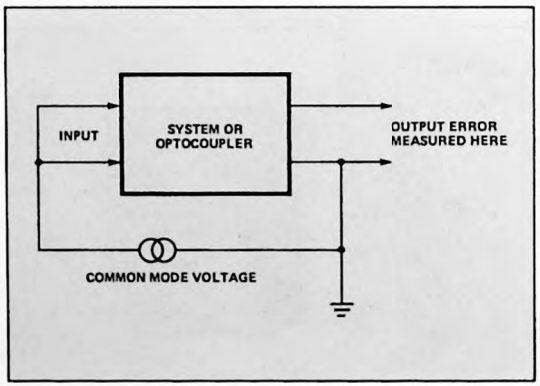


Figure 11. Common Mode Measurement Circuit.

HEWLETT PACKARD

APPLICATION NOTE 951-1

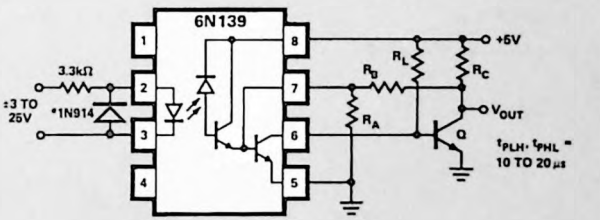
Applications for Low Input Current, High Gain Optocouplers

Optically coupled isolators are useful in applications where large common mode signals are encountered. Examples are: line receivers, logic isolation, power lines, medical equipment and telephone lines. This application note has at least one example in each of these areas for the 6N138/9 series high CTR couplers.

HP's 6N138/9 series couplers contain a high gain, high speed photodetector that provides a minimum current transfer ratio (CTR) of 300% at input currents of 1.6 mA for the 6N138 and 400% at 0.5 mA for the 6N139. The excellent low input current CTR enables these devices to be used in applications where low power consumption is required and those applications that do not provide sufficient input current for other couplers. Separate pin connections for the photodiode and output transistor permit high speed operation and TTL compatible output. A base access terminal allows a gain bandwidth adjustment to be made.

RS-232C COMPATIBLE LINE RECEIVER

- 2500V 60Hz Common Mode Rejection
- Allows use of Low Cost Line
- Full 40kbs Data Rate for Line Lengths up to 5000'
- Hysteresis for Increased Noise Immunity



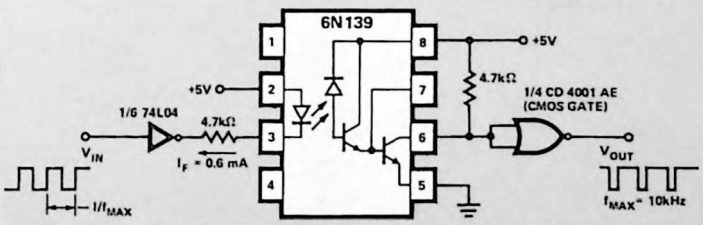
*ANTIPARALLEL DIODE IS NEEDED ONLY IF REVERSE LINE VOLTAGE EXCEEDS 15V (TO PREVENT HIGH REVERSE VOLTAGE FROM CAUSING POWER DISSIPATION IN EXCESS OF INPUT DIODE MAXIMUM RATING).

REMOVE R_A AND R_B FOR NO HYSTERESIS

R_A	R_B	R_C	R_L	Q
680kΩ	1.5MΩ	1.8kΩ	15kΩ	2N3904

LOW POWER INTERFACE

- Operation at $I_F \geq 0.5mA$
- 10kHz f_{MAX}
- Low Power Consumption

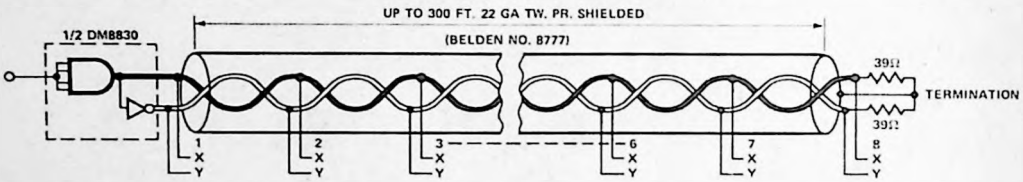


f_{MAX} IS THE FREQUENCY AT WHICH A 50% DUTY FACTOR AT THE INPUT IS DEGENERATED TO 10% OR 90% DUTY FACTOR AT THE OUTPUT.

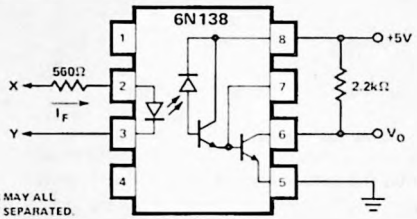
APPLICATIONS

LINE RECEIVER FOR PARTY LINE

- 1-8 Receivers can be used with circuit shown
- Uses conventional IC Line Driver
- Total Line Length 1-300'
- Typical Data Rate —180kbs (t_{PHL}, t_{PLH} = 3 μsec)
- Allows use of Low Cost Line



ISOLATOR LOADS MAY BE DISTRIBUTED RANDOMLY ALONG THE LENGTH OF THE LINE, OR ALL MAY BE LUMPED AT THE END. I_F FOR 1 AND 8 ISOLATOR LOADS WOULD BE 2.7 AND 1.8mA RESPECTIVELY.

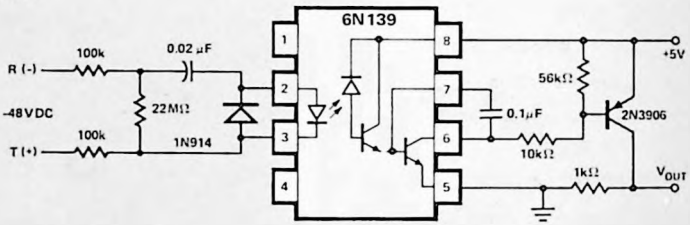


PROPAGATION DELAY: t_{PHL}, t_{PLH} = 0.5 to 5μs

OUTPUT GROUNDS MAY ALL BE ELECTRICALLY SEPARATED.

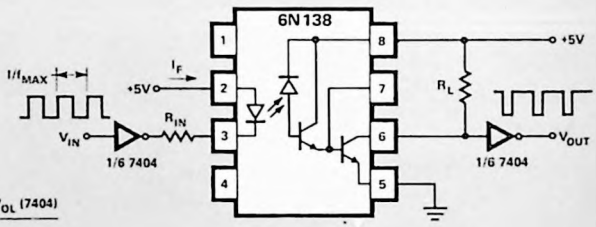
TELEPHONE RING DETECTOR

- Discriminates between Ring and Dial Signals
- Minimal Line Loading
- 2500V Insulation from Telephone Line
- Small Size
- Integrator Included



TTL TO TTL INTERFACE

- Direct Input and Output Compatibility
- Adjustable Data Rate
- High Fan-Out



$$I_F = \frac{5V - V_F - V_{OL}(7404)}{R_{IN}}$$

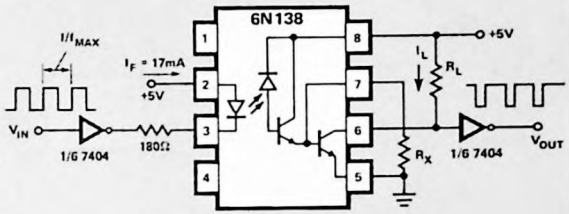
FOR HIGHER FANOUT WITH COMPARABLE DATA RATES USE SMALLER VALUES OF R_{IN}

f_{MAX} IS THE FREQUENCY AT WHICH A 50% DUTY FACTOR AT THE INPUT IS DEGENERATED TO 10% OR 90% DUTY FACTOR AT THE OUTPUT.

R_L(Ω)	R_{IN}(Ω)	I_F(mA)	f_{MAX} (kHz)
2200	1800	1.7	40
270	390	8	125
100	180	17	250

GAIN/SPEED TRADE OFF

- Obtain Maximum Speed at Required Gain
- Single Resistor Required
- Use same device for Multiple Applications

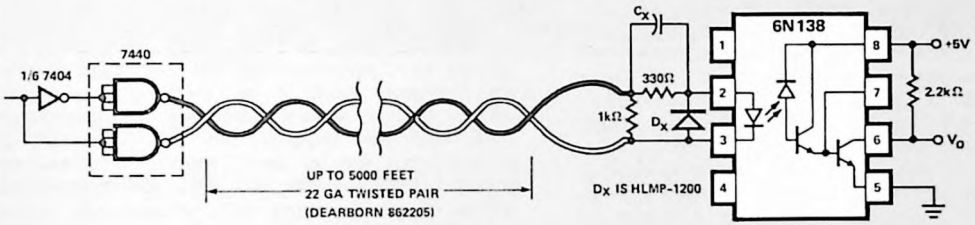


I_{MAX} IS THE FREQUENCY AT WHICH A 50% DUTY FACTOR AT THE INPUT IS DEGENERATED TO 10% or 90% DUTY FACTOR AT THE OUTPUT.

R_X (Ω)	R_L (Ω)	I_L (mA)	f_{MAX} (kHz)
NONE	100	46	250
820	1000	4.6	650

1-5000 FT. LINE RECEIVER

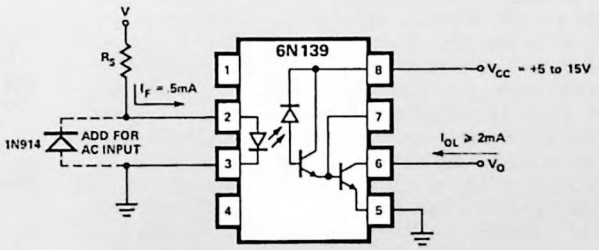
- Drive with Standard TTL Buffer Gate
- 2500V 60Hz Common Mode Rejection
- Allows use of Low Cost Line
- 40kbs Data Rate
- TTL Compatible Output



PROPAGATION DELAY: WITHOUT C_X,D_X, t_{PLH} = 2 to 5 μs; t_{PHL} = 25μs
WITH D_X, C_X > 0.002μF, t_{PLH} = 2μs; t_{PHL} = 7μs

HIGH VOLTAGE STATUS INDICATOR

- Low Power Consumption
- TTL Compatible Output
- High Speed
- Use for Power Turn On Anticipation Circuit, 117V Line Monitor or Other High Voltage Sensing

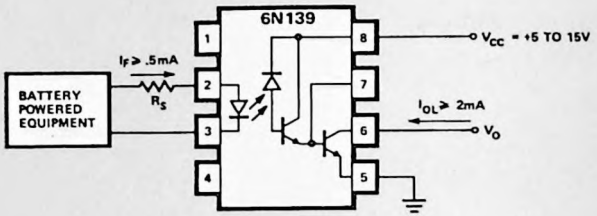


V(Vdc or Vrms)	R_S	V • I_F (mW)
24	47kΩ	11
48	100kΩ	22
117	220kΩ	62
230	470kΩ	113

APPLICATIONS

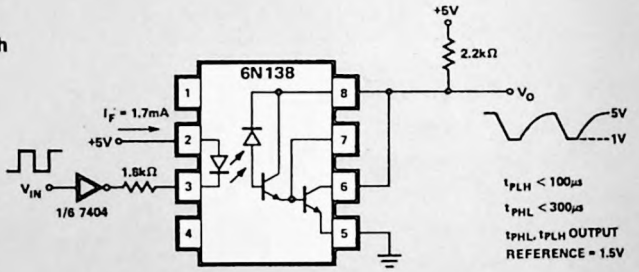
MEDICAL EQUIPMENT ISOLATION

- Low Power Consumption
- 2500V 60Hz Isolation
- Digital or Analog Operation



CONVENTIONAL DARLINGTON

- No Bias Supply Required
- Base Lead available for Gain/Bandwidth Adjust
- Data Rates of 2kbs



HEWLETT PACKARD

APPLICATION NOTE 951-2

Linear Applications of Optocouplers

Optocouplers are useful in applications where analog or DC signals need to be transferred from one module to another in the presence of a large potential difference or induced noise between the ground or common points of these modules.

Potential applications are those in which large transformers, expensive instrumentation amplifiers or complicated A/D conversion schemes are used. Examples are: sensing circuits (thermocouples, transducers ...), patient monitoring equipment, power supply feedback, high voltage current monitoring, adaptive control systems, audio amplifiers and video amplifiers.

HP's optocouplers have integrated photodetector/amplifiers with speed and linearity advantages over conventional phototransistors. In a photo transistor, the photodetector is the collector-base junction so the capacitance impairs the collector rise time. Also, amplified photocurrent flows in the collector-base junction and modulates the photo-response, thereby causing non-linearity. The photodetector in an HP optocoupler is a separately integrated diode so its photoresponse is not affected by amplified photocurrent and its capacitance does not impair speed. Some linear isolation schemes employ digital conversion techniques (A/D-D/A, PWM, PCM, etc.) in which the higher speed of the integrated photodetector permits better linearity and bandwidth.

The 6N135/6N136 is recommended for single channel AC analog designs. The HCPL-2530/31 is recommended for dual channel DC linear designs. The 6N135/6 series or the 6N137 series are recommended for digital conversion schemes.

If the output transistor is biased in the active region, the current transfer relationship for the 6N135 series optocoupler can be represented as:

$$I_C = K \left(\frac{I_F}{I_F'}\right)^n$$

where I_C is the collector current; I_F is the input LED current; I_F' is the current at which K is measured; K is the collector current when $I_F = I_F'$; and n is the slope of I_C vs. I_F on logarithmic coordinates.

The exponent n varies with I_F, but over some limited range of ΔI_F, n can be regarded as a constant. The current transfer relationship for an opto isolator will be linear only if n equals one.

For the 6N135 series optocoupler, n varies from approximately 2 at input currents less than 5mA to approximately 1 at input currents greater than 16mA. For AC coupled applications, reasonable linearity can be obtained with a single optocoupler. The optocoupler is biased at higher levels of input LED current where the ratio of incremental photodiode current to incremental LED current ($\partial I_D/\partial I_F$) is more nearly constant.

For better linearity and stability, servo or differential linearization techniques can be used.

The servo linearizer forces the input current of one optocoupler to track the input current of the second optocoupler by servo action. Thus, if $n_1 \approx n_2$ over the excursion range, the non linearities will cancel and the overall transfer function will be linear. In the differential linearizer, an input signal causes the input current of one optocoupler to increase by the same amount that input current of the second optocoupler is decreased. If $n_2 \approx n_2 \approx 2$, then a gain increment in the first optocoupler will be balanced by a gain decrement in the second optocoupler and the overall transfer function will be linear. With these techniques, matching of K will not effect the overall linearity of the circuit but will simplify circuit realization by reducing the required dynamic range of the zero and offset potentiometers.

Gain and offset stability over temperature is dependent on the stability of current sources, resistors, and the optocoupler. For the servo technique, changes of K over temperature will have only a small effect on overall gain and offset as long as the ratio of K_1 to K_2 remains constant. With the differential technique, changes of K over temperature will cause a change in gain of the circuit. Offset will remain stable as long as the ratio of K_1 to K_2 remains constant. In the AC circuit, since ($\partial I_D/\partial I_F$) varies with temperature, the gain will also vary with temperature. A thermister can be used in the output amplifiers of the Differential and AC circuits to compensate for this change in gain over temperature.

There are also several digital techniques to transmit an optocoupler analog signal. Optocouplers can be used to transmit a frequency or pulse width modulated signal. In these applications, overall circuit bandwidth is determined by the required linearity as well as the propagation delay of the optocoupler. The 6N137 series optocoupler features propagation delays typically less than 50ns and

the 6N135 series optocoupler features propagation typically less than 300ns.

In several places the circuits shown call for a current source. They can be realized in several ways. If V_{CC} is stable, the current source can be a mirror type circuit as shown in Figure 1.

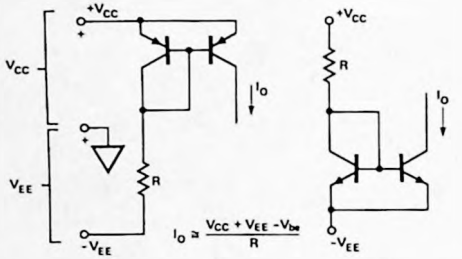


Figure 1.

If V_{CC} is not stable, a simple current source such as the ones shown in Figure 2 can be realized with an LED as a voltage reference. The LED will approximately compensate the transistor over temperature since $\Delta V_{be}/\Delta T \cong \Delta V_F/\Delta T = -2mV/°C$:

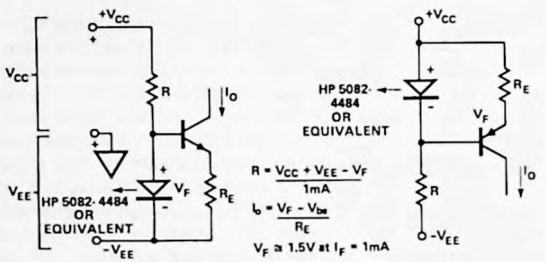


Figure 2.

SERVO ISOLATION AMPLIFIER

The servo amplifier shown in Figure 3 operates on the principle that two optocouplers will track each other if their gain changes by the same amount over some operating region. U_2 compares the outputs of each optocoupler and forces I_{F2} through D_2 to be equal to I_{F1} through D_1. The constant current sources bias each I_F at 3mA quiescent current. R_1 has been selected so that I_{F1} varies over the range of 2mA to 4mA as V_{IN} varies from −5V to +5V. R_1 can be adjusted to accommodate any desired range. With V_{IN}=0, R_2, is adjusted so that V_{OUT}=0. Then with V_{IN} at some value, R_4 can be adjusted for a gain of 1. Values for R_2 and R_4 have been picked for a worst case spread of optocoupler or current transfer ratios. The transfer function of the servo amplifier is:

$$V_{OUT} = R_4\left[\left(I_F'_2\right)\left(\frac{K_1 R_2 (I_{CC_1})^{n_1}}{K_2 R_3 (I_F'_1)^{n_1}}\right)^{1/n_2}\left(1+\frac{V_{IN}}{R_1 I_{CC_1}}\right)^{n_1/n_2} - I_{CC_2}\right]$$

After zero adjustment, this transfer function reduces to:

$$V_{OUT} = R_4 I_{CC_2}\left[(1+x)^n - 1\right], \text{ where } x = \frac{V_{IN}}{R_1 I_{CC_1}}, \; n = \frac{n_1}{n_2}$$

The non linearities in the transfer function where $n_1 \neq n_2$ can be written as shown below. For example, if $|x| \leq .35$, $n = 1.05$, then the linearity error is 1% of the desired signal.

$$\frac{\text{linearity error}}{\text{desired signal}} = \frac{(1+x)^n - n\,x - 1}{n\,x}$$

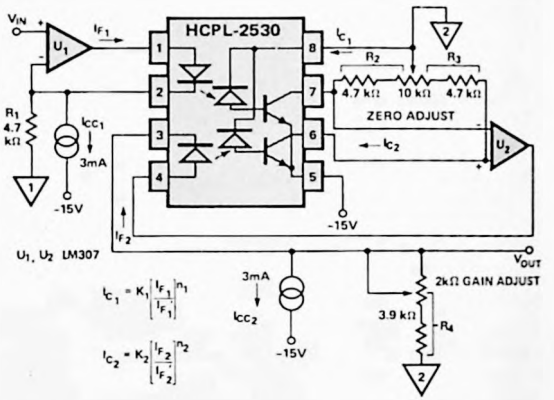


Figure 3. Servo Type DC Isolation Amplifier.

Typical Performance for the Servo Linearized DC Amplifier:

1% linearity for 10V p-p dynamic range
Unity voltage gain
25 kHz bandwidth (limited by U_1, U_2)
Gain drift: −.03%/°C
Offset drift: ±1 mV/°C
Common mode rejection: 46dB at 1 kHz
500V DC insulation (3000V if 2 single couplers are used)

DIFFERENTIAL ISOLATION AMPLIFIER

The differential amplifier shown in Figure 4 operates on the principle that an operating region exists where a gain increment in one optocoupler can be approximately balanced by a gain decrement in the second optocoupler. As I_{F1} increases due to changes in V_{IN}, I_{F2} decreases by an equal amount. If $n_1 = n_2 = 2$, then the gain increment caused by increases in I_{F1} will be balanced by the gain decrement caused by decreases in I_{F2}. The constant current source biases each I_F at 3mA quiescent current. R_1 and R_2 are designed so that I_F varies over the range of 2mA to 4mA as V_{IN} varies from −5V to +5V. R_1 and R_2 can be adjusted to accommodate any desired dynamic range. U_3 and U_4 are used as a differential current amplifier:

$$V_{OUT} = R_5\left[(R_3/R_4)\, I_{C1} - I_{C2}\right]$$

R_3, R_4, R_5 have been picked for an amplifier with a gain of 1 for a worst case spread of coupler current transfer ratios. The transfer function of the differential amplifier is:

$$V_{OUT} = R_5\left[\left(\frac{K_1 R_3}{R_4}\right)\left(\frac{I_{CC}}{2\,I_F'_1}\right)^{n_1}\left(1+\frac{V_{IN}}{R\,I_{CC}}\right)^{n_1} - K_2\left(\frac{I_{CC}}{2\,I_F'_2}\right)^{n_2}\left(1-\frac{V_{IN}}{R\,I_{CC}}\right)^{n_2}\right]$$

if $R \equiv R_1 \equiv R_2$

After zero adjustment, this transfer function reduces to:

$$V_{OUT} = R_5 K' \left[\left(1 + \frac{V_{IN}}{R\ I_{CC}}\right)^{n_1} - \left(1 - \frac{V_{IN}}{R\ I_{CC}}\right)^{n_2} \right],$$

$$\text{where } K' = \frac{K_1 R_3}{R_4} \left(\frac{I_{CC}}{2\ I_{F'_1}}\right)^{n_1} = K_2 \left(\frac{I_{CC}}{2\ I_{F'_2}}\right)^{n_2}$$

The non linearities in the transfer function when $n_1 \neq n_2 \neq 2$ can be written as shown below. For example, if $|x| \leq .35$, $n_1 = 1.9$, $n_2 = 1.8$, then the linearity error is 1.5% of the desired signal.

$$\frac{\text{linearity error}}{\text{desired signal}} = \frac{(1+x)^{n_1} - (1-x)^{n_2} - (n_1 + n_2)\,x}{(n_1 + n_2)\,x}, \text{ where } x = \frac{V_{IN}}{R\ I_{CC}}$$

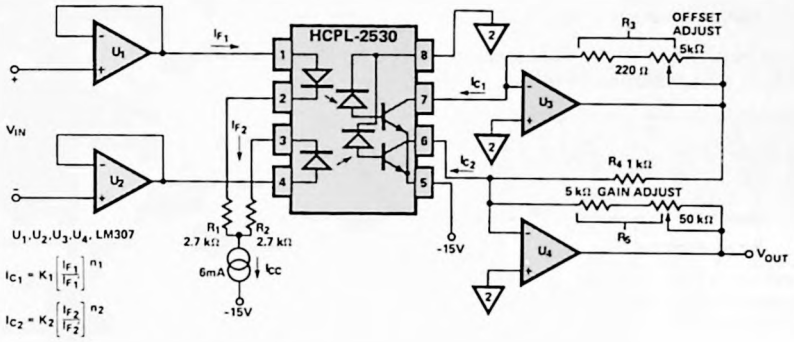


Figure 4. Differential Type DC Isolation Amplifier.

Typical Performance of the Differential Linearized DC Amplifier:

3% linearity for 10V p-p dynamic range
Unity voltage gain
25 kHz bandwidth (limited by U_1, U_2, U_3, U_4)
Gain drift: −.4%/°C
Offset drift: ±4mV/°C
Common mode rejection: 70dB at 1 kHz
3000V DC insulation

AC COUPLED AMPLIFIER

In an AC circuit, since there is no requirement for a DC reference, a single optocoupler can be utilized by biasing the optocoupler in a region of constant incremental CTR ($\partial I_D/\partial I_F$). An example of this type of circuit is shown in Figure 5. Q_1 is biased by R_1, R_2 and R_3 for a collector quiescent current of 20mA. R_3 is selected so that I_F varies from 15mA to 25mA for V_{IN} of 1V p-p. Under these operating conditions, the 6N136 operates in a region of almost constant incremental CTR. Linearity can be improved at the expense of signal-to-noise ratio by reducing I_F excursions. This can be accomplished by increasing R_3, then adding a resistor from the collector of Q_1 to ground to obtain the desired quiescent I_F of 20mA. Q_2 and Q_3 form a cascade amplifier with feedback applied through R_4 and R_6. R_6 is selected as V_{be}/I_3 with I_3 selected for maximum gain bandwidth product of Q_3. R_7 is selected to allow maximum excursions of V_{OUT} without clipping. R_5 provides DC bias to Q_3. Closed loop gain ($\Delta V_{OUT}/\Delta V_{IN}$) can be adjusted with R_4. The transfer function of the amplifier is:

$$\frac{V_{OUT}}{V_{IN}} \cong \left(\frac{\partial I_D}{\partial I_F}\right)\left(\frac{1}{R_3}\right)\left(\frac{R_4\ R_7}{R_6}\right)$$

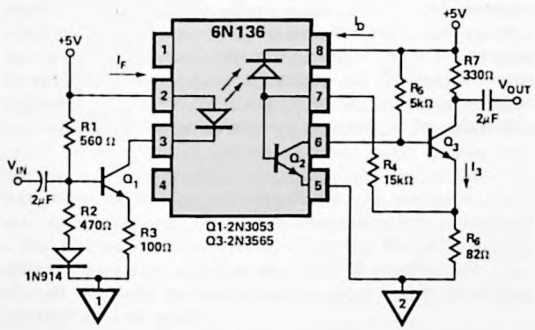


Figure 5. Wide Bandwidth AC Isolation Amplifier.

Typical Performance of the Wide Bandwidth AC Amplifier:

2% linearity over 1V p-p dynamic range
Unity voltage gain
10 MHz bandwidth
Gain drift: −.6%/°C
Common mode rejection: 22dB at 1 MHz
3000V DC insulation

DIGITAL ISOLATION TECHNIQUES

Digital conversion techniques can be used to transfer an analog signal between two isolated systems. With these techniques, the analog signal is converted into some digital form and transmitted through the optocoupler. This digital information is then converted back to the analog signal at the output. Since the optocoupler is used only as a switch, the overall circuit linearity is primarily dependent on the accuracy by which the analog signal can be converted into digital form and then back to the analog signal. However, the overall circuit bandwidth is limited by the propagation delays of the optocoupler.

Figure 6 shows a pulse width modulated scheme to isolate an analog signal. The oscillator operates at a fixed frequency, f, and the monostable multivibrator varies the duty factor of the oscillator proportional to the input signal, V_{IN}. The maximum frequency at which the oscillator can be operated is determined by the required linearity of the circuit and the propagation delay of the opto isolators:

$$(t_{max} - t_{min})\ (\text{required linearity}) \geq |t_{PLH} - t_{PHL}|$$

At the output, the pulse width modulated signal is then converted back to the original analog signal. This can be accomplished with an integrator circuit followed by a low pass filter or through some type of demodulator circuit that gives an output voltage proportional to the duty factor of the oscillator.

Figure 7 shows a voltage to frequency conversion scheme to isolate an analog signal. The voltage to frequency converter gives an output frequency proportional to V_{IN}. The maximum frequency that can be transmitted through the optocoupler is approximately:

$$f_{max} \approx \frac{1}{t}, \text{ where } t = t_{PLH} \text{ or } t_{PHL}, \text{ whichever is larger.}$$

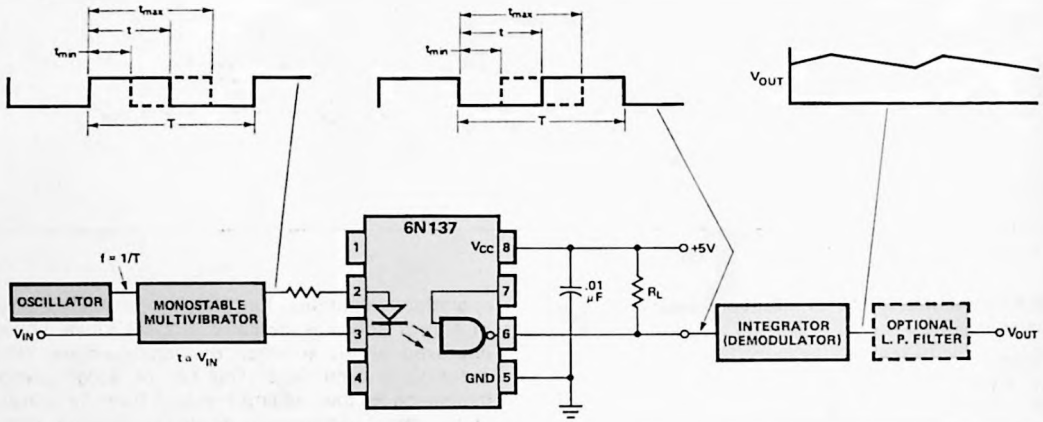


Figure 6. Pulse Width Modulation.

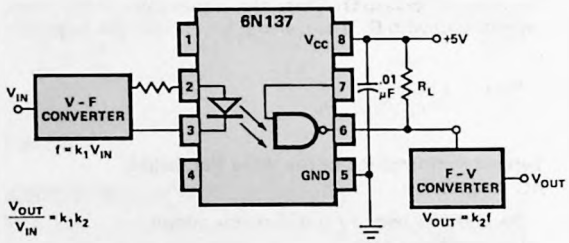


Figure 7. Voltage to Frequency Conversion.

At the output, the frequency is converted back into a voltage. The overall circuit linearity is dependent only on the linearity of the V-F and F-V converters.

Another scheme similar to voltage to frequency conversion is frequency modulation. A carrier frequency, f_o, is modulated by Δf such that $f_o \pm \Delta f$ is proportional to V_{IN}. Then at the output, V_{OUT} is reconstructed with a phase locked loop or similar circuit.

One further scheme to isolate an analog signal is to use A-D and D-A converters and transfer the binary or BCD information through optocoupler. The information can be transmitted through the optocoupler in parallel or serial format depending on the outputs available from the A-D converter. If serial outputs are not available, the A-D outputs can be converted into serial form with a PISO shift register and transmitted through one high speed optocoupler. This scheme becomes economical especially where high resolution is required allowing several optocouplers to be replaced with one high speed optocoupler. Refer to HP Application Note 947 for further discussion of digital data transmission techniques.

HEWLETT PACKARD

APPLICATION NOTE 1000

Digital Data Transmission With the HP Fiber Optic System

Fiber optics can provide solutions to many data transmission system design problems. The purpose of this application note is to aid designers in obtaining optimal benefits from this relatively new technology. Following a brief review of the merits, as well as the limitations, of fiber optics relative to other media, there is a description of the optical, mechanical, and electrical fundamentals of fiber optic data transmission system design. How these fundamentals apply is seen in the detailed description of the Hewlett-Packard system. The remainder of the note deals with techniques recommended for operation and maintenance of the Hewlett-Packard system, with particular attention given to deriving maximum benefit from the unique features it provides.

ELECTRICAL WIRE VS. FIBER OPTICS

In fiber optic cables, the signals are transmitted in the form of energy packets (photons) which have no electrical charge. Consequently, it is physically impossible for high electric fields (lightning, high-voltage, etc.) or large magnetic fields (heavy electrical machinery, transformers, cyclotrons, etc.) to affect the transmission. Although there can be a slight leakage of flux from an optical fiber, shielding is easily done with an opaque jacket, so signal-bearing fibers cannot interfere with each other or with the most sensitive electric circuits, and the optically-transmitted information is, therefore, secure from external detection. In some applications, optical fibers carry signals large enough to be energetically useful (e.g., for photocoagulation) and potentially harmful, but in most data communication applications, economy dictates the use of flux levels of 100μW or less. Such levels are radiologically safe and in the event of a broken or damaged cable, the escaping flux is harmless in explosive environments where a spark from a broken wire could be disastrous. Jacketed fiber optic cables can tolerate more mechanical abuse (crush, impact, flexure) than electrical cables of comparable size; moreover, fiber optic cables have an enormous weight and size advantage — for equivalent information capacity. Properly cabled optical fibers can tolerate any kind of weather and can, without ill-effect, be immersed in most fluids, including polluted air and water.

Bandwidth considerations clearly give the advantage to fiber optics. In either parallel- or coaxial-wire cable, the bandwidth varies inversely as the square of the length, while in fiber optic cable it varies inversely as only the FIRST power of the length. Here are some typical values for length, ℓ, in metres:

(1) $f_{3dB} = \frac{12{,}000}{\ell}$ MHz for HFBR-3000/-3100 cables

(2) $f_{3dB} = \frac{225{,}000}{\ell^2}$ MHz for typical 50Ω coax (RG-59)

For example, if ℓ = 100m, the 3dB frequency is only 22.5MHz for the coax cable, but for the fiber optic cable it is 120MHz.

The limitations of fiber optics arise mainly from the means for producing the optical flux and from flux losses. While the power into a wire cable can easily and inexpensively be made several watts, the flux into a fiber optic cable is typically much less than a milliwatt. Wire cable may have several signal "taps"; multiple taps on fiber optic cables are economically impractical at present.

The losses in a point-to-point fiber optic system are insertion loss at the input and output, connector loss, and transmission loss proportional to cable length. Variations in these losses require a receiver with a dynamic range capable of accommodating these variations and yet able to provide adequate BW (bandwidth) and SNR (signal-to noise) ratio at the lowest flux level. Fortunately, no noise is picked up by a fiber optic cable so the receiver SNR at any BW is limited only by the noise produced within the receiver.

Fiber optics is not the best solution to every data transmission problem; but where safety, security, durability, electrical isolation, noise immunity, size, weight, and bandwidth are paramount, it has a clear advantage over wire.

FIBER OPTIC FUNDAMENTALS

Flux coupled into an optical fiber is largely prevented from escaping through the wall by being re-directed toward the center of the fiber. The basis for such re-direction is the index of refraction, n_1, of the core relative to the index of refraction, n_2, of the cladding.

Index of refraction is defined as the ratio of the velocity of light in a given medium to the velocity of light in a vacuum.

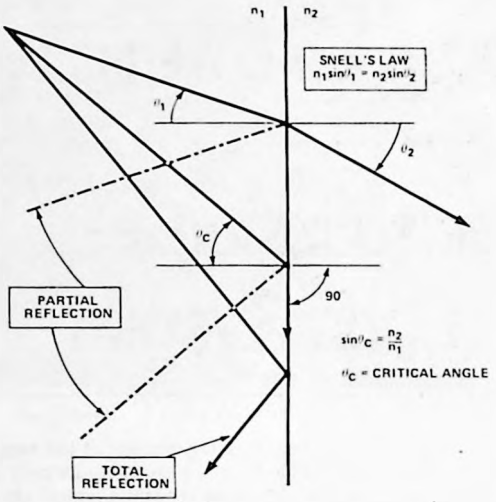


Figure 1. Snell's Law.

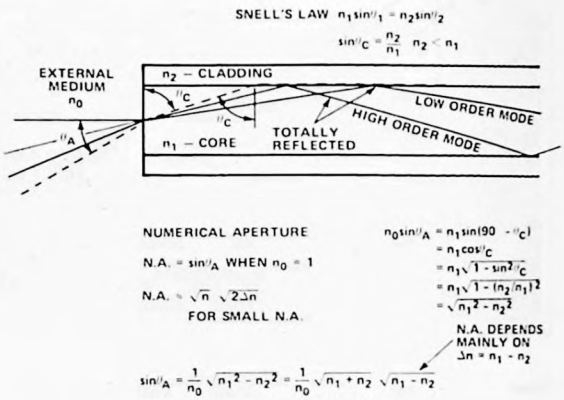


Figure 2. Total Internal Reflection.

As a ray of light passes from one medium into another of a different index of refraction, the direction changes according to Snell's Law:

(3) $n_1 \sin\theta_1 = n_2 \sin\theta_2$ SNELL'S LAW

This is illustrated in Figure 1. Notice that the relationship between the angles is the same, whether the ray is incident from the high-index side (n_1) or low-index side (n_2). For rays incident from the high-index side, there is a particular incidence angle for which the exit angle is ninety degrees. This is called the critical angle. At incidence angles less than the critical angle, there is only a partial reflection, but for angles greater than the critical angle, the ray is totally reflected. This phenomenon is called TOTAL INTERNAL REFLECTION (TIR).

Numerical Aperture.

Rays within the core of an optical fiber may be incident at various angles, but TIR applies only to those rays which are incident at angles greater than the critical angle. TIR prevents these rays from leaving the core until they reach the far end of the fiber. Figure 2 shows how the reflection angle at the core/cladding interface is related to the angle at which a ray enters the face of the fiber. The acceptance angle, θ_A, is the maximum angle, with respect to the fiber axis, at which an entering ray will experience TIR. With respect to the index of refraction, n_0, of the external medium, the acceptance angle is related to the indices of refraction of the core and cladding. When the external medium is air ($n_0 \approx 1$), the sine of the acceptance angle is called the NUMERICAL APERTURE (N.A.) of the fiber:

(4) NUMERICAL APERTURE, N.A. = $\sin\theta_A$

The derivation in Figure 2 applies only to meridional rays, i.e., rays passing through the axis of the fiber; skew rays (non-meridional) can also be transmitted, and these account for the observation that the reception and radiation patterns of optical fibers are not perfect step functions at the acceptance angle. For this reason, the practical definition of N.A. is somewhat arbitrary.

Modes of Propagation

Within the limits imposed by the N.A., rays may propagate at various angles. Those propagating at small angles with respect to the fiber axis are called LOW-ORDER MODES, and those propagating at larger angles are called HIGH-ORDER MODES. These modes do not exist as a continuum. At any given wavelength, there are a number of discrete angles where propagation occurs. SINGLE-MODE fibers result when the core area and the N.A. are so small that only one mode can propagate.

In addition to high- and low-order modes, there are others, called LEAKY MODES, which are trapped as skew rays — partly in the core, but mostly in the cladding where they are called CLADDING MODES. As implied by the term, leaky modes do not propagate as well as the more nearly meridional modes; their persistence, depending mainly on the structure of the optical fiber, ranges from less than a metre to more than fifty metres. The presence of leaky modes will, of course, affect the results obtained in measurement of N.A. and transmission loss, making them both artificially high. For this reason, N.A. is usually specified in terms of the EXIT N.A. for a fiber of length adequate to assure that leaky modes have effectively disappeared. Since most leaky mode propagation is in the cladding, it can be "stripped." Such cladding mode stripping is done by surrounding the unjacketed fiber with a material having a refractive index higher than that of the cladding.

EXIT N.A. is defined as the sine of the angle at which the radiation pattern (relative intensity vs. off-axis angle) has a particular value. This value is usually taken at 10% of the axial (maximum) value.

Transmission Loss

Regular core (non-leaky) modes also exhibit transmission losses. These are due to (1) scattering by foreign matter, (2) molecular (material) absorption, (3) irregularities at the core/cladding interface, and (4) microbending of the optical fiber by the cable structure. The first two loss mechanisms depend on the length of path taken by a ray; the third depends on the number of reflections of the ray before it emerges. It is clear from Figure 2 that the higher order modes have longer paths and more reflections with consequently higher loss. Larger N.A. fibers permit higher-order-mode propagation and, therefore, exhibit generally a higher transmission loss. Transmission loss is exponential and is, therefore, usually expressed in "dB per km." Coupling loss consideration usually favors larger N.A.

The four main loss mechanisms for coupling between fibers or between fibers and the optical ports of other devices are: (1) relative N.A.'s, (2) relative areas, (3) relative index gradings of the optical ports, and (4) Fresnel (reflection) loss. In addition to these, there may be coupling loss due to misalignment and/or separation of optical ports.

Relative N.A. loss can be ignored (≈ zero dB) whenever the N.A. of the receiving port (fiber or detector) is larger than the N.A. of the source port (flux generator or fiber), otherwise:

$$(5)\ \text{N.A. LOSS (dB)} = 20 \log \frac{\text{N.A. of Source Port}}{\text{N.A. of Receiver Port}} = \alpha_{NA}$$

Relative area loss can be ignored whenever the area of the receiver port is larger than the area of the source port, otherwise:

$$(6)\ \text{AREA LOSS (dB)} = 20 \log \frac{\text{Diam. of Source}}{\text{Diam. of Receiver}} = \alpha_A$$

In applying equation (6) to coupling between single fibers, the diameter to be used is the CORE DIAMETER.

Relative index grading loss can be ignored whenever the index grading coefficient for the receiving port is larger than the index grading coefficient of the source port, otherwise:

$$(7)\ \text{INDEX GRADING LOSS (dB)} = 10 \log \frac{1+\frac{2}{\alpha_R}}{1+\frac{2}{\alpha_S}} = \alpha_I$$

where

α_R = index grading coefficient of the receiving port

and

α_S = index grading coefficient of the source port

The index grading coefficient is described later under Construction of Fiber Optics.

Fresnel loss occurs when a ray passes from one medium to another having a different index of refraction. Part of the flux is reflected; the fraction transmitted is described by the transmittance, τ, so the loss is:

$$(8)\ \text{FRESNEL LOSS (dB)} = 10 \log \frac{1}{\tau} = 10 \log \frac{2+\frac{n_x}{n_y}+\frac{n_y}{n_x}}{4}$$

n_x = index of refraction of medium x
n_y = index of refraction of medium y

It is clear from equation (8) that the loss is the same in either direction. If two fibers are joined with an air gap between their faces, taking $n_x = 1$ for air and $n_y = 1.49$ for the cores of the fibers, the fiber-to-air Fresnel loss is 0.17dB. The air-to-fiber loss is the same, so the total airgap loss is 0.34dB. If several such connections are made, the loss could be high enough to make it worthwhile to use a coupling medium, such as silicone, to remove the air gap.

The use of a coupling medium is more significant when a fiber is coupled to an LED or IRED source. These sources are usually of gallium arsenide, or related substances, with a refractive index of 3.6. With such a high index of refraction, the use of an epoxy cement can reduce coupling loss by approximately 1dB. Figure 3 shows how the flux coupling is derived.

At the receiving end, where the silicon of the detector has an index of refraction of nearly 3.6, the Fresnel loss is also very high.

Fresnel losses at the emitter and detector surfaces can generally be ignored in designing systems with components having either connectors or pigtail fiber optic ports. This is possible because performance of such components is usually specified with reference to the external optical port so the internal Fresnel losses have already been taken into account.

Rise Time Dispersion

Bandwidth limitation in fiber optics is the result of a phenomenon called DISPERSION, which is a composite of MATERIAL dispersion and MODAL dispersion. Both of these relate to the velocity of flux transmission in the core. Velocity varies inversely as the index of refraction, and if the index of refraction varies over the wavelength spectrum of the source, the flux having a wavelength at which the refractive index is lower will travel faster than the flux having a wavelength at which the index is higher. Thus, all portions of the spectrum of flux launched simultaneously will not arrive simultaneously, but will suffer time dispersion due to differences in travel time. This is MATERIAL DISPERSION. It is reduced by using sources of narrow spectrum (e.g., lasers) or fibers with a core index of refraction which is constant over the source spectrum.

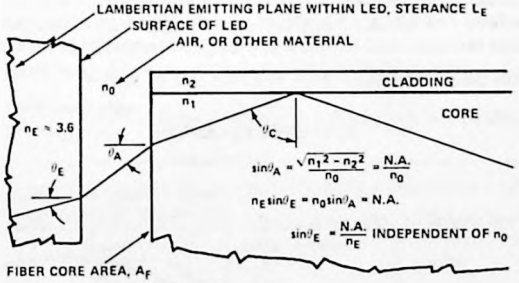


Figure 3. Acceptance Angle and Fresnel Loss Effects.

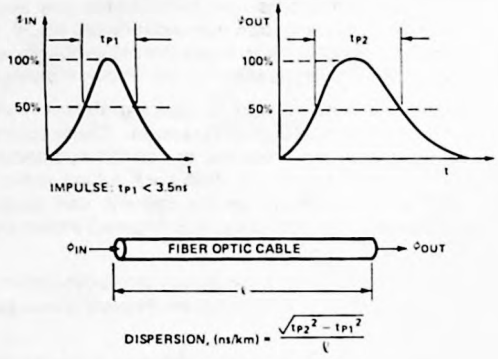


Figure 4. Rise Time Dispersion.

In Figure 2, notice that rays moving parallel to the axis travel a path length which is shorter than that of rays which are not paraxial. Those rays propagating in the higher-order modes will, therefore, have a longer travel time than those in lower-order modes, and simultaneously launched rays will suffer dispersion of their arrival times. This is MODAL DISPERSION. It can be reduced by reducing the N.A. (smaller acceptance angle) to allow only lower-order modes to propagate, or by using graded-index fiber.

Whether the dispersion is material or modal (or both), it is measured, as shown in Figure 4, by applying an impulse of flux and measuring the 3dB pulse widths at the input and output of a fiber long enough to exhibit significant dispersion. Time dispersion is then defined as

(9) RISE TIME DISPERSION

$$\frac{\Delta t}{\ell} \text{ (ns/km)} = \frac{1}{\ell} \left[t_{P2}^2 - t_{P1}^2\right]^{0.5}$$

where ℓ is the length (in kilometers) of the fiber and t_{P1} and t_{P2} are the 3dB widths in nanoseconds (or FWHM) of the pulses into and out of the fiber.

Modulation frequency response of a fiber has a 6dB per octave roll-off, so the effect of rise time dispersion can also be described in terms of a length-bandwidth product:

(10) 3dB BANDWIDTH • LENGTH (MHz • km) =

$$\frac{350}{\text{DISPERSION (ns/km)}}$$

Construction of Fiber Optics

Fibers having a sharp boundary between core and cladding, as in Figure 2, are called STEP INDEX fibers. The reflection at the boundary is not a "zero-distance" phenomenon — the ray, in being reflected, is actually entering a minute distance into the cladding and there is some loss. This loss can be seen as a faint glow along the length of unjacketed lossy fibers carrying visible flux. To reduce such reflection loss, it is possible to make the rays turn less sharply by reducing the index of refraction gradually, rather than sharply, from core to cladding. A fiber of such a form is called a GRADED INDEX fiber and the rays propagate as shown in Figure 5. Graded index fiber has not only a very low transmission loss, but modal dispersion is also very low. Higher-order modes do travel longer paths, but in the off-axis, lower-index regions they travel faster so the travel time differential between high-order and low-order modes is not as large as it is in step index fibers.

From the center of the core to the outer limit of the core (inner wall of the cladding) the grading of the index of refraction is described by the index grading coefficient, α, with this approximate relationship:

$$\left(\frac{n_1^2 - n^2}{n_1^2 - n_2^2}\right) = \left(\frac{r}{a}\right)^{\alpha} \quad \begin{array}{l}\text{at radius, r} \\ 0 < r < a\end{array}$$

where

a = radius of the core
n = index of refraction at r
n_2 = index of refraction at r = a
n_1 = index of refraction at r = 0

With $\alpha = 2$, the index of refraction profile is approximately parabolic, and modal dispersion is minimized. This is called fully graded index. However, as seen in Equation (7), there is additional coupling loss when flux is sent from a high-index fiber into a low-index fiber. For moderate distances and data rates there is some value of the index grading coefficient ($\alpha \approx 8$) that optimizes performance, resulting in what is called partially graded index. In step index fiber the grading coefficient is so high ($\alpha \approx 100$) that the index grading loss can be ignored.

Graded index fiber has higher coupling loss and may be more costly than step index fiber. It is, therefore, used mainly in applications requiring transmission over many kilometres at modulation bandwidths over 50MHz. For shorter distances and/or lower bandwidths, a variety of step index fibers are available at a variety of costs.

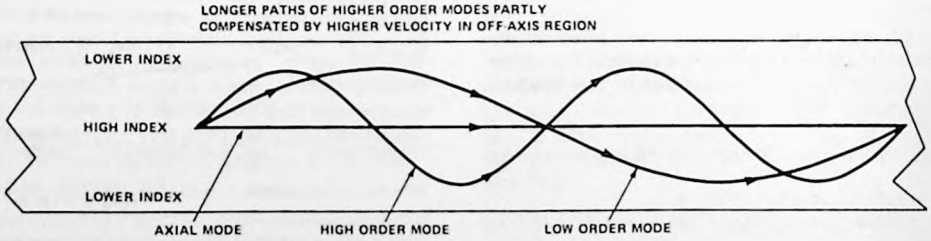


Figure 5. Graded Index Fiber Modes.

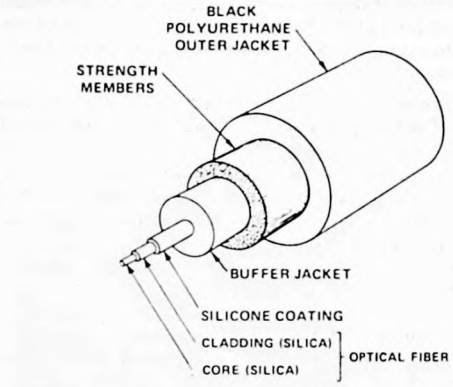


Figure 6. Step Index Fiber Optic Cable Construction.

Figure 6 shows the construction of a Hewlett-Packard fiber optic cable. Over the fused-silica, step-index, glass-clad fiber there is a silicone coating to protect the thin (20μm) cladding from scuffing. Over the buffer jacket are the tensile strength members, which allow the cable to be pulled through long conduits, and an outer jacket to protect the cable against crush and impact damage. This cable tolerates far more abuse than most wire cable. A sample was laid across the main entrance to the Hewlett-Packard headquarters and factory at 1501 Page Mill Road, Palo Alto. After several weeks of being driven over, night and day, there was no impairment of performance.

Other materials used in step index fibers are glass-clad glass, plastic-clad glass or fused silica, and plastic-clad plastic. These have N.A.'s ranging from less than 0.2 to more than 0.5, and transmission losses from less than 10dB/km to more than 1000dB/km. Some manufacturers offer bundled fibers in which the individual glass fibers are small enough to allow the cable to be very flexible. In earlier days of fiber optic development, bundled fibers were considered necessary for reliability because breakage of one or more fibers could be tolerated without total loss of signal transmission. Also, the large diameter of the fiber bundle allowed more tolerance in connector alignment. The popularity of fiber bundles has dwindled because the single-fiber cable durability is better than had been anticipated, and connectors are now available which are capable of providing the precise alignment required for low coupling loss with small-diameter single fibers.

Flux Budgeting

Flux requirements for fiber optic systems are established by the characteristics of the receiver noise and bandwidth, coupling losses at connectors, and transmission loss in the cable.

The flux level at the receiver must be high enough that the signal-to-noise ratio (SNR) allows an adequately low probability of error, P_e. In the Hewlett-Packard fiber optic system, the receiver bandwidth and noise properties allow a $P_e < 10^{-9}$ with a receiver input flux of 0.8μW under worst-case conditions. At higher flux levels, the P_e is reduced.

From the receiver flux requirement (for given P_e), the flux which the transmitter must produce is determined from the expression for a point-to-point system:

$$(11)\quad 10 \log \left(\frac{\phi_T}{\phi_R} \right) = \alpha_0 \ell + \alpha_{TC} + \alpha_{CR} + n\alpha_{CC} + \alpha_M$$

where ϕ_T is the flux (in μW) available from the transmitter
ϕ_R is the flux (in μW) required by the Receiver at P_e
α_0 is the fiber attenuation constant (dB/km)
ℓ is the fiber length (km)
α_{TC} is the Transmitter-to-Fiber coupling loss (dB)
α_{CC} is the Fiber-to-Fiber loss (dB) for in-line connectors
n is the number of in-line connectors; n does not include connectors at the transmitter and receiver optical ports
α_{CR} is the Fiber-to-Receiver coupling loss (dB)
α_M is the Margin (dB), chosen by the designer, by which the Transmitter flux exceeds the system requirement

Equation (11) is called the FLUX BUDGET and it is represented graphically in Figure 7. The same basic units (watts) are used for flux and for power, so it is correct and convenient to express flux in "dBm".

$$(12)\quad \phi(\text{dBm}) = 10 \log \left(\frac{\phi(\text{mW})}{1\ \text{mW}} \right) = 10 \log \left(\frac{\phi\ (\mu\text{W})}{1000\ \mu\text{W}} \right)$$

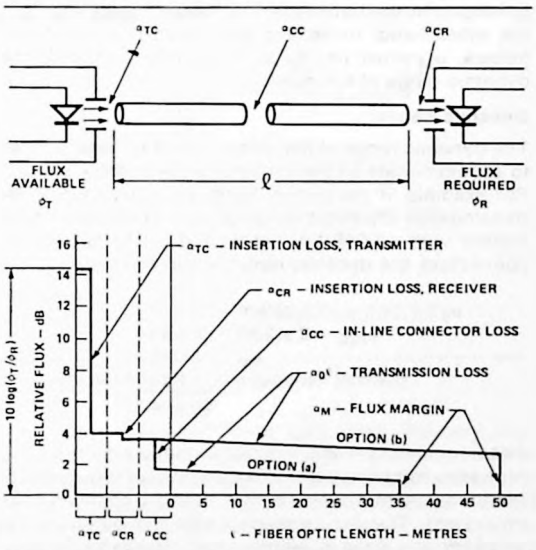


Figure 7. Flux Budget — Graphical Representation.

Here is an example of how the flux budget works:

1. Transmitter $\phi_T = 44\mu W^*$
2. Receiver $\phi_R = 1.6\mu W^*$ $\Big\rangle$ $10 \log \left(\frac{\phi_T}{\phi_R} \right) = 14.39\text{dB}$

*peak-to-peak

Transmitter optical port: N.A. = 0.5, diam. = 200μm, α = 100

Optical fiber (cable): N.A. = 0.3, core diam. = 100μm, α = 10

3. From Equations (5), (6), (7):

$$\alpha_{TC} = \alpha_{NA} + \alpha_A + \alpha_I$$

$$= 20 \log \left(\frac{0.5}{0.3} \right) + 20 \log \left(\frac{200}{100} \right) + 10 \log \left(\frac{1 + \frac{2}{10}}{1 + \frac{2}{100}} \right)$$

$$= 4.44\text{dB} + 6.02\text{dB} + 0.71\text{dB} = 11.17\ \text{dB}$$

Receiver optical port: N.A. = 0.5, diam. = 200μm, α = 100

4. Because the N.A., diameter, and α of the receiver are all larger than those of the fiber, there remains only a small amount of Fresnel loss, making $\alpha_{CR} \approx 0.17$ dB.

APPLICATIONS

5. Apply equation (11) to see what the flux budget allows:

$$14.39dB = \alpha_0 \ell + 11.17dB + n\alpha_{CC} + 0.17dB + \alpha_M$$

$$\alpha_0 \ell + n\alpha_{CC} + \alpha_M = (14.39 - 11.17 - 0.17)dB = 3.05dB$$

6. In accounting for cabling losses, two options are considered:

   (a) with one in-line connector, possibly to allow for later insertion of a repeater. Taking 2.0dB for the connector leaves:

$$\alpha_0 \ell + \alpha_M = 3.05 - 2.0 = 1.05dB$$

   With cable having attenuation of 20dB/km a length of 35 metres leaves:

$$\alpha_M = 1.05 - (0.02dB/m)(35m) = 0.35dB$$

   (b) Without in-line connector, there is only attenuation to consider. A length of 50 metres leaves:

$$\alpha_M = 3.05 - (0.02dB/m)(50m) = 2.05dB$$

In flux budgeting, α_M should always be large enough to allow for degradation of the efficiency of the flux generator in the transmitter (LED, IRED, laser, etc.). On the other hand, in dealing with more powerful transmitters, α_M must not be so large that it exceeds the dynamic range of the receiver.

Dynamic Range

The dynamic range of the receiver must be large enough to accommodate all the variables a system may present. For example, if the system flexibility requirement is for transmission distances ranging from 10 metres to 1000 metres with 12.5dB/km cable, and up to two in-line connectors, the dynamic range requirement is:

$$\begin{aligned} \alpha_0 \ell = 1km \times 12.5dB/km &= 12.5dB \\ n\alpha_{CC} = 2 \times 2dB &= 4.0dB \\ \alpha_M &= 3.0dB \\ \text{thermal variations} &= 1.0dB \text{ (estimated)} \\ &\overline{\quad 20.5dB} \end{aligned}$$

Accommodating a 20dB dynamic range plus providing high sensitivity requires the receiver to have two important features: automatic level control, and a-c coupling or its equivalent. The a-c coupling keeps the output of the amplifier at a fixed quiescent level, relative to the logic thresholds, so that signal excursions as small as the specified minimum can cause the amplifier output to exceed the logic threshold. This function can also be called d-c restoration.

ALC (automatic level control) adjusts the gain of the amplifier. Low-amplitude excursions are amplified at full gain; high-amplitude excursions are amplified at a gain which is automatically reduced enough to prevent saturation of the output amplifier. Saturation affects propagation delay adversely so ALC is needed to allow high speed performance at high, as well as low, signal levels.

HEWLETT-PACKARD'S FIBER OPTIC SYSTEM

A number of objectives were established as targets for this development. Convenience and simplicity of installation and operation were the primary objectives, along with a probability of error $P_e < 10^{-9}$ at 10Mb/s NRZ, over moderate distances. In addition, there were the traditional Hewlett-Packard objectives of rugged construction and reliable performance. Manufacturing costs had to be low enough to make the system attractively priced relative to its performance.

Electrical convenience is provided by several system features. The Receiver and the Transmitter require only a single +5-volt supply. All inputs and outputs function at TTL logic levels. No receiver adjustments are ever necessary because the dynamic range of the Receiver is 21dB or more, accommodating fiber length variations as well as age and thermal affects. When the system is operated in its internally coded mode, it has NRZ (arbitrarily timed data) capability and is no more complicated to operate than a non-inverting logic element. Built-in performance indicators are available in the Receiver; the Link Monitor indicates satisfactory signal conditions and the Test Point allows simple periodic maintenance checks on the system's flux margin.

There are also several optical and mechanical convenience features. The optical ports of the Transmitter and Receiver are well defined by optical fiber stubs built into receptacles that mate with self-aligning connectors. Low-profile packaging and low power dissipation permit the modules to be mounted without heat-sink provision on P.C. boards spaced as close as 12.5mm (0.5 in.).

The internally-coded mode of operation is the simplest way to use the Hewlett-Packard system. This mode places no restriction on the data format as long as either positive or negative pulse duration is not less than the minimum specified. The simplicity is achieved by use of a 3-level coding scheme called a PULSE BI-POLAR (PBP) code. This mode is selected simply by applying a logic low (or grounding) to the Mode Select terminal on the Transmitter — no conditioning signal or adjustment is necessary in the Hewlett-Packard Receiver because it automatically responds to the PBP code.

The externally coded mode makes the waveform of the output flux a digital replica of the Data Input signal. This 2-level mode is called the FULL ON-OFF (FOO) mode; it is selected by applying a logic high (or V_{CC}) to the Mode Select terminal. When used with the Hewlett-Packard Receiver, the FOO mode must have a Data Input signal with a 50% duty factor, as seen later.

Transmitter Description

Figure 8 shows symbolically the logical arrangement of the Transmitter, and waveforms for the output flux. The arrangement shown is logically correct but circuit details are not actually realized as shown. For example, the current sources actually have partial compensation for the negative temperature coefficient of the LED (or IRED). In Figure 8, there are five important things to notice.

First, notice that the bias current, I_C, is never turned off — not even when the Transmitter is operated in the externally coded mode (Mode Select "high"). This is done to enhance the switching speed of the LED (or IRED) in either internally- or externally-coded mode. The bias current also stabilizes the flux excursion ratio (k in Equation 14) symmetry in the internally-coded mode.

Second, notice that

ϕ_L, the low-level flux, is produced by I_C
ϕ_M, the mid-level flux, requires $I_B + I_C$
ϕ_H, the high-level flux, requires $I_A + I_B + I_C$

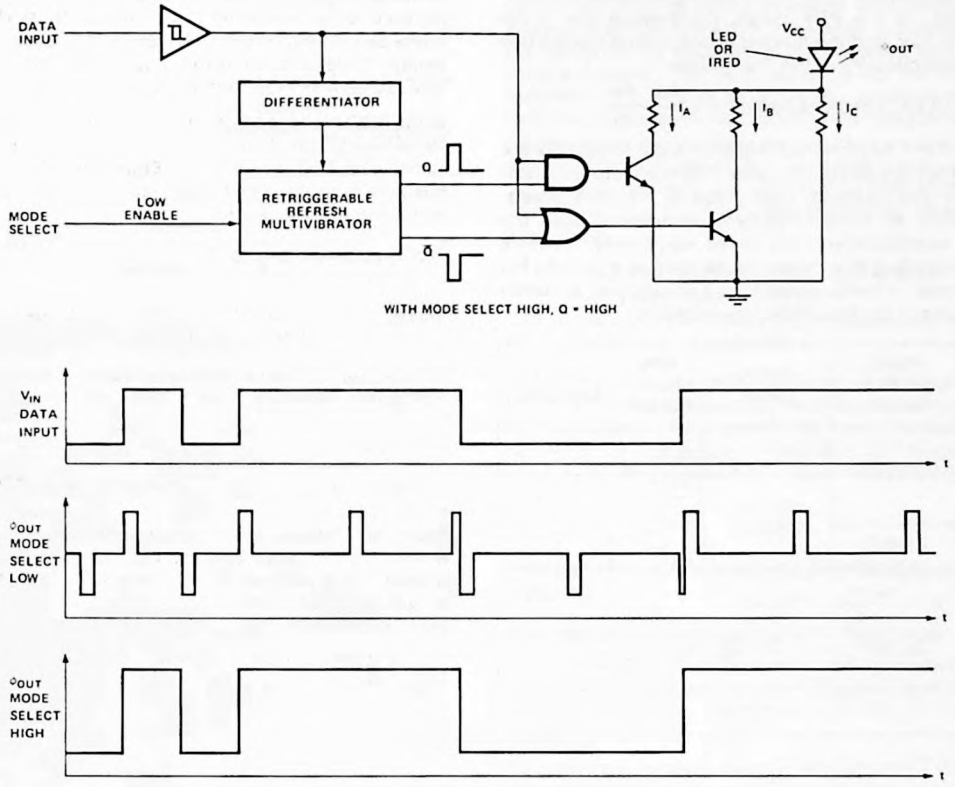


Figure 8. Transmitter Block Diagram and Waveforms.

As far as the Receiver is concerned, the excursion flux, $\Delta\phi$, produced by switching I_A and I_B, is the important parameter of the Transmitter. Average flux is, of course, related to excursion flux but is not as important in establishing the SNR of the system.

Third, notice that with Mode Select "low" and a 500kHz signal at Data Input, there will be only one refresh pulse generated in each logic state. The excursions (ϕ_H-ϕ_M) and (ϕ_M-ϕ_L) are nearly balanced so an average-reading flux meter will indicate the mid-level flux, ϕ_M, within +0.6% or -0.6% depending on whether the flux excursion ratio, k, is at its maximum or at its minimum limit.

Fourth, notice that, with Mode Select "low", any Data Input transition (either H-L or L-H) retriggers the Refresh Multivibrator to start a new train of pulses. All refresh pulses for either logic state have the same duration. This keeps the average flux very near the mid-level even when the duration in either logic state of arbitrarily timed input data is very short. Notice also that any refresh pulse is overridden (abbreviated) by the occurrence of a Data Input transition so there is additional jitter (≈ 15ns) when the duration of the Data Input in either state is the same length of time as the refresh interval. The refresh interval is very long, relative to the refresh pulse duration, making a duty factor of approximately 2%, this also is done to keep the average flux near mid-level regardless of how long Data Input remains in either logic state. The only condition under which the average flux can deviate significantly from the mid-level occurs when Data Input remains in one state for a period of time LESS than the duration of the refresh pulse. If this is likely to occur, the format should be configured so the numbers of 1's and 0's are balanced as they would be in Manchester code. Observing this data format allows the use of the internally-coded mode of the Hewlett-Packard system at data rates ranging from arbitrarily low to higher than 10M baud, with the absolute limit being that at which the signal intervals become as short as t_{PHL} and/or t_{PLH}.

Fifth, notice that with Mode Select "high," the Q output of the Refresh Multivibrator is "high" (and $\overline{Q}$ is "low"). Under this condition, I_A and I_B are both ON when Data Input is "high" and both OFF when it is "low". This makes the output flux excursion a logical replica of the Data Input.

Flux Measurement

The Transmitter has two important flux parameters, flux excursion and flux excursion ratio. The flux excursion is defined as half of the peak-to-peak value:

(13) FLUX EXCURSION, $\Delta\phi = \frac{\phi_H - \phi_L}{2}$

Flux excursion ratio is defined as the ratio of excursion above the average level to the excursion below the average value. In the PBP mode, the average flux is the mid-level flux, and the flux excursion ratio is established by internal circuitry of the Transmitter:

(14) FLUX EXCURSION RATIO, $k = \frac{\phi_H - \phi_M}{\phi_M - \phi_L}$

Ideally, k = 1 because the Receiver logic thresholds are referred to the average flux level, and therefore specifications for the "k-factor" are given in the data sheets. Verification of these important parameters does not require sophisticated high-speed equipment; a simple average-reading flux meter can be used by operating the Transmitter in three conditions and applying a simple calculation to the flux meter observations:

STEP	MODE SELECT (MODE)	DATA INPUT	AVG. FLUX OUTPUT	FLUX OBSERVED
1	H (FOO)	L	ϕ_L	A
2		500 kHz 50% D.F.	$\frac{\phi_H + \phi_L}{2}$	B
3	L (PBP)		ϕ_M	C

$$\Delta\phi = \frac{\phi_H - \phi_L}{2} = (B - A)$$

$$k = \frac{\phi_H - \phi_M}{\phi_M - \phi_L} = \frac{\phi_H - \phi_L}{\phi_M - \phi_L} - 1 = \frac{2\,(B - A)}{C - A} - 1$$

It appears that the observation might be further simplified by omitting the 500-kHz modulation in Step 2, and measuring ϕ_H directly by making Data Input a steady High, with Mode Select High (FOO). However, this would raise the emitter diode junction to an unrealistically high temperature and give an incorrect measurement.

In the FOO mode there is, of course, no mid-level of flux. Nevertheless, the definition of flux excursion ratio is the same as for PBP mode, and in Equation (14) the average flux value is used in place of the mid-level flux, ϕ_M. In FOO mode, the average flux is:

(15) AVERAGE FLUX (FOO mode) $= \frac{\phi_H \Sigma t_H + \phi_L \Sigma t_L}{\Sigma t_H + \Sigma t_L}$

where Σt_H is the total time the flux is at level ϕ_H
Σt_L is the total time the flux is at level ϕ_L

Substitution of the expression in Equation (15) for ϕ_M in Equation (14) leads to:

(16) FLUX EXCURSION RATIO = $k = \frac{\Sigma t_L}{\Sigma t_H}$

Equation (16) shows why it is that when the FOO mode is used (e.g., with Mode-Select "high" in the Hewlett-Packard Transmitter) the data input signal must, on average, have a 50% duty factor to make k = 1. That is, in the averaging interval, the total number of "mark" intervals should be equal to the total number of "space" intervals, such as in Manchester code.

Use of the FOO mode also requires that the input flux remain for less than 5μs at either high or low level. This is

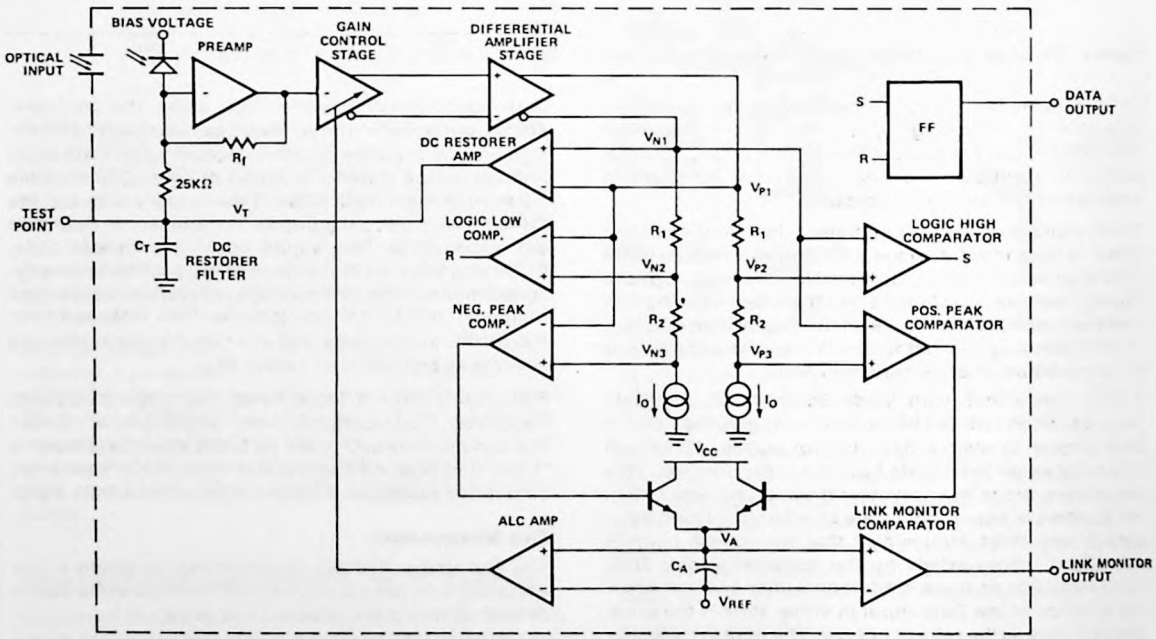


Figure 9. Receiver Block Diagram.

necessary to avoid "pulling" the receiver dc restorer voltage too far away from the value corresponding to the average flux, and possibly losing occasional bits.

Receiver Description

The Hewlett-Packard Receiver block diagram is shown in Figure 9. There are four functional blocks:

1. The amplifier, including a gain-control stage and split-phase outputs with a voltage divider for each.
2. The dc-restorer with a long time constant.
3. Logic comparators with an R-S latch.
4. Positive and negative peak comparator with single-ended output for the ALC and link monitor circuits.

Optical flux at the input is converted by the PIN photodiode to a photocurrent, I_P, which is converted to a voltage by the PREAMPLIFIER. This voltage is amplified to a positive-going output, V_{P1}, and a negative-going output, V_{N1}. A rising input flux will cause V_{P1} to rise and V_{N1} to fall. These voltages are applied to the differential inputs of the DC RESTORER AMPLIFIER whose output, V_T, falls until it is low enough to draw the average photocurrent away from the preamplifier via the 25k resistor. This makes $V_{P1} \approx V_{N1}$ when the input flux is at the average level. The output impedance of the dc restorer amplifier is very high, making a long time constant with the filter capacitor, C_T. The long time constant is required for loop stability when input flux levels are so low that there is little or no ALC gain reduction, with consequently high loop gain. With no input flux, $V_T = V_{TMAX}$; as input flux rises, V_T falls proportionately, so the voltage at the TEST POINT can be used as an indicator of the average input flux. With respect to the Receiver optical port, the responsivity of the PIN photodiode is approximately 0.4A/W, leading to the expression:

$$(17)\ \text{AVERAGE INPUT FLUX}, \phi_{AV}\ (\mu W) = \frac{|V_{TMAX} - V_T|\ (mV)}{10}$$

where V_{TMAX} = Test Point Voltage with no optical input signal.

The instrument for observing V_T must not load the Test Point significantly, so an input resistance of 10MΩ is recommended.

As described above, when the input flux is at the average level, the positive-going and negative-going output voltages V_{P1} and V_{N1} are approximately equal. Notice that this makes the outputs of both logic comparators low. A positive flux excursion, rising faster than the dc restorer (with its long time constant) can follow, will cause V_{P1} to rise and V_{N1} to fall. If the positive flux excursion is high enough, the LOGIC HIGH COMPARATOR input voltage ($V_{P2} - V_{N1}$) becomes positive, and a SET pulse is produced for the R-S flip-flop. [Similarly, a negative flux excursion of such amplitude would make ($V_{N2} - V_{P1}$) become positive and a RESET pulse would be produced.] A larger amplitude of positive flux excursion would make the POSITIVE PEAK DETECTOR input voltage ($V_{P3} - V_{N1}$) change from negative to positive and cause current to flow into the ALC FILTER capacitor. When the voltage V_A starts to rise above V_{REF}, the ALC AMPLIFIER output will operate on the GAIN CONTROL AMPLIFIER to limit the Receiver's forward gain. Notice that the ALC action is the same for a negative flux excursion, so that the Receiver's gain limitation is determined EITHER by positive flux excursion OR by negative flux excursion — whichever is the larger. For this reason, the positive and negative excursions must be nearly balanced with respect to the average flux. The allowable imbalance is determined by the values of the resistors in the negative and positive voltage dividers. The ALC action limits the maximum excursion to a voltage $I_O\ (R_1 + R_2)$, whereas the logic threshold is only $I_O R_1$. Actual limits are established by the tolerances on the resistors and current sources. Notice that the ALC voltage, V_A, activates both the ALC COMPARATOR and the LINK MONITOR COMPARATOR. Therefore, a "high" LINK MONITOR signifies two conditions:

1. The input flux excursions are high enough to cause ALC action (gain limitation).
2. The excursions are more than adequate for operation of the logic comparator.

Notice that the LINK MONITOR could be "high," but it could be outside the specified limits such that P_e exceeds 10^{-9}. Conversely, because of safety margin in the Receiver design, it is also possible to have $P_e < 10^{-9}$ when the flux excursions are too small to make the LINK MONITOR "high".

OPERATION OF THE HEWLETT-PACKARD SYSTEM

With Hewlett-Packard Components Exclusively

The main concern in a fiber optic link is the flux budget. Other areas of concern are: data rate, data format, and the interface with other elements of a data transmission system.

Flux budgeting, using the Hewlett-Packard Transmitter, Receiver, Connector, and Cable components is very straight forward for most applications. It is necessary only to use the data sheet information correctly in making the coupling loss and transmission loss allowances.

When used with other Hewlett-Packard components, the optical characteristics of the Receivers are not critical. Their optical ports have a diameter and N.A. which are both greater than the size and N.A. of the Hewlett-Packard Cable. The Receivers also have a high responsivity and the spectral response is nearly constant over the spectrums radiated by Hewlett-Packard Transmitters.

With Components From Other Manufacturers

When using the Hewlett-Packard Receivers with other cables, it may be necessary to account for N.A. loss and/or area mismatch loss. When other sources are used, it may be necessary to compute an effective flux ratio:

$$(18)\ \text{EFFECTIVE FLUX RATIO, EFR}_S = \frac{\int \phi_\lambda R_{r\lambda} d\lambda}{\int \phi_\lambda d\lambda}$$

(Source Spectrum)

where $R_{r\lambda}$ is the relative response of the Receiver (from data sheet)

ϕ_λ is the spectral flux function of the source

If the transmission loss of the cable varies sharply over the wavelength range of the source spectrum, then the spectral transmittance of the cable should be included in the computation of EFR. The spectral transmittance varies

APPLICATIONS

with cable length, so the integration must be performed using the cable length required in a particular installation:

$$(19)\ \text{EFFECTIVE FLUX RATIO (Cable and Source)},\ EFR_{CS} = \frac{\int \tau_\lambda \phi_\lambda R_{r\lambda} d_\lambda}{\int \tau_\lambda \phi_\lambda d_\lambda}$$

where τ_λ is the spectral transmittance of the installed length of fiber optic cable, computed as:

$$(20)\ \tau_\lambda = 10^{-\left(\frac{\ell}{10}\right)\alpha_{0\lambda}}$$

where $\alpha_{0\lambda}$ is the spectral function in (dB/km) of the fiber optic cable and ℓ is the installed cable length (km)

Notice that as the length is reduced, τ_λ becomes more nearly a constant and may be factored out of both numerator and denominator of Equation (19). When EFR is significantly less than unity, it enters the flux budget expression, Equation (11).

$$(21)\ 10 \log\left(\frac{\phi_T}{\phi_R}\right) = \alpha_{TC} + \alpha_{CR} + n\alpha_{CC} + \alpha_0 \ell + \alpha_M \underset{-10 \log (EFR)}{}$$

See Equations 11, 18, and 19 for definition of terms.

The optical ports of Hewlett-Packard Transmitters are designed for mating with Hewlett-Packard Cable/Connector assemblies, but their characteristics require a little more attention than do the Receiver optical ports. The Transmitter and Cable/Connector data sheets should be consulted for the correct values of size and N.A., or for the directly-given value of transmitter-to-fiber coupling loss, α_{TC}, to use in flux budgeting. In applications having very short transmission distances, but requiring a number of in-line (cable-to-cable) connections, it is likely to be advantageous to use fiber optics of larger core diameter and N.A., such as some of the plastic types. The larger core diameter reduces the likelihood of losses in connectors due to misalignment. Depending on the size and N.A. of the Transmitter optical port, a larger core diameter and N.A. in the fiber optic cable may also reduce α_{TC}, but if the cable core diameter is too large, the cable-to-receiver loss, α_{CR}, may be excessive.

Data Rate and Format

The other areas of concern (data rate, data format, and interface) are interactive, depending on system requirements. In any single transmitter-to-receiver link, the flux budget along with probability of error P_e, establish the signaling rate, in baud units (symbols per second), while the data rate, in bits per second, depends also on the data format, or transmission code. NRZ (Non-Return-to-Zero) is the term for a transmission code in which the signal does not periodically return to zero. If a stream of NRZ data contains a series of consecutive "1s", the signal remains at the "1" level; similarly, the signal remains at the "0" level for consecutive "0s". RZ (Return-to-Zero) code signals a "1" by changing from low level to high level and back, never remaining at high level for a period of time longer than half a bit interval. Some examples of codes are given in Figure 10. Notice that NRZ code uses the channel capacity most efficiently since it requires only one code symbol per bit. The RZ code illustrated uses two code symbols per bit while other codes may require an even higher channel capacity for a given data rate. NRZ code requires a clock signal at the receiving end to define, for each interval, the point in time at which the data is valid. The time at which the data is clocked must be sufficiently clear of the interval edges to avoid phase-shift errors due to jitter, rise time, or propagation delay. Since the clock signal is separately transmitted, phase shift in the clock channel can contribute to the phase-shift error unless it is equal, in direction and magnitude, to the phase shift in the data channel. For this reason, fiber optic channels carrying clock signals should use the same type of cable and the same length, unless the transmission distance is very short. Note that the transmission time delay in an optical fiber depends on the core index of refraction:

$$(22)\ \text{TRANSMISSION DELAY},\ t_\ell = \left(\frac{1}{c}\right)\ell n$$

where c is the velocity of light in a vacuum, $c = 3 \times 10^8$ m/s
ℓ is the fiber optic cable length (m)
n is the core index of refraction

and differential delay between a data channel and a clock channel is:

$$(23)\ \text{DIFFERENTIAL DELAY},\ t = \left(\frac{1}{c}\right)[\ell_2 n_2 - \ell_1 n_1]$$

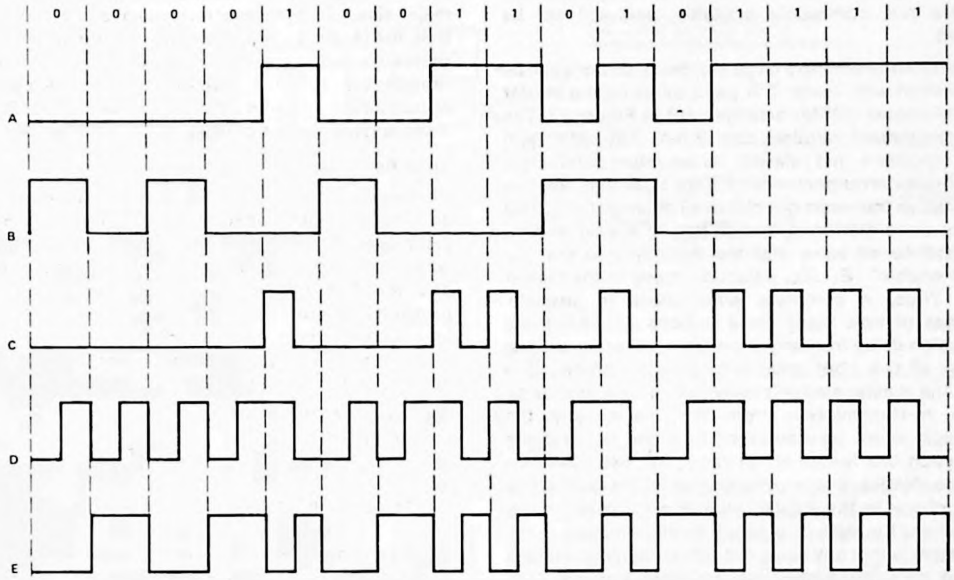
Some codes are self-clocking — i.e., a separate channel to transmit the clock signal is not required, so there is no problem with differential delay. For this reason, self clocking codes may be preferred even though the data rate is less than that of NRZ. Note that in its internally coded mode, the Hewlett-Packard fiber optic system transmits either NRZ or codes of arbitrary format and duty factor. In the externally coded mode, the system requires the duty factor of the code to be 50% and the signal must remain LESS than 5μs in either high state or low state.

The Hewlett-Packard system is capable of a 10 Mbaud signaling rate. If a higher data rate is required, the data stream can be divided among additional channels. If each channel is coded, such as with Manchester code, the capacity of each channel is 5Mb/s and if the total data rate requirement is 20Mb/s, four channels are required. Using NRZ, the 20Mb/s data can be transmitted on two channels, with a third channel for the clock signal. Thus, if the data rate requirement exceeds 15Mb/s, the NRZ format requires fewer fiber optic channels.

System Configuration

The simplex arrangement in Figure 11 allows data in one direction only, and the format should, therefore, include error checks, such as parity bits. The full duplex arrangement requires two Transmitter/Receiver (T/R) pairs and two cables but allows data to go in both directions simultaneously. If, at a given time, Station 1 is transmitting, the return transmission from Station 2 can be unrelated to the information from Station 1, but could also be a relay or re-transmission of the data received by Station 2, so a logic delay and comparator circuit in Station 1 can check for errors and allow corrections. The same is true for the full triplex arrangement. Extension to larger numbers of stations is possible and the benefits are the same, but the number of T/R pairs increase rapidly, as shown by the series in Figure 11, requiring n (n-1) T/R pairs for n stations.

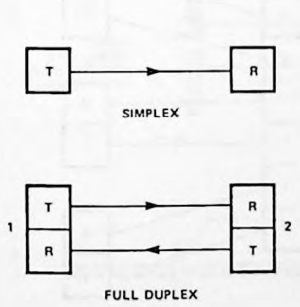
Half-duplex (not illustrated) is a means for allowing two stations to alternately use the same transmission medium. With a wire cable, half-duplex operation is commonly and easily done; it can also be done with fiber optic cable but

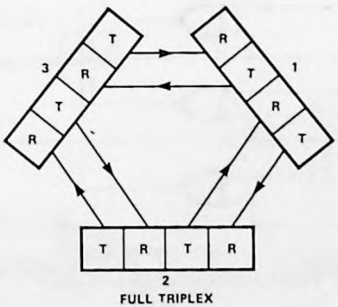


	CODE	DESCRIPTION	CHANNEL REQUIRED	REQUIRES DC?	REQUIRES CLOCK?
A	NRZ (NON-RETURN TO ZERO)	High during entire "mark", low during entire "space" interval	1 Mbaud per Mb/s	YES	YES
B	NRZI (NRZ INVERTABLE) (SELF-CLOCKING)	Transition for "space" No transition for "mark"	1 Mbaud per Mb/s	YES	NO*
C	RZ (RETURN TO ZERO)	Low during entire "space", momentarily high during "mark" interval	2 Mbaud per Mb/s	NO	YES
D	MANCHESTER (SELF-CLOCKING)	Positive transition for "space", negative transition for "mark"	2 Mbaud per Mb/s	NO	NO
E	BIPHASE MARK (MANCHESTER II) (SELF-CLOCKING)	Each bit period begins with a transition. "Space" has NO transition during bit period — "mark" has one transition during bit period	2 Mbaud per Mb/s	NO	NO

NOTE THAT C, D, E HAVE 50% DUTY FACTOR (k = 1.00)
*WITH PHASE-LOCK LOOP AND BIT STUFFING

Figure 10. Examples of NRZ and RZ Code Patterns.





NO. OF STATIONS	NO. OF T/R PAIRS
2	2
3	6
4	12
5	20
n	n(n-1)

Figure 11. Simplex, Full-Duplex, Full Triplex, Full-n-plex Fiber Optic Links.

APPLICATIONS

the fiber-furcating couplers for accomplishing it are very lossy, are not commonly available, and will not be discussed.

Data interchange among a large number of stations can be accomplished with fewer T/R pairs by using the Master Station Multiplex (MSM) arrangement in Figure 12. The MSM arrangement requires only 2(n-1) T/R pairs for n stations (master + (n-1) slaves). Its operation differs from the full n-plex arrangement of Figure 11 in that only the master station transmits directly to all other stations. Data from any slave station is transmitted to master and re-transmitted to all slave stations according to the "re-transmit enable" (E_1...Ex) selection made in the master station. Thus, a complete error check is possible. Regardless of how many slave stations are added, the transmission delay from any slave to any other slave is just the delay of two fiber optic links plus the propagation delay in the master station's relay circuit. The time delay between re-transmission from the master and the error-check return transmissions from the slaves is the same if each link length is the same, i.e., two links plus relay time. Notice that a complete error check requires an error check in the master, plus an error check in the station where the data originated. Another feature of the MSM system is that any slave station can be disconnected or turned off without affecting the other stations. With slightly more complicated relay control logic in the master stations, the MSM system can provide even more flexibility in the control of data movement — the schematic in Figure 12 is intended only to illustrate the potential flexibility of MSM.

At the expense of less flexibility and longer transmission delay, multiplex operation can be done with an even smaller number of T/R pairs by means of Looped-Station Multiplexing (LSM) as in Figure 13. In addition to requiring only n T/R pairs for n stations, LSM offers the advantage that an error check is required only at the station from which the data originates. There are some disadvantages. A relatively minor disadvantage is the data delay around the loop to where the data originated. A less minor disadvantage is the fact that, even if one of the stations in the loop is designated for loop control, it does not have control as absolute as that of the master station in MSM. A major disadvantage is that removal of one or more stations from the loop may require a re-run of the fiber optic cable unless the flux budget allows insertion of a connector to replace the station(s) removed. There is some error accumulation around the loop, but this is not a disadvantage if error correction is applied.

Error Accumulation

Where error correction is inconvenient or impossible, the accumulation of error through data relay units may be significant. With Hewlett-Packard components operated within the limits prescribed by the data sheet parameters and the flux budget, any point-to-point link has a probability of error $P_e < 10^{-9}$. This means that $P_e < 10^{-9}$ as long as the loss margin, α_M(dB) is above zero. With a number, n, of repeater links, the worst case estimate of cumulative probability of error is the RMS value:

(24) CUMULATIVE PROBABILITY OF ERROR,

$$P_{e,n} = 1 - \prod_{i=1}^{n} (1 - P_{e,i}) \approx \sum_{i=1}^{n} P_{e,i}$$

where $P_{e,i}$ is the probability of error in link "i"

If each link has the same probability of error, P_e, then the cumulative value of P_e is estimated at:

(25) CUMULATIVE PROBABILITY OF ERROR FOR EQUAL P_e's $\quad P_{e,n} \approx nP_e$

However, as in any chain, the probability of error is usually just that of the "weakest link," that is, the link having the highest probability of error.

Measuring the probability of error can be very time-consuming if P_e has a very low value. For instance, if $P_e = 10^{-9}$ at 10 Mbaud (BER = 10^{-9}), this suggests that if the system is operated for 100 seconds at 10 Mbaud (accumulate 10^9 bits) with one error, the $P_e = 10^{-9}$ is verified. This is not necessarily true. The significance of $P_e = 10^{-9}$ is that over several such periods the average error is one per 100 seconds. A less time-consuming procedure is to lower the signal (flux) level until the error rate, $P_{e,N}$ is measurably high in a comfortable period of time, and note

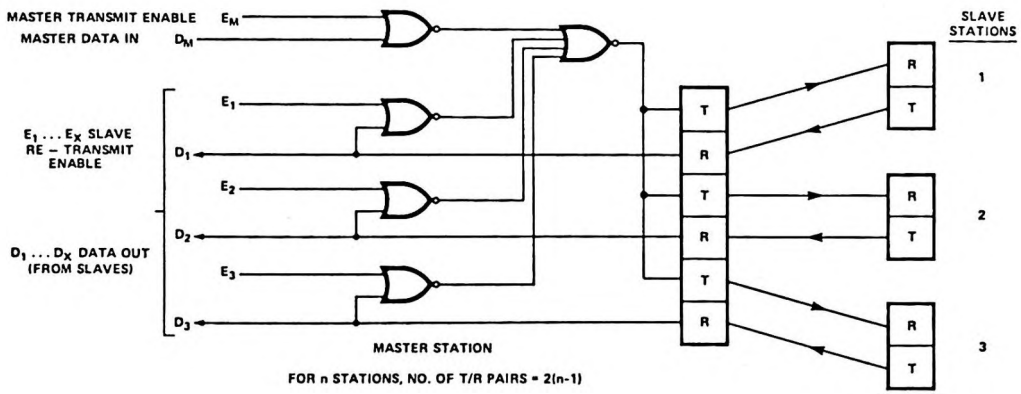


Figure 12. Master Station Multiplex Arrangement for Fiber Optic Links.

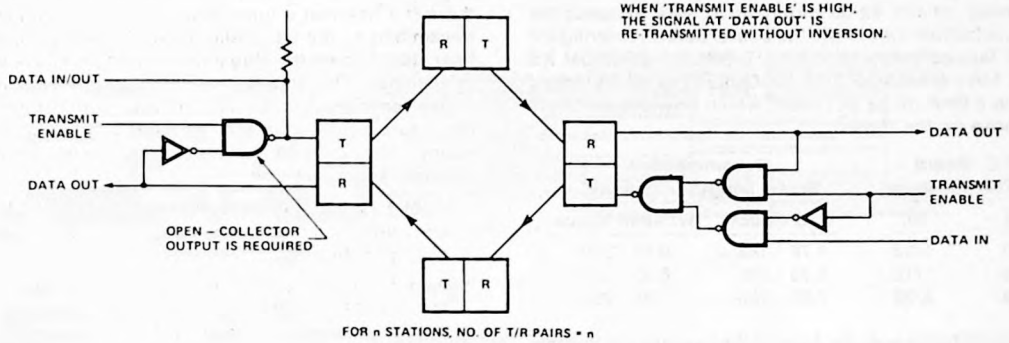


Figure 13. Looped-Stations Multiplex Arrangement for Fiber Optic Links.

the Bit Error Rate (BER) as a function of flux level into the Receiver. At these lower levels of flux, the Probability of Error (P_e) is:

$$P_e = BER = \frac{\text{NO. OF ERRORS IN A PERIOD}}{\text{NO. OF BITS IN SAME PERIOD}}$$

Since the occurrence of error is random, the probability of error can be described by the Complementary Error Function, erfc:

$$(26)\ P_e = 0.5\ \text{erfc}\ [(\phi - C)/\sigma\sqrt{2}]$$

where

σ = standard deviation (W) referred to Receiver input.
c = logic comparator level as referred to Receiver input (W)
ϕ = input flux (W)

With the BER observations made at two or more flux levels, the arguments of the Complementary Error Function values corresponding to these data points can be used to form a set of simultaneous equations to be solved for "c" and "σ". Due to the randomness of the data, a curve-fitting approach is recommended, using:

$$\text{erfc}^{-1}(2P_e) = y_i = [(x_i - b)/\sigma\sqrt{2}]$$

where x_i = flux level

Values of the inverse of the Complementary Error Function can be obtained from a table, but when $P_e < 10^{-4}$ adequate precision is obtained from the approximation:

$$\text{erfc}\ X \approx 0.54/(X\epsilon^{X^2}) = 0.54\,\epsilon^{-(X^2 + \ell nX)}$$

(see Appendix)

INSTALLATION, MEASUREMENT, AND MAINTENANCE

The shielded metal packages of Hewlett-Packard Fiber Optic Modules are very sturdy and can be mounted in any position. Both Transmitter and Receiver dissipate very low power, so heat sinking is not required. A cool location is preferred, especially for the Transmitter. The main concern in selecting the locations of both modules is accessibility of the optical ports.

Mounting

The preferred mounting is with two #2-56 screws on a printed circuit board. Clearance must be provided for the Lock Nut, which protrudes 0.5mm to 1.0mm (depending on angular position) beyond the plane of the module's bottom surface. The usual way to deal with this is to allow the Lock Nut to overhang the edge of the P.C. board as in Figure 14. Lock Nut clearance could also be provided by

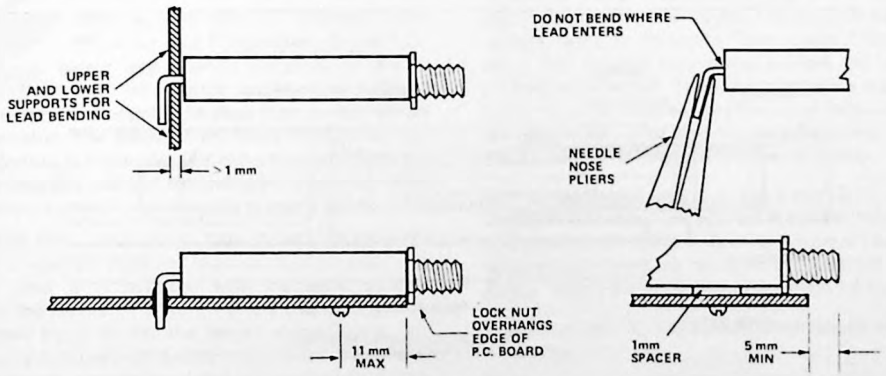


Figure 14. Lead Bending and P.C. Board Mounting.

APPLICATIONS

an opening in the board, or by using washers of 1mm thickness on the #2-56 mounting screws to space the Module bottom 1mm from the board. Screws entering the #2-56 tapped holes MUST NOT TOUCH BOTTOM AS THIS MAY DAMAGE THE MODULE. The #2-56 tapped hole is 5.6mm (0.22 in.) deep, which provides an ample purchase on the thread.

P.C. Board Thickness		Recommended Screw Length — mm (In.)	
mm	In.	W/O Spacer	W/1-mm Spacer
0.79	1/32	4.78 (.188)	6.35 (.250)
1.59	1/16	6.35 (.250)	6.35 (.250)
2.38	3/32	6.35 (.250)	6.35 (.250)

The #2-56 holes near the front of the package are the only screw holes that may be used for mounting the module. UNDER NO CIRCUMSTANCES MAY THE SCREWS ALREADY INSTALLED OR THE SET SCREW BE DISTURBED. Disturbing these may cause interior damage.

For additional support, the electrical leads may be bent down and soldered into the P.C. board. In bending the leads, care must be taken to avoid strain at the point where the leads enter the glass seal. This can be done by applying mechanical support between the module and the bending point which should be at least 1.0mm (0.04 in.) from the end of the module. A needle-nose pliers can also be used to bend the leads individually, providing no bending moment is transferred to the seal. See Figure 14 for details fo these techniques.

Panel mounting can also be used. This is an especially attractive mounting when R.F. shield integrity must be maintained. As seen in Figure 15, the panel thickness must be less than 4mm (5/32 in.) and have a counter-bore to receive the Lock Nut. This will make the mounting secure and leave enough of the Barrel outside the panel to permit installation of an external mounting nut as well as the Cable Connector.

Fiber Optic Cable Connections

The data sheet cautions against disturbing the Lock Nut and Barrel. This is to prevent damage by someone who has not read the following material:

As seen in Figure 16, there is a clearance between the interior end of the Barrel and a shoulder on the Fiber Alignment Sleeve. If this clearance is not maintained, there is a risk that a force applied to the Barrel may be transmitted by the Fiber Alignment Sleeve to the optical fiber stub, forcing the stub against the face of the source or detector. The source (or detector) is an extremely fragile semiconductor device and even a very small force can cause severe damage. Should it be necessary to remove the Lock Nut and Barrel, they should be reinstalled with this procedure:

1. Lightly and carefully thread the Barrel into the Module body until it comes against the shoulder of the Fiber Alignment Sleeve.
2. Back the Barrel OUT ONE FULL TURN, then HOLD THE BARREL FROM TURNING while seating the Lock Nut securely against the body. During final tightening of the Lock Nut, the Barrel may be allowed to enter no more than HALF A TURN. Final barrel position must be between a HALF-TURN and a FULL TURN from the alignment sleeve shoulder.

When Hewlett-Packard Cable Connectors are joined, either to each other or to the optical port of a Transmitter or Receiver, there is a cylindrical spring Sleeve that aligns the Ferrules. This is shown in Figures 16 and 17. It may be difficult to see, but the Sleeve does have a slightly flattened "leaf" on either side of a notch. The notch makes the leaves spring separately, allowing the Ferrules at

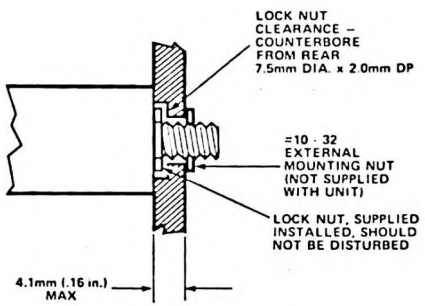


Figure 15. Panel Mounting.

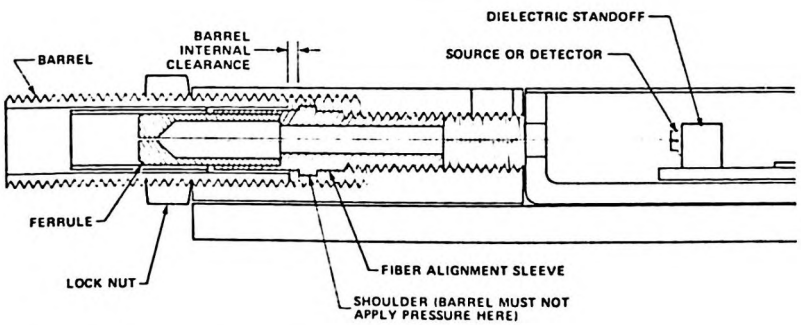


Figure 16. Opto-Mechanical Structure of T/R Modules.

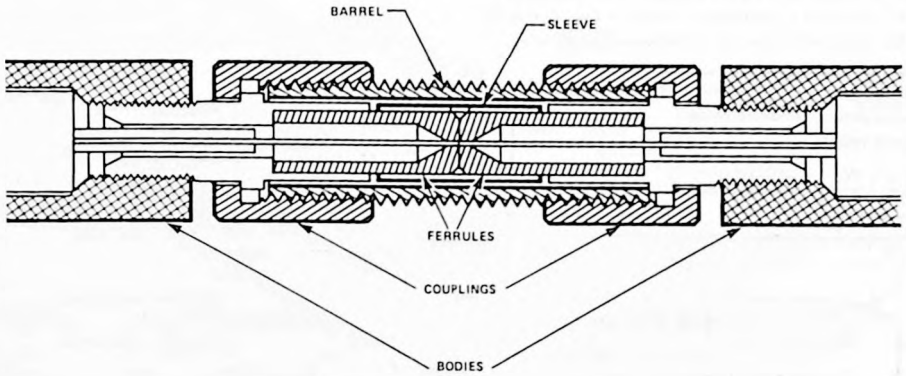


Figure 17. In-Line Connector Arrangement.

opposite ends of the sleeve to have slightly different diameters and yet be firmly aligned by the curved interior wall. A chamfer on the edge of the Ferrule aids insertion. In making temporary Cable-to-Cable connection, it is permissible, and often convenient, to omit the Barrel, since it does not perform an alignment function. When the Barrel is used for a more sturdy joint, the connection procedure is:

1. Install the Sleeve and Barrel on one Connector, using only FINGER TIGHTNESS of the Coupling on the Barrel.
2. Start the Ferrule of the second Connector into the Sleeve.
3. Engage the Coupling on the Barrel threads and tighten FINGER TIGHT.

Alignment of the Ferrules (and hence the fiber optics) is performed by the Sleeve; the Barrel and Couplings are intended only for tensile support, but if they are OVER tightened, they may cause misalignment. Loss of coupling due to misalignment can be observed at the V_T (Test Point) on the Receiver when the System is active:

$$\Delta V_T/\Delta\phi \approx 10mV/\mu W.$$

The procedure above applies also to making Cable connection at the Receiver and Transmitter, except that the Sleeve and Barrel are already installed. In manufacture, the Sleeve in the Module is pre-stressed for a tighter fit on the Ferrule in the Module than on the Ferrule in the Connector. The Sleeve is not likely to be pulled out when the Module is disconnected, but if that does happen, it can be reinstalled without removing the Barrel by using the Connector Ferrule to guide and support it.

In connecting fiber optics other than those from Hewlett-Packard to a Hewlett-Packard module, it is necessary to center the fiber in a cylinder with the same outside diameter as the Hewlett-Packard Ferrule over a length (to first shoulder) equal to half the length of the Sleeve, i.e., 3.5mm. This is adequate for a temporary connection. For a more permanent connection, add a coupling to fit the #10-32 thread on the Barrel.

Power Supply Requirements

Power supply lines for the Transmitter and the Receiver should each have a pi filter of two 60μF shunt capacitors and a 2.2μH (<1Ω) inductor. The Transmitter needs this filter to prevent transients from reaching other equipment when the LED (or IRED) currents are switched. The Receiver needs the filter to keep line transients from interfering with its extremely sensitive amplifier. In addition, the Receiver may need its own regulator, as shown in the data sheet, to prevent low-frequency transients or ripple from interfering with the data stream. If a regulator is used, the pi filter should be between the regulator output and the Receiver supply terminal. The Transmitter needs no regulator if the supply voltage is in the specified range.

System Performance Evaluation

System performance checks may be done by using error-detection equipment, such as the Hewlett-Packard Mod. 3760A Word Generator and 3761 Error Detector as indicated in Figure 18. The Mod. 3780A Pattern Generator/Error Detector which contains both word generator and error detector is also usable, although it has less flexibility in word generation and a lower data rate capability. These instruments have low-impedance (50Ω and 75Ω) inputs and outputs. The outputs have adequate voltage swing to drive the Fiber Optic Transmitter Data Input, but ringing may occur unless the signal line is properly terminated. The low-impedance inputs require a buffer amplifier between the Receiver output and the Error Detector input. Here also the voltage swing is ample, so a simple emitter follower will do as a buffer.

With Mode Select "low" (on the Fiber Optic Transmitter), the Word Generator may be set for either NRZ or RZ code, and there is no restriction of any kind on word length or composition (pseudo random or selected). With Mode Select "high", the code selection must be such that:

1. No interval > 5μs of consecutive marks or consecutive spaces
2. Duty factor: .44 < DF < .57 or .75 < k < 1.25

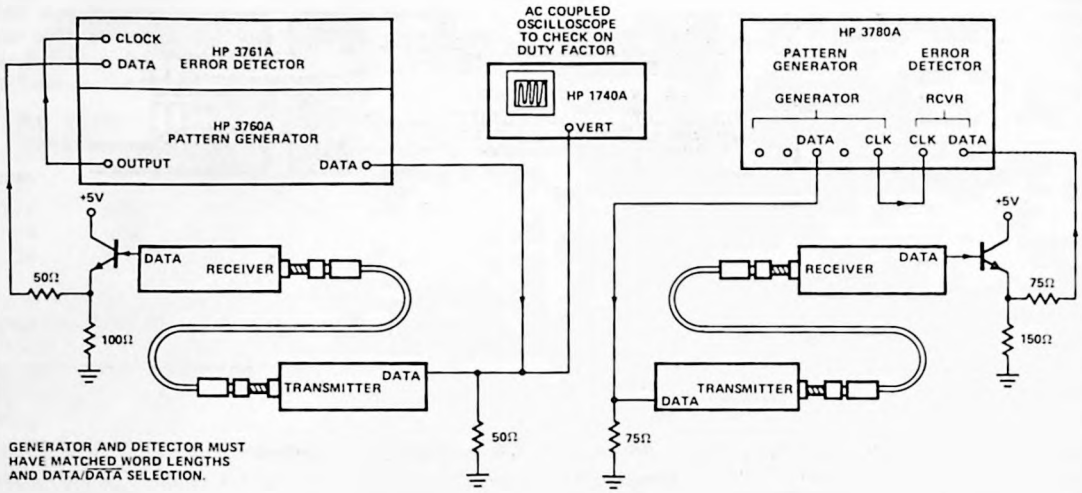


Figure 18. Bit Error Rate Measurement Arrangement.

The first condition can be examined with an oscilloscope, but if word length is such that:

$$\frac{\text{word length (bits)}}{\text{data rate (bits/second)}} < 5 \text{ microseconds}$$

then there is no way that any consecutive marks or spaces can extend over 5μs.

The easiest way to check duty factor is by observing k directly on an ac coupled oscilloscope: first establish the baseline position (e.g., center of scope face) with zero signal input, then with the data signal applied:

$$k = \frac{\text{excursion above baseline position}}{\text{excursion below baseline position}}$$

where the oscilloscope deflects upward for positive input. For this observation, the oscilloscope need not be synchronized — it could be free-running. The word composition should be adjusted to bring k within the specified limits. The word composition can be adjusted by adding zeroes, changing word length, or by handselecting the bit sequence.

Either error detector has two modes of operation: BER (Bit Error Rate) mode and "count" mode. The count mode is simplest to use and gives an earlier indication of the result of any system adjustment.

With the System at normal operating flux level, the error rate is so low that it would take several hours or even days to make an accurate BER measurement. If the flux level is reduced, SNR falls and BER rises until it becomes measurable. Then the error function [see Equation (26)] can be applied to determine the BER at the normal flux level in terms of the constants "a" and "b". The problem now is that the flux may be too low to measure with equipment at hand. The solution is in the Receiver Test Point voltage, V_T, which varies linearly as Receiver input flux —see Equation (17). But even this method has limits: when the flux becomes a small fraction of a microwatt, the voltage difference (V_{TMAX} - V_T) cannot be accurately observed. The solution to this problem is in the Transmitter-to-Cable connection. Just back off the Coupling, noting the number of turns while observing V_T, then plot a curve like that of Figure 19. The curve is quite repeatable if care is taken to avoid backlash and rotation of the Connector Body (rotate Coupling only) but the curve is not the same for each System.

Operating Margin Measurement

The approximate flux margin, α_M, for a system can be found using the Connector on the Transmitter as an adjustable attenuator as described above, proceeding as follows:

1. Prepare a curve similar to Figure 19.
2. Count the turns, N, needed to get measurable error, $P_e, N \approx 10^{-6}$
3. Find α_N(dB) from N and the curve from Step 1.

(27) $\alpha_M(dB) = \alpha_N(dB) - 0.5dB$

The 0.5 dB in Equation (27) is to allow for the fact that the operating BER should be 10^{-9}, but the BER at which error is easily observed is near 10^{-5}. At BER = 10^{-5} the flux level is 0.5 dB below the flux level needed for BER = 10^{-9}.

If any kind of relative flux indicator is available (e.g., a photodiode or radiometer) the flux margin can be observed in a similar manner, but the counting of turns, N,

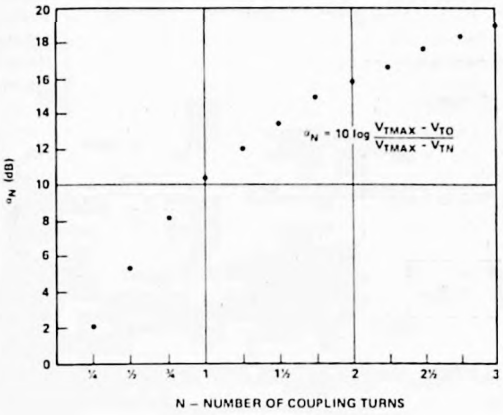


Figure 19. Flux Decoupling by Rotation of Connector Coupling.

and use of Figure 19 become unnecessary. The procedure is:

1. Unscrew the Transmitter connector until error is observed at the Receiver.
2. Transfer the Receiver connector to the flux indicator and note indication I_1 then, without changing the coupling to the flux indicator, reseat the Transmitter connector and note indication I_2.
3. α_M (dB) = 10 log (I_2/I_1) -0.5 dB

Absolute flux levels at "N" turns can be found by measuring the flux level when N = 0 and applying a ratio. A rough measurement can be made using the Test Point voltage, V_T, and Equation (15). A more precise measurement requires a calibrated radiometer, such as the EG&G Mod. 550, used as shown in Figure 20a. With its "flat" filter installed, the EG&G Mod. 550 reads the radiant incidance, E, in W/cm² on an aperture area, A_D = 1 cm² and N.A. = 1. With the filter removed, a fiber optic cable can be placed so close to the aperture that there is no flux loss, and since the radiometer N.A. exceeds the fiber N.A., the radiometer will have a reading in W/cm² which is numerically equal to the flux in watts. However, a correction must be made for the removal of the filter.

The insertion loss of the filter must be evaluated at the measurement wavelength because it varies with wavelength to compensate for spectral variation in the response of the silicon detector. The arrangement shown in Figure 20 for measurement of radiant intensity is a good one for measuring insertion loss of the filter. Two observations are made — one with and one without the filter. Error due to ambient radiation is avoided by working in subdued ambient and for each observation taking two radiometer readings (source off and source on); the difference in readings is the observation of the radiant incidance, E_e, produced by the radiant intensity, I_e, of the source. The ratio of the two observations gives:

(28) FILTER INSERTION LOSS, $\alpha_F = 10 \log \frac{E_{e(\text{filter out})}}{E_{e(\text{filter in})}}$

This same arrangement can be used to measure the average flux of the Transmitter as shown in Figure 20b. From the observation of E_e with the filter IN:

(29) AVERAGE INTENSITY, $I_e\left(\frac{\mu W}{sr}\right) = E_e\left(\frac{\mu W}{cm^2}\right) \times d^2\ (cm^2)$

(30) AVERAGE FLUX, $\phi_e(\mu W) = I_e \left(\frac{\mu W}{sr}\right)\left[\frac{\phi(\theta)}{I(0)}\ (MAX)\right]$

I_e: from Equation (29)

$\frac{\phi(\theta)}{I(0)}$ (MAX): value from radiation pattern integral in Transmitter Data Sheet

SYSTEM MAINTENANCE

Preventive Maintenance

Good system performance requires clean surfaces at the faces of the optical fibers to avoid obstruction of the optical path. This is true for the fiber faces in the Transmitter/Receiver modules, as well as in the Cable Connectors. Compressed air is often sufficient to remove particles of foreign matter; methanol or Freon™ on a cotton swab also works well. If it is necessary to remove the threaded barrel and lock nut to clean the Transmitter (or Receiver) optical port, refer to the earlier section "Fiber Optic Cable Connections" for re-assembly instructions. Severely ground-in or adhering foreign material may require repeated cleaning efforts to restore original optical performance.

Long-term degradation occurs in any LED and LED degradation affects the Hewlett-Packard Fiber Optic System in two ways: reduced average flux, affecting either externally- or internally-coded mode, and altered flux excursion ratio, affecting only the internally-coded mode. Significant degradation of either the flux or the flux excursion ratio can be detected by regular observation of the flux margin, α_M, and of k.

α_M is evaluated as explained under Operating Margin Measurement from Equation (27). A plot of α_M against the logarithm of the cumulative hours of operation will allow an estimate to be made of the operating time remaining until α_M = 0 FOR THE P_e DESIRED.

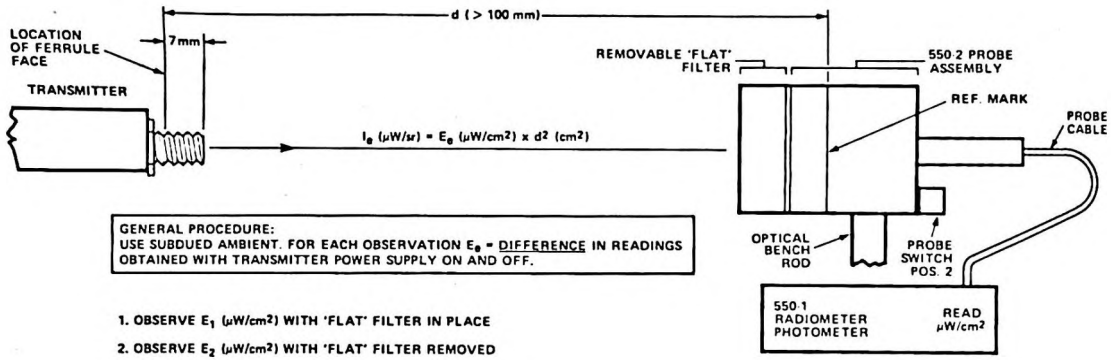
k must be evaluated by measuring ϕ_H, ϕ_M, and ϕ_L as explained in the Transmitter description. The Test Point voltage can be used in making this measurement — see Equation (15). The upper and lower margins on k for a particular Receiver can be found by operating the Transmitter with Mode Select "high" and a rectangular signal (f ≈ 500kHz) at Data Input. As the duty factor of the signal is varied, the limits on k are found as those at which the Receiver fails to follow the Data Input signal.

(31) $k = \left(\frac{1}{ft_P}\right) - 1 = \frac{1}{\frac{1}{ft_N} - 1}$

where ft_P is the positive-pulse duty factor
ft_N is the negative-pulse duty factor

Changes in k of the Transmitter do not affect the Receiver performance in externally-coded (FOO) mode, and if this mode is used, then flux margin, α_M, is the only concern.

APPLICATIONS



GENERAL PROCEDURE:
USE SUBDUED AMBIENT. FOR EACH OBSERVATION E_e = DIFFERENCE IN READINGS OBTAINED WITH TRANSMITTER POWER SUPPLY ON AND OFF.

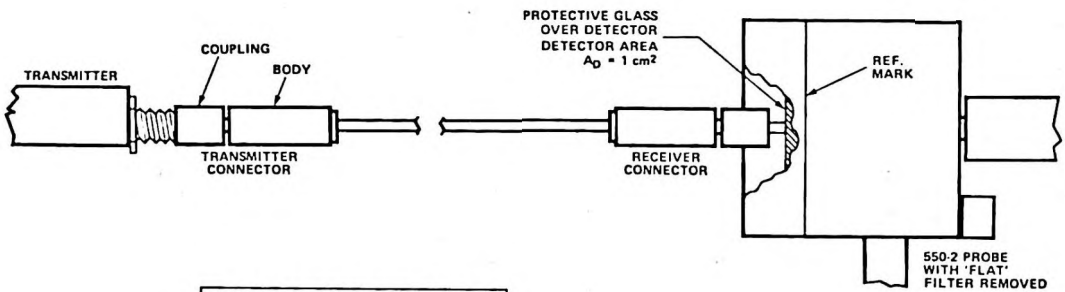
1. OBSERVE E_1 (μW/cm²) WITH 'FLAT' FILTER IN PLACE
2. OBSERVE E_2 (μW/cm²) WITH 'FLAT' FILTER REMOVED

FILTER TRANSMITTANCE: $\tau_F = E_1 / E_2$

AVERAGE FLUX FROM TRANSMITTER: $\phi\,(\mu W) = \left[E_1\left(\frac{\mu W}{cm^2}\right)\right]\left[d^2(cm^2)\right]\left[\left(\frac{\phi}{I}\right)_{MAX}\right]$

$\left(\frac{\phi}{I}\right)_{MAX}$ IS THE MAXIMUM VALUE OF THE RADIATION PATTERN INTEGRAL: $\frac{\phi(\eta)}{I(0)}$ (SEE DATA SHEET)

(a) MEASUREMENT OF TRANSMITTER AVERAGE FLUX



GENERAL PROCEDURE SAME AS ABOVE

3. WITH TRANSMITTER CONNECTOR SEATED, CENTER RECEIVER CONNECTOR OVER DETECTOR, THEN POSITION AGAINST GLASS. (DO NOT SLIDE – SLIDING MAY CAUSE SCRATCH DAMAGE.) OBSERVE E_D (μW/cm²).
4. WITHOUT ROTATING THE BODY, ROTATE THE COUPLING BY SMALL INCREMENTS OF TURNS, NOTING THE NUMBER OF TURNS, N, AND FOR EACH VALUE OF N: OBSERVE E_N (μW/cm²).

RECEIVER INPUT FLUX, AT OPERATING LEVEL $\phi_D\,(\mu W) = \frac{[E_D\,(\mu W/cm^2)]\,[A_D\,(cm^2)]}{\tau_F\ (\text{SEE ABOVE})}$

FLUX DECOUPLING (SEE FIG. 19) $\alpha_N = 10 \log_{10}(E_D / E_N)$

(b) MEASUREMENT OF AVERAGE RECEIVER INPUT FLUX AND FLUX DECOUPLING AT TRANSMITTER CONNECTOR.

Figure 20. Flux Measurement with EG&G Mod 550 Radiometer.

Corrective Maintenance

Trouble in the System may range from complete breakdown to excessive BER. The flux used in the Hewlett-Packard System is visible so the cause of complete breakdown can sometimes be localized by simply looking at the output of the Cable and the Transmitter. If there is visible output from the cable, then, when the Cable is connected to the Receiver, there should be an 8mV change in Test Point voltage, V_T, as the Transmitter (Mode Select "low") is turned on and off by switching V_{CC}. If ΔV_T is more than 8mV but the system is not working, then either the Receiver logic is not functioning properly or the flux excursion ratio, k, is either too high or too low. Excursion ratio can be checked as described above, using V_T. If k is satisfactory, the logic malfunction could be due to incorrect supply voltage or output loading.

If the System is functioning but has excessive BER, either the flux and flux excursion ratio are marginal (can be checked as described above) or there is too much interference from noise or other effects. If the Data Input voltage levels are correct, either random noise is high or errors are occurring due to incorrect supply voltage or output loading, or due to noise on the supply line. Random noise effects can be checked by lowering the flux level to a point where P_e is measurably high. If P_e varies with flux level according to $P_e = \text{erfc}(X)$, as in Equation (26), then the problem is excessive random noise. Random noise can also be checked by changing the data rate while the flux level is low enough to make P_e measurable. If P_e is the same at any data rate, the problem is excessive random noise. Excessive random noise is more likely to occur in the Receiver than in the Transmitter; the best way to check is by replacement of the Receiver. Noise on the supply line is difficult to trace. If there is any doubt, the Receiver should be operated from its own supply (e.g., a 5V regulator). Receiver noise should be low enough to make $P_e < 10^{-9}$ at 10 Mbaud with normal flux level ($\Delta V_T > 8$ mV by the method described above indicates normal flux level).

APPENDIX

Find the values of the constants, c and σ for Equation (26) by least-squares curve fitting to data of errors vs. input flux level, using the approximation:

(A1) $Y = \text{erfc}\, X \approx 0.54\, \epsilon^{-x^2 + \ell n x} = 0.54/(X \epsilon^{x^2})$

which has adequate precision for $10^{-3} < Y < 10^{-12}$

The value of X corresponding to a given Y is easily obtained by repetitively computing:

(A2) $$X_{m+1} = \sqrt{\ell n \frac{0.54}{Y} + \ell n \frac{1}{X_m}}$$

until $X_{m+1} = X_m$ (4 to 10 loops for 9-place accuracy)

then, $X \approx \text{erfc}^{-1} Y$

$$\overset{n}{\text{DATA}\atop\text{PAIRS}} \left\{ \begin{matrix} X_i = \text{flux level } (\mu W) \\ P_{ei} = \text{bit error rate at } X_i \end{matrix} \right\} 1 \le i \le n$$

Using Equation (A2) with $Y = 2\, P_{ei}$, compute:

(A3) $Y_i \approx \text{erfc}^{-1}(2\, P_{ei})$

Then, for the n data pairs, prepare the summations:

$$\sum_{i=1}^{n} X_i \,,\ \sum_{i=1}^{n} X_i^2 \,,\ \sum_{i=1}^{n} Y_i \,,\ \sum_{i=1}^{n} X_i Y_i \,,\ n = \sum_{i=1}^{n} 1$$

The constant for a least-squares fit to Equation (26) are:

(A4) $$\sigma = \frac{1}{\sqrt{2}} \left[\frac{n \left(\sum X_i^2\right) - \left(\sum X_i\right)^2}{n \left(\sum X_i Y_i\right) - \left(\sum X_i\right)\left(\sum Y_i\right)} \right]$$

(A5) $$C = \frac{\left(\sum X_i\right)\left(\sum X_i Y_i\right) - \left(\sum Y_i\right)\left(\sum X_i^2\right)}{n \left(\sum X_i Y_i\right) - \left(\sum X_i\right)\left(\sum Y_i\right)}$$

HEWLETT PACKARD

APPLICATION NOTE 1002

Consideration of CTR Variations in Optocoupler Circuit Designs

INTRODUCTION — Optocouplers Aging Problem

A persistent, and sometimes crucial, concern of designers using optocouplers is that of the current transfer ratio, CTR, changing with time. The CTR is defined as the ratio of the output current, I_O, of the optocoupler divided by the input current, I_F, to the light emitting diode expressed as a percentage value at a specified input current. The resulting optocoupler's gain change, ΔCTR^+, with time is referred to as CTR degradation. This change, or degradation, must be accounted for if long, functional lifetime of a system is to be guaranteed.

A number of different sources for this degradation will be explained in the next section, but numerous studies have demonstrated that the predominant factor for degradation is reduction of the total photon flux being emitted from the LED, which, in turn, reduces the device's CTR. This degradation occurs to some extent in all optocouplers.

$$^+\Delta CTR = CTR_{final} - CTR_{initial} \quad (1)$$

Causes

The main cause for CTR degradation is the reduction in efficiency of the light emitting diode within the optocoupler. Its quantum efficiency, η, defined as the total photons per electron of input current, decreases with time at a constant current. The LED current is comprised primarily of two components, a diffusion current component, and a space-charge recombination current:

$$I_F(V_F) = \underbrace{A\, e^{qV_F/kT}}_{\text{Diffusion}} + \underbrace{B\, e^{qV_F/2kT}}_{\text{Space-Charge Recombination}} \quad (2)$$

where A and B are independent of V_F, q is electron charge, k is Boltzmann's constant, T is temperature in degrees Kelvin, and V_F is the forward voltage across the light emitting diode.

The diffusion current component is the important radiative current and the non-radiative current is the space-charge recombination current. Over time, at fixed V_F, the total current increases through an increase in the value of B. From another point of view, with fixed total current, if the space-charge recombination current increases, due to an increase in the value of B, then the diffusion current, the radiative component, will decrease. The specific reasons for this increase in the space-charge recombination current component with time are not fully understood.

The reduction in light output through an increase in the proportion of recombination current at a specific I_F is due to both the junction current density, J, and junction temperature, T_J. In any particular optocoupler, the emitter current density will be a function of not only the required current necessary to produce the desired output, but also of the junction geometry and of the resistivity of both the P and N regions of the diode. For this reason, it is important not to operate a coupler at a current in excess of the manufacturer's maximum ratings. The junction temperature is a function of the coupler packaging, power dissipation and ambient temperature. As with current density, high T_J will promote a more rapid increase in the proportion of recombination current.

The junction and IC detector temperature of Hewlett-Packard optocouplers can be calculated from the following expressions:

$$T_J = T_A + \theta_{11}(V_F I_F) + \theta_{12}(V_o I_o + V_{cc} I_{cc})$$

$$T_D = T_A + \theta_{21}(V_F I_F) + \theta_{22}(V_o I_o + V_{cc} I_{cc}) \quad (3)$$

where the T_J is the junction temperature of the LED emitter, T_D is the junction temperature of the detector IC, T_A is ambient temperature, and the internal thermal resistances are $\theta_{11} = \theta_{22} = 370°C/W$, and $\theta_{12} = \theta_{21} = 170°C/W$. V_F, I_F are the forward LED voltage and current; V_o, I_o are the output stage voltage, and current and V_{CC}, I_{cc} are the power supply voltage and current to the device. In general, it is desirable to maintain $T_J \leq 125°C$.

A useful model can be constructed to describe the basic optocoupler's parameters which are capable of influencing the current transfer ratio. The 6N135 optocoupler, Figure 1 is the simplest device and one which is easily accessible for needed parameter measurements. However, any optocoupler can be modeled in this fashion within its linear region. Figure 1 shows the system block diagram which yields the relationship of input current, I_F, to output current, I_o. The resulting expression for CTR is:

$$CTR = \frac{I_o}{I_F}(100\%) = K\,R\,\eta(I_F,t)\,\beta(I_P,t) \qquad (4)$$

where K represents the total transmission factor of the optical path, generally considered a constant as is R, the responsivity of the photodetector, defined in terms of electrons of photocurrent per photon. η is the quantum efficiency of the emitter defined as the photons emitted per electron of input current and depends upon the level of input current, I_F, and upon time. Finally, β is the gain of the output amplifier and is dependent upon I_P, the photocurrent, and time. Temperature variations would, of course, cause changes in η, β as well.

From Equation (4), a normalized change in CTR, at constant I_F, can be expressed as:

(5)

$$\frac{\Delta CTR}{CTR} = \left(\frac{\Delta\eta}{\eta}\right)_{I_F} + \left(\frac{\Delta\eta}{\eta}\right)_{I_F}\left(\frac{\partial \ln\beta}{\partial \ln I_P}\right)_t + \left(\frac{\Delta\beta}{\beta}\right)_{I_P}$$

The first term, $\Delta\eta/\eta$, represents the major contribution to ΔCTR due to the relative emitter efficiency change; generally, over time, $\Delta\eta$ is negative. This change is strongly related to the input current level, I_F, as discussed earlier and more elaboration will be given later. The second term, $(\Delta\eta/\eta)_{I_F}\ (\partial\ln\beta/\partial\ln I_P)_t$, represents a second order effect of a shift, positive or negative, in the operating point of the output amplifier as the emitter efficiency changes. The third term, $(\Delta\beta/\beta)_{I_P}$, is a generally negligible effect which represents a positive or negative change in the output transistor gain over time. The parameters K and R are considered constants in this model.

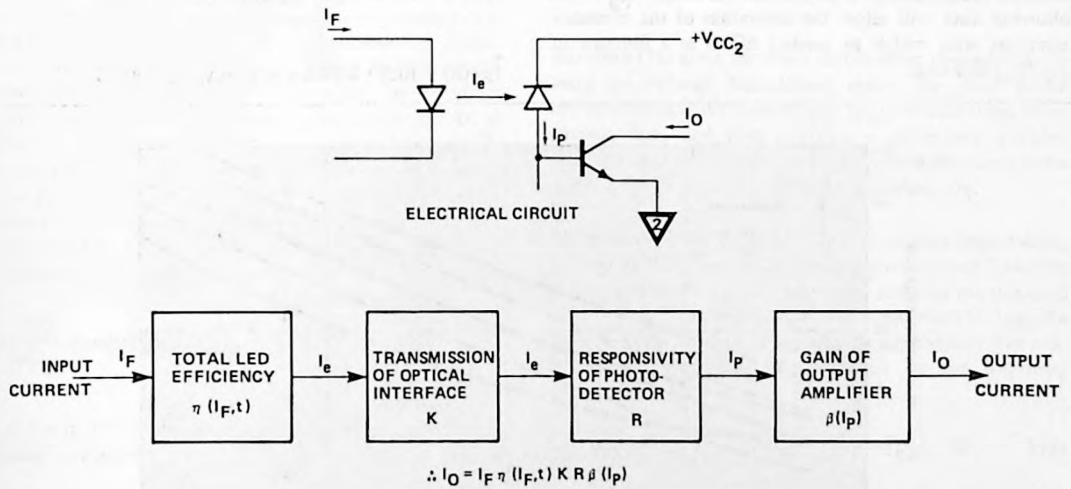


Figure 1. System Model for an Optocoupler

APPLICATIONS

Degradation Model

In this section, an extensive test program conducted at Hewlett-Packard to characterize the CTR degradation of optocouplers is discussed. The development which will follow is mainly of interest to those concerned with reliability and quality assurance. From the basic data, the CTR degradation equations will be developed in order to predict the percentage change in CTR with time. Complete data and analysis of CTR degradation will be found in an internal Hewlett-Packard report.

This study is based on a total of 640 optocouplers of the 6N135 type (Figure 1) with 700 nm $GaAs_{.7}P_{.3}$ LEDs from twenty different epitaxial growth lots representing a range of n-type doping and radiance. The 6N135 allows access to measurement of the emitter degradation via the relative percentage change in photodiode current, $\Delta I_P/I_P$, as well as output amplifier β change. Stress currents of I_{FS} = .6, 7.5, 25 and 40 mA were applied to different groups of optocouplers, and at each measurement time of t=0, 24, 168, 1000, 2000, 4000 and 10,000 hours, measurement currents of I_{FM} = .5, 1.6, 7.5, 25 and 40 mA were used to determine the CTR.

The important results to be noted are the following. First, a factor of major significance in the study of CTR degradation is the ΔCTR varies as a function of the ratio of $I_{FS}/I_{FM} \equiv R$. Large values of R will result in greater CTR degradation than at lower R values with the same magnitude of I_{FS}. However, knowledge of the ratio of I_{FS}/I_{FM} alone does not give a complete picture of degradation because ΔCTR is also dependent upon the absolute magnitude of the stress current, $|I_{FS}|$. The following data will allow the derivation of the necessary equations with which to predict ΔCTR as a function of I_{FS}, I_{FM} and time.

Figure 2 displays the mean and mean plus 2σ values of emitter degradation versus R for 1K, 4K, and 10K hours at 25°C. Accelerated degradation can be seen at larger R values.

The data of Figure 2 can be replotted to illustrate the percentage degradation versus time as a function of R. Figure 3 illustrates the mean and mean plus 2σ distribution with R = 1 and 50.

From this curve, a useful expression which relates the average degradation in emitter efficiency to time is obtained for the mean or mean plus 2σ distributions. [The symbol "D" will refer to CTR degradation due solely to emitter degradation, $\Delta\eta/\eta$, whereas ΔCTR/CTR will refer to total CTR degradation as expressed in Equation (5)].

$$\overline{D}_{\overline{x}} \text{ or } \overline{D}_{\overline{x}} + 2\sigma \equiv \frac{-\Delta I_P}{I_P} = A_o R^{\alpha} t^{n(R)} \text{ in \% for } I_{FS} = \overline{I}_{FS} \quad (6)$$

where t is in 10^3 hours and A_0 and α differ for mean or mean plus 2σ. Equation (6) represents an average degradation corresponding to a specific R, t, and an average stress current $\overline{I_{FS}}$. A knowledge of $\overline{I_{FS}}$ and the actual device operating stress I_{FS} can be utilized to correct $\overline{D}$ to a value D which reflects the actual absolute magnitude of I_{FS}. This will be shown in the development of Equations (11) and (13). The data shows that $\overline{I_{FS}}$ increases with R and can be represented as follows:

$$\overline{I}_{FS}(R) = 14.13 + 9.06 \log_{10} R, \text{ mA}, T_A = 25°C \quad (7)$$

$$\overline{I}_{FS}(R) = 10.5 + 5.76 \log_{10} R, \text{ mA}, T_A = 85°C \quad (8)$$

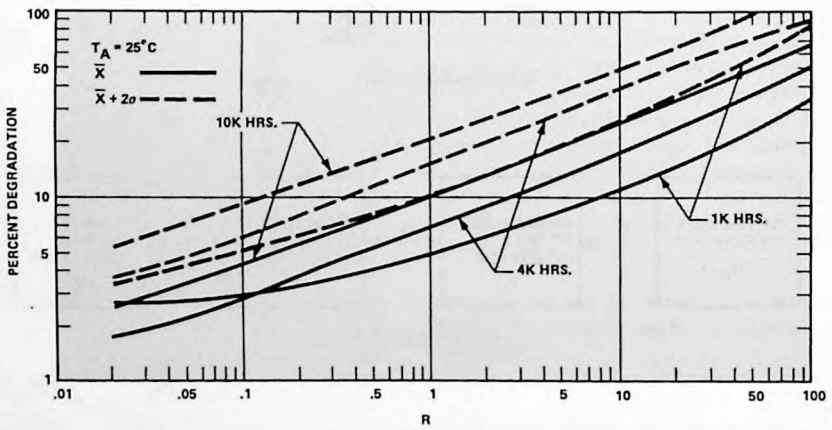


Figure 2. Emitter Degradation vs. R (Ratio of Stress Current to Measurement Current) for 1k, 4k, and 10k Hours, Mean, Mean +2σ Distribution, T_A = 25°C.

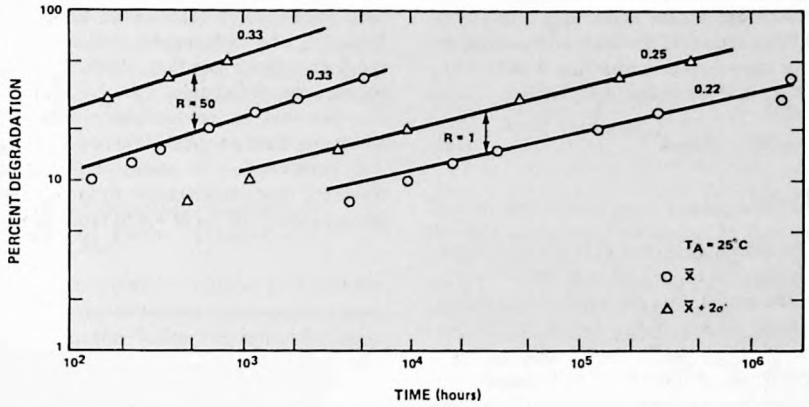


Figure 3. Emitter Degradation vs. Time at R = 1 and R = 50 for Mean, Mean + 2σ Distributions, T_A = 25°C

These equations are obtained from averaged degradation data versus I_{FS} at different measurement times.

The expression for n(R) was found to obey the relationship

$$n(R) = .0475 \log_{10} R + .25 \qquad (9)$$

A_o and α were determined from degradation data versus R and are found in Figure 7, "Matrix of Coefficients."

Equation (6) gives a direct relationship between the average degradation, $\overline{D}$, and time. As mentioned earlier, the magnitude of the stress current also determines the amount of degradation. In order to allow for the effect of $|I_{FS}|$, empirical observations were made on D at different I_{FS} and at different times for several values of R. The dependence of degradation on stress current is linear up to I_{FS} = 40 mA, for all values of R. From these observations, the average rate of change, or slope, S(R,t), of degradation D with I_{FS} over time was found to behave in the following fashion for any R:

$$S \equiv \frac{\partial D}{\partial I_{FS}} = \alpha(R) \log_{10} t + \beta(R) \quad \%/mA \qquad (10)$$

where t is in 10^3 hours, the coefficients $\alpha(R)$ and $\beta(R)$ can be found on Figure 7.

Along with Equation (10), the mean distribution degradation, $D_{\bar{x}}$, can be estimated for any specific stress current, I_{FS}, ratio R, and time t via the subsequent expression:

$$D_{\bar{x}} = \overline{D}_{\bar{x}} + S\,[I_{FS} - \overline{I}_{FS}] \quad \% \qquad (11)$$

or substituting Equation (6),

$$D_{\bar{x}} = A_o R^{\alpha} t^{n(R)} + S\,[I_{FS} - \overline{I}_{FS}] \quad \% \qquad (12)$$

where, again, $\overline{D}_{\bar{x}}$ is the average degradation at time t, in units of 10^3 hours, corresponding to an average stress current, $\overline{I}_{FS}$, given by Equations (7) and (8); I_{FS} is the actual stress current. In equation (12) $R = I_{FS}/I_{FM}$; S is the expression (10) for the change of slope of D versus I_{FS} with time; n(R) is a power of t, given by Equation (9), and A_o, α are found in Figure 7.

Equation (11) gives the mean distribution degradation by using an average degradation value, $\overline{D}_{\bar{x}}$ (first term), corresponding to the ratio of I_{FS}/I_{FM}, or an average stress current, $\overline{I}_{FS}$, and then applying a correction quantity (second term) to $\overline{D}_{\bar{x}}$ due to the magnitude of the actual stress current, I_{FS}, yielding the actual degradation $D_{\bar{x}}$.

The expression for the mean + 2σ distribution degradation, $D_{\bar{x}+2\sigma}$, (worst case) is almost of the same form as Equation (11). The dissimilarity arises from the fact that the standard deviation, σ, is dependent upon the stress current, I_{FS}, the ratio R, and upon time. This complex dependency was analytically deduced from the data to be the following expression:

$$D_{\bar{x}+2\sigma} = \overline{D}_{\bar{x}+2\sigma} + [S + 2P]\,[I_{FS} - \overline{I}_{FS}] \quad \% \qquad (13)$$

or substituting Equation (6)

$$D_{\bar{x}+2\sigma} = A_o R^{\alpha} t^{n(R)} + [S + 2P]\,[I_{FS} - \overline{I}_{FS}] \quad \% \qquad (14)$$

where $\overline{D_{\bar{x}} + 2\sigma}$ is the average degradation for $\bar{x} + 2\sigma$ distribution corresponding to the average stress current $\overline{I}_{FS}$,

Equations (7) and (8). In equation (14) A_0 and α are found in Figure 7 under the $\bar{x} + 2\sigma$ category. S [Equation (10)] represents the slope to correct for actual I_{FS} versus $\bar{I}_{FS}$ current levels, and P [Equation (15)] is the new term which is a slope to correct for the σ variation with I_{FS}, R and t. The coefficients $\gamma(R)$, $\delta(R)$ in P are found in Figure 7.

$$P = \gamma(R) \log_{10} t + \delta(R) \quad \%/mA \qquad (15)$$

where t is in 10^3 hours.

The degradation Equations (11) and (13) are considered accurate for the ranges of $I_{FS} \leq 40$ mA and $R \leq 20$; outside this range, the model does not predict degradation as well. Hence, check to see if I_{FS} and R satisfy the above conditions. If I_{FS} or R exceed these limits, prediction of D will be, in general, greater than the actual degradation due to large values for S and P which do not reflect actual S and P. If $\bar{I}_{FS}$ is approximately equal to the actual I_{FS}, then the second term in the degradation equations need not be determined. Otherwise, the second term needs to be determined to obtain true emitter degradation, D. If $I_{FS} < \bar{I}_{FS}$, then the degradation, D, will be less than the degradation, $\bar{D}$, corresponding to $\bar{I}_{FS}$, and vice versa when $I_{FS} > \bar{I}_{FS}$. A quick and coarse estimate for degradation $\bar{D}$ can be obtained by using $\bar{D} = A_0 R^{\alpha} t^{n(R)}$ for a specific R with approximate values for $\alpha \approx 0.4$ and $n \approx 0.3$. Figure 4 represents plots of Equations (11) and (13) for R = 1 and I_{FS} = 1.6, 6.3, and 16mA at both T_A = 25°C and T_A = 85°C. These plots are very useful in making a quick approximation of D for the specific conditions for which the plots have been made. These conditions represent the recommended operating conditions for the three HP optocoupler families.

This discussion of reliability data and its interpretation with model equations is qualified to specific optocouplers, 6N135 and 6N138, where continuous LED operation was maintained, and extrapolation of data for times beyond 10,000 hours is assumed to be valid. Different types of LEDs or preparation processes may produce different results than those presented in this section. These expressions only incorporate the first order effect, emitter degradation $\Delta\eta/\eta$, whereas comments about higher order effects upon total CTR degradation will be given in the following section. With these expressions for degradation, accelerated testing may be accomplished by employing large values of R. Such testing can provide a means by which to determine acceptable emitter lots for optocoupler fabrication, acceptable degradation performed for lot selection, or predict functional lifetime expectance for optocouplers under specific operational conditions.

An important point to note is that the total operational life of an optocoupler is greater than the worst case mean plus 2σ distribution implies. Specifically, the worst case degradation given in Figures 4a (25°C) and 4b (85°C) are for the continuous operation of the 6N135 optocoupler. The actual lifetime for an optocoupler is greater than Figures 4a and 4b would indicate since the majority of units will be centered around the mean distribution lifetime. Secondly, the optocoupler which is operated at some signal duty factor less than 100%, for example 50%, would increase the optocoupler's life by a factor of two. Third, the fact that an optocoupler is used within equipment which may have a typical 2000 hours per year (8 hours/day – 5 days/week – 50 weeks/year) instrument or system operating time, could expect to increase the optocoupler's life by another factor of 4.4 in terms of years of useful life.

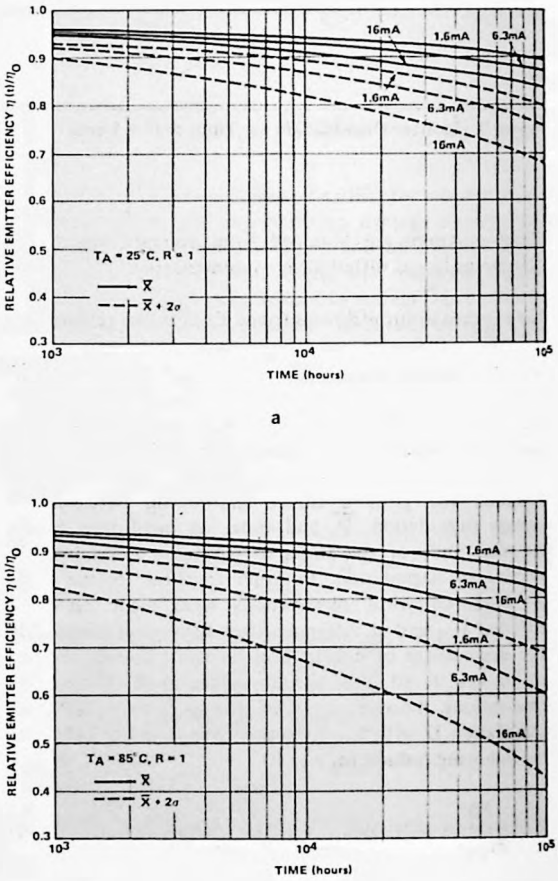


Figure 4. Calculated Curves of Relative Emitter Efficiency vs. Time for R = 1: $I_{FS} = I_{FM}$ = 1.6, 6.3, and 16mA which are Recommended I_F for 6N138, 6N137, and 6N135 Optocouplers Respectively. Mean, Mean + 2σ Distributions. a) T_A = 25°C, b) T_A = 85°C.

The appropriate operating time considerations will vary depending upon the designer's knowledge of the system in which the optocoupler will be used. The operating lifetime of an optocoupler can be expressed, for a maximum allowable degradation at a particular I_{FS}, by using Figures 4a and 4b for $t_{continuous\ lifetime}$ and the following expression:

$$t_{\text{continuous lifetime}} = \left[t_{\text{system lifetime}}\right]\left[\text{Data Duty Factor}\right]\left[\text{System Use Data Factor}\right] \quad (16)$$

Another equally important point to observe is that of the worst case conditions under which the optocoupler is used. As will be illustrated in the design examples, the worst possible combination of variations in V_{cc1}, V_{cc2}, R_{in}, CTR, R_L, I_{IL}, and temperature still result in the optocoupler functioning over an extended length of time (10^5 hours) for a particular maximum allowable degradation. However, the likelihood of seven parameters all deviating in their worst directions at the same time is extremely remote. A thorough statistical error accumulation analysis would illustrate that this worst-worst case is not a representative situation from which to design.

Higher Order Effects

The first order effect of emitter degradation, $\Delta\eta/\eta$, has a pronounced influence upon the ΔCTR as explained in the previous sections; however, consideration of higher order effects is important as well.

Consider the second term in Equation (5) $(\Delta\eta/\eta)_{I_F}$ $(\partial \ln\beta/\partial \ln I_P)_t$, the emitter degradation part has been explained; however, $(\partial \ln\beta/\partial \ln I_P)_t$ represents a shift in the operating point of the output amplifier of an optocoupler. The term $(\partial \ln\beta/\partial \ln I_P)$ can be rewritten as $(1/2.3\beta)$ $(\partial\beta/\partial \log_{10} I_P)$ which is more convenient to use with the accompanying typical curves of β versus $\log_{10} I_P$ for the two optocouplers 6N135 and 6N138, given in Figure 5a.

If the operating photocurrent, I_P, is to the right of the maximum β point of either curve, then with reduced emitter efficiency over time, I_P will decrease, but the increasing β will tend to compensate for this degradation. However, if the operating I_P is to the left of the maximum β and then I_P decreases, the β change will accentuate the emitter's degradation, yielding a larger CTR loss. The magnitude of the contributions of $\partial \ln\beta/\partial \ln I_P$ to overall CTR degradation can be illustrated by the following examples.

Consider a 6N138 optocoupler of Figure 5c operating at its recommended I_F = 1.6 mA which corresponds to an $I_P \approx 1.6\mu A$. (An I_F to I_P relationship for Hewlett-Packard optocouplers is 1 mA input current yields approximately 1μA of photodiode current.) At $I_P = 1.6\mu A$, the slope of the V_{CE} = 5V curve is equal to -15,000 and the gain is β = 26,000; hence, $\partial \ln\beta/\partial \ln I_P \approx$ -0.25. If, for instance, the emitter degradation $\Delta\eta/\eta$ is -10%, then the second order term would improve the overall CTR degradation, i.e.,

$$\frac{\Delta CTR}{CTR} = \left(\frac{\Delta\eta}{\eta}\right) + \left(\frac{\Delta\eta}{\eta}\right)\left(\frac{\partial \ln\beta}{\partial \ln I_P}\right) + \ldots = -10\% + 2.5\% = -7.5\% \quad (17)$$

This improvement is what was expected while operating on the right side of the β maximum. In fact, with an I_F = 4 mA or $I_P \approx 4\mu A$, the term $\partial \ln\beta/\partial \ln I_P$ = -0.8, and again, if $\Delta\eta/\eta$ = -10%, the resulting ΔCTR/CTR = -2%, nearly cancelling the emitter's degradation.

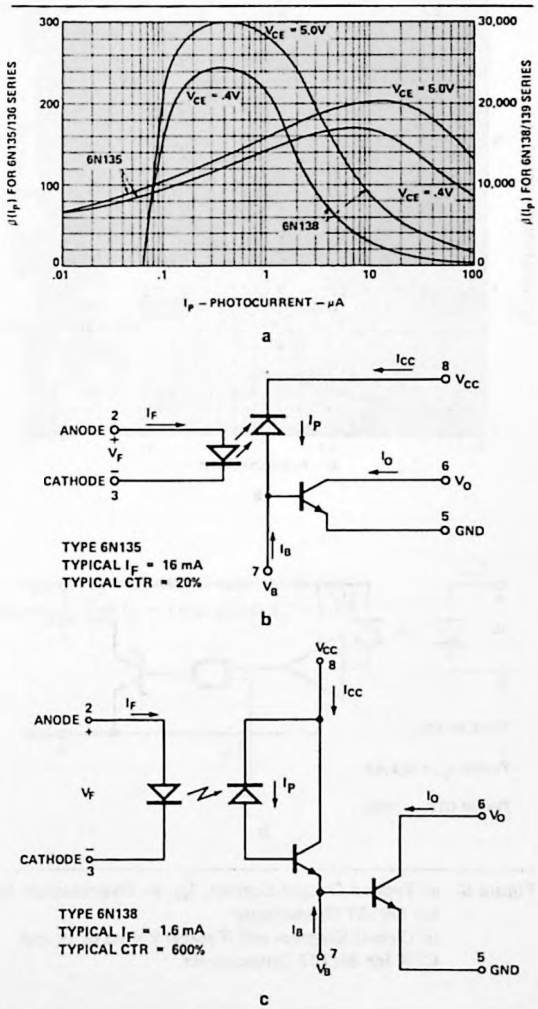


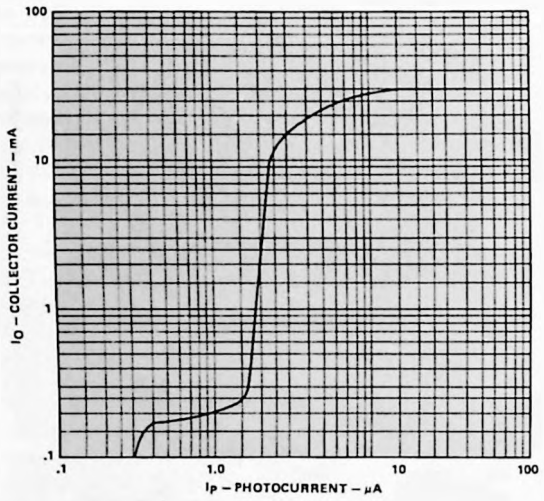
Figure 5. a) Typical DC Current Gain, β, vs. Photocurrent, I_P, for 6N135 and 6N138 Optocouplers. Current Diagrams and Typical Values of I_F and CTR for Hewlett-Packard Optocouplers, b) 6N135, c) 6N138.

APPLICATIONS

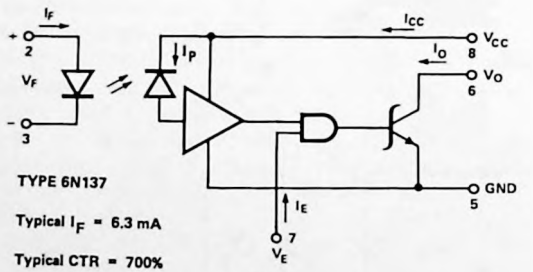
With the 6N135 optocoupler, Figure 5b operating at I_F = 10 mA, or $I_P \approx 10\mu A$, which corresponds to the maximum β point on the V_{CE} = .4V curve, the slope is zero and the total CTR degradation is basically the emitter's degradation.

Another subtle effect is seen from the third term in Equation (5), $(\Delta\beta/\beta)I_P$, over time. At constant I_P, β can increase or decrease by a few percent over 10,000 hours. This change is so small that the third term is generally neglected.

For the optocouplers containing an output amplifier, such as the 6N137, which switches abruptly about a particular threshold input current, the actual emitter degradation can be determined from Equations (11) and (13). An appropriate $I_{F_{initial}}$ can be determined to provide for adequate guard band current which will allow the optocoupler emitter to degrade while maintaining sufficient I_P to switch the amplifier. An actual design procedure to determine the needed $I_{F_{initial}}$ for proper operation of Hewlett-Packard optocouplers is given in the design examples section.



a



b

Figure 6. a) Typical Output Current, I_O, vs. Photocurrent, I_P, for 6N137 Optocoupler.
b) Circuit Diagram and Typical Values of I_F and CTR for 6N137 Optocoupler.

MATRIX OF COEFFICIENTS

	25°C		85°C			
	$\bar{X}$	$\bar{X}+2\sigma$	$\bar{X}$		$\bar{X}+2\sigma$	
			R < 6	6 < R	R < 8	8 < R
A_o	4.95	9.7	6.8	5.0	15.0	11.0
α	.388	.428	.302	.467	.284	.430
	25°C		85°C			
	R < 1	R > 1	R < 1		R > 1	
$\alpha(R)$	$.19\ R^{.052}$	$.19\ R^{.32}$	$.32\ R^{.08}$		$.32\ R^{.30}$	
$\beta(R)$	.055	$.055\ R^{.68}$	$.11\ R^{.25}$		$.11\ R^{.65}$	
	25°C		85°C			
$\gamma(R)$	$.063\ R^{.30}$		$.154\ R^{.26}$			
$\delta(R)$	$.081\ R^{.38}$		$.196\ R^{.39}$			

Figure 7. Matrix of Coefficients.

Procedure for Calculation of CTR Degradation

1. Specify I_{FS}, I_{FM}

2. Determine $R = I_{FS}/I_{FM} \leq 20$, $I_{FS} \leq 40$ mA — Degradation Model Equations (11) and (13) Valid

3. First Approximation of Degradation

$$\bar{D}_{\bar{x}} = A_o R^{\alpha} t^n \quad (\%)$$ with $\alpha \approx .4$, A_o (Figure 7), $n \approx .3$, t in 10^3 hours ($\bar{D}$ corresponds to $\overline{I_{FS}}$)

or

$$\bar{x} + 2\sigma$$

4. Calculate $\overline{I_{FS}}$ =

$14.13 + 9.06 \log_{10} R$ @ 25°C mA — Equation (7)

$10.5 + 5.76 \log_{10} R$ @ 85°C mA — Equation (8)

If $I_{FS} \approx \overline{I_{FS}}$, Step 6 and the second terms in Equations (11) and (13) do not need to be calculated.

5. Calculate $n(R) = .0475 \log_{10} R + .25$

6. Calculate $S = \alpha(R) \log_{10} t + \beta(R)$ %/mA $\alpha(R), \beta(R)$; $P = \gamma(R) \log_{10} t + \delta(R)$ %/mA $\gamma(R), \delta(R)$ — Figure 7; t in 10^3 hours

7. Calculate Mean, Mean + 2σ Degradation (No Approximation)

$$D_{\bar{x}} = A_o R^{\alpha} t^{n(R)} + S\,[I_{FS} - \overline{I_{FS}}] \quad \% \quad \text{Equation (11)}$$

$$D_{\bar{x}+2\sigma} = A_o R^{\alpha} t^{n(R)} + [S + 2P]\,[I_{FS} - \overline{I_{FS}}] \quad \% \quad \text{Equation (13)}$$

(A_o, α via Figure 7, t in 10^3 hours)

8 For Second Order Effect, Determine Slope

$$\frac{\partial \ln \beta}{\partial \ln I_P} = \frac{1}{2.3\beta} \frac{\partial \beta}{\partial \log_{10} I_P}$$

Figure 5a — typical curves with an approximation for HP optocouplers of I_F = 1 mA yields $I_P \approx 1\mu A$

9a. Total CTR Degradation for Mean Distribution

$$\frac{\Delta CTR}{CTR} = D_{\bar{x}} + D_{\bar{x}} \left(\frac{\partial \ln \beta}{\partial \ln I_P} \right)$$

9b. Total CTR Degradation for Mean + 2σ Distribution

$$\frac{\Delta CTR}{CTR} = D_{\bar{x}+2\sigma} + D_{\bar{x}+2\sigma} \left(\frac{\partial \ln \beta}{\partial \ln I_P} \right)$$

APPLICATIONS

Practical Application

A very common application of an optocoupler is to function as the interfacing element between digital logic. In this section, the designer will be shown an approach which will insure the initial and long term performance of such an interface, and take into account the practical aspects of the system that surrounds it. These system elements include the data rate, the logic families being interfaced, the variations of the power supply, the tolerances of the components used, the operational temperature range, and lastly the expected lifetime of the system.

The system data speed can be considered as the primary selection criteria for selecting a specific optocoupler family. Figure 9 lists the ranges of data rates for four Hewlett-Packard optocoupler families when driven at specified LED input current, I_F. With this table, and the knowledge of the system data rate requirements, it is possible to select an optimum coupler.

An example of an optocoupler interconnecting two logic gates is shown in Figure 8. A logic low level is insured when the saturated output sinking current, I_O, is greater than the combined sourcing currents of the pull-up resistor, and the logic low input current, I_{IL}, of the interconnecting gate. Using the coupler specifications selected from Figure 9 and the corresponding CTR (MIN) from Figure 10,

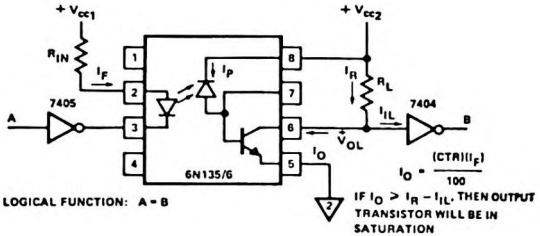


Figure 8. Typical Digital Interface Using an Optocoupler.

$$I_{F\,(MIN)} = \frac{V_{cc1\,(MIN)} - V_{F\,(MAX)} - V_{OL}}{R_{in\,(MAX)}} \quad (18)$$

$$I_{F\,(MAX)} = \frac{V_{cc1\,(MAX)} - V_{F\,(MIN)} - V_{OL}}{R_{in\,(MIN)}} \quad (19)$$

$$I_F = \frac{I_o \times 100}{CTR(MIN)} \quad (20)$$

$$R_{in} = \frac{V_{cc1} - V_F - V_{OL}}{I_F} \quad (21)$$

FAMILY	NRZ DATA RATE BITS/S	INPUT CURRENT – I_F						
		.5mA	1.0mA	1.6mA	7.5mA	10mA	12mA	16mA
6N135/6 SINGLE TRANSISTOR	MIN							333k
	TYP							2M
6N138/9 SPLIT DARLINGTON	MIN	12k		22k			125k	
	TYP	100k		200k			840k	
4N45/6 DARLINGTON	MIN					1.8k		
	TYP		640			6.5k		
6N137 OPTICALLY COUPLED GATE	MIN				6.7M			
	TYP				10M			

Figure 9. Figure 13.5-2. Optocoupler Data Rates Specifications.

FAMILY		% CTR @ I_F = (mA)						TEMP °C	V_{OL}
		.5	1.0	1.6	5	10	16		
SINGLE TRANSISTOR	6N135						7	25	0.4
	6N136						19		
SPLIT DARLINGTON	6N138		300					0–70	0.4
	6N139	400	500					0–70	0.4
DARLINGTON	4N45		250			200		0–70	1.0
	4N46	350	500			200		0–70	1.0
OPTICALLY COUPLED GATE	6N137				400			0–70	0.6

Figure 10. Optocoupler CTR (MIN).

it is possible to determine from Equation (20) the minimum initial value of I_F for the coupler. The design criteria is that $I_O \geq I_{IL} + I_R$ for the V_{IL} specified in Figure 11.

Using Equation (21), the typical value of R_{in} can be calculated for the selected I_F and the logic low output voltage, V_{OL}, of the driving gate. The V_{OL} of the logic family is given in Figure 11. The next step is to determine the worst case value of the LED input current, I_F, resulting from the tolerance variations of the LED current limiting resistor, R_{in}, and the power supply voltage, V_{cc1}. The conditions of $I_{F(MIN)}$ and the initial CTR(MIN) are then used to determine the initial worst case value of $I_{O(MIN)}$. Conversely, the worst case CTR degradation will occur when the LED is stressed at $I_{F(MAX)}$ conditions; thus, $I_{F\ (MAX)}$ will be used to determine the worst case degradation of the optocoupler performance. Using the maximum V_{cc1} and the minimum R_{in} will accomplish this worst case calculation, as shown in Equation (19).

TTL FAMILY	I_{IL}	V_{IL}	I_{IH}	V_{IH}	I_{OL}	V_{OL}	I_{OH}	V_{OH}
74S	−2 mA	.8V	50 μA	2V	20 mA	.5V	−1000 μA	2.7V
74H	−2 mA	.8V	50 μA	2V	20 mA	.4V	− 500 μA	2.4V
74	−1.6 mA	.8V	40 μA	2V	16 mA	.4V	− 400 μA	2.4V
74LS	−.36 mA	.8V	20 μA	2V	8 mA	.5V	− 400 μA	2.7V
74L	−.18 mA	.7V	10 μA	2V	3.6 mA	.4V	− 200 μA	2.4V

Figure 11. Logic Interface Parameters.

The change in CTR from the initial value at time t = 0 to a final value at some later time can be compensated by choosing a value of R_L which is consistent with $I_{o(MIN)} - mI_{IL}$ at the end of system life. Equation (22) describes this worst case calculation.

(22)

$$R_{L\ (MIN)} \geq \frac{V_{cc2\ (MAX)} - V_{OL}}{\left[\frac{I_{F(MIN)} \cdot CTR(MIN)}{100}\left(1 - \frac{D_{\overline{x}} + 2\sigma}{100}\right) - mI_{IL}\right]}$$

$D_{x + 2\sigma}$ = worst case CTR degradation

The selection of the maximum value of R_L is also of important in that its value insures that the collector is pulled up to the logic one voltage conditions, V_{IH}, under the conditions of maximum I_{OH} of the coupler, and the I_{IH} of the interconnecting gate.

(23)

$$R_{L\ (MAX)} \leq \frac{V_{cc2\ (MIN)} - V_{OH}}{I_{OH\ (MAX)} + m\, I_{IH}}$$

The selection of the value of R_L between the boundaries of $R_{L\ (MIN)}$, and $R_{L\ (MAX)}$ has certain trade offs. As in any open collector logic system, T_{PLH} increases with increasing R_L. Conversely, as R_L is increased above $R_{L_{MIN}}$, a larger guardband between $I_{O_{MIN}}$ and $I_{IL} + I_R$ is achieved. Engineering judgement should be employed here to achieve the optimum trade off for desired performance.

APPLICATIONS

Using the coefficient Figure 7 and Equations (11) and (13), the following examples are developed to demonstrate the methods of optocoupler system design in the presence of the mean and mean plus two sigma CTR degradation.

Example 1.

System Specifications

Data Rate	20 k bit NRZ
Logic Family	Standard TTL
Power Supply 1 & 2	5V ± 5
Component Tolerances	± 5%
Temperature Range	0 – 70°C
Expected System Lifetime	350 k hr (40 yr) at 50% system use time and 50% Data Duty Factor

Interface Specifications

Coupler 6N139

$CTR\ (MIN) = 500\% @ I_F = 1.6\ mA$
$V_{OL\ (MAX)} = .4V @ I_F = 1.6\ mA$
$I_{OH\ (MAX)} = 250\mu A @ V_{cc2} = 7V$
$V_{F\ (MAX)} = 1.7V @ I_F = 1.6\ mA$
$V_{F\ (MIN)} = 1.4V @ I_F = 1.6\ mA$
$V_{F\ (TYP)} = 1.6V @ I_F = 1.6\ mA$

Logic Standard TTL

$I_{IL} = 1.6\ mA$ $\quad I_{IH} = 40\mu A$
$V_{IL} = .8V$ $\quad V_{IH} = 2V$
$I_{OL} = 16\ mA$ $\quad I_{OH} = 400\mu A$
$V_{OL} = .4V$ $\quad V_{OH} = 2.4V$

Step 1. $R_{in\ (TYP)}$

$$R_{in} = \frac{V_{cc1} - V_{F\ (TYP)} - V_{OL}}{I_{F\ (TYP)}} \qquad (24)$$

$$R_{in} = \frac{5.0 - 1.6 - .4}{1.6 \times 10^{-3}} = 1.87k\Omega, \text{ select } 1.8k\Omega \pm 5\%$$

$R_{(MIN)} = 1710\Omega$
$R_{(MAX)} = 1890\Omega$

Step 2. $I_{F\ (MAX)}$

$$I_{F\ (MIN)} = \frac{V_{cc1\ (MIN)} - V_{F\ (MAX)} - V_{OL}}{R_{in\ (MAX)}} \qquad (25)$$

$$I_{F\ (MIN)} = \frac{4.75 - 1.7 - .4}{1890\Omega} = 1.4\ mA$$

Step 3. $I_{F\ (MAX)}$

$$I_{F\ (MAX)} = \frac{V_{cc1\ (MAX)} - V_{F\ (MIN)} - V_{OL}}{R_{in\ (MIN)}} \qquad (26)$$

$$I_{F\ (MAX)} = \frac{5.25 - 1.4 - .4}{1710\Omega} = 2.02\ mA$$

Step 4. Determine continuous operation time for LED emitter.

$$t_{\text{continuous lifetime}} = \left[t_{\text{system lifetime}}\right]\left[\text{Data Duty Factor}\right]\left[\text{System Use Duty Factor}\right]$$

$$= (40\ yr \times 8.76\ k\ hr/yr)(50\%)(50\%)$$

$$t_{\text{continuous lifetime}} = 87.60K\ hr$$

Step 5. Obtain the mean and mean + 2σ CTR degradation at $I_{F\ (MAX)}$ and $t_{\text{continuous lifetime}}$ either as an approximation from Figure 4 or by calculations as shown below.

Step 5a. Determine $D_{\overline{x}}$

$$D_{\overline{x}} = A_o t^{.25} + S\,[I_{FS} - \overline{I}_{FS}] \qquad (27)$$

$$D_{\overline{x}} = 4.95 t_{(k\ hr)}^{.25} + [.186 \log t_{(k\ hr)} + .055]$$

$$[I_{F\ (MAX)} - 14.13\ mA]$$

$$D_{\overline{x}} = 4.95\ (87.6)^{.25} + (.186 \log 87.6 + .055)$$

$$(2.02\ mA - 14.13\ mA)$$

$D_{\overline{x}} = 10.10\%$ for 40 yr system operation

Step 5b. Determine $\overline{D}_{x + 2\sigma}$

$$D_{\overline{x} + 2\sigma} = A_o t^{.25} + [S + 2P]\ [I_{FS} + \overline{I}_{FS}] \qquad (28)$$

$$D_{\overline{x} + 2\sigma} = 9.7 t_{(k\ hr)}^{.25} + [2\ (.063 \log t_{(k\ hr)} + .081)$$

$$+ (.186 \log t_{(k\ hr)} + .055)]$$

$$\times [I_{F\ (MAX)} - 14.13\ mA]$$

$$D_{\bar{x}+2\sigma} = 9.7\ (87.6)^{.25} + [2\ (.063 \log 87.6 + .081)$$

$$+ (.186 \log 87.6 + .055)]$$

$$\times [2.02\ mA - 14.13\ mA]$$

$$D_{\bar{x}+2\sigma} = 19.71\%$$

Step 6. Guardband the worst case value of CTR degradation.

It is often desirable to add some additional operating margin over and above conditions dictated by simple worst case analysis. The use of engineering judgement to increase the worst possible CTR degradation by an additional 5% margin would insure that the entire distribution would fall within the analysis. Thus,

$$D_{\bar{x}+2\sigma} + 5\% = 24.71\%$$

Step 7. Selecting $R_{L\ (MIN)}$ for guardbanded worst case

$D_{\bar{x}+2\sigma} + 5\%$, m = 1

(22)

$$R_{L(MIN)} \geqslant \frac{V_{cc2\ (MAX)} - V_{OL}}{\frac{I_{F(MIN)} \cdot CTR_{(MIN)}\left(1 - \frac{D_{\bar{x}+2\sigma} + 5\%}{100}\right)}{100} - mI_{IL}}$$

$$R_{L(MIN)} \geqslant \frac{5.25 - .4}{\frac{1.4 \times 10^{-3} \cdot 500\% \left(1 - \frac{24.71\%}{100}\right)}{100} - 1\ (1.6\ mA)}$$

$$R_{L\ (MIN)} = 1.32k\Omega$$

Step 8. Select $R_{L\ (MAX)}$

$$R_{L\ (MAX)} \leqslant \frac{V_{cc2\ (MIN)} - V_{OH}}{I_{OH\ (MAX)} + mI_{IH}} \qquad (29)$$

$$R_{L\ (MAX)} \leqslant \frac{4.75 - 2.4}{250\mu A + 40\mu A} = 8.1k$$

The range of R_L is from 1.32kΩ to 8.1kΩ. It is desirable to select a pull-up resistor which optimizes both speed performance and additional I_O guardband. This criteria leads to a tradeoff between a value close to $R_{L\ (MIN)}$ for speed performance and one bordering near $R_{L(MAX)}$ for I_O guardbanding. In this design example, the system's lifetime has a higher priority than does the moderate speed performance demanded from the optocoupler. An R_L of 3.3kΩ ± 5% is selected under this condition.

An additional guardband of 5% was added to the worst case $D_{\bar{x}+2\sigma}$ CTR degradation guardband to insure that even a greater percentage of the distribution would be accounted for. The actual percentage difference between $I_{OL\ (MAX)}$ and $I_{O\ (MIN)}$ at the end of system life is shown below:

(30)

$$I_{O\ (MIN)} = \frac{CTR_{(MIN)} \cdot I_{F\ (MIN)}\left(1 - \frac{D_{\bar{x}+2\sigma}}{100}\right)}{100}$$

(31)

$$I_{OL\ (MAX)} = \frac{V_{cc2\ (MAX)} - V_{OL}}{R_{L\ (TYP-5\%)}} + m|I_{IL}|$$

$$\%\ Guardband = \left[1 - \frac{I_{OL\ (MAX)}}{I_{O\ (MIN)}}\right] X\ 100 \qquad (32)$$

For the example shown, the additional end of system life I_O guardband results from the selection of an R_L greater than the $R_{L\ (MIN)}$ as shown in Steps 9, 10, and 11.

Step 9. $I_{O\ (MIN)}$ at end of system life

$$I_{O\ (MIN)} = \frac{500\% \cdot 1.4\ mA \cdot \left(1 - \frac{19.17\%}{100}\right)}{100} = 5.65\ mA$$

Step 10. $I_{OL\ (MAX)}$ for worst case of $I_{R\ (MAX)} + I_{IL}$

(33)

$$I_{OL\ (MAX)} = \frac{5.25 - .4}{3.13k\Omega} + 1.6\ mA = 3.14\ mA$$

Step 11. % Guardband

$$\% = 1 - \frac{3.14\ mA}{5.65\ mA}\ 100 = 44.4\% \qquad (34)$$

APPLICATIONS

Thus, this circuit interface design offers an additional 44.4% I_O guardband beyond the 19.71% required to compensate for the CTR change caused by 86.7k hr of continuous operation at an $I_{F\ (MAX)}$ of 2 mA. This extra guardband results from having chosen an R_L=3.3k rather than the lowest allowable value of R_L plus the engineering guardband chosen in Step 6.

Example 2.

System Specifications

Data Rate	250K bit NRZ
Logic Family	TTL to LSTTL
Power Supply 1 and 2	5V ± 5%
Component Tolerance	± 5%
Temperature Range	25°C
Expected System Lifetime	175 k hr (20 yr) at 50% System Use Time and 50% Data Duty Factor

Interface Conditions

Coupler 6N136

$CTR_{(MIN)}$ = 19% @ I_F = 16 mA
V_{OL} = .4V
I_{OH} = 500 nA @ V_{cc2} = 5.0V
$V_{F(TYP)}$ = 1.6V @ I_F = 16 mA
$V_{F(MIN)}$ = 1.5V @ I_F = 16 mA
$V_{F(MAX)}$ = 1.7V @ I_F = 16 mA

Logic LSTTL

I_{IL} = .36 mA I_{OL} = 8 mA
V_{IL} = .8V V_{OL} = .5V
I_{IH} = 40μA I_{OH} = 400μA
V_{IH} = 2V V_{OH} = 2.7V

Again using Figure 7, the data rate dictates the use of a 6N136 at an $I_{F\ (TYP)}$ of 16 mA. Using the same 12 step worst case analysis, it is possible to determine the values of R_{in}, R_L and the degree of guardbanding of I_O at end of system lifetime.

Step 1. R_{in} = 187Ω, select 180Ω ± 5%
$R_{L\ (MIN)}$ = 179Ω
$R_{L\ (MAX)}$ = 189Ω

Step 2. $I_{F\ (MIN)}$ = 14.02 mA

Step 3. $I_{F\ (MAX)}$ = 19 mA

Step 4. System Lifetime

t = 43.8k hr

Step 5. $D_{\bar{x}}$ and $D_{\bar{x}+2\sigma}$ for $I_{F\ (MAX)}$ of 19 mA by calculation or from Figure 4

$D_{\bar{x}}$ = 14.5%
$D_{\bar{x}+2\sigma}$ = 28.5%
} 43.8k hr continuous lifetime

Step 6. Engineering Guardband of 5%,

$D_{\bar{x}+2\sigma}$ + 5% = 33.5%

Step 7. R_L selection with guardbanding of $D_{x+2\sigma}$ + 5%

$R_{L\ (MIN)}$ = 3.44kΩ

Step 8. $R_{L\ (MAX)}$ = 50kΩ

Step 9. $R_{L\ (TYP)}$ = 5.1kΩ ± 5%, $R_{L\ (TYP-5\%)}$ = 4.84kΩ, $R_{L\ (MAX+5\%)}$ = 5.35kΩ

Step 10. End of System Life $I_{O\ (MIN)}$

$I_{O\ (MIN)}$ = 1.5 mA

Step 11. $I_{OL\ (MAX)}$ = 1.36 mA

Step 12. Engineering % Guardband of $I_{O\ (MIN)}$ = 9.3%

Example 3.

If a particular design requirements specifies a maximum tolerable degradation over a system lifetime, the optimum value of $I_{F(TYP)}$ can be obtained from Figure 12. For example, if a maximum acceptable degradation, $D_{\bar{x}+2\sigma}$, is 40%, and a continuous operation of 400k hr is desired, this curve specifies that $I_{F\ (TYP)}$ should be less than or equal to 10 mA. A 400k hr continuous operation with 100% system duty factor as might be encountered in telephone switching equipment is equivalent to 45 years of system lifetime.

If a 6N139 split Darlington were used to interface an LSTTL logic gate with the system specifications stated, a collector pull-up resistor of as low as 160Ω could be used. If an R_L of 1k were selected, this optocoupler would offer an additional end of life guardband of 81.8%. This worst case analysis points out that with the knowledge of selecting proper values of R_L, the CTR performance of the

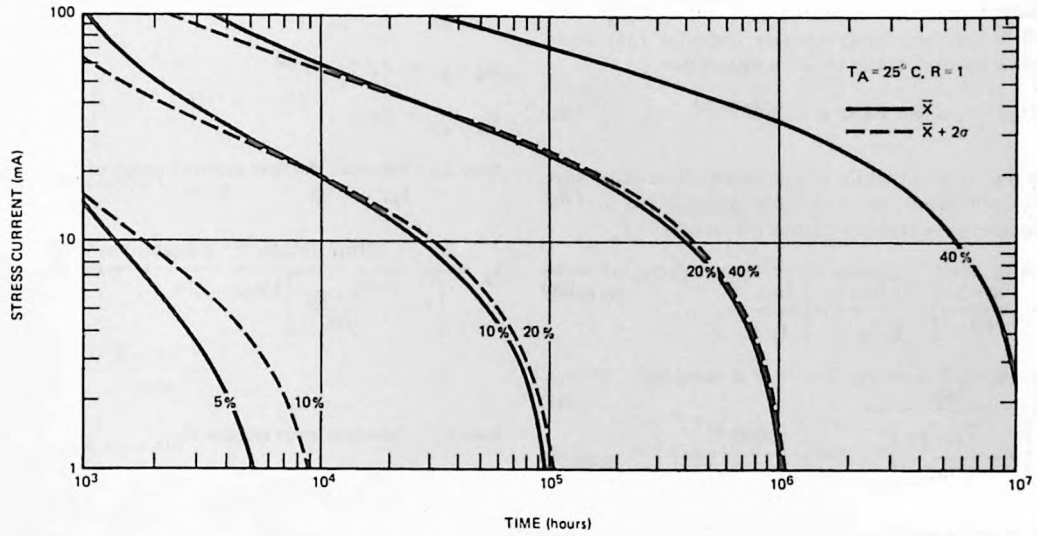


Figure 12. Stress Current (I_{FS}) vs. Time vs. % Degradation.

coupler far exceeds the normal MTBF requirements for most commercial electronic systems.

Consideration of the Optically Coupled Gate

System data speed requirements in the multi-megabit range can also be communicated through an optocoupler. The first three coupler families listed in Figure 9 are not applicable in these very high speed data interface applications; however, the optically coupled gate, 6N137, will function to speeds of up to 10 MHz. This type of coupler differs in operation from the single transistor and Darlington style units in that it exhibits a non-linear transfer relationship of I_F to I_O. This is shown in Figure 13. The relationship is described as a minimum threshold of LED input current, I_{Fth} which is required to cause the output transistor to sink the current supplied by the pull-up resistor and interconnected gate. As the LED degrades, the effect is that a larger value of $I_{F\,th}$ is required to create the same detector photodiode current necessary to switch the output gate.

In the previous interface examples, the worst case analysis and guardbanding is based on the output collector current, I_O. With the optically coupled gate, worst case guardbanding is concerned with the selection of the initial value of the I_F, which at end of system lifetime will generate the necessary threshold photocurrent demanded by the gate's amplifier to change state.

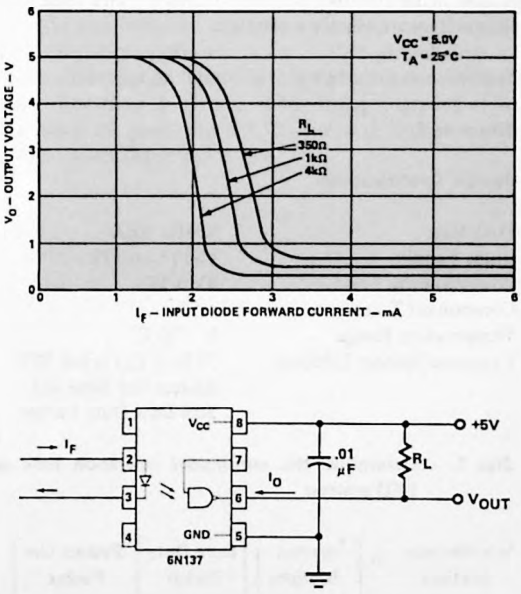


Figure 13. 6N137 Input – Output Characteristics.

The calculation of the required I_F to allow for worst case LED degradation is approached by guardbanding the guaranteed minimum isolator input current, I_{FH}, for a specified I_{OL} and V_{OL} interface. Equation (35) shows the relationship of the I_P to I_F for this coupler.

$$I_P \alpha (I_F)^n \quad \text{, where } 1.1 \leq n \leq 1.3 \tag{35}$$

Using the concept that the guardbanding of the initial value of I_F will result in a similarly guardbanded I_P, the relationship presented in Equation (36) results:

$$\left[1 - \frac{D_{\bar{x}} + 2\sigma}{100}\right] = \left[\frac{I_{PH}}{I_P}\right] = \left[\frac{I_{FH}}{I_F}\right]^n \tag{36}$$

$$I_F = \frac{I_{FH}}{\left[1 - \frac{D_{\bar{x}} + 2\sigma}{100}\right]^n} \tag{37}$$

The previous interface example showed that the first term of the $D_x + 2\sigma$ equation dominated the magnitude of the worst case degradation. This term, $A_0 R^{\alpha_t n(R)}$, i.e., $(9.7\ t_{(k\ hr)}^{.25})$, does not contain an I_F current dependent term; thus, an approximation of the worst case LED degradation can be made that relates to the system's lifetime. This initial value of $D_x + 2\sigma$ can be used in Equation (37) to calculate the initial value of the I_F. With this initial I_F, a more accurate degradation value can be calculated using Equation (28). This procedure results in an iterative process to zero in on a value of I_F that will insure reliable operation.

The following example will illustrate this approach.

Example 4.

System Specifications

Data Rate	6 MHz NRZ
Logic Family	LSTTL to TTL
Power Supply 1 and 2	5V ± 5%
Component Tolerance	± 5%
Temperature Range	0 – 70°C
Expected System Lifetime	203k hr (23 yr) at 50% System Use Time and 50% Data Duty Factor

Step 1. Determine the continuous operation time for LED emitter

$$t_{\text{continuous lifetime}} = \left[t_{\text{system lifetime}}\right]\left[\text{Data Duty Factor}\right]\left[\text{System Use Factor}\right]$$

$$= \left[23\ \text{yr}\ \ 8.76\text{k hr/yr}\right]\left[50\%\right]\left[50\%\right]$$

$$= 50.3\text{k hr}$$

Step 2. Calculate the worst case LED degradation

$$D_x + 2\sigma \approx 9.7\ t_{(k\ hr)}^{.25}$$

$$D_x + 2\sigma \approx 9.7\ (50.3)^{.25}$$

$$D_x + 2\sigma \approx 26\%$$

Step 3. Calculate the first approximation of guardbanded I_F, n = 1.2

$$I_F = \frac{I_{FH}}{\left[1 - \frac{(\approx D_{\bar{x}} + 2\sigma)}{100}\right]^{1/n}} = \frac{5\ \text{mA}}{.78} = 6.41\ \text{mA}$$

Step 4. Calculate input resistor R_{in}

$$R_{in} \leq \frac{V_{cc1\ (MIN)} - V_{F\ (MAX)} - V_{OL}}{I_F}$$

$$R_{in} \leq \frac{4.75 - 1.7 - .4}{.00641}$$

$$R_{in} \leq 413\Omega \text{ select } R_{in} = 390\Omega \pm 5\%$$

Rin (MAX)

$$R_{in\ (MAX)} = 409\Omega$$

$$R_{in\ (MIN)} = 370\Omega$$

Step 5. Calculate the $I_{F\ (MAX)}$

$$I_{F\ (MAX)} = \frac{V_{cc1\ (MAX)} - V_{F\ (MIN)} - V_{OL}}{R_{in\ (MIN)}}$$

$$I_F = \frac{5.25 - 1.4 - .4}{370}$$

$$I_F = 9.32\ \text{mA}$$

Step 6. Calculate the worst case $D_{\bar{x}} + 2\sigma$ for $I_{F\ (MAX)}$

$$D_{\bar{x}} + 2\sigma = 25.8\% + .747\ (9.32\ \text{mA} - 14.13\ \text{mA})$$

$$D_{\bar{x}} + 2\sigma = 22.2\%$$

Step 7. Calculate the new minimum required I_F at end of life based on degradation found in Step 6.

$$I_{F(EOL)} = \frac{I_{FH}}{\left[1 - \frac{22.2}{100}\right]^{1/1.2}} = \frac{5}{.81} = 6.16\,mA$$

Step 8. Calculate $I_{F\,(MIN)}$

$$I_{F\,(MIN)} = \frac{V_{cc1\,(MIN)} - V_{F\,(MAX)} - V_{OL}}{R_{in\,(MAX)}}$$

$$I_{F\,(MIN)} = \frac{4.75 - 1.7 - .4}{409}$$

$$I_{F\,(MIN)} = 6.47\,mA$$

Step 9. $R_{L\,(MIN)}$, m = 1

$$R_{L\,(MIN)} = \frac{V_{cc2\,(MAX)} - V_{OL}}{I_{OL\,(MIN)} - mI_{IL}}$$

$$= \frac{5.25 - .6}{.016 - .0016}$$

$$R_{L\,(MIN)} = 332\Omega$$

Step 10. $R_{L\,(MAX)}$, m = 1

$$R_{L\,(MAX)} = \frac{V_{cc2\,(MAX)} - V_{OH}}{I_{OH\,(MAX)} + mI_{IH}}$$

$$R_{L\,(MAX)} = \frac{4.75 - 2.4}{250\mu A + 40\mu A}$$

$$R_{L\,(MAX)} = 8.1k\Omega$$

Step 11. Minimum % Emitter Degradation Guardband

$$\%_{(MIN)} = \left[1 - \frac{I_{F\,(EOL)}}{I_{F\,(MIN)}}\ 100\right] \qquad (38)$$

$$4.8\% = \left[1 - \frac{6.16\,mA}{6.47\,mA}\ 100\right]$$

where I_F (EOL) represents the switching threshold at the end of life.

Step 12. Maximum % Emitter Degradation Guardband

$$\%_{(MAX)} = \left[1 - \frac{I_{F\,(EOL)}}{I_{F\,(MAX)}}\right]100 \qquad (39)$$

$$34\% = \left[1 - \frac{6.16\,mA}{9.32\,mA}\ 100\right]$$

The conclusions that are to be drawn from this analysis are that as long as the $I_{F\,(MAX)}$ is less than $I_{\overline{FS}} = 14.13$ mA, the worst-worst case CTR degradation may be calculated using only the first term, $A_o R^{\alpha_t n(R)}$, of the $D_{\overline{x}+2\sigma}$ case. In the example presented, 26% degradation was determined from the first term, and when the more accurate calculation using Equation (28) was used, a 22% degradation resulted. The end of life I_F guardband may be calculated using Equations (38) and (39). Using Equation (38), the minimum guardband is 5.7%, and with Equation (39), the maximum guardband is 35%.

HEWLETT PACKARD

APPLICATION NOTE 1003

Interfacing 18 Segment Displays to Microprocessors

INTRODUCTION

Over the past four years, the need for alphanumeric displays has grown very rapidly due to the extensive use of microprocessors in new system designs. The HDSP-6508 and HDSP-6300 alphanumeric displays were developed to provide a low cost, easy-to-use alternative to 5x7 dot matrix displays. These displays use an 18 segment display font that includes a centered decimal point and colon for increased readability. This font is capable of displaying the 64 character ASCII subset (numbers, punctuation symbols, and upper case alphabet) as well as many special purpose symbols. The HDSP-6504 and HDSP-6508 are 3.81 mm (0.150") red 4 or 8 character displays in a dual-in-line package. The HDSP-6300 is a 3.56 mm (0.140") red 8 character display in a dual-in-line package. The HDSP-6508 has character-to-character spacing on 6.35 mm (0.250") centers while the HDSP-6300 has character-to-character spacing on 5.08 mm (0.200") centers. Paralleling the development of these alphanumeric displays have been the introduction of several new display interface circuits that simplify the use of the 18 segment display. These circuits include an ASCII to 18 segment decoder/driver and improved NPN Darlington digit drivers that are designed to interface directly to 5 volt digital logic. This Application Note deals with several techniques to interface the 18 segment display to microprocessor systems. Depending upon the overall system configuration, microprocessor time available to dedicate to display support, and the type of information to be displayed, the system designer would choose the best interface technique to drive an 18 segment display.

DISPLAY INTERFACE TECHNIQUES

This application note will deal with four different techniques, as shown in Figure 1a-d, for interfacing the HDSP-6508 and HDSP-6300 displays to microprocessor systems.

1a. The REFRESH CONTROLLER interfaces the microprocessor system to a multiplexed LED display. The controller periodically interrupts the microprocessor and after each interrupt, the microprocessor supplies new display data for the next refresh cycle of the display.

1b. The DECODED DATA CONTROLLER refreshes a multiplexed LED display independently from the microprocessor system. A local RAM stores decoded display data. This data is continuously read from the RAM and then used to refresh the display. Whenever the display message is changed, the microprocessor decodes each character in software and writes the decoded data into the local RAM.

1c. The CODED DATA CONTROLLER also refreshes a multiplexed LED display independently from the microprocessor system. The local RAM stores ASCII data which is continuously read from the RAM, decoded, and used to refresh the display. The display message is changed by writing new ASCII characters within the local RAM.

1d. The DISPLAY PROCESSOR CONTROLLER uses a separate microprocessor to drive the LED display. This microprocessor provides ASCII storage, ASCII decode, and display refresh independently from the main microprocessor system. Software within the dedicated microprocessor provides many powerful features not available in the other controllers. The main microprocessor updates the LED display by sending new ASCII characters to the slave microprocessor.

COMPARISON OF INTERFACE TECHNIQUES

The choice of a particular interface is an important consideration because it affects the design of the entire microprocessor system. Each interface requires one or more memory or I/O addresses. These addresses are generated by decoding the microprocessor address bus. The display decoder can be located within the microprocessor program or as circuitry within the display interface. Location of the display decoder within the microprocessor program gives the designer total control of the display font within the program. This feature can be particularly important if the display will be used to display different languages and special graphics symbols. The interface technique chosen may limit or interfere with some programming techniques used in the rest of the microprocessor program. For example, the use of an

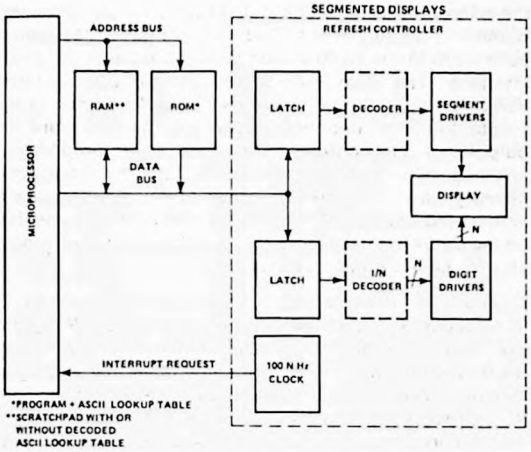


Figure 1a. REFRESH CONTROLLER Display Interface

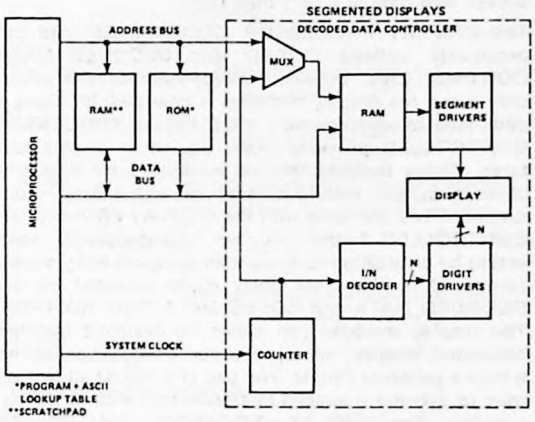


Figure 1b. DECODED DATA CONTROLLER Display Interface

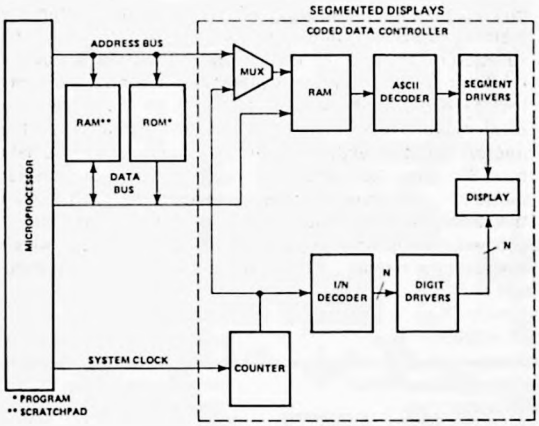


Figure 1c. CODED DATA CONTROLLER Display Interface

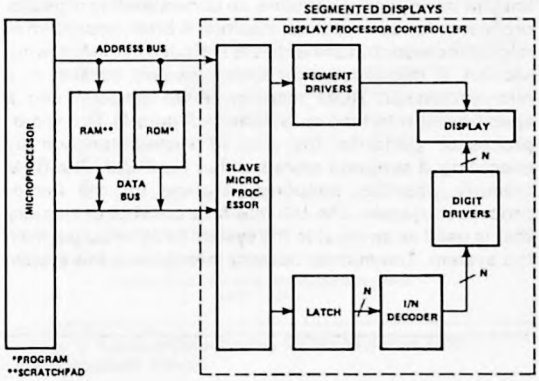


Figure 1d. DISPLAY PROCESSOR CONTROLLER Display Interface

interrupt may restrict the use of some programming techniques used in the interruptable portions of the microprocessor program.

The REFRESH CONTROLLER requires continuous interaction from the microprocessor system. Since the microprocessor actively strobes the LED display, the display interface circuitry is reduced. Generally, this technique provides the lowest hardware cost for any given display length. The display decoder can be located either within the microprocessor program or as circuitry within the interface. Display strobing is accomplished through use of the microprocessor interrupt circuitry. Demands upon microprocessor time are directly proportional to display length.

The DECODED DATA CONTROLLER and CODED DATA CONTROLLER require microprocessor interaction only when the display message is changed. Both techniques employ a local RAM memory that is continuously scanned by the display interface electronics. For the DECODED DATA CONTROLLER, the display decoder is located within the microprocessor software and the local RAM stores decoded display data. The CODED DATA CONTROLLER includes the display decoder within the display interface circuitry and the local RAM stores ASCII data. Since ASCII data is more compact than decoded display data, the CODED DATA CONTROLLER uses a smaller RAM than the DECODED DATA CONTROLLER. Both techniques allow the microprocessor to individually

change each display character by a memory or I/O write to a specific display address. These interface techniques can accept new data at a very high rate.

The DISPLAY PROCESSOR CONTROLLER, like the previously defined CODED and DECODED DATA CONTROLLERS, requires microprocessor interaction only when the display message is changed. By using a dedicated microprocessor, the DISPLAY PROCESSOR CONTROLLER provides many additional display features. These features include multiple entry modes, a blinking cursor, editing commands, and a data output function. The software with the DISPLAY PROCESSOR CONTROLLER further reduces microprocessor interaction by providing more sophisticated data entry modes compared to the RAM entry mode provided by the DECODED DATA and CODED DATA CONTROLLERS. The display decoder can either be designed into the dedicated display microprocessor or can be located within a separate PROM. The use of a PROM allows the user to provide a special character font with additional circuitry. The DISPLAY PROCESSOR CONTROLLER does not allow as high a data entry rate as either the DECODED DATA or CODED DATA CONTROLLERS.

MICROPROCESSOR OPERATION

In order to effectively utilize the interface techniques outlined in the following sections, an understanding of microprocessor fundamentals is required. A brief description of microprocessor fundamentals is included in the following section. A microprocessor system usually consists of a microprocessor, ROM memory, RAM memory, and a specific I/O interface as outline in Figure 2. The microprocessor performs the desired system function by executing a program stored within the ROM. The RAM memory provides temporary storage for the microprocessor system. The I/O interface consists of circuitry that is used as an input to the system or as an output from the system. The microprocessor interfaces to this system through an address bus, data bus, and control bus. The address bus consists of several outputs (A_0, A_1,...A_n) from the microprocessor which collectively specify a binary number. This number or "address" uniquely specifies each word in the ROM memory, RAM memory, and I/O interface. The data bus serves as an input to the microprocessor during a memory or input read and as an output from the microprocessor during a memory or output write. The control bus provides the required timing and signals to the microprocessor system to distinguish a memory read from a memory write, and in some systems an I/O read from an I/O write. These control lines and the timing between the address bus, data bus, and control bus vary for different microprocessors.

The address, data, and control buses provide the flow of instructions and data into the microprocesor. Program execution consists of a series of memory reads (instruction fetches) which are sometimes followed by a memory read or write (instruction execution). The microprocessor performs a memory read by outputting the memory address of the word to be read on the address bus. This address uniquely specifies a word within the memory system. The microprocessor also outputs a signal on the control bus, which instructs the memory system to perform a memory read. The address selects one memory element, either RAM or ROM, within the memory system. Then, the desired word within the selected memory element is gated on the data bus by the read signal. Meanwhile, the unselected memory elements tristate their output lines so that only the selected memory element is active on the data bus. After sufficient delay, the microprocessor reads the word that appears on the data bus. Similarly, for a memory write, the microprocessor outputs the memory address of the word to be written on the address bus. After sufficient delay, the microprocessor outputs a signal on the control bus, which instructs the memory system to perform a memory write.

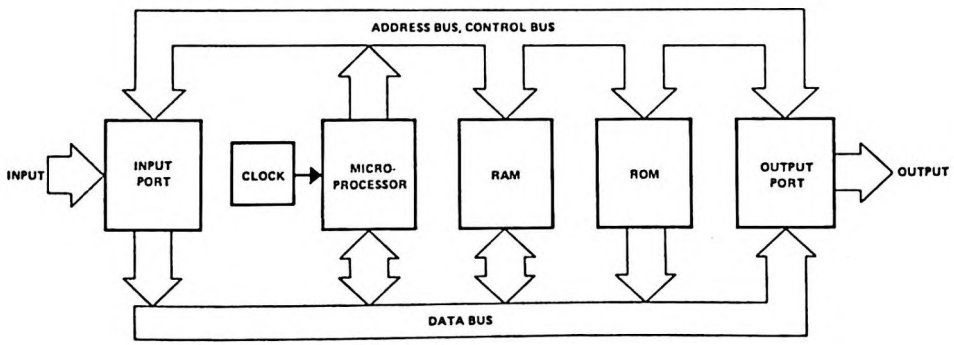


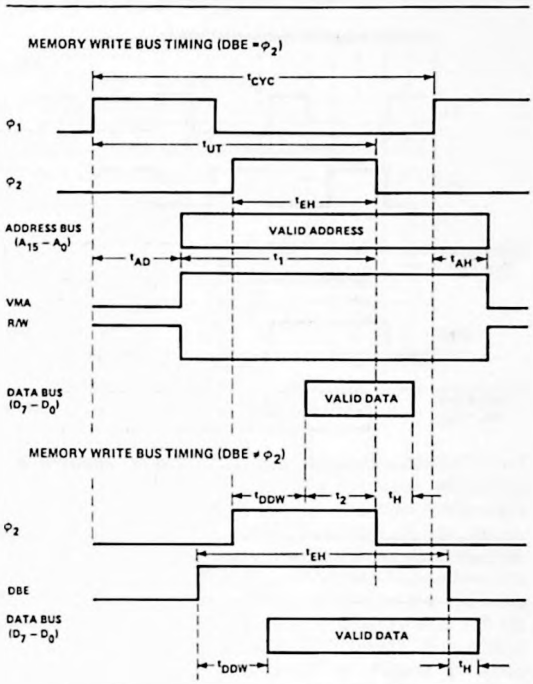
Figure 2. Block Diagram of a Typical Microprocessor System

The microprocessor also outputs the desired memory word on the data bus. The address selects one RAM memory element within the memory system. The write signal causes the memory element to read the word on the data bus and store it at the desired location. After the write cycle has been completed, the new word will have replaced the previous word within the RAM memory. During the memory write, outputs from the unselected memory elements remain tristated so that only the microprocessor is active on the data bus. These control lines and the timing for the address bus, data bus, and control bus vary for different microprocessors.

Some microprocessors, such as the Motorola 6800 microprocessor family, handle memory and I/O in exactly the same way. Memory and I/O occupy a common address space and are accessed by the same instructions. With this type of microprocessor, the hardware decoding of the address bus determines whether the read or write is to a memory or I/O element. Other microprocessors, such as the Intel 8080A, Intel 8085A, and the Zilog Z-80 have separate address spaces for memory and I/O. These microprocessors use different instructions for a memory access or an I/O access and provide signals on the control bus to distinguish between memory and I/O. One advantage of this approach is that the I/O address space can be made smaller to simplify device decoding. However, the I/O instructions that are available are usually not as powerful as the memory reference instructions. Of course, the user can always locate specific I/O devices within the memory address space through proper decoding of the address and control buses. This would allow these I/O devices to be accessed with memory reference instructions.

The 6800 microprocessor family has a 16 line address bus, 8 line data bus, and a control bus that includes the signals VMA (Valid Memory Address), R/$\overline{W}$ (Read/Write), DBE (Data Bus Enable), and clock signals ϕ_1 and ϕ_2. R/$\overline{W}$ specifies either a memory read or write while VMA is used in conjunction with R/$\overline{W}$ to specify a valid memory address. DBE gates the internal data bus of the 6800 to the external data bus. In many applications, DBE is connected to ϕ_2. Additional data hold time, t_H, can be achieved by delaying ϕ_2 to the microprocessor or by extending DBE beyond the falling edge of ϕ_2. The timing between the address bus, data bus, VMA, and R/$\overline{W}$ for a memory write is shown in Figure 3.

For the 8080A microprocessor, the address bus consists of 16 lines, the data bus consists of 8 lines, and the control bus consists of several lines including DBIN (Data Bus In), $\overline{WR}$ (Write), SYNC (Synchronizing Signal), READY, and clock signals ϕ_1 and ϕ_2. DBIN and $\overline{WR}$ are used to specify a read or write operation. The 8080A microprocessor distinguishes memory from I/O through the use of a status word that precedes every machine cycle. When SYNC is high, the status word should be loaded into an octal latch on the positive edge of ϕ_1. The outputs from the latch can then be decoded to specify whether the machine cycle is a memory write, memory read, I/O write, or I/O read. The Intel 8228 or 8238 System Controller provides this status latch and additionally encodes the outputs of the status latch with DBIN and $\overline{WR}$ to generate four timing signals $\overline{MEM\ R}$ (Memory Read), $\overline{MEM\ W}$ (Memory Write), $\overline{I/O\ R}$ (I/O Read), and $\overline{I/O\ W}$ (I/O Write). However, the 8228 and 8238 do not provide the outputs of the status latch. The timing between the address bus, data bus, $\overline{WR}$, and SYNC



6800 MICROPROCESSOR	MINIMUM TIMES (nS)				
	t_{DDW} (MAX)	t_1	t_{AH}	t_2	t_H
6800, t_{CYC} = 1000	225	630	30	225	10
68A00, t_{CYC} = 666	200	420	30	80	10
68B00, t_{CYC} = 500	160	290	30	60	10

$t_1(MIN) = t_{UT}(MIN) - t_{AD}(MAX)$

$t_2(MIN) = t_{EH}(MIN) - t_{DDW}(MAX)$

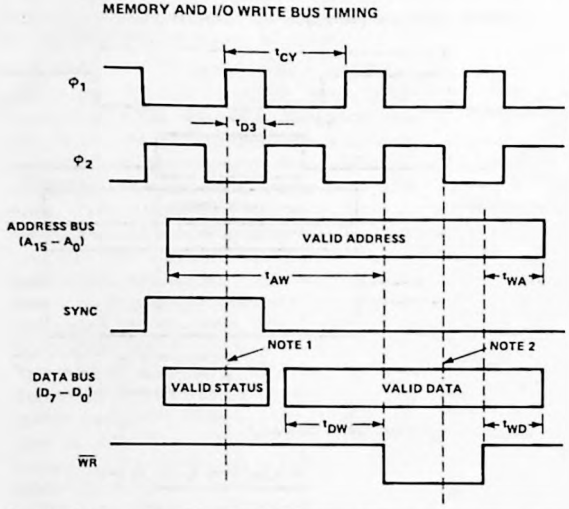
From MOTOROLA SEMICONDUCTOR MC6800 Data Sheet (DS9471), 1978

Figure 3. Memory Write Timing for the Motorola 6800 Microprocessor Family.

for both a memory write and an I/O write is shown in Figure 4. The 8080A also provides an input, READY, which allows the memory system to extend the time the address and data bus is valid by integral clock cycles.

REFRESH CONTROLLERS

Figure 5 shows a REFRESH CONTROLLER for a 16 character 18 segment alphanumeric display. The circuit operates by interrupting the microprocessor at a 1600 Hz rate. Following each interrupt, the microprocessor responds by outputting a new ASCII character to the Texas Instruments AC5947 ASCII to 18 Segment Decoder/Driver and a new digit word to the 74LS174. The character font for the AC5947 is shown in Figure 6. The outputs of the 74LS174 are decoded such that digit word 00_{16} turns the leftmost display character on, digit word $0F_{16}$ turns the rightmost display character on, and digit word $1F_{16}$ turns all digits off. The interface can be expanded to 24 characters with an additional Signetics NE590 driver. This change would also require modifications in I_F peak, and the interrupt rate.



8080 MICROPROCESSOR WITH 8228 CLOCK	MINIMUM TIMES (nS)			
	t_{AW}	t_{WA}	t_{DW}	t_{WD}
8080A, t_{CY} = 480	740	90	230	90
8080A-2, t_{CY} = 380	560	80	140	80
8080A-1, t_{CY} = 320	470	70	110	70

$t_{AW} = 2t_{CY} - t_{D3} - [140(A), 130(A-2), 110(A-1)]$

$t_{WA} = t_{WD} = t_{D3} + 10$

$t_{DW} = t_{CY} - t_{D3} - [170(A), 170(A-2), 150(A-1)]$

From INTEL Component Data Catalog, 1978

NOTE 1: Status Word should be loaded into an octal latch when SYNC = 1 on positive edge of φ_1.

NOTE 2: Additional wait cycles can be inserted here. A wait cycle is added by forcing READY low prior to the falling edge of φ_2 during the clock cycle preceeding the falling edge of $\overline{WR}$.

Figure 4. Memory and I/O Write Timing for the Intel 8080A Microprocessor Family

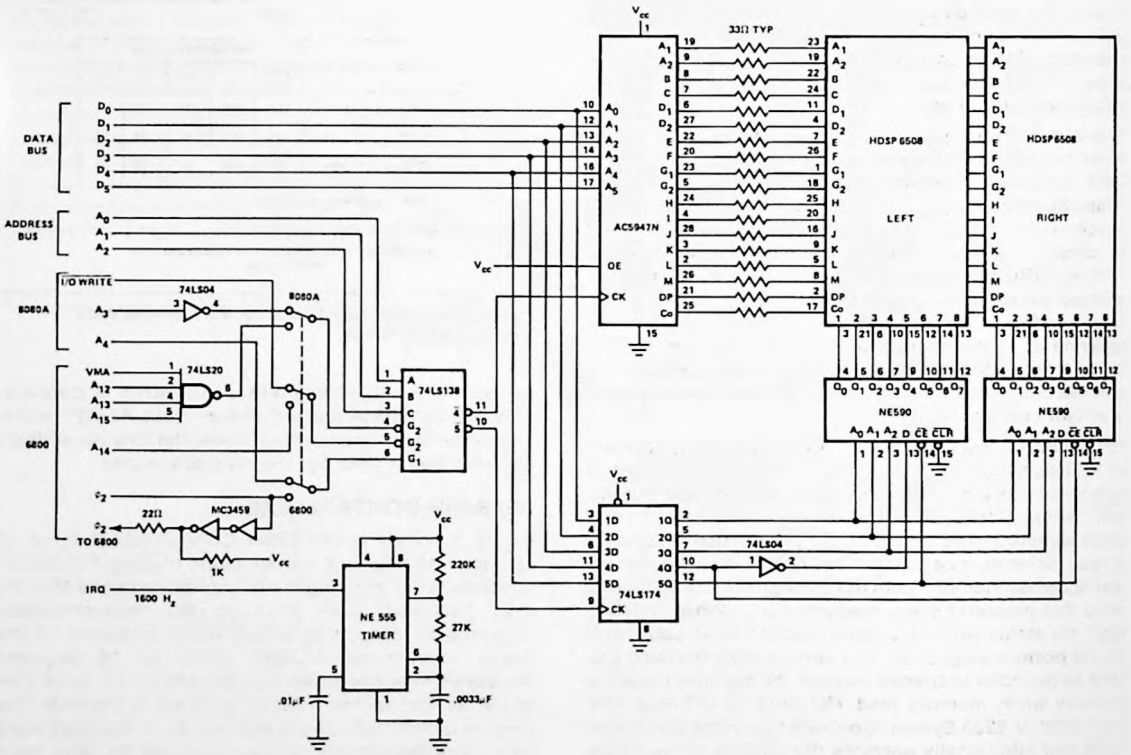


Figure 5. 6800 or 8080A Microprocessor Interface to the HDSP-6508 REFRESH CONTROLLER Utilizing the Texas Instruments AC5947 ASCII to 18 Segment Decoder/Driver

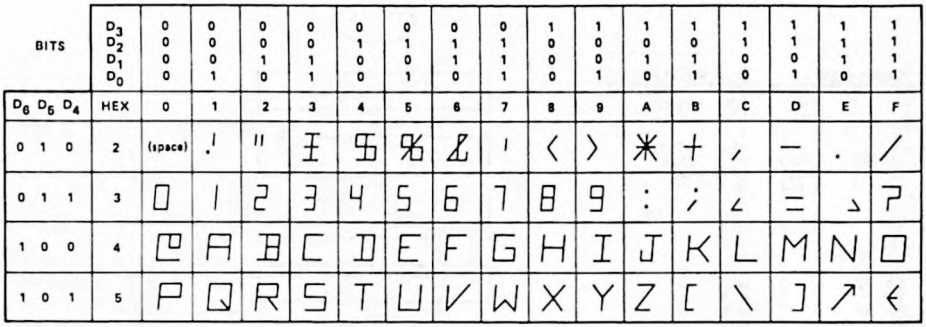


Figure 6. 18 Segment Display Font for the Texas Instruments AC5947 ASCII to 18 Segment Decoder/Driver

A 6800 microprocessor program that interfaces to this REFRESH controller is shown in Figure 7. Following each interrupt, the program "RFRSH" is executed. The program uses a scratch pad register "POINT" that points to the location within a 16 byte ASCII message of the next ASCII character to be stored in the display interface. The scratch pad register "DIGIT" contains the next digit word to be loaded into the display interface. The program interfaces to the circuit through two memory or I/O addresses. A memory write to address "SEG" writes a six bit word into the AC5947, and a memory write to address "DIG" writes a five bit word into the 74LS174. To prevent undesirable ghosting, the digit drivers are turned off prior to loading the next ASCII character into the AC5947. After sufficient delay, the next digit is turned on. Registers "POINT" and "DIGIT" are then updated by the program. Following execution of the "RTI" instruction, execution of the main program is resumed. A similar program written for an 8080A microprocessor is shown in Figure 8. The 6800 microprocessor program shown in Figure 7 operated with a 1 MHz clock requires 0.11% + 0.72n% of the available microprocessor time to refresh the display at a 100 Hz refresh rate, where n is the display length. The 8080A microprocessor program shown in Figure 8 when operated with a 2 MHz clock requires 0.31% + 0.96n% of the available microprocessor time to refresh the display at a 100 Hz refresh rate, where n is the display length. For example, the 16 character display shown in Figure 5

```
LOC   OBJECT CODE        SOURCE STATEMENTS
      BF04               SEG     EQU   $BF04
      BF05               DIG     EQU   $BF05

0000  0003               POINT   FDB   DATA
0002  00                 DIGIT   FCB   0
0003                     DATA    RMB   16

0400                     ORG     $0400
0400  DE  00     RFRSH   LDX     D,POINT
0402  E6  00             LDA B   X,0
0404  86  1F             LDA A   I,$1F
0406  B7  BF05           STA A   E,DIG
0409  F7  BF04           STA B   E,SEG
040C  96  02             LDA A   D,DIGIT
040E  81  0F             CMP A   I,15
0410  27  0A             BEQ     LOOP1
0412  7C  0002           INC     E,DIGIT
0415  08                 INX
0416  B7  BF05           STA A   E,DIG
0419  DF  00             STX     D,POINT
041B  3B                 RTI
041C  7F  0002   LOOP1   CLR     E,DIGIT
041F  F6  0001           LDA B   E,POINT+1
0422  B7  BF05           STA A   E,DIG
0425  C0  0F             SUB B   I,15
0427  D7  01             STA B   D,POINT+1
0429  24  03             BCC     LOOP2
042B  7A  0000           DEC     E,POINT
042E  3B         LOOP2   RTI
```

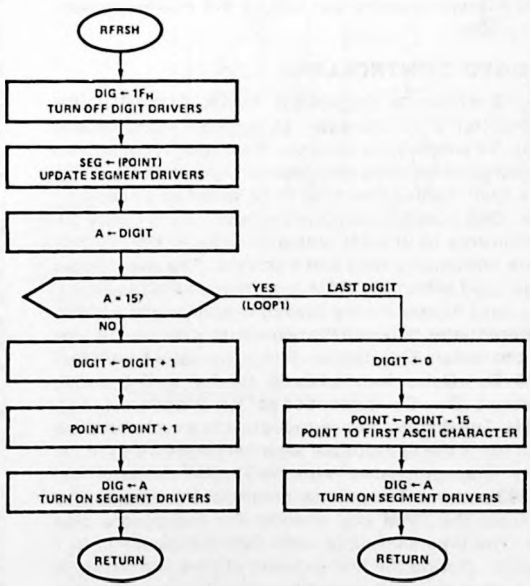


Figure 7. 6800 Microprocessor Program and Flowchart that Interfaces to the REFRESH CONTROLLER Shown in Figure 5

```
LOC   OBJECT CODE          SOURCE STATEMENTS

001C                SEG    EQU   001CH
001D                DIG    EQU   001DH

                           ORG   0E000H
E000  03  E0        POINT  DW    DATA
E002  00            DIGIT  DB    00H
E003  00            DATA   DS    16

                           ORG   0E400H
E400  F5            RFRSH  PUSH  PSW
E401  E5                   PUSH  H
E402  2A  00E0             LHLD  POINT
E405  3E  1F               MVI   A,1FH
E407  D3  1D               OUT   DIG
E409  7E                   MOV   A,M
E40A  D3  1C               OUT   SEG
E40C  3A  02E0             LDA   DIGIT
E40F  D3  1D               OUT   DIG
E411  FE  0F               CPI   15
E413  CA  21E4             JZ    LOOP1
E416  3C                   INR   A
E417  32  02E0             STA   DIGIT
E41A  23                   INX   H
E41B  22  00E0  LOOP2      SHLD  POINT
E41E  E1                   POP   H
E41F  F1                   POP   PSW
E420  C9                   RET
E421  3E  00    LOOP1      MVI   A,0
E423  32  02E0             STA   DIGIT
E426  7D                   MOV   A,L
E427  D6  0F               SUI   15
E429  6F                   MOV   L,A
E42A  D2  1BE4             JNC   LOOP2
E42D  25                   DCR   H
E42E  C3  1BE4             JMP   LOOP2
```

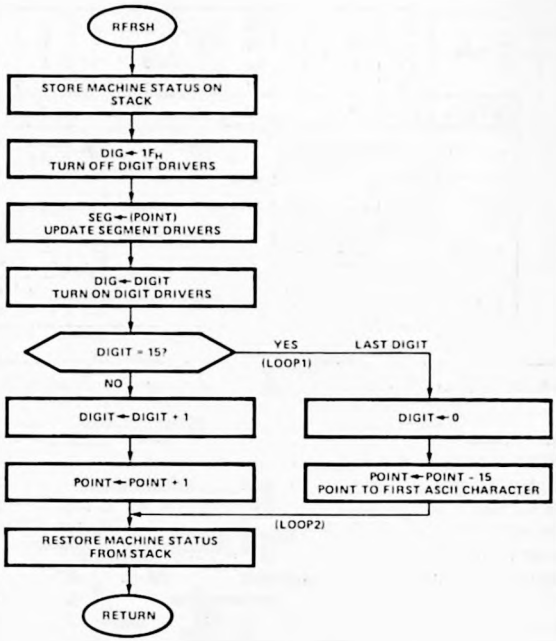


Figure 8. 8080A Microprocessor Program and Flowchart that Interfaces to the REFRESH CONTROLLER Shown In Figure 5

requires 11.6% of the 6800 microprocessor time or 15.7% of the 8080A microprocessor time to refresh the display at a 100 Hz refresh rate. Faster versions of the 6800 and 8080A microprocessors can reduce this microprocessor time by 50%.

DECODED CONTROLLERS

Figure 9 shows a DECODED DATA CONTROLLER designed for a 32 character 18 segment alphanumeric display. To simplify the circuitry, the display is configured as a 14 segment display with decimal point and colon. This allows each display character to be specified by two 8 bit words. One possible display font is shown in Figure 10. The Motorola 6810 RAM stores 64 bytes of display data that are continually read and displayed. The display data is organized within the RAM such that addresses A_5, A_4, A_3, A_2, and A_1 specify the desired character and address A_0 differentiates between the two words of display data for each character. The display data is formatted such that word 0 (D_7—D_0) is decoded as G_2, G_1, F, E, D, C, B, and A; and word 1 (D_7—D_0) is decoded as COLON, DP, M, L, K, J, I, and H. The display data is coded low true such that a low output turns the appropriate segment on. Strobing of the display is accomplished with the 74LS14 oscillator and 74LS393 counter. The counter continuously reads display data from the RAM and enables the appropriate digit driver. The time allotted to each digit is broken into four segments. During the first segment of time, the display is turned off and work 0 is read from the RAM and stored in the 74LS273 octal register. During the next three segments of time, word 1 is read from the RAM and the display is turned on. Thus, the display duty factor is (1/32) (3/4) or 1/42.6. For values of R and C specified, the display is strobed at a 130 Hz refresh rate.

Data is entered into the RAM from the address and data bus of the microprocessor via two control lines, Chip Select and Write. When Chip Select goes low, the address generated by the counter is disabled and the microprocessor address and data bus is gated to the RAM. Then, after sufficient delay, the Write input is pulsed, which stores the data within the RAM. The data entry timing for the 18 segment DECODED DATA CONTROLLER is shown in Figure 11. Because of the requirement that the address inputs of the 6810 RAM must be stable prior to the falling edge of Write, Chip Select should go low for time t_{CW} prior to the falling edge of Write. To guarantee that the address and data inputs of the RAM remain stable until after Write goes high, Chip Select should remain low for time t_{CH} following the rising edge of Write. This requirement for two separate timing signals is also required for the CODED DATA CONTROLLER shown in Figure 15. Because this interface timing is somewhat more difficult than the previously described circuits, the following methods are presented for interfacing to commonly used microprocessors.

Interface to the 6800 microprocessor family is accomplished by NANDing together VMA and some specified combination of high order address lines to generate Chip Select and using ϕ_2 to generate Write.

For the 8080A and 8085A microprocessor families, the limited flexibility of the output instruction requires that the 18 segment DECODED DATA CONTROLLER must be addressed as memory instead of I/O. The 8080A micro-

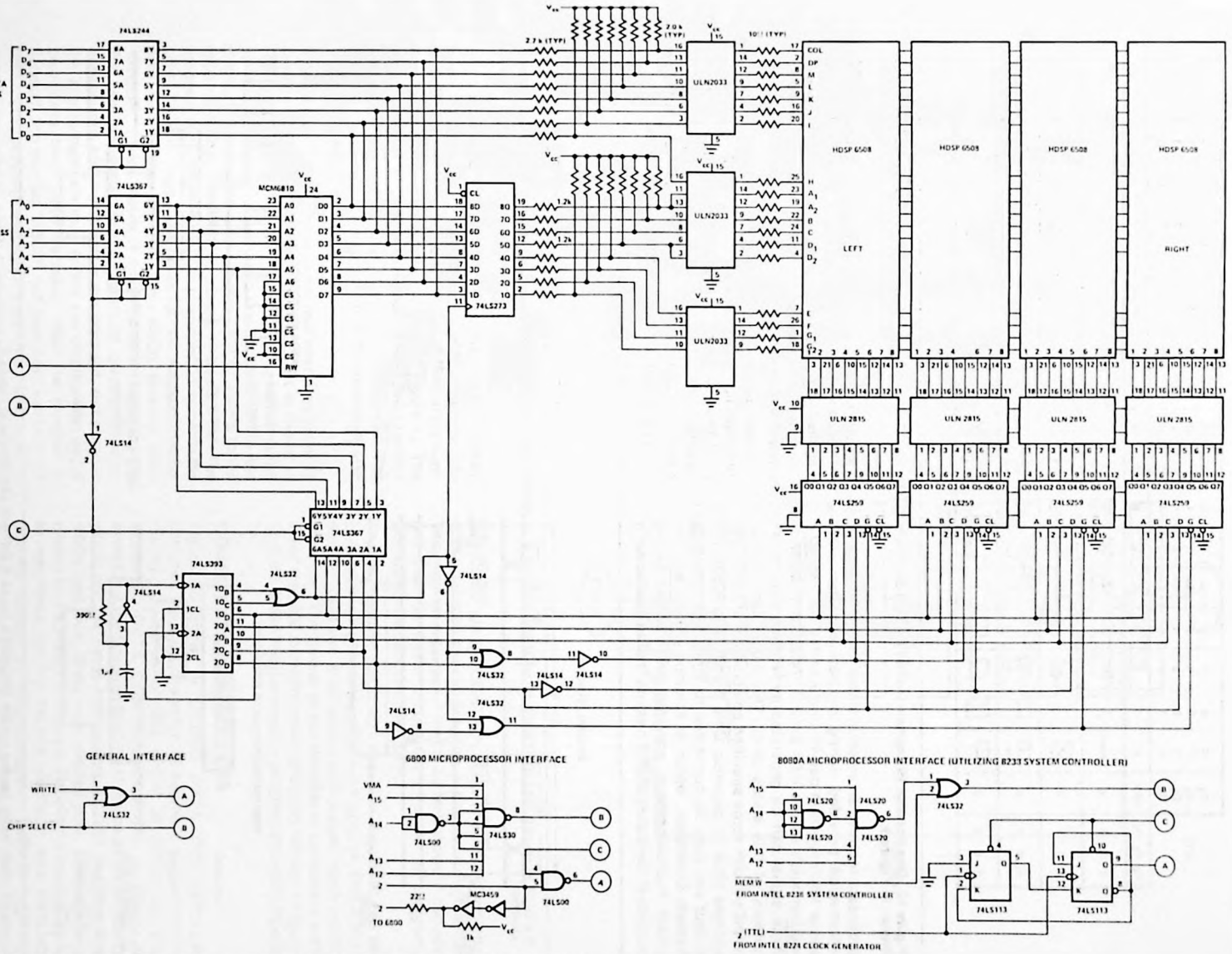


Figure 9. 6800, 8080A, and General Interface to the HDSP-6508 DECODED DATA CONTROLLER

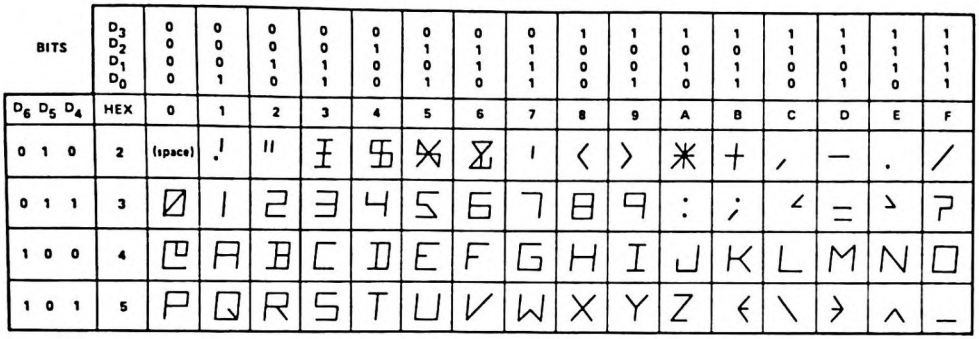
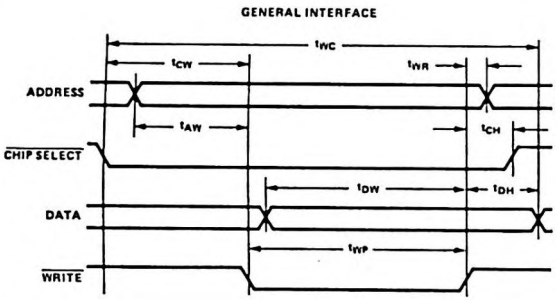


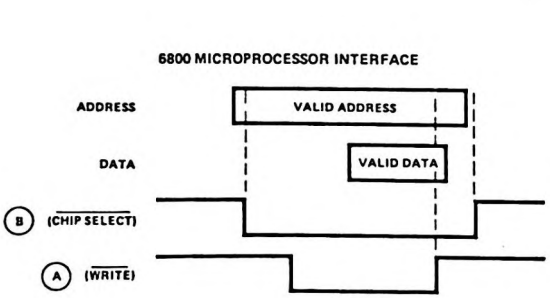
Figure 10. One Possible 16 Segment Display Font (14 Segments Plus Decimal Point and Colon) for the DECODED DATA CONTROLLER Shown in Figure 9.

processor requires an external status latch to hold status information provided during program execution. This status latch function can be implemented with an octal register such as the Intel 8212 or 74LS273. A Memory Write signal can be generated by NORing together all outputs of this status latch. This signal can then be NANDed with some specified combination of high order address lines to generate Chip Select. The 8080A WR output can then be connected to Write. The Intel 8238 System Controller, which is commonly used with the 8080A microprocessor, prevents direct access to the outputs of the status latch. An example of an interfacing to a system utilizing the 8238 is illustrated in Figure 9. MEM W from the 8238 is inverted and then NANDed with some specified combination of high order address lines to generate Chip Select. The 74LS113 generates Write from the microprocessor clock, ϕ_2 (TTL).

Interface to the 8085A microprocessor family can be accomplished by inverting the I/O/M output and NANDing the resulting signal with the S_0 output and some specified combination of high order address lines to generate Chip Select. The WR output from the microprocessor is connected directly to Write.



PARAMETER	SYMBOL	MIN.
WRITE CYCLE	t_{WC}	425ns
WRITE DELAY	t_{AW}	65ns
CHIP ENABLE TO WRITE	t_{CW}	65ns
DATA SETUP	t_{DW}	210ns
DATA HOLD	t_{DH}	35ns
WRITE PULSE	t_{WP}	325ns
WRITE RECOVERY	t_{WR}	25ns
CHIP ENABLE HOLD	t_{CH}	35ns



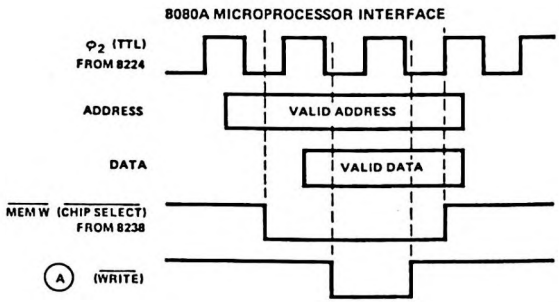


Figure 11. Data Entry Timing for the DECODED DATA CONTROLLER Shown in Figure 9

```
LOC   OBJECT CODE          SOURCE STATEMENTS

      BF00          DSPLY  EQU  $BF00
      0600          DECDR  EQU  $0600

0000  0006          ASCII  FDB  MESSGE
0002  BF00          PAD1   FDB  DSPLY
0004  0600          PAD2   FDB  DECDR
0006                MESSGE RMB  32

0400                       ORG  $0400
0400  CE  BF00       LOAD   LDX  I,DSPLY
0403  DF  02                STX  D,PAD1
0405  CE  0600              LDX  I,DECDR
0408  DF  04                STX  D,PAD2
040A  DE  00       LOOP1   LDX  D,ASCII
040C  A6  00               LDA A X,0
040E  08                   INX
040F  DF  00               STX  D,ASCII
0411  48                   ASL A
0412  97  05               STA A D,PAD2+1
0414  DE  04               LDX  D,PAD2
0416  A6  00               LDA A X,0
0418  E6  01               LDA B X,1
041A  DE  02               LDX  D,PAD1
041C  A7  00               STA A X,0
041E  08                   INX
041F  E7  00               STA B X,0
0421  08                   INX
0422  DF  02               STX  D,PAD1
0424  8C  BF40             CPX  I,DSPLY+64
0427  26  E1               BNE  LOOP1
0429  39                   RTS
```

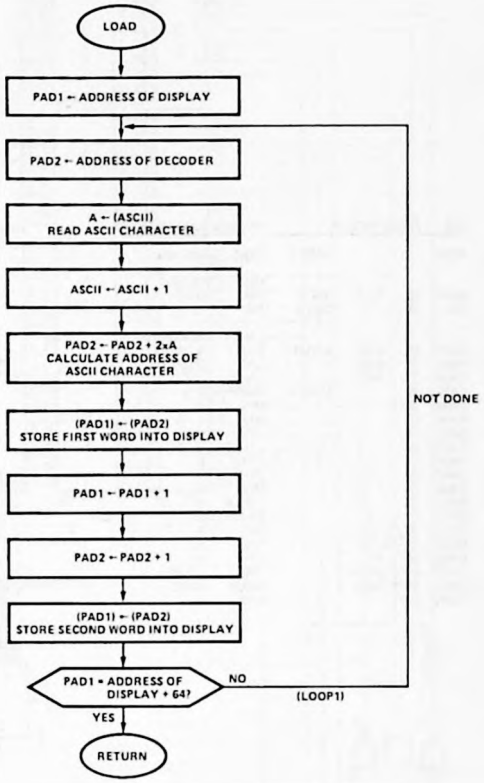


Figure 12. 6800 Microprocessor Program and Flowchart that Interfaces to the DECODED DATA CONTROLLER Shown in Figure 9

The simplest interface to the Z-80 microprocessor family is accomplished by addressing the 18 segment DECODED DATA CONTROLLER as I/O instead of memory. An example of this interface is shown in Figure 15. The $\overline{IORQ}$ output is inverted and NANDed with some specified combination of address lines to generate Chip Select. The 74LS113 circuit generates $\overline{Write}$ from the inverted microprocessor clock $\overline{\phi}$.

A 6800 microprocessor program that interfaces to the 18 segment DECODED DATA CONTROLLER is shown in Figure 12. This program decodes 32 ASCII characters and stores the resulting decoded display data within the display. The scratch pad register "ASCII" points to the location of the next ASCII character to be decoded. The program reads the first ASCII character, increments the point, "ASCII," and then looks up two words of display data within the 64 character ASCII look-up table "DECDR." These words of display data are then stored at the two addresses for the leftmost display location. Subsequent ASCII characters are decoded, and stored at the appropriate address within the display until all 32 characters have been decoded. After the program is finished, the pointer "ASCII" will have been incremented by 32. This program requires 2.4 ms for a 1 MHz clock to decode and load 32 ASCII characters into the 18 segment DECODED DATA CONTROLLER. The corresponding 8080A microprocessor program is shown in Figure 13. This program requires 1.4 ms for a 2 MHz clock to decode and load 32 ASCII characters into the 18 segment DECODED DATA CONTROLLER.

The 64 character ASCII font shown in Figure 10 can be generated using the table shown in Figure 14. This ASCII decoder uses two 8 bit words to represent each ASCII character. The format of the decoder is consistent with either the 6800 microprocessor program shown in Figure 12 or the 8080A microprocessor program shown in Figure 13.

CODED DATA CONTROLLERS

Figure 15 shows a CODED DATA CONTROLLER designed for a 32 character 18 segment alphanumeric display. Operation of this circuit is similar to the DECODED DATA CONTROLLER shown in Figure 9 except that the Motorola 6810 RAM stores 32 six bit ASCII words and the Texas Instruments AC5947 decodes this ASCII data into 18 segment display data. The resulting display font is shown in Figure 6. Strobing of the display is accomplished by the 74LS14 oscillator and 74LS393 counter. Because the long propagation delay through the AC5947 tends to cause display ghosting, the display is

```
LOC   OBJECT CODE          SOURCE STATEMENTS
BF00                DSPLY  EQU   0BF00H

                           ORG   0E000H
E000  02  E0        ASCII  DW    DATA
E002  00            DATA   DS    32

                           ORG   0E400H
E400  01  00BF      LOAD   LXI   B,DSPLY
E403  11  00E5             LXI   D,DECDR
E406  2A  00E0             LHLD  ASCII
E409  7E            LOOP1  MOV   A,M
E40A  23                   INX   H
E408  07                   RLC
E40C  5F                   MOV   E,A
E40D  1A                   LDAX  D
E40E  02                   STAX  B
E40F  13                   INX   D
E410  03                   INX   B
E411  1A                   LDAX  D
E412  02                   STAX  B
E413  03                   INX   B
E414  79                   MOV   A,C
E415  FE  40               CPI   64
E417  C2  09E4             JNZ   LOOP1
E41A  22  00E0             SHLD  ASCII
E41D  C9                   RET
```

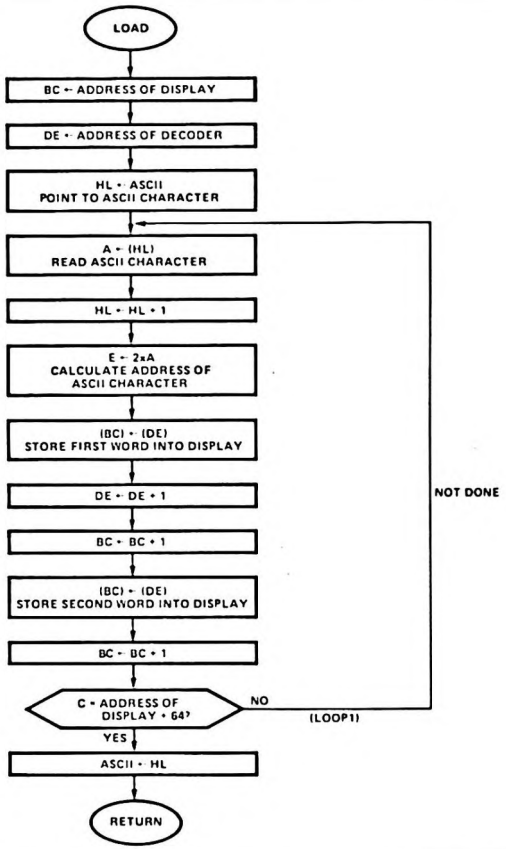


Figure 13. 8080A Microprocessor Program and Flowchart that Interfaces to the DECODED DATA CONTROLLER Shown in Figure 9

ASCII	SYMBOL	WORD 0	WORD 1
20	(SPACE)	FF	FF
21	!	FF	BD
22	"	DF	FD
23	#	36	ED
24	$	12	ED
25	%	1B	D2
26	&	F2	CA
27	'	FF	FD
28	(	FF	F3
29	)	FF	DE
2A	*	3F	C0
2B	+	3F	ED
2C	,	FF	DF
2D	-	3F	FF
2E	.	FF	BF
2F	/	FF	DB
30	0	C0	DB
31	1	FF	ED
32	2	24	FF
33	3	30	FF
34	4	19	FF
35	5	96	F7
36	6	02	FF
37	7	F8	FF
38	8	00	FF
39	9	18	FF
3A	:	FF	3F
3B	;	FF	5F
3C	<	7F	FB
3D	=	37	FF
3E	>	BF	FE
3F	?	7C	EF

ASCII	SYMBOL	WORD 0	WORD 1
40	@	44	FD
41	A	08	FF
42	B	70	ED
43	C	C6	FF
44	D	F0	ED
45	E	86	FF
46	F	8E	FF
47	G	42	FF
48	H	09	FF
49	I	F6	ED
4A	J	E1	FF
4B	K	8F	F3
4C	L	C7	FF
4D	M	C9	FA
4E	N	C9	F6
4F	O	C0	FF
50	P	0C	FF
51	Q	C0	F7
52	R	0C	F7
53	S	12	FF
54	T	FE	ED
55	U	C1	FF
56	V	CF	DB
57	W	C9	D7
58	X	FF	D2
59	Y	FF	EA
5A	Z	F6	DB
5B	[	7F	F3
5C	\	FF	F6
5D	]	BF	DE
5E	^	FF	D7
5F	_	F7	FF

Figure 14. 64 Character ASCII Decoder Table for the Microprocessor Programs Shown in Figures 12 and 13. 18 Segment Display Font is Shown in Figure 10.

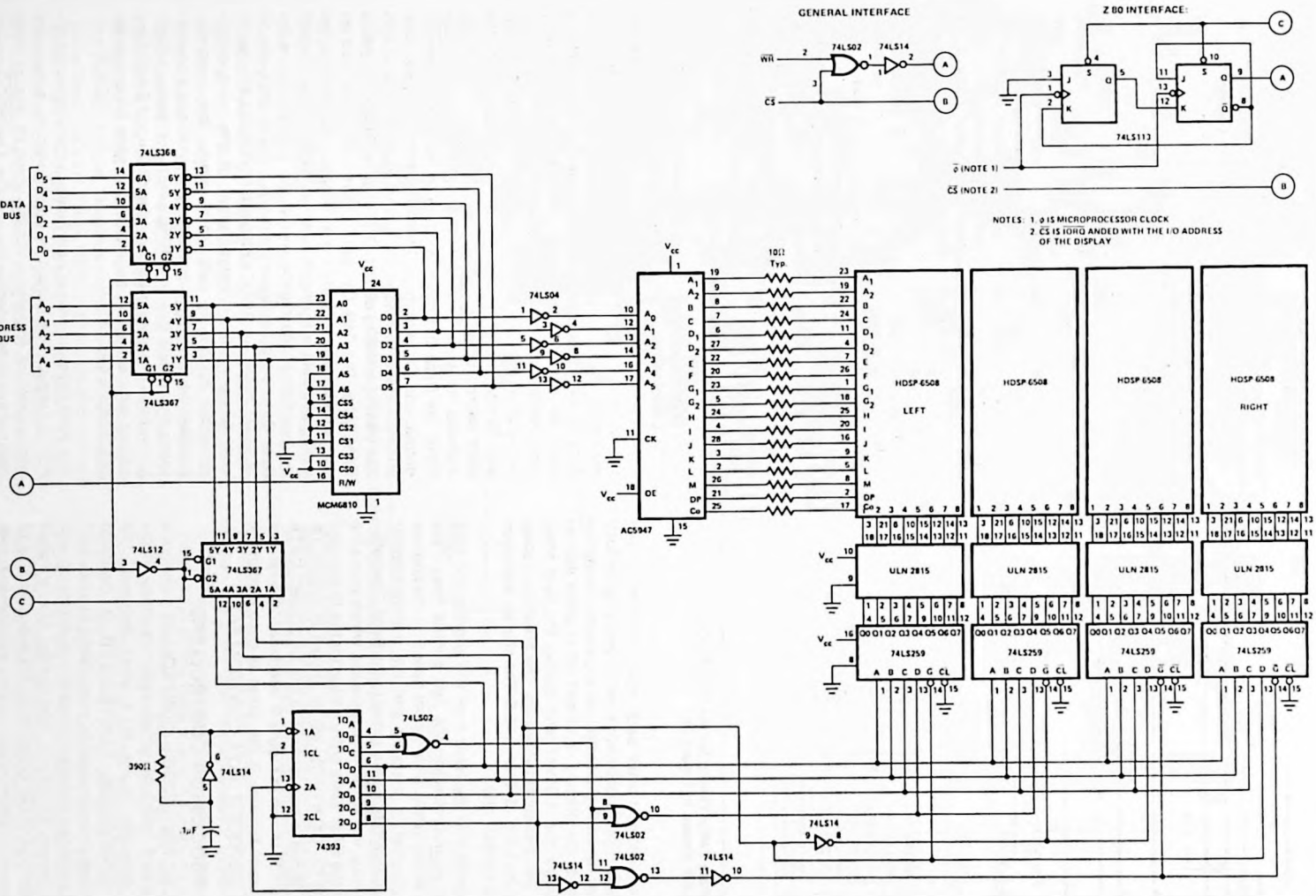
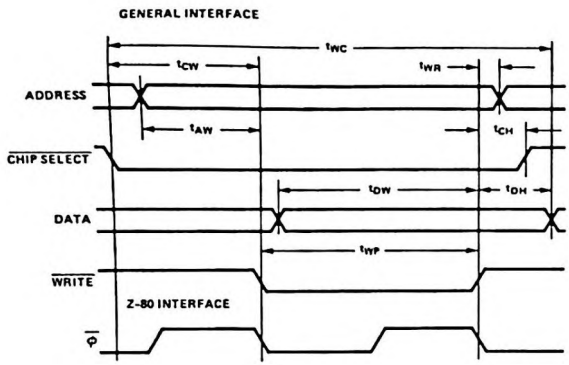


Figure 15. General Interfaces to the HDSP-6508 CODED DATA CONTROLLER



PARAMETER	SYMBOL	MIN.
WRITE CYCLE	t_{WC}	455ns
WRITE DELAY	t_{AW}	65ns
CHIP ENABLE TO WRITE	t_{CW}	65ns
DATA SETUP	t_{DW}	215ns
DATA HOLD	t_{DH}	50ns
WRITE PULSE	t_{WP}	340ns
WRITE RECOVERY	t_{WR}	40ns
CHIP ENABLE HOLD	t_{CH}	50ns

Figure 16. Data Entry Timing for the CODED DATA CONTROLLER Shown in Figure 15

blanked momentarily after each new character is read from the RAM. This is accomplished by breaking the total time allotted for each digit into four segments. During the first segment, the display is turned off to allow data to ripple through the AC5947 and during the next three segments, the display is turned on. The resulting display duty factor is (1/32) (3/4) or 1/42.6. The display is strobed at a 130 Hz refresh rate.

Data is entered into the RAM from the address and data bus of the microprocessor via two control lines Chip Select and Write. When Chip Select goes low, the address from the counter is tristated and the microprocessor address bus and data bus is gated to the RAM. Then after sufficient delay, the Write input is pulsed, which stores the data within the RAM. Data entry timing for the 18 segment CODED DATA CONTROLLER is shown in Figure 16. Since this timing is very similar to the DECODED DATA CONTROLLER shown in Figure 9, interface to the various microprocessor families is the same as described in the section on DECODED DATA CONTROLLERS.

DISPLAY PROCESSOR CONTROLLERS

The DISPLAY PROCESSOR CONTROLLER provides a powerful, smart interface which performs many of the functions normally found in a small terminal. The DISPLAY PROCESSOR CONTROLLER is designed around a slave microprocessor or custom LSI integrated circuit that provides display storage and multiplexing with a very minimum of circuit complexity. The simplest DISPLAY PROCESSOR CONTROLLER designed for a 16 digit 18 segment alphanumeric display is shown in Figure 17. This circuit is designed around the Intel 8279 Programmable Keyboard/Display Interface. This LSI chip contains the circuitry necessary to interface directly to a microprocessor bus and provides a 16 x 8 RAM, programmable scan counter, and keyboard debounce and control logic. While the 8279 is specifically designed for 7 segment displays, inclusion of the Texas Instruments AC5947 ASCII to 18 segment decoder/driver allows the use of an 18 segment alphanumeric display. The 8279 Keyboard/Display Controller interfaces to a microprocessor via an eight line bidirectional Data Bus, control lines $\overline{RD}$ (Read), $\overline{WR}$ (Write), $\overline{CS}$ (Chip Select), A_0 (Command/Data), RESET, IRQ (Interrupt Request), and a clock input, CLK. The display is scanned by outputs A_{0-3} and B_{0-3} which are connected to the inputs of the AC5947, and outputs SL_{0-3} which are connected to the digit scanning circuitry. The 74LS122 is used to provide interdigit blanking to prevent display ghosting. In addition to display scanning, the 8279 also has the ability to scan many different types of encoded or decoded keyboards, X-Y matrix keyboards, or provide a strobed data input to the microprocessor. The 8279 provides for either block data entry, where data enters from left to right across the display overflowing to the leftmost display location; right data entry, where data enters at the righthand side of the display and previous data shifts toward the left; and RAM data entry, where a four bit field in the control word specifies the address at which the next data word will be written. The 8279 allows data written into the display to be read by the microprocessor, and provides commands to either blank or clear the display.

The HDSP-8716/-8724/-8732/-8740 DISPLAY PROCESSOR CONTROLLER shown in Figure 18 is designed to provide a flexible 18 segment display interface for displays up to 40 characters in length. This circuit utilizes a dedicated Intel 8048 single chip microprocessor to provide features such as a blinking cursor, display editing routines, multiple data entry modes, variable display string length, and data out. This controller is available as a series of printed circuit board subsystems of 16, 24, 32, and 40 characters in length. The user interfaces to the 8048 microprocessor through eight Data In inputs, six Address inputs, a Chip Select input, Reset input, Blank input, six Data Out outputs, Data Valid output, Refresh output, and Clock output. The software within the 8048 microprocessor provides four data entry modes — Left Entry with a blinking cursor, Right Entry, Block Entry, and RAM Entry. The Data Out port allows the user to read the ASCII data stored within the display, determine the configured data entry mode and display length, and locate the position of the cursor within the display. Since the Data Out port is separate from the Data In port, the 18 segment DISPLAY PROCESSOR CONTROLLER can be used for text editing independent of the main microprocessor system. In Left Entry mode, the controller provides the Clear, Carriage Return, Backspace, Forwardspace, Insert, and Delete editing functions; while in Right Entry mode, the controller provides Clear and Backspace editing functions. The controller can also be expanded into multiple line panels.

The 8048 microprocessor interfaces to the display via the Port 2 output. The output is configured to enable the microprocessor to send a six bit word to one of three destinations as selected by P_{26} and P_{27}. The PROG output

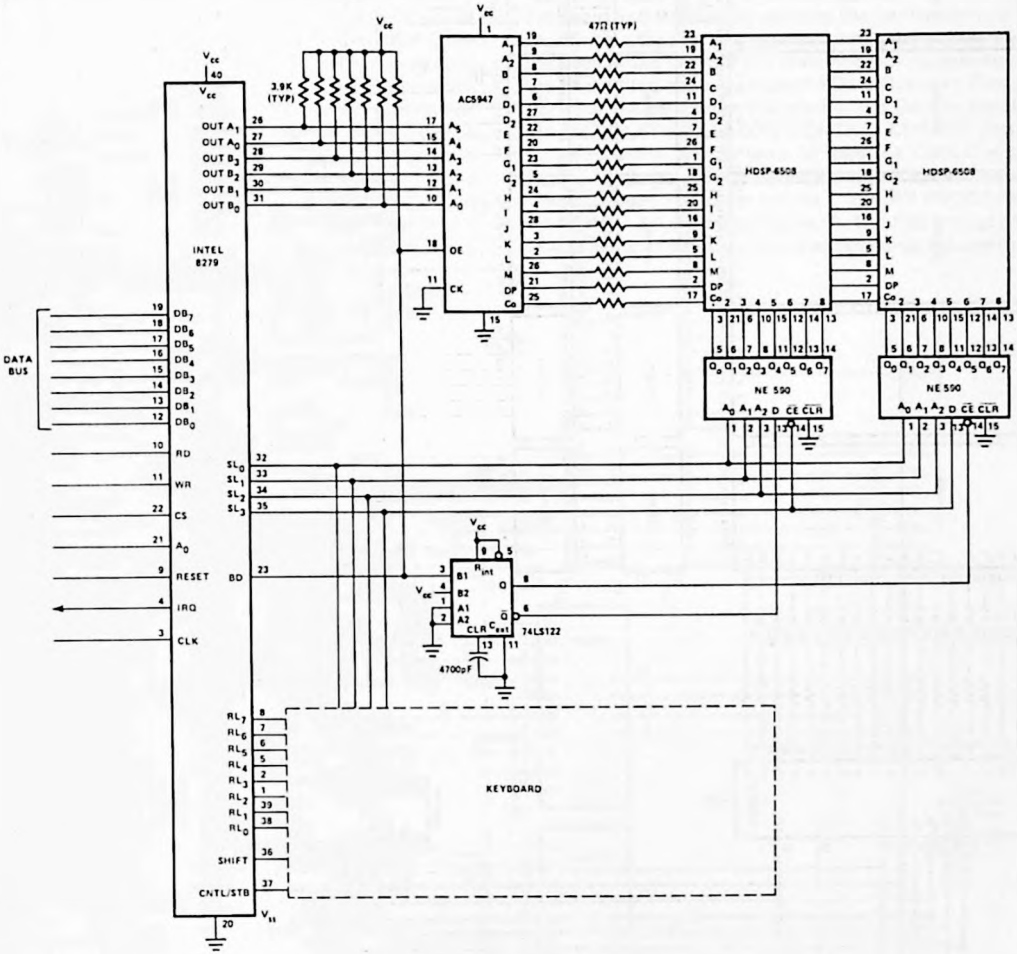


Figure 17. HDSP-6508 DISPLAY PROCESSOR CONTROLLER Utilizing the Intel 8279 Programmable Keyboard Display Interface

is then used to store this word at the specified destination. Destination$_0$ is the 74LS174 hex register. The outputs of this register are decoded by the 74LS259 addressable latches and Sprague ULN 2815 digit drivers. Output $3F_{16}$ is decoded to turn on the rightmost display digit while the address of the leftmost display digit varies from 18_{16} for a 40 character display to 30_{16} for a 16 character display. Destination$_1$ is the AC5947 18 segment decoder/driver. The positive edge of $\overline{\text{PROG}}$ stores a six bit ASCII code within the AC5947. Because destination$_1$ is pulsed once every time a digit is refreshed, this output is also used as the $\overline{\text{Refresh}}$ output. Destination$_2$ is the Data Valid output of the Data Out port. Thus, Data Out actually consists of a series of six bit words that are sent to Destination$_2$. Display refresh is accomplished by first turning off the digit drivers by outputting a 0_{16} to the 74LS174. Then a new ASCII character is stored within the AC5947. Finally, a new digit word is stored within the 74LS174. The actual time that each digit is on varies according to the configured display length so as to provide a fixed 100 Hz refresh rate.

Interfacing the DISPLAY PROCESSOR CONTROLLER shown in Figure 18 to microprocessor systems depends on the needs of the particular application. Since the information on the Data In and Address inputs is loaded into the controller through a program within the 8048 microprocessor, the time required to read these inputs varies from about 100 to 700 microseconds. A latch as shown in the HDSP-8716/-8724/-8732/-8740 Data Sheet can be used as a buffer between these inputs and the data bus and address bus of the main microprocessor system. The latch provides temporary storage to avoid making the main microprocessor wait for the DISPLAY PROCESSOR CONTROLLER to accept data.

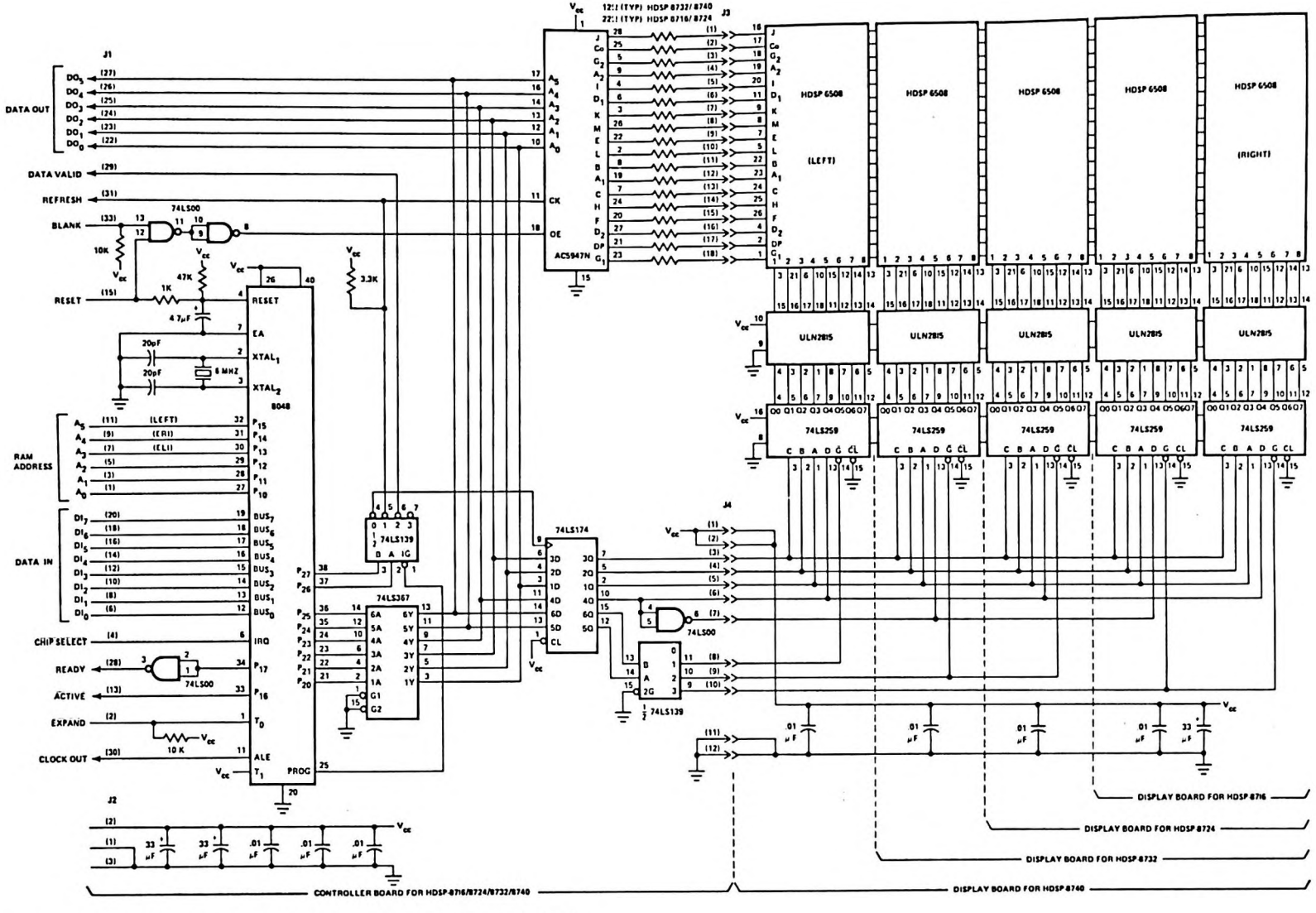


Figure 18. HDSP-8716/-8724/-8732/-8740 DISPLAY PROCESSOR CONTROLLER

The 18 segment DISPLAY PROCESSOR CONTROLLER shown in Figure 18 can also be interfaced to the main microprocessor system through a Peripheral Interface Adapter (PIA). The Data In inputs of the controller would be connected to an output port of the PIA. In RAM Entry mode, the Address inputs of the controller would be connected to another output port of the PIA. The PIA provides a handshake back to the main microprocessor system that tells when the DISPLAY PROCESSOR CONTROLLER is ready to accept another data input word from the main microprocessor. This allows the microprocessor to load data into the controller at the highest possible rate. A PIA can also be used to allow the 18 segment DISPLAY PROCESSOR CONTROLLER to act as a buffer between a keyboard and the main microprocessor. In this configuration, the main processor could output a prompting message to the user via the DISPLAY PROCESSOR CONTROLLER. The user could then enter data from the keyboard into the display utilizing the controller's editing capability. After the message has been entered and edited, the user would instruct the main microprocessor to read the final edited message from the Data Out port. One port from the PIA can be used to control the Data In inputs of the DISPLAY PROCESSOR CONTROLLER and another port of the PIA can be used to read the Data Out port. Figure 19 shows a 6800 microprocessor system using a Motorola 6821 PIA to control the DISPLAY PROCESSOR CONTROLLER shown in Figure 18. The PB_7 output of the PIA determines whether data is entered into the controller

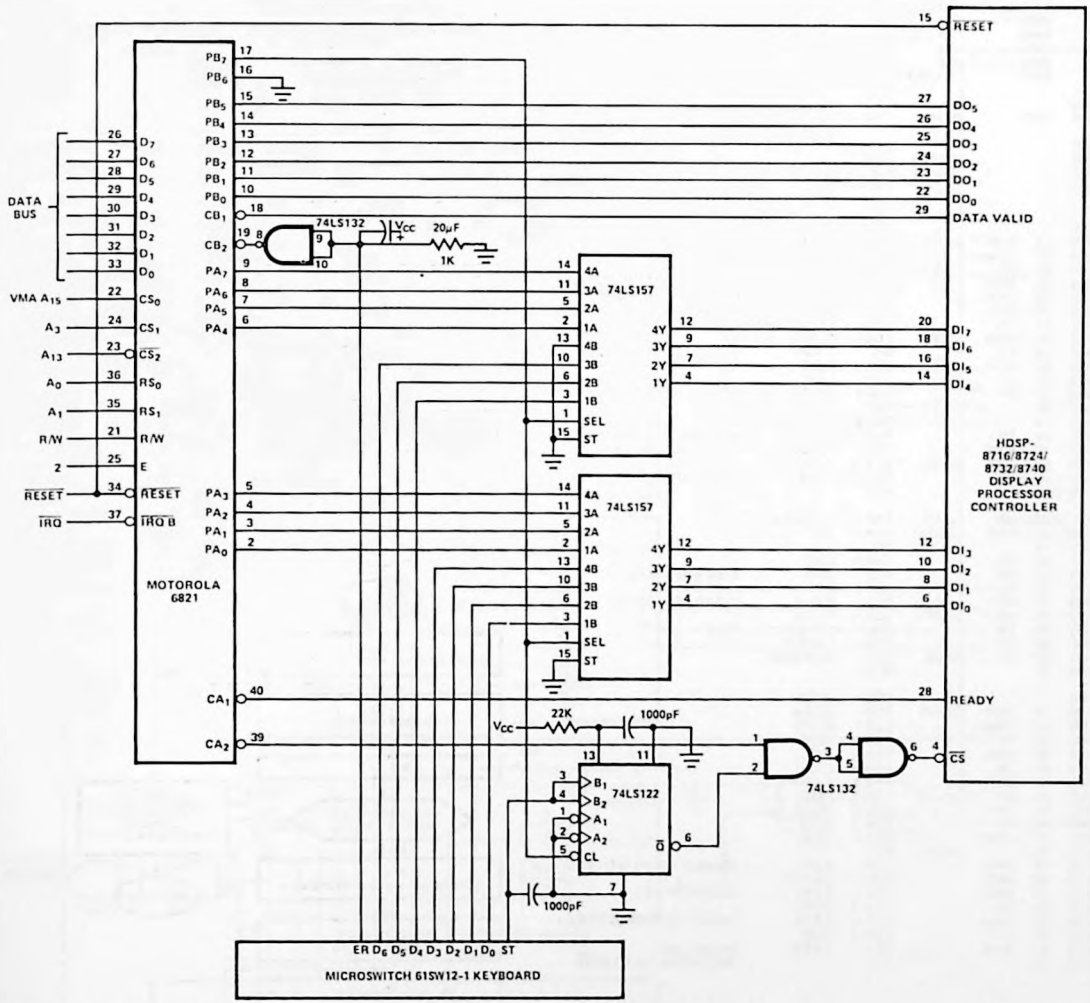


Figure 19. 6800 Microprocessor Interface to the DISPLAY PROCESSOR CONTROLLER Shown in Figure 18 Utilizing a Motorola 6821 PIA

APPLICATIONS

```
* PORT CONFIGURATION:
* 1. PORT A:
*        PA0-PA7 OUTPUTS TO DATA IN OF HDSP-87XX
*        CA1 (INPUT) MODE 00 SETS FLAG NEG EDGE OF READY
*        CA2 (OUTPUT) MODE 100 CLEARED MPU READ PRA, SET
*        NEGATIVE EDGE OF READY
* 2. PORT B:
*        PB0-PB5 INPUTS DATA TO 6800 FROM DATA OUT OF HDSP
*        CB1 (INPUT) MODE 10 SETS FLAG POS EDGE OF DATA VA
*        CB2 (INPUT) MODE 000 SETS FLAG NEG EDGE OF ER KEY
*        CB2 (INPUT) MODE 001 SETS FLAG NEG EDGE OF ER KEY
*        CAUSING IRQ
*        PB7 (OUTPUT) LOW ENABLES PA0-PA7 TO MUX
*                     HIGH ENABLES KEYBOARD TO MUX AND KEY

        8008        PRA     EQU     $8008
        8008        DRA     EQU     $8008
        8009        CRA     EQU     $8009
        800A        PRB     EQU     $800A
        800A        DRB     EQU     $800A
        800B        CRB     EQU     $800B
        0028        LENGTH  EQU     40          MUST BE SAME AS LENGTH

0000                        ORG     $0000
0000    0002        MESSGE  FDB     TEXT

0100                        ORG     $0100
0100                STATUS  RMB     1
0101                CURSOR  RMB     1
0102                DATA    RMB     40

0400                        ORG     $0400
0400    CE  0100    READ    LDX     I,STATUS
0403    7F  800A            CLR     E,PRB       ENABLE PORT A TO MUX
0406    86  FF              LDA A   I,$FF
0408    B7  8008            STA A   E,PRA       BEGIN DATA OUT SEQUENCE
040B    7D  8008            TST     E,PRA       CLEAR CA1 AND CA2
040E    7D  800A            TST     E,PRB       CLEAR CB1 AND CB2
0411    C6  2A              LDA B   I,LENGTH+2
0413    B6  800B    LOOP1   LDA A   E,CRB
0416    2A  FB              BPL     LOOP1       WAIT FOR DATA VALID
0418    B6  800A            LDA A   E,PRB
041B    84  3F              AND A   I,$3F
041D    A7  00              STA A   X,0         STORE IN RAM
041F    08                  INX
0420    5A                  DEC B
0421    26  F0              BNE     LOOP1       NEXT DATA OUT WORD
0423    7D  8008            TST     E,PRA       CLEAR CA1 AND CA2
0426    B6  8009    LOOP2   LDA A   E,CRA
0429    2A  FB              BPL     LOOP2       WAIT UNTIL READY
042B    39                  RTS

042C    DE  00      LOAD    LDX     D,MESSGE
042E    A6  00      LOOP10  LDA A   X,0
0430    08                  INX
0431    81  FF              CMP A   I,$FF
0433    27  0D              BEQ     ENDL        JUMP WHEN DONE
0435    B7  8008            STA A   E,PRA
0438    7D  8008            TST     E,PRA       CLEAR CA1 AND CA2
043B    B6  8009    LOOP11  LDA A   E,CRA
043E    2A  FB              BPL     LOOP11      WAIT
0440    20  EC              BRA     LOOP10
0442    DF  00      ENDL    STX     D,MESSGE
0444    39                  RTS

0500                        ORG     $0500
0500    7F  8009    START   CLR     E,CRA
0503    7F  800B            CLR     E,CRB
0506    86  FF              LDA A   I,$FF
0508    B7  8008            STA A   E,DRA
050B    86  24              LDA A   I,$24
050D    B7  8009            STA A   E,CRA
0510    86  80              LDA A   I,$80
0512    B7  800A            STA A   E,DRB
0515    86  06              LDA A   I,$06
0517    B7  800B            STA A   E,CRB
051A    0E          MAIN    CLI
051B    7F  800A            CLR     E,PRB       DISABLE KEYBOARD FROM MUX
051E    BD  042C            JSR     E,LOAD
0521    7D  800A            TST     E,PRB       CLEAR CB1, CB2
0524    86  80              LDA A   I,$80
0526    B7  800A            STA A   E,PRB       ENABLE KEYBOARD TO MUX
0529    86  0E              LDA A   I,$0E
052B    B7  800B            STA A   E,CRB       ENABLE IRG
052E    0F                  SEI                 IRQ CAUSES JSR TO READ
```

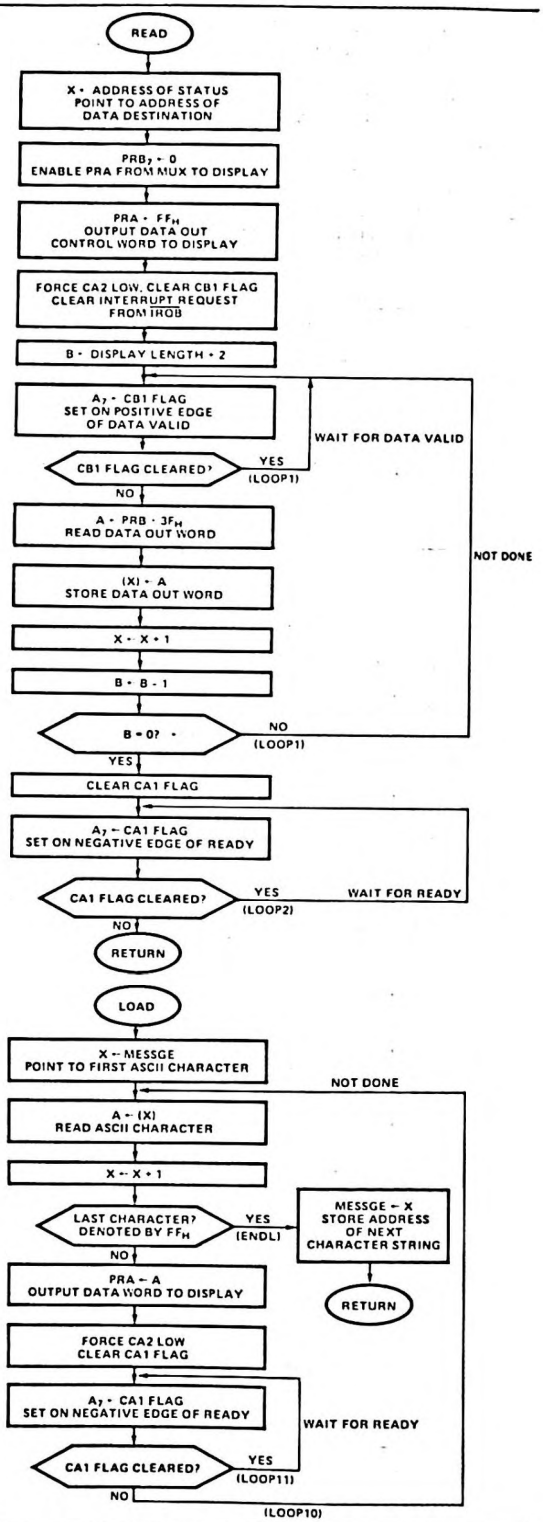


Figure 20. 6800 Microprocessor Program and Flowchart that Interfaces to the Circuit Shown in Figure 19

from the microprocessor system or from the keyboard. Control lines CA_1 and CA_2 are used to provide a data entry handshake to allow data to be loaded into the controller at the highest possible rate. Data is read into the main microprocessor system through Port B of the PIA using the CB_1 input as a data strobe.

The 6800 microprocessor program shown in Figure 20 is used to operate the PIA interface described in Figure 19. The microprocessor program following "START" is used to initialize the 6821 PIA. Once initialized, the PIA can be used either to load data into the controller via the main microprocessor, allow data to be loaded into the controller via the keyboard, or to read data from the Data Out port into the main microprocessor. The instruction CLR E, PRB at location $051B_{16}$ forces PB_7 low to connect the outputs of Port A to the Data In inputs of the controller. Subroutine "LOAD" then loads a series of eight bit words into the controller. "LOAD" continues to output words until it reads an FF_{16} to denote the end of the prompting message. The instruction sequence LDA A I, $80 and STA A E, PRB at location 0526_{16} forces PB_7 high to connect the output of the keyboard to the Data In inputs of the controller. In this mode, the user can enter or edit data into the DISPLAY PROCESSOR CONTROLLER. The 4B input of the 74LS157 has been grounded to prevent the keyboard from loading a control word into the DISPLAY PROCESSOR CONTROLLER. The instructions LDA A I, $0E and STA A E, CRB at location $052B_{16}$ enables the "ER" key on the keyboard to interrupt the microprocessor when the edited message is complete. Subroutine "READ" would then be used to read data into the 6800 system. First, subroutine "READ" outputs a special control word,

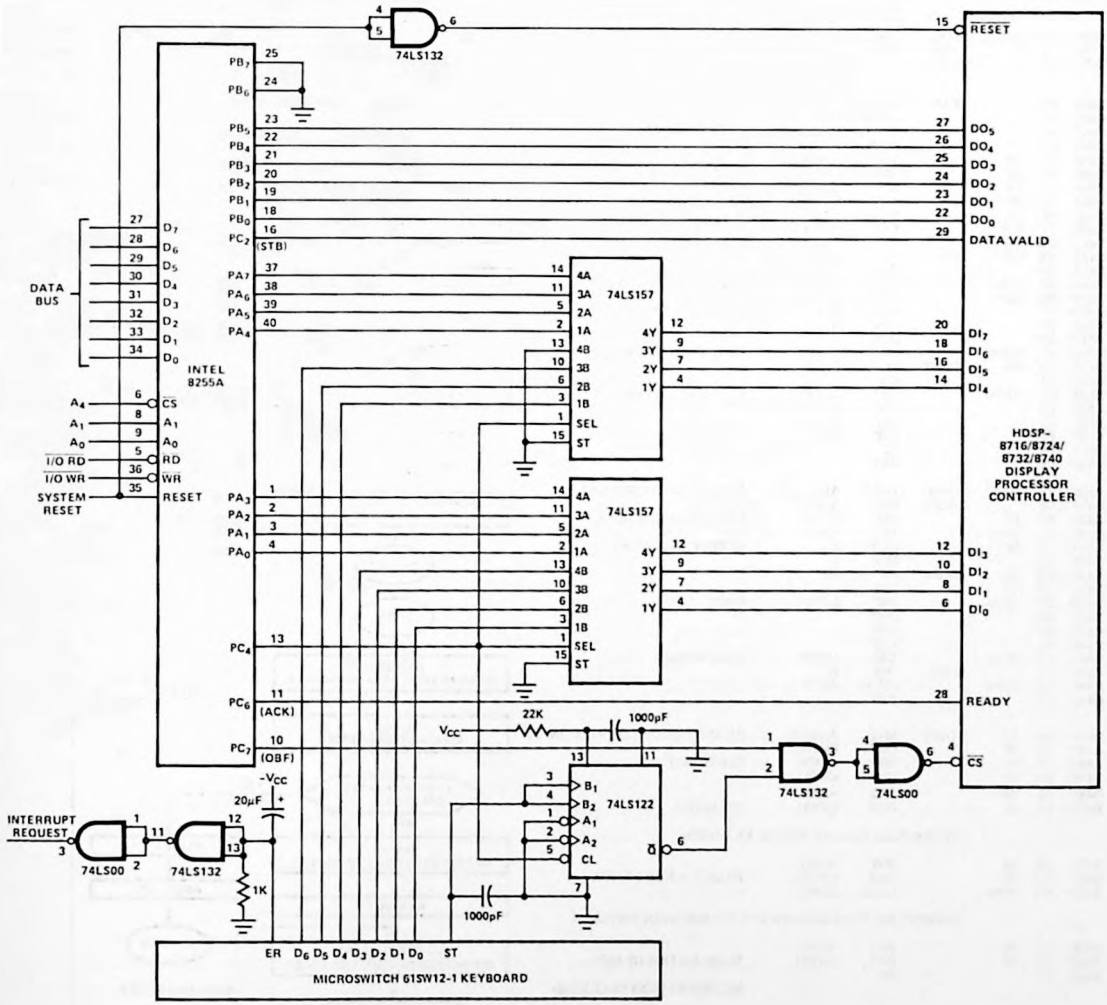


Figure 21. 8080A Microprocessor Interface to the DISPLAY PROCESSOR CONTROLLER Shown in Figure 18 Utilizing an Intel 8255 PIA

APPLICATIONS

```
;THIS PROGRAM IS WRITTEN IN 8080 ASSEMBLY LANGUAGE.
;THIS PROGRAM USES AN 8255 PIA TO ACCESS THE HDSP-87XX
;ALPHANUMERIC DISPLAY SYSTEM.
;
;PORT CONFIGURATION:
;1. PORT A (MODE 1 OUTPUT):
;       PA0-PA7 OUTPUTS TO DATA IN OF HDSP-87XX
;       PC7 (OBF) OUTPUT; TO CHIP SELECT
;       PC6 (ACK) INPUT; TO READY
;       FLAG PC7 (OBF) CLEARED BY OUTPUT; SET BY READY
;
;2. PORT B (MODE 1 INPUT):
;       PB0-PB6 INPUTS DATA FROM DATA OUT OF HDSP-87XX
;       PC2 (STB) INPUT; LOADS DATA ON POS EDGE OF DATA VALID
;       FLAG PC0 (INTR) CLEARED BY INPUT; SET BY DATA VALID
;
;3. PORT C:
;       PC4 OUTPUT; LOW ENABLES PA0-PA7 TO HDSP-87XX
;                   HIGH ENABLES KEYBOARD TO HDSP-87XX

000C              PA      EQU   0CH
000D              PB      EQU   0DH
000E              PC      EQU   0EH
000F              CNTRL   EQU   0FH
0028              LENTH   EQU   40          MUST BE DISPLAY LENGTH
                  ORG     0E000H
E000  02  E0      ASCII   DW    TEXT
E002  00          TEXT    DS    40
                  ;
                  ORG     0E100H
E100  00          STAT    DB    0
E101  00          ADDR    DB    0
E102  00          DATA    DB    0
                  ;
                  ORG     0E400H
E400  F3          READ    DI
E401  F5                  PUSH  PSW
E402  E5                  PUSH  H
E403  C5                  PUSH  B
E404  3E  08              MVI   A,08H
E406  D3  0F              OUT   CNTRL       ENABLE A SIDE OF MUX
E408  3E  FF              MVI   A,0FFH
E40A  D3  0C              OUT   PA          BEGIN DATA OUT SEQUENCE
E40C  0E  2A              MVI   C,LENTH+2
E40E  21  00E1            LXI   H,STAT      FIRST WORD
E411  DB  0D              IN    PB          CLEAR INTR
E413  DB  0E    LOOP1     IN    PC
E415  1F                  RAR
E416  D2  13E4            JNC   LOOP1       WAIT UNTIL INTR IS SET
E419  DB  0D              IN    PB
E41B  77                  MOV   M,A         STORE IN RAM
E41C  23                  INX   H
E41D  0D                  DCR   C
E41E  C2  13E4            JNZ   LOOP1       READ LENGTH+2 WORDS
E421  DB  0E    LOOP2     IN    PC
F423  17                  RAL
E424  D2  21E4            JNC   LOOP2       WAIT UNTIL READY
E427  C1                  POP   B
E428  E1                  POP   H
E429  F1                  POP   PSW
E42A  FB                  EI
E42B  C9                  RET
                  ;
E42C  2A  00E0    LOAD    LHLD  ASCII       FIRST WORD OF MESSAGE
E42F  7E    LOOP5 MOV     A,M
E430  FE  FF              CPI   0FFH        CHECK TO SEE IF DONE
E432  CA  44E4            JZ    ENDL
E435  D3  0C              OUT   PA          OUTPUT TO DISPLAY
E437  23                  INX   H
E438  DB  0E    LOOP6     IN    PC
E43A  17                  RAL
E43B  D2  38E4            JNC   LOOP6       WAIT
E43E  00                  NOP
E43F  00                  NOP
E440  00                  NOP
E441  C3  2FE4            JMP   LOOP5       NEXT WORD
E444  23    ENDL  INX     H
E445  22  00E0            SHLD  ASCII
E448  C9                  RET
                  ;
E449  3E  A7      START   MVI   A,0A7H       PA AS M1 OUTPUT, PB AS M1 INPUT
E44B  D3  0F              OUT   CNTRL
E44D  3E  0C              MVI   A,0CH       CLEAR INTE A
E44F  D3  0F              OUT   CNTRL
E451  3E  05              MVI   A,05H
E453  D3  0F              OUT   CNTRL       SET INTE B
                  ;
                  ;PROCEDURE TO LOAD HDSP-87XX SYSTEM
                  ;
E455  3E  08              MVI   A,08H
E457  D3  0F              OUT   CNTRL       ENABLE A SIDE OF MUX
E459  CD  2CE4            CALL  LOAD
                  ;
                  ;PROCEDURE TO READ DATA OUT OF HDSP-87XX SYSTEM
                  ;
E45C  3E  09              MVI   A,09H
E45E  D3  0F              OUT   CNTRL       ENABLE B SIDE OF MUX
E460  FB                  EI
                  ;                         INTERRUPT MUST CALL READ
```

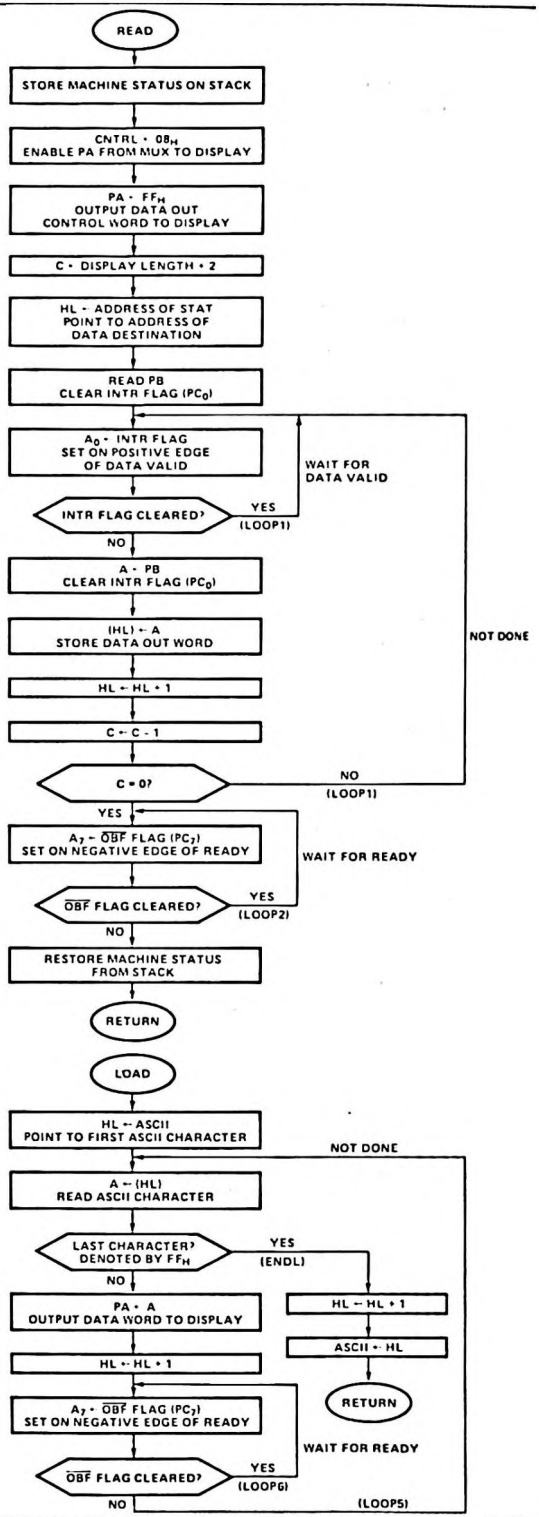


Figure 22. 8080A Microprocessor Program and Flowchart that Interfaces to the Circuit Shown in Figure 21

FF_{16}, to the Data In inputs of the DISPLAY PROCESSOR CONTROLLER. This control word causes the controller to begin its data output sequence. The controller outputs a series of data output words that define the configured entry mode and display length, location of the cursor, and the ASCII text stored within the DISPLAY PROCESSOR CONTROLLER. "LOOP 1" within the program continuously reads the Data Valid output and waits until the controller outputs the STATUS word. This STATUS word, the subsequent CURSOR ADDRESS word, and the string of ASCII characters are then stored in consecutive words of scratch pad memory starting at address "STATUS."

A similar PIA interface designed for an 8080A microprocessor system that uses an Intel 8255A PIA is shown in Figure 21. This interface operates in much the same way as the 6821 PIA interface that was previously described. The PC_4 output of the PIA determines whether the Data In inputs of the 18 segment DISPLAY PROCESSOR CONTROLLER shown in Figure 18 are connected to the PIA or to the keyboard. Control lines PC_6 and PC_7 are used to provide a data entry handshake between the 8080A microprocessor and the DISPLAY PROCESSOR CONTROLLER. Data is read into the 8080A microprocessor system through Port B of the PIA using PC_2 as the data strobe.

The 8080A microprocessor program shown in Figure 22 is used to operate the PIA interface described in Figure 21. The microprocessor program following "START" is used to initialize the 8255A PIA. The instructions MVI A, 08H and OUT CNTRL at location $E457_{16}$ force PC_4 low to connect Port A of the PIA to the Data In inputs of the DISPLAY PROCESSOR CONTROLLER. Subroutine "LOAD" would then be used to load a prompting message into the controller. The instructions MVI A, 09H and OUT CNTRL at location $E45E_{16}$ connect the keyboard to the Data In inputs of the controller. In this mode, the user can enter data into the DISPLAY PROCESSOR CONTROLLER, or to edit an existing line. Subroutine "READ" would then be used to read the data from the Data Out port into the 8080A microprocessor system.

Subroutine "READ" begins the data output sequence by outputting the special control word FF_H to the Data In inputs of the DISPLAY PROCESSOR CONTROLLER. Then, the subroutine reads the series of data output words that are outputted by the controller and stores them in consecutive words of scratch pad memory starting at address STAT.

HEWLETT PACKARD

APPLICATION NOTE 1004

Threshold Sensing For Industrial Control Systems With the HCPL-3700 Interface Optocoupler

INTRODUCTION

The use of electronic logic circuitry in most applications outside of a controlled environment very quickly brings the design engineer into contact with the problems and hazards involved in interfacing between the logic function and the controlled function. These problems have always been particularly evident in the field of industrial control where the electrically "noisy" environment produced by motors, power lines, lightning and other sources of interference may mask the desired signal, and in some cases even result in the destruction of the logic control system itself. In these situations, the designer must resort to solutions which will provide isolation between the logic system and the input or output function Traditional methods of isolation involve the use of such devices as capacitors, relays, tranformers, and optocouplers. Of these methods, the optocoupler provides an ideal combination of speed, dc response, high common mode rejection, and low input to output coupling capacitance.

In the implementation of an interface from an electrically noisy environment into logic systems, it is often desirable, if not mandatory, to establish some current or voltage switching point or threshold at which the input signal is considered true. Since the input, or feedback, signal in industrial control systems may be ac or dc and may range from low, 5 volt, levels to 110 or 240 volts ac, the design of such a threshold switching system can become more than a trivial problem. This is especially true when using the optocoupler, considering the relatively large range of current transfer ratio (CTR) found in most devices.

The problem of establishing an input switching threshold is resolved in the design of the Hewlett-Packard HCPL-3700 optocoupler. This device combines an ac or dc voltage and/or current detection function with a high insulation voltage optocoupler in a single eight pin plastic dual in-line package.

As shown in the block diagram of Figure 1, this device consists of a full-wave bridge rectifier and threshold detection integrated circuit, an LED, and an optically coupled detector integrated circuit. The detector circuit is a combination of a photodiode and a high current gain, split Darlington, amplifier.

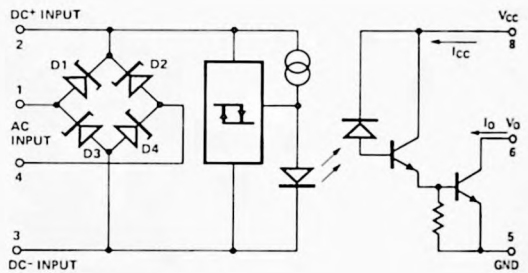


Figure 1. Block Diagram of the HCPL-3700

The input circuit will operate from an ac or dc source and provide a guaranteed, temperature compensated threshold level with hysteresis. The device may be programmed for higher switching thresholds through the use of a single external resistor.

With threshold level detection provided prior to the optical isolation path and subsequent gain stage, variations in the current transfer ratio of the device with time or from unit to unit are no longer important.

In addition to allowing ac or dc input signals, the Zener diodes of the bridge circuit also provide input voltage clamping to protect the threshold circuitry and LED from over voltage/current stress conditions. The LED current is provided by a switched current source.

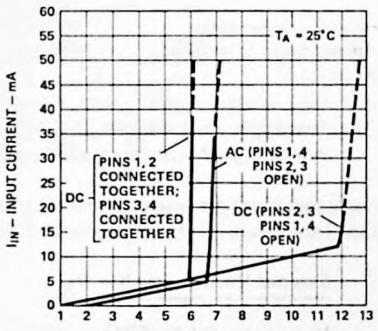
The HCPL-3700 optocoupler output is an open collector, high gain, split Darlington configuration. The output is compatible with TTL and CMOS logic levels. High common mode rejection, or transient immunity of 600V/μs, allows excellent isolation. Insulation capability is 3000 volts dc. The recommended operating temperature range is 0°C to 70°C.

The HCPL-3700 meets the requirements of the industrial control environment for interfacing signals from ac or dc power equipment to logic control electronics. Isolated monitoring of relay contact closure or relay coil voltages, monitoring of limit or proximity switch operation or sensor signals for temperature or pressure, etc., can be accomplished by the HCPL-3700. The HCPL-3700 may also be used for sensing low power line voltage (Brown Out) or loss of line power (Black Out).

Device Characteristics

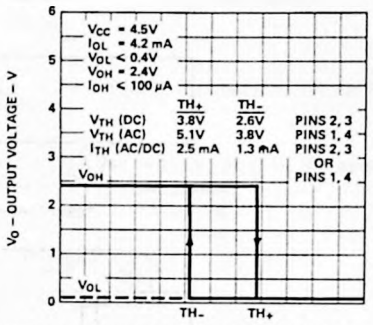
The function of the HCPL-3700 can best be understood through a review of the input V/I function and the input to output transfer function. Figure 2 shows the input characteristics, I_{IN} (mA) versus V_{IN} (volts), for both the ac and dc cases.

The dc input of the HCPL-3700 appears as a 1000Ω resistor in series with a one volt offset. If the ac pins (1, 4) are left unconnected, the dc input voltage can increase to 12V (two Zener diode voltages) before the onset of input voltage clamping occurs. If the ac pins (1, 4) are connected to ground or to dc pins (2, 3) respectively, the dc input voltage will clamp at 6.0V (one Zener diode voltage). Under clamping conditions, it is important that the maximum input current limits not be exceeded. Also, to prevent excessive current flow in a substrate diode, the dc input can not be backbiased more than −0.5V. The choice of the input voltage clamp level is determined by the requirements of the system design. The advantages of clamping the input at a low voltage level is in limiting the magnitude of forward current to the LED as well as limiting the input power



NOTE: AC VOLTAGE VALUES REPRESENT INSTANTANEOUS PEAK.

Figure 2. Typical Input Characteristics, I_{IN} vs. V_{IN}



NOTE: AC VOLTAGE VALUES REPRESENT INSTANTANEOUS PEAK.

Figure 3. Typical Transfer Characteristics of the HCPL-3700

to the device during large voltage or current transients in the industrial control environment. The internal limiting will in some cases eliminate the need for additional protection components.

The ac input appears similar to the dc input except that the circuit has two additional diode forward voltages. The ac input voltage will clamp at 6.7V (one Zener diode voltage plus one forward biased diode voltage), and is symmetric for plus or minus polarity. The ac voltage clamp level can not be changed with different possible dc pin connections.

The transfer characteristic displayed in Figure 3 shows how the output voltage varies with input voltage, or current, levels. Hysteresis is provided to enhance noise immunity, as well as to maintain a fast transition response (t_r, t_f) for slowly changing input signals.

The hysteresis of the device is given in voltage terms as $V_{HYS} = V_{TH+} - V_{TH-}$, or in terms of current as $I_{HYS} = I_{TH+} - I_{TH-}$. The optocoupler output is in the high state until the input voltage (current) exceeds $V_{TH+}(I_{TH+})$. The output state will return high when the input voltage (current) becomes less than $V_{TH-}(I_{TH-})$.

As is shown in Figure 3, the HCPL-3700 has preprogrammed ac and dc switching threshold levels. Higher input switching thresholds may be programmed through the use of a single series input resistance as defined in Equation (1). In some cases, it may be desirable to split this resistance in half to achieve transient protection on each input lead and reduce the power dissipation requirement of each of the resistors.

Figure 4 illustrates three typical interface situations which a designer may encounter in utilizing a microprocessor as a controller in industrial environments.

Example 1. A dc voltage applied to the motor is monitored as an indication of proper speed and/or load condition.

APPLICATIONS

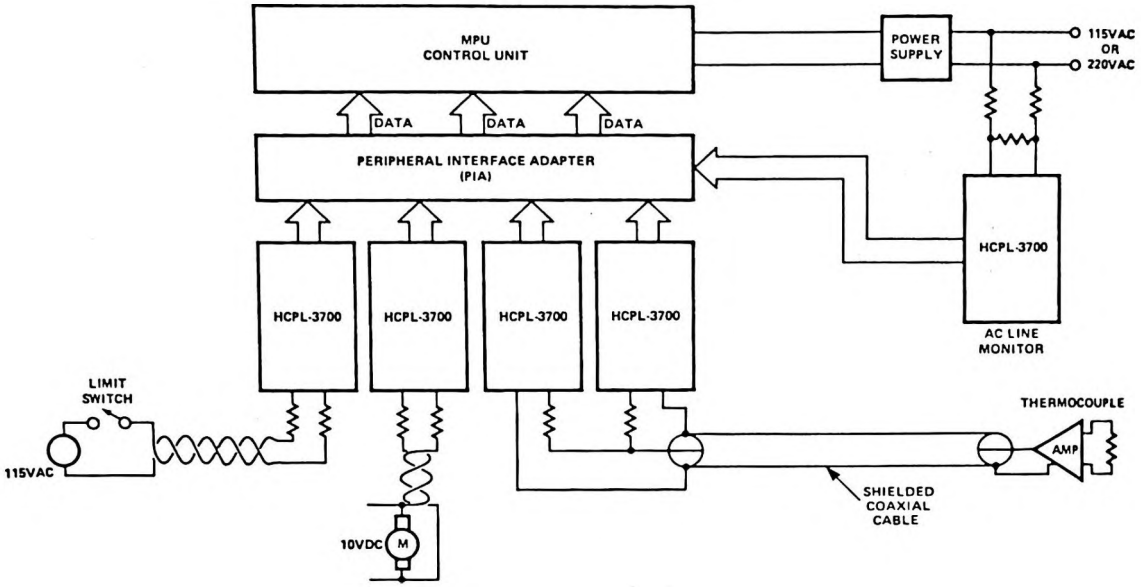


Figure 4. Applications of the HCPL-3700 for Interfacing AC and DC Voltages to a Microprocessor

Example 2. A limit switch uses a 115V ac or 220V ac control loop to improve noise immunity and because it is a convenient high voltage for that purpose.

Example 3. An HCPL-3700 is used to monitor a computer power line to sense a loss of line power condition. Use of a resistive shunt for improvement of threshold accuracy is analyzed in this example.

Also illustrated is an application in which two HCPL-3700's are used to monitor a window of safe operating temperatures for some process parameters. This example also requires a rather precise control of the optocoupler switching threshold. An additional dedicated leased line system example is also shown (Example 4).

Example 1. DC Voltage Sensing

The dc motor monitor function is established to provide an indication that the motor is operating at a minimum desired speed prior to the initiation of another process phase. If the applied voltage, V_M, is greater than 5V, it is assumed that the desired speed is obtained. The maximum applied voltage in the system is 10V. The HCPL-3700 circuit configuration for this dc application is shown in Figure 5.

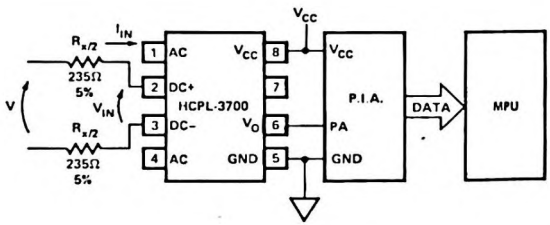


Figure 5. Interfacing a DC Voltage to an MPU using the HCPL-3700

NOTE: See Appendix for a definition of terms and symbols for this and all other examples.

The following conditions are given for the external voltage threshold level and input requirements of the HCPL-3700:

External Voltage Levels — V_M

V_+ = 5V dc (50%)

V_{peak} = 10V dc

HCPL-3700 Input Levels

$V_{TH+} = 3.8V$

$V_{TH-} = 2.6V$

$V_{ICH3} = 12V$

$I_{TH+} = 2.5mA$

$I_{TH-} = 1.3mA$

For the 5V threshold, R_x is calculated via the expression:

$$R_x = \frac{V_+ - V_{TH+}}{I_{TH+}} \quad (1)$$

$$= \frac{5V - 3.8V}{2.5mA}$$

$R_x = 480\Omega \quad (470\Omega \pm 5\%)$

The resultant lower threshold level is formed by using the following expression:

$$V_- = I_{TH-} R_x + V_{TH-} \quad (2)$$

$$= (1.3mA)\ 470\Omega + 2.60V$$

$V_- = 3.21V$

With the possible unit to unit variations in the input threshold levels as well as ±5% tolerance variations with R_x, the variation of V_+ is +12.4%, −15% and V_- varies +14%, −23.5%. (NOTE: With a low, external, voltage threshold level, V_+, which is comparable in magnitude to the V_{TH+} voltage threshold level of the optocoupler ($V_+ \leq 10V_{TH+}$) the tolerance variations are not significantly improved by the use of a 1% precision resistor for R_x. However, at a large external voltage threshold level compared to V_{TH+} ($V_+ > 10V_{TH+}$), the use of a precision 1% resistor for R_x does reduce the variation of V_+.)

For simultaneous selection of external upper, V_+, and lower, V_-, voltage threshold points a combination of a series and parallel input resistors can be used. Refer to the example on "ac operation with improved threshold control and accuracy" for detailed information.

Calculation of the maximum power dissipation in R_x is determined by knowing which of the following inequalities is true:

$$\frac{V_+}{V_{peak}} > \frac{V_{TH+}}{V_{IHC}} \quad (V_{IN} \text{ will not clamp}) \quad (3)$$

$$\frac{V_+}{V_{peak}} < \frac{V_{TH+}}{V_{IHC}} \quad (V_{IN} \text{ will clamp}) \quad (4)$$

where V_{IHC} is the particular input clamp voltage listed on the data sheet.

For this dc application with ac pins (1, 4) open, input voltage clamping will not occur, i.e.,

$$\frac{V_+}{V_{peak}} > \frac{V_{TH+}}{V_{IHC3}}$$

$$\frac{5V}{10V} > \frac{3.8V}{12.0V}$$

Consequently, a conservative value for the maximum power dissipation in R_x for the unclamped input voltage condition ignoring the input offset voltage is given by:

$$P_{R_x} = \frac{\left[V_{peak}\left(\frac{R_x}{R_x + 1\ k\Omega}\right)\right]^2}{R_x} \quad \text{(Unclamped Input)} \quad (5)$$

$$= \frac{\left[10V\left(\frac{470\Omega}{1470\Omega}\right)\right]^2}{470\Omega}$$

$P_{R_x} = 21.8mW$

If $V_+/V_{peak} < V_{TH+}/V_{IHC}$ was true (clamped input voltage condition), then the formula for the maximum power dissipation in R_x becomes:

$$P_{R_x} = \frac{(V_{peak} - V_{IHC})^2}{R_x} \quad \text{(Clamped Input)} \quad (6)$$

The maximum input current or power must be determined to ensure that it is within the maximum input rating of the HCPL-3700. For the clamped input voltage condition,

$$I_{IN} = \frac{V_{peak} - V_{IHC}}{R_x} < I_{IN\ (max)} \quad (7)$$

or

$$P_{IN} = V_{IHC}\ (I_{IN}) < P_{IN\ (max)} \quad (8)$$

Clamped Condition

APPLICATIONS

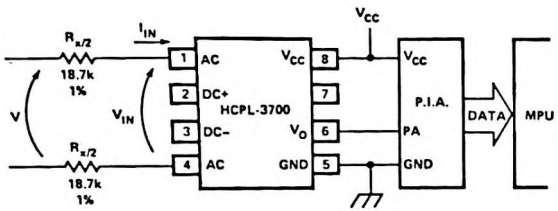


Figure 6. Interfacing an AC Voltage to an MPU using the HCPL-3700

For the unclamped input voltage condition, the maximum input current, or power will not be exceeded, because maximum input current and power will occur only under clamp conditions.

An output load resistance is not needed in this application because the peripheral interface adapter, such as MC6821, has an internal pullup resistor connected to its input.

Example 2. AC Operation

As shown in Figure 6, an ac application is that of a monitored 115V ac limit switch. Ac sensing is commonly used and the HCPL-3700 conveniently provides an internal rectification circuit. With the HCPL-3700 interfacing to the P.I.A., a choice can be made not to filter the ac signal or to filter the ac signal at the input or output of the device. All three conditions will be explored. Simplicity is obtained with no filtering at all, but software detection techniques must be used. Output filtering is a standard method, but may present problems with slow RC rise time of the output waveform when TTL logic is used. Input filtering avoids the RC rise time problem of output filtering, but introduces an extra time delay at the input.

AC Operation With No Filtering

In this example, a V_+ value of 98V is selected based on a criteria of 60% of V_{peak}. Monitoring a limit switch for a 60% level of the signal will give sufficient noise immunity from an open 115V ac line while allowing the HCPL-3700 to turn on under low line voltage conditions of −15% from nominal values when the limit switch is closed.

The value of R_x for the upper threshold detection level without the filter capacitor, C, across the dc input, can be obtained from the following expression.

$$R_x = \frac{V_+ - V_{TH+}}{I_{TH+}} \qquad (9)$$

V_{TH+} = 5.1V (ac instantaneous)

I_{TH+} = 2.5mA

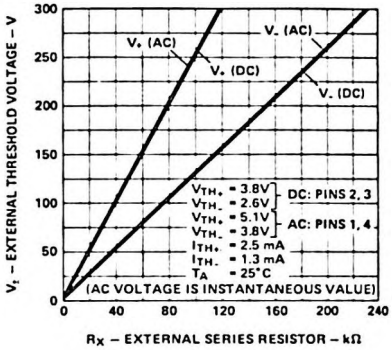


Figure 7. Typical External Threshold Characteristic, $V_\pm$ – vs. R_X

$$R_x = \frac{98V - 5.1V}{2.5mA}$$

R_x = 37.2kΩ (use $R_x/2$ = 18.7kΩ, 1% resistor for each input lead)

The resulting lower threshold point is

$$V_- = I_{TH-}R_x + V_{TH-} \qquad (10)$$

$$= (1.3mA)(37.4k\Omega) + 3.8V$$

V_- = 52.4V (32% of peak input voltage)

Figure 7 provides a convenient, graphical choice for the external series resistor, R_x, and a particular external threshold voltage $V_\pm$.

The corresponding R_x value and output waveform of the HCPL-3700 for a V_+ = 98V (60% of peak) is shown in Figure 8.

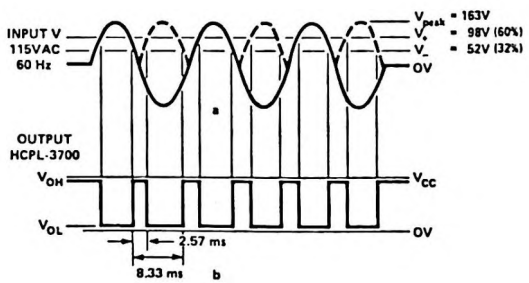


Figure 8. Output Waveforms of the HCPL-3700 Design in Figure 7 with no Filtering Applied

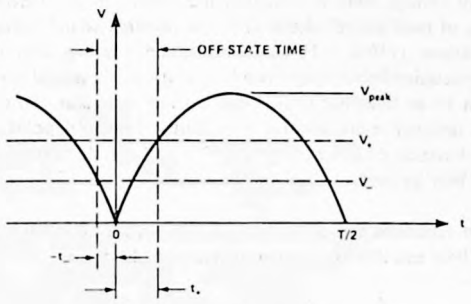


Figure 9. Determination of Off/On State Time

To determine the time in the high state, refer to Figure 9 and Equation (11).

Due to symmetry of sinusoidal waveform, the high state time is $t_- + t_+$ where $t_\pm$ is given by:

$$t_\pm = \frac{T}{360^\circ} \sin^{-1}\left(\frac{V_\pm}{V_{peak}}\right) \qquad (11)$$

where arc sine is in degrees and T = period of sinusoidal waveform.

In the unfiltered condition, the output waveform of Figure 8 must be used as sensed information. Software can be created in which the microprocessor will examine the waveform from the optocoupler at specific intervals to determine if ac is present or absent at the input to the HCPL-3700. This technique eliminates the problem of filtering, and accompanying delays, but requires more sohpisticated software implementation in the microprocessor.

Input Filtering for AC Operation

A convenient method by which to achieve a continuous output low state in the presence of the applied ac signal is to filter the input dc terminals (pins 2–3) with a capacitance C while the ac signal is applied to the ac input (pins 1–4) of the full wave rectifier bridge. Input filtering allows flexibility in using the HCPL-3700 output for direct interfacing with TTL or CMOS devices without the slow rise time which would be encountered with output filtering. In addition, the input filter capacitor provides extra transient and contact bounce filtering. Because filtering is done after R_x, the capacitor working voltage is limited by the V_{IHC2} clamp voltage rating which is 6.7V peak for ac operation. The disadvantage of input filtering is that this technique introduces time delays at turn on and turn off of the optocoupler due to initial charge/discharge of the input filter capacitor.

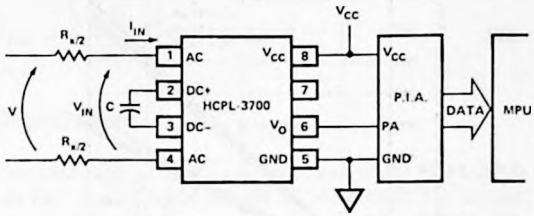


Figure 10. Input Filtering with the HCPL-3700

The application of ac input filtering is illustrated in Figure 10 and is described in the following example. The ac input conditions are the same as in the previous example of the 115V ac limit switch.

The minimum value of capacitance C to ensure proper ac filtering is determined by the parameters of the optocoupler. At low ac input voltage, the capacitor must charge to at least V_{TH+} in order to turn on, but must not discharge to V_{TH-} during the discharge cycle. A conservative estimate for the minimum value of C is given by the following equations.

$$V_{TH+} - V_{TH-} = V_{TH+}e^{-t/\tau},\ \tau = R_{IN}C_{min} \qquad (12)$$

where R_{IN} is the equivalent input resistance of the HCPL-3700.

$$C_{min} = \frac{t}{R_{IN} \ln\left(\frac{V_{TH+}}{V_{TH+} - V_{TH-}}\right)} \qquad (13)$$

with R_{IN} = 1kΩ, V_{TH+} = 3.8V, V_{TH-} = 2.6V and t = 8.33ms for 60 Hz or t = 10ms for 50 Hz.

C_{min} = 7.23μF for 60 Hz

C_{min} = 8.68μF for 50 Hz

To ensure proper filtering, the recommended value of C should be large enough such that with the tolerance variation, C will always be greater than C_{min} (C should otherwise be kept as small as possible to minimize the inherent delay times which are encountered with this technique). Since the filter capacitor affects the input impedance, a slightly different value of R_x is required for the input filtered condition. Figure 11 shows the R_x versus $V_\pm$ threshold voltage for C = 10μF, 22μF, and 47μF. For an application of monitoring a 115V RMS line for 65% of nominal voltage condition (75V RMS), an R_x = 26.7kΩ ± 1% with C = 10μF will yield the desired threshold. The power dissipation for R_x is determined from the clamped

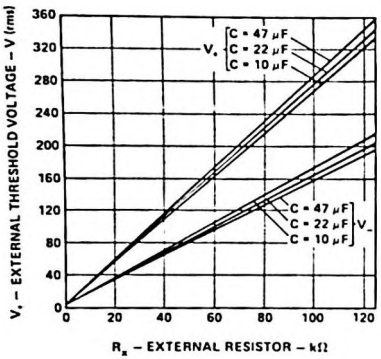


Figure 11. External Threshold Voltage versus R_X for Applications Using an Input Filter Capacitor C (Figure 10)

condition ($V_+/V_{peak} < V_{TH+}/V_{ICH2}$) and is 455mW (see Figure 6) which suggests $R_x/2$ of 1/2 watt resistors for each input lead.

Example 3. AC Operation with Improved Threshold Control and Accuracy

Some applications may occur which require threshold level detection at specific upper and lower threshold points. The ability to independently set the upper and lower threshold levels will provide the designer with more flexibility to meet special design criteria. As illustrated in Figure 12, a computer power line is monitored for a power failure condition in order to prevent loss of memory information during power line failure.

In this design, the HCPL-3700 optocoupler monitors the computer power line and the output of the optocoupler is interfaced to a TTL Schmitt trigger gate (7414).

In the earlier ac application of the HCPL-3700 (limit switch example), a single external series resistor, R_X, was used to determine one of the threshold levels. The other threshold level was determined by the hysteresis of the device, and not the designer. A potential problem of single threshold

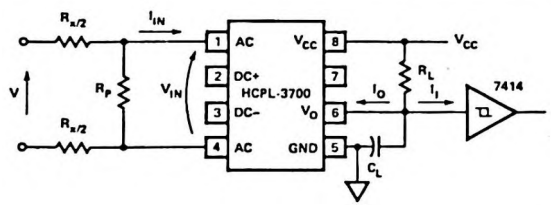


Figure 12. An AC Power Line Monitor with Simultaneous Selection of Upper and Lower Threshold Levels and Output Filtering

selection with 115V line application would be to determine R_x for a lower threshold level of 50% of nominal peak input voltage, only to find that the upper threshold level is 90% of peak input voltage. With the possible ac line voltage variations (+10%, −15%), it would be possible that the optocoupler could never reach the upper threshold point with an ac line that is at −15% of nominal value. To give the designer more control over both threshold points, a combination of series resistance, R_x, and parallel resistance, R_P, may be used, as shown in Figure 12.

Two equations can be written for the two external threshold level conditions. At the upper threshold point,

$$V_+ = R_X\left(I_{TH+} + \frac{V_{TH+}}{R_P}\right) + V_{TH+} \quad (14)$$

and at the lower threshold point,

$$V_- = R_X\left(I_{TH-} + \frac{V_{TH-}}{R_P}\right) + V_{TH-} \quad (15)$$

Solving these equations for R_x and R_P yield the following expressions:

$$R_X = \frac{V_{TH-}(V_+) - V_{TH+}(V_-)}{I_{TH+}(V_{TH-}) - I_{TH-}(V_{TH+})} \quad (16)$$

(16)

$$R_P = \frac{V_{TH-}(V_+) - V_{TH+}(V_-)}{I_{TH+}(V_- - V_{TH-}) + I_{TH-}(V_{TH+} - V_+)} \quad (17)$$

Equations (16) and (17) are valid only if the conditions of Equations (18) or (19) are met. The desired external voltage threshold levels, V_+ and V_-, are established and the values for $V_{TH\pm}$ and $I_{TH\pm}$ are found from the data sheet. With the $V_{TH\pm}$, $I_{TH\pm}$ values, the denominator of R_x, Equation (16) is checked to see of it is positive or negative. If it is positive, then the following ratios must be met:

$$\frac{V_+}{V_-} \geqslant \frac{V_{TH+}}{V_{TH-}} \text{ and } \frac{V_+ - V_{TH+}}{V_- - V_{TH-}} < \frac{I_{TH+}}{I_{TH-}} \quad (18)$$

Conversely, if the denominator of R_x Equation (16) is negative, then the following ratios must hold:

$$\frac{V_+}{V_-} \leqslant \frac{V_{TH+}}{V_{TH-}} \text{ and } \frac{V_+ - V_{TH+}}{V_- - V_{TH-}} > \frac{I_{TH+}}{I_{TH-}} \quad (19)$$

Consider that the computer power line is monitored for a 50% line drop condition and a 75% line presence condition. The 115V 60 Hz ac line (163V peak) can vary from 85% (139V) to 110% (179V) of nominal value.

Require:

V_- = 81.5V (50%) – Turn off threshold

V_+ = 122.5V (75%) – Turn on threshold

Given:

V_{TH+} = 5.1V I_{TH+} = 2.5mA V_{IHC2} = 6.7V

V_{TH-} = 3.8V I_{TH-} = 1.3mA

Using the Equations (16, 17) for R_x, R_P with the conditions of Equations (18, 19) being met yields

R_x = 17.4 kΩ use 18 kΩ 5%

R_P = 1.2 kΩ use 1.2 kΩ 5%

To complete the input calculations for maximum input current, I_{IN}, to the device and maximum power dissipation in R_x and R_P, a check must be made to determine if the input voltage will clamp at peak applied voltage. Using Equations (3) and (4) to determine if a clamp or no clamp exists, it is found that the ratios

$$0.75 = \frac{V_+}{V_{peak}} \approx \frac{V_{TH+}}{V_{IHC2}} = 0.76$$

indicate that V_{IN} slightly entered clamp condition. In this application, the operating input current, I_{IN}, is given approximately by

$$I_{IN} = \frac{V - \frac{V_{IHC2}}{\sqrt{2}}}{R_x} - \frac{\frac{V_{IHC2}}{\sqrt{2}}}{R_P} < I_{IN\,(max)} \qquad (20)$$

$$= \frac{115V - \frac{6.7V}{\sqrt{2}}}{18\,k\Omega} - \frac{\frac{6.7V}{\sqrt{2}}}{1.2\,k\Omega}$$

I_{IN} = 2.18mA RMS < 34.3mA

Power dissipation in R_x is determined from the following equation,

$$P_{R_X} = \frac{\left(V - \frac{V_{IHC2}}{\sqrt{2}}\right)^2}{R_x} \qquad (21)$$

which yields 0.675W. With the clamp condition existing, the maximum power dissipation for R_P is 18.7mW which is determined from

$$P_{RP} = \frac{\left(\frac{V_{IHC2}}{\sqrt{2}}\right)^2}{R_P} \qquad (22)$$

Output Filtering

The advantages of filtering at the output of the HCPL-3700 are that it is a simple method to implement. The output waveform introduces only one additional delay time at turn off condition as opposed to the input filtering method which introduces additional delay times at both the turn on and turn off conditions due to initial charge or discharge of the input filter capacitor. The disadvantage of output filtering is that the long transition time, t_r, which is introduced by the output RC filter requires a Schmitt trigger logic gate to buffer the output filter circuit from the subsequent logic circuits to prevent logic chatter problems. The determination of load resistance and capacitance is illustrated in the following text.

The following given values specify the interface conditions.

HCPL-3700

V_{OL} = 0.4V

I_{OL} = 4.2mA

I_{OH} = 100μA max

V_{CC} = 5.0V ± 5%

7414

$V_{T+\,(min)}$ = 1.5V } Schmitt trigger upper

$V_{T+\,(max)}$ = 2.0V } threshold level

I_{IH} = 40μA max

I_{IL} = –1.2mA max

With the current convention shown in Figure 12, the minimum value of R_L which ensures that the output transistor remains in saturation is:

$$R_{L\,(min)} \geq \frac{V_{CC\,(max)} - V_{OL}}{I_{OL} + I_{IL}} \qquad (23)$$

$$= \frac{5.25V - 0.4V}{4.2mA - 1.2mA} = 1.62\,k\Omega$$

The maximum value for R_L is calculated allowing for a guardband of 0.4V in $V_{T+\,(max)}$ parameter, or $V_{IH} = V_{T+\,(max)} + 0.4V$.

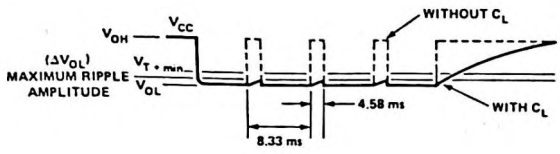


Figure 13. Output Waveforms of the HCPL-3700

$$R_{L\,(max)} \leq \frac{V_{CC\,(min)} - V_{IH}}{I_{OH} - I_{IH}} \qquad (24)$$

$$= \frac{4.75V - 2.4V}{0.1mA + 0.04mA} = 16.8\ k\Omega$$

R_L is chosen to be 1650Ω.

C_L can be determined in the following fashion. As illustrated in Figure 8, the output of the optocoupler will be in the high state for a specific amount of time dependent upon the selected V_+ levels. In this example, V_+ = 122.5V (75%) and V_- = 81.5V (50%) and allowing for a minimum peak line voltage of 138V (−15%), the high state time (without C_L) is from Equation (11), 4.58ms. With the appropriate C_L value, the output waveform (solid line) shown in Figure 13 is filtered.

The maximum ripple amplitude above V_{OL} is chosen to be 0.6V; that is, $V_{OL} + \Delta V_{OL}$ = 1.0V. This gives a 0.5V noise margin before $V_{T+\,(min)}$ = 1.5V is reached. The exponential ripple waveform is caused by the C_L being charged through R_L and input resistance, $R_{IN_{TTL}}$, of TTL gate. An expression for the allowable change in V_{OL} can be written:

$$\Delta V_{OL} = (V_{OH} - V_{OL})\,(1 - e^{-t/\tau}) \qquad (25)$$

where $\tau = R'_L C_L$ with R'_L equal to parallel combination of R_L and $R_{IN_{TTL}}$.

Below V_{T+} = 1.5V (min), $R_{IN_{TTL}}$ is constant and nominally 6 kΩ. Hence:

$$R'_L = \frac{R_L\,R_{IN_{TTL}}}{R_L + R_{IN}} \qquad (26)$$

$$= \frac{(1.65\ k\Omega)\,(6\ k\Omega)}{1.65\ k\Omega + 6\ k\Omega}$$

$$R'_L = 1.29\ k\Omega$$

Solving Equation (25) for τ yields

$$\tau = \frac{t}{\ln\left(\dfrac{V_{OH} - V_{OL}}{V_{OH} - V_{OL} - \Delta V_{OL}}\right)} \qquad (27)$$

and substituting previous parameter values and using $V_{OH} = V_{CC} - (I_{OH} + I_{IH})\,R_L$ results in

$$= \frac{4.58ms}{\ln\left(\dfrac{4.8V - 0.4V}{4.8V - 0.4V - 0.6V}\right)}$$

$$\tau = 31.24ms$$

C_L can be calculated directly,

$$C_L = \frac{\tau}{R'_L} \qquad (28)$$

$$= \frac{31.24ms}{1.29\ k\Omega}$$

C_L = 24.2μF use 27μF ± 10%

or 33μF ± 20%

With this value of C_L, the time the $R'_L C_L$ filter network takes to reach V_{T+} of the TTL gate is found as follows.

$$V_{OL} + (V_{OH} - V_{OL})\,(1 - e^{-t/\tau}) = V_{T+} \qquad (29)$$

Solving for t,

$$t = \tau \ln\left(\frac{V_{OH} - V_{OL}}{V_{OH} - V_{T+\,(min)}}\right) \qquad (30)$$

and substituting V_{OH} = 4.8V, V_{OL} = 0.4V, $V_{T+\,(min)}$ = 1.5V, and τ = 31.24ms yields

$$t = 9.0ms$$

This is the delay time that the system takes to respond to the ac line voltage going below the 50% (V_-) threshold level. In essence, the response time is slightly more than a half cycle (8.33ms) of 60 Hz ac line with worst case line variation taken into account. This delay time is acceptable for system power line protection. In this example, a complete worst case analysis was not performed. A worst case analysis should be done to ensure proper function of the circuit over variations in line voltage, unit to unit device parameter variations, component tolerances and temperature.

Threshold Accuracy Improvement

In the above example on output filtering, the two external threshold levels were selected for turn on conditions at V_+ = 122.5V (75%) and turn off at V_- = 81.5V (50%). The calculated external resistor values were R_x = 17.4 kΩ and R_P = 1.2 kΩ. Using standard 5% resistors of 18 kΩ and 1.2 kΩ respectively, the upper threshold voltage was actually 126.6V nominal.

Examination of the worst possible combination of variations of the HCPL-3700 optocoupler V_{TH+}, I_{TH+}, levels from unit to unit, and the ± 5% variations of R_x and R_P can result in the V_+ level changing +23% to −25% from design nominal.

If higher threshold accuracy is desired, it can be accomplished by decreasing the value of R_P in order to allow R_P to dominate the input resistance variations of the optocoupler. Using a 1% resistor for R_P and resistance of sufficiently small magnitude, the V_+ tolerance variations can be significantly improved. The following analysis will allow the designer to obtain nearly optimum threshold accuracy from unit to unit. It should be noted that the HCPL-3700 demonstrates excellent threshold repeatability once the external resistors are adjusted for a particular level and unit. The compromise which is made for the added control on threshold accuracy is that more input power must be consumed within the R_P, R_x resistors.

In Figure 14, assume the circuit is at the upper threshold point. At constant V_{TH+}, it is desired to maintain I_+ to within ± 5% variation of nominal value while allowing ± 1% variation in I_{P+}. With this requirement, Equations (31) and (32) can be written and solved for the magnitude of I_{P+} which is needed to maintain the desired condition on I_+. I_+ is the sum of I_{P+} and I_{TH+}.

$$1.05\, I_+ = 1.01\, I_{P+} + I_{TH+\,(max)} \quad (31)$$

$$0.95\, I_+ = 0.99\, I_{P+} + I_{TH+\,(min)} \quad (32)$$

} at constant V_{TH+}

where

$I_{TH+\,(max)}$ = 3.11mA

$I_{TH+\,(min)}$ = 1.96mA

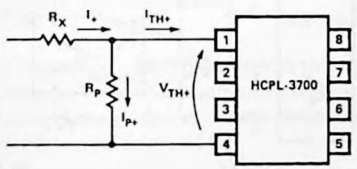


Figure 14. Threshold Accuracy Improvement through the Use of External R_x and R_P Resistors

Solving for I_{P+} yields

I_{P+} = 11.2mA,

and

$$R_P = \frac{V_{TH+}}{I_{P+}} \quad (33)$$

$$= \frac{5.1V}{11.2mA}$$

R_P = 433Ω (use 453Ω, 1% resistor)

This new value of R_P replaces the earlier R_P = 1.2 kΩ, and the circuit requires a new R_x value to maintain the same V_+ threshold level.

$$R_x = \frac{V_+ - V_{TH+}}{I_+} \quad \text{where} \quad I_+ = I_{P+} + I_{TH+} \quad (34)$$

$$= 11.2mA + 2.5mA$$

$$= \frac{122.5V - 5.1V}{13.7mA}$$

R_x = 8.57 kΩ (use 8.66 kΩ, 1% resistor)

With the possible variation of ± 1% in R_P and R_x, as well as unit to unit variations in the optocoupler V_{TH+}, I_{TH+}, the upper threshold level V_+ will vary significantly less than in the 5% resistor design case. The variations in V_+, which is given by $V_+ = R_x I_+ + V_{TH+}$, where $I_+ = I_{P+} + I_{TH+}$, are compared in Table 1.

Table 1 illustrates the possible improvements in V_+ tolerance as R_x and R_P are adjusted to limit the variation of the external input threshold current, I_+, to the resistor network and optocoupler. This table is centered at a nominal external input threshold voltage of V_+ = 122.5V. It is the designer's compromise to keep power consumption low, but threshold accuracy high.

NOTE: The above method for selection of R_P and R_x can be adapted for applications where larger sense currents (wet sensing) may be appropriate.

Example 4. Dedicated Lines for Remote Control

In situations involving a substantial separation between the signal source and the receiving station, it may be desirable to lease a dedicated private line metallic circuit (dc path) for supervisory control of remote equipment. The HCPL-3700 can provide the interface requirements of voltage threshold detection and optical isolation from the metallic line to the remote equipment. This greatly reduces the expense of using a sophisticated modem system over a convention telephone line.

R_x	TOL.	R_P	TOL.	I_+ TOLERANCE	V_+ TOLERANCE		MAXIMUM TOTAL POWER IN $R_x + R_P$ (RMS)
18 kΩ	5%	1.2 kΩ	5%	+17.5% −21.2%	+ 23%	− 25%	0.69 W
8.66 kΩ	1%	453Ω	1%	±5%	+12.7%	−19.3%	1.45 W
4.32 kΩ	1%	205Ω	1%	±3%	+11.2%	−18.9%	2.92 W
2.15 kΩ	1%	97.5Ω	1%	±2%	+10.6%	−18.8%	5.89 W

Table 1. Comparison of the V_+ Threshold Accuracy Improvement versus R_x and R_p and Power Dissipation for a Nominal V_+ = 122.5 V

Figure 15 represents the application of the HCPL-3700 for a line which is to control tank levels in a water district.

Some comments are needed about dedicated metallic lines. The use of a private metallic line places restrictions upon the designer's signal levels. The line in this example would be used in the interrupted dc mode (duration of each interruption greater than one second), the maximum allowed voltage between any conductor and ground is ⩽ 135 volts. Maximum current should be limited to 150mA if the cable has compensating inductive coils in it. Balanced operation of the line is strongly recommended to reduce possible cross talk interference as well as to allow larger signal magnitudes to be used. Precaution also should be taken to protect the line and equipment. The line needs to be fused to ensure against equipment failure causing excessive current to flow through telephone company equipment. In addition, protection from damaging transients must be taken via spark gap arrestors and commercial transient suppressors. Details of private line metallic circuits can be founded in the American Telephone and Telegraph Company publication 43401.

In this application, a 48V dc floating power source supplies the signal for the metallic line. The HCPL-3700 upper voltage threshold level is set for V_+ = 36V (75%). Consequently, R_x is

$$R_x = \frac{V_+ - V_{TH+}}{I_{TH+}} \quad (35)$$

$$= \frac{36V - 3.8V}{2.5mA}$$

$$= 12.9\ k\Omega \quad \text{(use } R_x/2 = 6.49\ k\Omega, 1\% \text{ resistor in each input level)}$$

The resulting lower voltage threshold level is

$$V_- = R_x I_{TH-} + V_{TH-} \quad (36)$$

$$= 13\ k\Omega\ (1.3mA) + 2.6V$$

$$V_- = 19.5V$$

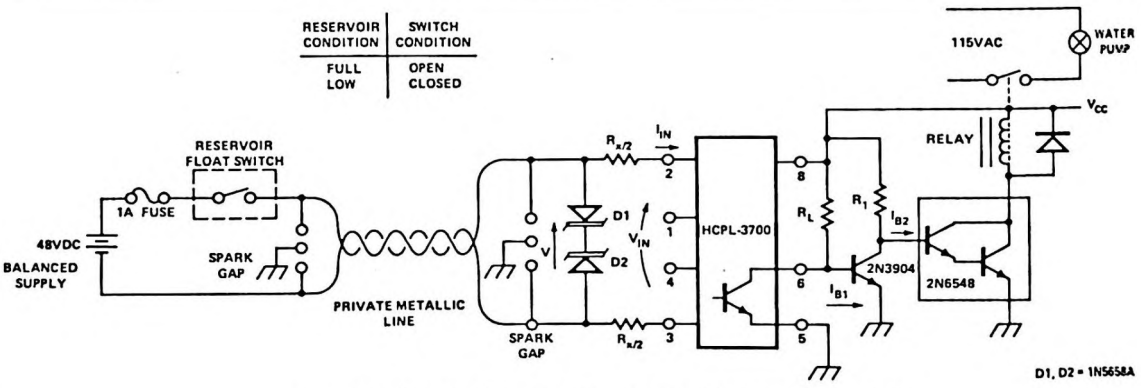


Figure 15. Application of the HCPL-3700 to Private Metallic Telephone Circuits for Remote Control

yielding V_{HYS} = 16.5V. The average induced ac voltage from adjacent power lines is usually less than 10 volts (reference ATT publication 43401) which would not falsely turn on, or off, the HCPL-3700, but could affect conventional optocouplers.

Under normal operation (full reservoir), the optocoupler is off. When the float switch is closed (low reservoir), the optocoupler output (V_{OL}) needs inversion, via a transistor, to drive the power Darlington transistor which controls a motor starting relay. The relay applies ac power to the system water pump. With V_{CC} = 10V, I_{B2} = 0.5mA, I_{B1} = 0.5mA.

$$R_1 = \frac{V_{CC} - 2V_{BE}}{I_{B2}} \quad (37)$$

$$= \frac{10V - 1.4V}{0.5mA}$$

$$R_1 = 17.2\ k\Omega$$

$$(R_1 = 18\ k\Omega)$$

$$R_L = \frac{V_{CC} - V_{BE}}{I_{B1}} \quad (38)$$

$$= \frac{10V - 0.7V}{0.5mA}$$

$$R_L = 18.6\ k\Omega$$

$$(R_L = 18\ k\Omega)$$

For this application, the ac inputs could also be used, which would remove any concern about the polarity of the input signal.

General Protection Considerations for the HCPL-3700

The HCPL-3700 optocoupler combines a unique function of threshold level detection and optical isolation for interfacing sensed signals from electrically noisy, and potentially harmful, environments. Protection from transients which could damage the threshold detection circuit and LED is provided internally by the Zener diode bridge rectifier and an external series resistor. By examination of Figure 1, it is seen that an input ac voltage clamp condition will occur at a maximum of a Zener diode voltage plus a forward biased diode voltage.

At clamp condition, the bridge diodes limit the applied input voltage at the device and shunt excess input current which could damage the threshold detection circuit or cause excessive stress to the LED.

The HCPL-3700 optocoupler can tolerate significant input current transient conditions. The maximum dc input current into or out of any lead is 50mA. The maximum input surge current is 140mA for 3ms at 120 Hz pulse repetition rate, and the maximum input transient current is 500mA for 10μs at 120 Hz pulse repetition rate. The use of an external series resistor, R_x, provides current limiting to the device when a large voltage transient is present. The amplitude of the acceptable voltage transient is directly proportional to the value of R_x.

However, in order to protect the HCPL-3700 when the input voltage to the device is clamped, the maximum input current must not be exceeded. An external means by which to enhance transient protection can be seen in Figure 16.

A transient R_xC_p filter can be formed with C_p chosen by the designer to provide a sufficiently low break point for the low pass filter to reduce high frequency transients. However, the break point must not be so low as to attenuate the signal frequency. Consider the previous ac application where no filtering was used. In that application, R_x = 37.4 kΩ, and if the bandwidth of the transient filter needs to be 600 Hz, then C_p is:

$$C_p = \frac{1}{2\pi f R_x} \quad (39)$$

$$C_p = 0.0071\mu F \quad \textbf{(use 0.0068}\mu\textbf{F capacitor @ 50V dc)}$$

Should additional protection be needed, a very effective external transient suppression technique is to use a commercial transient suppressor, such as a Transzorb ®, or metal oxide varistor, MOV ®, at the input to the resistor network prior to the optocoupler. The Transzorb ® will provide extremely fast transient response, clamp the input voltage to a definite level, and absorb the transient energy. Selection of a Transzorb ® is made by ensuring that the reverse stand off voltage is greater than the continuous peak operating voltage level. Transzorbs ® can be stacked in series or parallel for higher peak power ratings. Depending upon the designer's potential transient problems, a solution may warrent the expense of a commercial suppression device.

Thermal Considerations

Thermal considerations which should be observed with the HCPL-3700 are few. The plastic 8 pin DIP package is designed to be operated over a temperature range of −25°C to 85°C. The absolute maximum ratings are established for

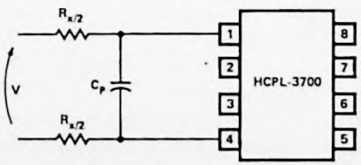


Figure 16. R_xC_p Transient Filter for the HCPL-3700

APPLICATIONS

a 70°C ambient temperature requiring slight derating to 85°C. In general, if operation of the HCPL-3700 is at ambient temperature of 70°C or less, no heat sinking is required. However, for operation between 70°C and 85°C ambient temperature, the maximum ratings should be derated per the data sheet specifications.

Mechanical and Safety Considerations

Mechanical Mounting Considerations

The HCPL-3700 optocoupler is a standard 8 pin dual-in-line plastic package designed to interface ac or dc power systems to logic systems. This optocoupler can be mounted directly onto a printed circuit board by wave soldering.

Electrical Safety Considerations

Special considerations must be given for printed circuit board lead spacing for different safety agency requirements. Various standards exist with safety agencies (U.L., V.D.E., I.E.C., etc.) and should be checked prior to PC board layout. The HCPL-3700 optocoupler component is recognized under the Component Program of Underwriters Laboratories, Inc. in file number E55361. This file qualifies the component to specific electrical tests to 220V ac operation.

The spacing required for the PC board leads depends upon the potential difference that would be observed on the board. Some standards that could pertain to equipment which would use the HCPL-3700 are UL1244, Electrical and Electronic Measuring and Testing Equipment, UL1092, Process Control Equipment, and IEC348, Electronic Measuring Apparatus. Spacing for the worst case in an uncontrolled environment with a 2000 volt-amperes maximum supplying source rating must be 3.2mm (0.125 inches) for 51 — 250 volts RMS potential difference over a surface (creepage distance), and 3mm (0.118 inches) through air (bare wire). These separations are between any uninsulated live part and uninsulated live part of opposite polarity, or uninsulated ground part other than the enclosure or an exposed metal part.

An uncontrolled environment is an environment which has contaminants, chemical vapors, particulates or any substances which would cause corrosion, decrease resistance between PC board traces or, in general, be an unhealthy environment to human beings.

For 0 — 50 volts RMS, the spacing is 1.6mm (0.063 inches) through air or over surfaces.

Electrical Connectors

The HCPL-3700 provides the needed isolation between a power signal environment and a control logic system. However, there exists a physical requirement to actually interconnect these two environments. This interconnection can be accomplished with barrier strips, edge card connectors, and PCB socket connectors which provide the electrical cable/field wire connection to the I/O logic system. These connectors provide for easy removal of the PC board for repair or substitution of boards in the I/O housing and are needed to satisfy the safety agency (U.L., V.D.E., I.E.C.) requirements for spacing and insulation. Connectors are readily available from many commercial manufacturers, such as Connection Inc., Buchanan, etc. The style of connector to choose is dependent upon the application for which the PC board is used. If possible it is wise to choose a style which does not mount to the PC board. This would enable the PC card to be removed without having to disconnect field wires. The use of connectors which are called "gas tight connectors" provide for good electrical and mechanical reliability by reducing corrosion effects over time.

APPENDIX I. List of Parameters

V ≡ Externally Applied Voltage
V_+ ≡ External Upper Threshold Voltage Level
V_- ≡ External Lower Threshold Voltage Level
V_{IHC1} = Device* Input Voltage Clamp Level; Low Voltage DC Case
V_{IHC2} = Low Voltage AC Case
V_{IHC3} = High Voltage DC Case
I_{IN} = Device Input Current
V_{IN} = Device Input Voltage
V_{TH+} = Device Upper Voltage Threshold Level
V_{TH-} = Device Lower Voltage Threshold Level
I_{TH+} = Device Upper Input Current Threshold Level
I_{TH-} = Device Lower Input Current Threshold Level
R_x = External Series Resistor for Selection of External Threshold Level
R_P = External Parallel Resistor for Simultaneous Selection/Accuracy Improvement of External Threshold Voltage Levels
I_+ = Total Input Current at Upper Threshold Level to External Resistor Network (R_x, R_P) and Device
I_{P+} = Current in R_P at Upper Threshold Levels
V_{peak} = Peak Externally Applied Voltage
V_O = Output Voltage of Device
V_{OL} = Output Low Voltage of Device
V_{OH} = Output High Voltage of Device
I_{OH} = Output High Leakage Current of Device
I_{OL} = Output Low Sinking Current of Device
I_{IH} = Input High Current of Driven Gate
I_{IL} = Input Low current of Driven Gate
V_{CC} = Positive Supply Voltage
R_{IN} = Input Resistance of HCPL-3700
V_{T+} ≡ Schmitt Trigger Upper Threshold Voltage of TTL Gate (7414)
R_L = Output Pullup Resistance
C_L = Output Filter Capacitance
C = Input Filter Capacitor
TH_+ = Upper Threshold Level
TH_- = Lower Threshold Level
P_{R_X} = Power Dissipation in R_x
P_{IN} = Power Dissipation in HCPL-3700 Input IC
PA = Input Signal Port to P.I.A.
t_+ = Turn On Time
t_- = Turn Off Time
T = Period of Waveform
C_P = Similar to R_P

*Device = HCPL-3700

HEWLETT PACKARD

APPLICATION NOTE 1005

Operational Considerations for LED Lamps and Display Devices

In the design of a display system, which incorporates LED lamps and display devices, the objective is to achieve an optimum between light output, power dissipation, reliability, and operating life. The performance characteristics and capabilities of each LED device must be known and understood so that an optimum design can be achieved. The primary source for this information is the LED device data sheet.

The data sheet typically contains Electrical/Optical Characteristics that list the performance of the device and Absolute Maximum Ratings in conjunction with characteristic curves and other data which describe the capabilities of the device. A thorough understanding of this information and its intended use provides the basis for achieving an optimum design.

This application note presents an in-depth discussion of the theory and use of the electrical and optical information contained within a data sheet. Two designs using this information in the form of numerical examples are presented, one for dc operation and one for pulsed (strobed) operation. The calculated results for each example are underlined and accented by an arrow (←) for each identification. Specific information on operation without derating and the soldering of plastic LED devices is also presented.

Typical Data Sheet Information

A data sheet typically contains Absolute Maximum Ratings, Electrical/Optical Characteristics, and typical operating graphs. The Absolute Maximum Ratings list such items as the maximum allowed forward currents, power dissipation, and operating ambient temperature range. The Electrical/Optical Characteristics list such data as the luminous intensity specification (I_V), forward voltage (V_F), peak wavelength (λ_{PEAK}), dominant wavelength (λ_d), and the device thermal resistance LED junction-to-pin on a per LED element basis ($R\theta_{J-PIN}$).

The five graphs that are usually contained within a data sheet are:

Figure 1: Pulsed Mode Operating Curves
Figure 2: Current Derating vs. Temperature
Figure 3: Relative Luminous Efficiency
Figure 4: Forward Voltage Characteristic
Figure 5: Light Output vs. DC Drive Current

The data sheet also provides an equation to calculate the expected maximum forward voltage at a given current.

Design Criteria

This application note assumes that the objective of a specific design is to achieve a maximum light output from a display that is operated in an elevated ambient temperature. The two criteria that establish the operating limits are the maximum drive current and the maximum LED junction temperature. The maximum drive current has been established to ensure a long operating life and the maximum LED junction temperature is governed by the device package. The data sheet will list the maximum allowed drive currents for a specific device. The absolute maximum allowed LED junction temperature (T_J MAX) differs for the various device package configurations. For most plastic display devices, T_J MAX = 100°C; for most plastic lamps, T_J MAX = 110°C; and for alphanumeric PC board monolithic displays, T_J MAX = 110°C (for some PC board monolithic displays, T_J MAX = 80°C).

Thermal Resistance

The LED junction temperature is the sum of the ambient temperature (T_A) and the temperature rise above ambient (ΔT_J), which is the product of the power dissipated within the junction (P_D) times the thermal resistance LED junction-to-ambient ($R\theta_{JA}$).

$$T_J\ (°C) = T_A + \Delta T_J \qquad (1)$$
$$T_J\ (°C) = T_A + P_D\ R\theta_{JA}$$

The cathode pins of an LED device are the primary thermal paths for heat dissipation from the LED junction into the surrounding environment. The data sheet lists the thermal resistance LED junction-to-pin ($R\theta_{J-PIN}$) for the device. This device junction-to-pin thermal resistance is added to the thermal resistance-to-ambient of the PC board mounting assembly ($R\theta_{PC-A}$) to obtain the overall value of $R\theta_{JA}$ on a per LED element basis. (NOTE: For monolithic displays, thermal resistance is calculated on a per digit basis.)

$$R\theta_{JA} = R\theta_{J-PIN} + R\theta_{PC-A} \qquad (2)$$
$$= °C/W/LED\ Element$$

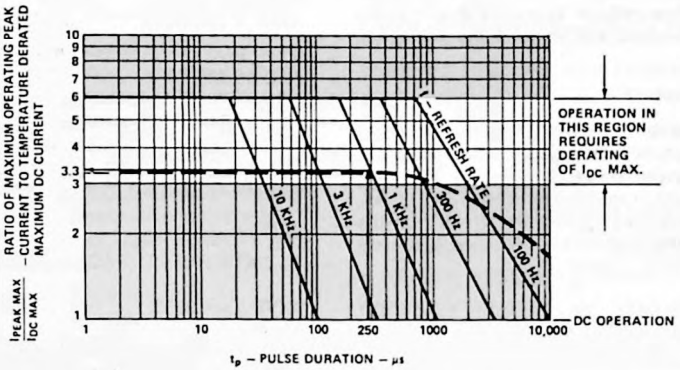


Figure 1. Maximum Tolerable Peak Current vs. Pulse Duration

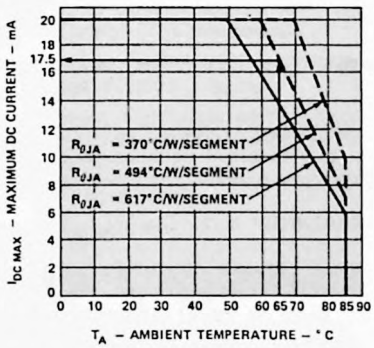


Figure 2. Maximum Allowable DC Current per Segment vs. Ambient Temperature. Deratings Based on Maximum Allowed Thermal Resistance Values, LED Junction-to-Ambient on a per Segment Basis. $T_J MAX = 100°C$

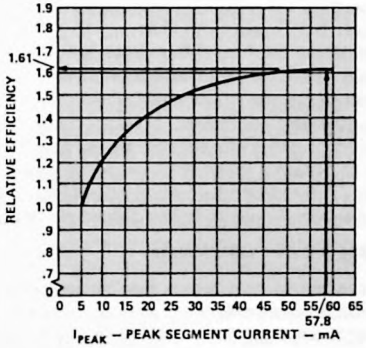


Figure 3. Relative Luminous Efficiency (Luminous Intensity per Unit Current) vs. Peak Segment Current

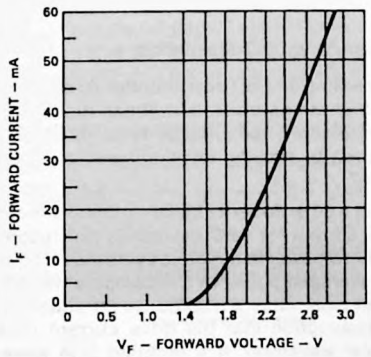


Figure 4. Forward Current vs. Forward Voltage Characteristic

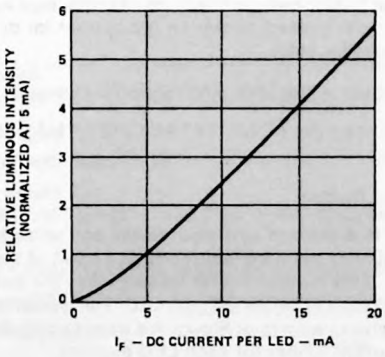


Figure 5. Relative Luminous Intensity vs. DC Forward Current

APPLICATIONS

For reliable operation, it is recommended that the value of $R\theta_{PC-A}$ be designed low enough to ensure that the LED junction temperature does not exceed the maximum allowed value.

Derating vs. Temperature

The derating vs. temperature, Figure 2, is derived from the LED junction temperature rise above ambient as estab- by the maximum allowed power dissipation (P_D MAX) which is derated linearly to zero power when $T_A = T_J$ MAX. The values of $R\theta_{JA}$ shown on Figure 2 are derived from the quotient of ΔT_J and P_D MAX for a specified operating temperature.

$$R\phi_{JA}\ (°C/W/LED) = \frac{\Delta T_J\ (°C)}{P_D\ MAX\ (W)} = \frac{T_J\ MAX - T_A\ OPERATING}{P_D\ MAX} \quad (3)$$

The value of P_D MAX is the power dissipation within a maximum forward voltage device when driven at the maximum data sheet current. Thus, $R\theta_{JA}$ is determined on the basis of worst case power dissipation.

The derating curve with the largest $R\theta_{JA}$ value in Figure 2, normally a derating from $T_A = 50°C$, represents a mandatory derating for a typical application that utilizes a single sided PC board with 0.51mm (0.020 inch) wide traces, assuming that no other provision is provided for heat dissipation. The other derating curves from higher ambient temperatures, shown as dashed lines on Figure 2, represent allowed increased drive currents when the design incorporates a more elaborate PC board mounting assembly to obtain a lower $R\theta_{JA}$ value for increased heat dissipation. The temperature deratings of Figure 2 ensure reliable operation for both dc and pulsed mode operation.

Worst Case Power Calculation

The worst case power is that power dissipated within the junction of a maximum forward voltage device. The worst case power is used for determining the worst case T_J that will result from a specific drive current and thermal resistance, see Equation 1. The expected maximum forward voltage (V_F MAX) at a selected drive current is determined by an equation on the data sheet of the form:

$$V_F MAX = V_{ON} + (I_{PEAK})(\text{LED Dynamic Resistance}) \quad (4)$$

The worst case power is the product of the time average current under pulsed operation (dc current for dc operation) times V_F MAX:

$$P_{WORST\ CASE} = (I_{DC})(V_F\ MAX);\ \text{For DC Operation} \quad (5)$$

$$P_{WORST\ CASE} = (I_{PEAK})(\text{DUTY FACTOR})(V_F\ MAX\ \text{at}\ I_{PEAK});\ \text{For Pulsed Operation}$$

Current Limiting

An LED is a current operated device and some kind of current limiter must be incorporated as part of the drive circuitry. This current limiter usually takes the form of a resistor placed in series with the LED. The typical forward voltage characteristic of Figure 4 is used to calculate the series current limiter for each LED element.

$$R_{LIMITER} = \frac{V_{CC(POWER\ SUPPLY)} - V_{SAT(DRIVE\ TRANSISTORS)} - V_{F(FIGURE\ 4)}}{I_{PEAK\ CURRENT\ PER\ LED\ ELEMENT}} \quad (6)$$

Light Output

The time averaged luminous intensity (I_v) at $T_A = 25°C$ for a particular drive condition may be calculated using the relative luminous intensity characteristic of Figure 5 for dc operation or the relative efficiency characteristic ($\eta_{I_{PEAK}}$) of Figure 3 for pulsed operation. For dc operation, I_v ($T_A = 25°C$) is equal to the product of the data sheet luminous intensity specification times the relative factor for a specific dc current from Figure 5.

$$I_v\ DC = (I_v\ DATA\ SHEET)(FACTOR\ FROM\ FIGURE\ 5) \quad (7)$$

FOR: $T_A = 25°C$

For pulsed operation, the time averaged luminous at $T_A = 25°C$ is calculated using the following equation:

$$I_v\ TIME\ AVG = \left[\frac{I_{AVG}}{I_{AVG}\ DATA\ SHEET}\right][\eta_{I_{PEAK}}]\ [I_v\ DATA\ SHEET] \quad (8)$$

Where: I_{AVG} = The average forward current through an LED element

$I_{AVG\ DATA\ SHEET}$ = The average current at which I_v DATA SHEET is measured

The luminous intensity value at $T_A = 25°C$ is adjusted by the following exponential equation to obtain the light output value at the operating ambient temperature.

$$I_v\ (T_A\ OPERATING) = I_v\ (25°C)e^{[k(T_A - 25°C)]} \quad (9)$$

LED	k
Standard Red	−.0188/°C
High Efficiency Red	−.0131/°C
Yellow	−.0112/°C
Green	−.0104/°C

Pulsed Mode vs. DC Operation

When operating an LED device under dc drive conditions, the junction temperature is a linear function of the dc power dissipation multiplied by $R\theta_{JA}$. The light output is proportional to the dc drive current as expressed in Equation 7.

The use of a 50 or 60 Hertz half or full-wave rectified ac as the drive current for LED devices is not recommended, since the rms power in a rectified sine wave is greater than the time averaged power of a rectangular waveform of an equivalent peak value. Pulsed drive conditions are based on the assumption that the drive current pulses are a rectangular waveform. If a rectified sine wave is to be used, in no case should the value of the peak current exceed the maximum allowed dc current value.

When operating an LED device in a pulsed mode, it is the peak junction temperature (not the average) that governs

the performance of the device as to the allowed time average power dissipation and light output. The lower the peak junction temperature (T_J PEAK) is in relationship to the time average junction temperature (T_J AVG), the greater is the light output of the device. At slow refresh rates (the number of times per second a device is pulsed) in the range of 100 Hz, T_J PEAK is greater than T_J AVG. As the refresh rate approaches 1000 Hz, the value of T_J PEAK approaches the value of T_J AVG. Therefore, it is recommended that whenever possible LED devices be refreshed at a 1 KHz rate or faster, since at these faster pulse rates T_J PEAK is assumed to be equal to T_J AVG and the light output is a function of T_J AVG.

Design Steps

In order to determine the derated drive conditions from the data sheet for an elevated ambient temperature, a value for $R\theta_{JA}$ must be selected. Once a value for $R\theta_{JA}$ has been selected, the required current derating can be determined for the operating ambient temperature directly from Figure 2. As illustrated in the pulsed mode design example, the dc derating is used to determine the pulsed current derating.

The four basic design steps are:

1. Determine derated drive currents.
2. Calculate the required value of $R\theta_{PC-A}$ for the PC board mounting configuration.
3. Calculate the value of the current limiting resistor. Use the nearest standard value resistor larger than the calculated value.
4. Calculate the light output.

DC Design Example

A high efficiency red seven segment display is to be operated in an ambient of T_A = 65° C. Pertinent data for this device are:

Maximum DC Current per segment (T_A = 50° C) = 20mA

Maximum Average Power Dissipation (T_A = 50° C) = 81mW

I_V TYPICAL = 300μcd per segment at I_{DC} = 5mA

$R\theta_{J-PIN}$ = 282° C/W/Segment

V_F MAX = 1.60V + I_{DC} (45Ω); for 5mA ≤ I_{DC} ≤ 20mA

T_J MAX = 100° C

The data sheet curves on page 2 apply to this device. It is assumed that a value of $R\theta_{JA}$ = 494° C/W/Segment or less will be incorporated into the display system design.

Step 1.
The derated dc drive current is determined from Figure 2.

At T_A = 65° C and $R\theta_{JA}$ ≤ 494° C/W/Segment,

I_{DC} MAX = 17.5mA ← I_{DC} MAX

Step 2.
The required maximum thermal resistance for the PC board assembly is calculated from Equation 2:

$R\theta_{PC-A}$ ≤ (494-282) = 212° C/W/Segment ← $R\theta_{PC-A}$

Step 3.
A value of V_{SAT} = 0.4 volts is assumed for the LED drive transistors. From Figure 4,

V_F TYP (17.5mA) = 2.0V

From Equation 6 and assuming V_{CC} = 5.0V:

$$R_{LIMITER} = \frac{5.0V - 0.4V - 2.0V}{0.0175A} = 149\Omega \leftarrow R_{LIMITER}$$

Use a 150Ω standard value resistor.

Step 4.
From Figure 5, the normalized light at 17.5mA is a factor of 4.4 x the light output at 5mA.

From Equation 7:

I_V (25° C) = (300μcd)(4.4) = 1320 μcd/segment

Using Equation 9 to adjust the light output for T_A = 65° C:

I_V (65° C) = (1320μcd)$e^{[-.0131/°C\ (65-25)°C]}$

I_V (65° C) = (1320)(0.592) = 782μcd/segment ← I_V

Pulsed Mode Design Example

A four digit display using the same high efficiency red seven segment display described in the DC Design Example is to be operated in a pulsed mode in an ambient of T_A = 65° C. Additional pertinent data for this device are:

Maximum Peak Current per Segment

(T_A = 50° C, Pulse Width = 2ms) = 60mA

V_F MAX = 1.75V + I_{PEAK} (38Ω); for I_{PEAK} ≥ 20mA

It is assumed that a value of $R\theta_{JA}$ = 494° C/W/segment or less will be incorporated into the display system design.

Figure 1 is used to select the refresh conditions for pulsed operation. These refresh conditions are junction temperature related to the dc current deratings of Figure 2. Figure 1 relates the ratio of maximum-peak current to temperature derated maximum dc current (I_{PEAK} MAX/I_{DC} MAX) and pulse duration (t_p) as a function of refresh rate (f). The allowed average power dissipation decreases below f = 1kHz since the difference between T_J PEAK and T_J AVG increases with decreasing refresh rates. This condition is illustrated by the dashed line shown on Figure 1, which shows the ratio of I_{PEAK} MAX to I_{DC} MAX decreasing with slower refresh rates with the duty factor fixed at 1 of 4.

Step 1.
For best performance, a refresh rate of 1kHz will be used:

f = 1kHz ← f

A four digit display sets the duty factor (D.F.) at one of four:

D.F. = 1/4 ← D.F.

t_p = (1/f)(D.F.) = (1/1000 Hz)(1/4) = 250μs ← t_p

From Figure 1:
I_{PEAK}/I_{DC} MAX = 3.3; for t_p = 250μs and f = 1kHz

From Figure 2:
I_{DC} MAX, at T_A = 65° C and $R\theta_{JA}$ = 494° C/W/Segment, is 17.5mA

I_{PEAK} = (I_{PEAK} MAX/I_{DC} MAX)(I_{DC} MAX from Figure 2)

I_{PEAK} = (3.3)(17.5mA) = 57.8mA per Segment ← I_{PEAK}

I_{AVG} = (I_{PEAK})(D.F.) = (57.8mA)(1/4) = 14.5mA ← I_{AVG}

These are the maximum pulsed mode drive currents for this design as defined by T_A = 65° C and $R\theta_{JA}$ ≤ 494° C/W/segment.

APPLICATIONS

Step 2.
The required maximum thermal resistance for the PC board assembly is calculated from Equation 2:

$R\theta_{PC-A} \leq (494-282) =$
$212°C/W/segment \longleftarrow R\theta_{PC-A\ MAX}$

Step 3.
A value of V_{SAT} = 1.2 volts is assumed for the LED drive transistors. From Figure 4,

V_F TYP (57.8mA) = 2.85V

From Equation 6 and assuming Vcc = 5.OV:

$$R_{LIMITER} = \frac{5.0V - 1.2V - 2.85V}{0.578A} = 16\Omega \longleftarrow R_{LIMITER}$$

Use a 17Ω standard value resistor.

Step 4.
From Figure 3, the relative efficiency for I_{PEAK} = 57.8mA is:

$\eta_{I_{PEAK}} = 1.61$

From Equation 8:

$$I_v(25°C) = \left[\frac{14.5mA}{5mA}\right][1.61][300\mu cd] =$$

1401μcd per segment

Using Equation 9 to adjust the light output for T_A = 65°C:

$I_v(65°C) = (1401\mu cd)e^{[-0131/°C\ (65-25)°C]}$

I_v (65°C) = (1401)(0.592) = 829μcd per Segment ⟵ I_v

Operation Without Derating

LED lamp and display devices may be operated in elevated ambient temperature environments without derating only when the PC board mounting configuration is designed for a sufficiently low thermal resistance. The critical criterion is that the LED junction temperature must not exceed the T_J MAX value for the device. This low thermal resistance design will typically include such items as a maximum metallized PC board and possible heat sinking to ensure adequate heat dissipation. In no situation should the absolute maximum current limitations be exceeded.

The necessary thermal resistance requirements for operation without derating are calculated using the value for worst case power dissipation. A numerical example using the LED display device from the above two examples will illustrate the calculation procedure.

Step 1.
Determine the maximum permissible value for $R\theta_{JA}$.

The absolute maximum power dissipation as listed on the data sheet for this particular LED device is 81mW. The operating ambient temperature is to be 65°C.

Referring to Equation 3

$$R\theta_{JA\ MAX} \leq \frac{T_{J\ MAX} - T_{A\ OPERATING}}{P_{MAX\ DATA\ SHEET}}$$

For this example:

$$R\theta_{JA\ MAX} \leq \frac{100°C - 65°C}{.081W} = 432°C/W/Segment$$

The required limit on the thermal resistance for the PC board mounting configuration is derived by rewriting Equation 2:

$R\theta_{PC-A\ MAX} \leq R\theta_{JA\ MAX} - R\theta_{J-PIN}$

For this example:

$R\theta_{PC-A} \leq (432-282) = 150°C/W/segment \longleftarrow R\theta_{PC-A\ MAX}$

The particular LED display device used in this example may be operated at maximum power dissipation in an ambient of T_A = 65°C without derating as long as the PC board mounting configuration is designed to have $R\theta_{PC-A} \leq 150°C/W/Segment$.

CAUTION: Since these calculations are based on only T_J AVG and exclude the consideration of T_J PEAK, pulsed operation without derating is only recommended for refresh rates of 1kHz or faster.

Soldering Plastic LED Devices

Because plastic LED devices utilizing a lead frame construction have the LED dice attached directly to the cathode lead, the cathode lead is the direct thermal and mechanical stress path to the LED dice. For this reason, it is necessary to carefully control the solder temperature and dwell time in the solder wave to ensure subsequent reliable operation. LED devices can be effectively wave soldered with a wave temperature of 245°C and a dwell time of 1½ to 2 seconds.

The post solder cleaning process is also crucial to ensuring reliable performance. In order to optimize device optical performance, specially developed plastics are used which restrict the solvents that may be used for cleaning. It is recommended that only mixtures of Freon (F113) and alcohol be used for vapor cleaning processes, with an immersion time in the vapors of less than two (2) minutes maximum. Some suggested vapor cleaning solvents are Freon TE, Genesolv DI-15 or DE-15, Arklone A or K. A 60°C (140°F) water cleaning process may also be used, which includes a neutralizer rinse (3% ammonia solution or equivalent), a surfactant rinse (1% detergent solution or equivalent), a hot water rinse and a thorough air dry. Room temperature cleaning may be accomplished with Freon T-35 or T-P35, Ethanol, Isopropanol or water with a mild detergent.

Some LED devices may require special handling during soldering, during post solder cleaning, or may not lend themselves to a wave soldering process. Three specific considerations are:

1. Plastic LED Lamps: The plastic encapsulant that forms the lamp package is the only supporting element for the leads. It is important to prevent stresses from entering the device package which could damage the LED die attach and wire bonds. The leads of a lamp may be bent to a desired angle by observing the following procedure. Firmly grasp the leads at the base of the lamp package with a pair of needle nose pliers to support the lamp while bending the leads. Overheating during soldering will cause melting of the plastic, allowing possible lead movement to occur which may result in the catastrophic failure of the die attach or wire bonds. Care should be taken to ensure that no stresses are applied to the leads during the soldering process. External stresses applied to the leads during soldering could induce strains within the device package that may induce latent failure. Once properly soldered in place, an LED lamp will typically exhibit a very high degree of reliability.

2. PC Board Monolithic Displays: Many PC board monolithic displays do not lend themselves to a wave soldering process. The plastic lens that covers the LED chips and wire bonds is attached to the PC board without forming a seal. The chemicals used in a wave soldering process can collect underneath the lens. The post solder cleaning process may not remove all of the trapped chemicals and prolonged exposure of the LED dice and wirebonds to these chemicals can cause permanent damage. Also, the plastic used to make some of the lenses is susceptible to damage from rosin fluxes and hydrocarbon cleaners. The two recommended installation procedures are either to hand solder flexible cable to the display contacts or use solderless connector pins such as the 022-002 series supplied by JAV Manufacturing, 125 Wilbur Place, Bohemia, NY 11716. Effective room temperature cleaning may be accomplished using Freon TP-35 or TE-35, solvent temperature $\leq 30°C$ and an immersion time ≤ 2 minutes.

3. Silver Lead Frames: Many plastic LED devices utilize a silver plated lead frame. Silver plating provides excellent solderability as long as the leads are kept free from tarnish buildup due to coming in contact with sulfur compounds. Application Bulletin 3 offers specific information on the effective use and soldering of silver lead frame devices.

It is suggested that the device data sheet be consulted for specific information on wave soldering.

HEWLETT PACKARD

APPLICATION NOTE 1006

Seven Segment LED Display Applications

INTRODUCTION

Hewlett-Packard's line of seven segment LED display products can be divided into two broad categories. The first product family is the large seven segment display which is constructed using individual LEDs for each segment. These large single digit LED display devices have become common in instruments throughout the industry. The other standard type of seven segment device is known as the monolithic display. Monolithic displays are constructed by diffusing several LED junctions in a single GaAsP die. This type of display is characterized by its small size, low cost, and low power requirements. The monolithic display typically has several digits per package and is often found in calculators and hand held or portable instruments.

This application note begins with a detailed explanation of the two basic product lines that Hewlett-Packard offers in the seven segment display market. This discussion includes mechanical construction techniques, character heights, and typical areas of application. The two major display drive techniques, dc and strobed, are covered. The resultant tradeoffs of cost, power, and ease of use are discussed. This is followed by several typical instrument applications including counters, digital voltmeters, and microprocessor interface applications. Several different microprocessor based drive techniques are presented incorporating both the monolithic and the large seven segment LED displays.

The application note contains a discussion of intensity and color considerations made necessary if the devices are to be end stacked. Hewlett-Packard has made several advances in the area of sunlight viewability of LED displays. The basic theory is discussed and recommendations made for achieving viewability in direct sunlight. Information concerning display mounting, soldering, and cleaning is presented. Finally, an extensive set of tables has been compiled to aid the designer in choosing the correct hardware to match a particular application. These tables include seven segment decoder/drivers, digit drivers, LSI chips designed for use with LEDs, printed circuit board edge connectors, and filtering materials.

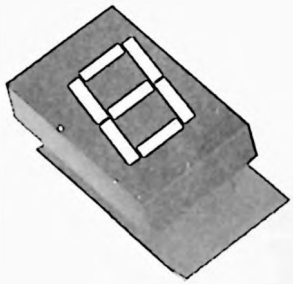


Figure 1. Large Seven Segment Display

LARGE SEVEN SEGMENT DISPLAYS

The large seven segment displays are designed to be easy to read single digit LED devices (Figure 1). They are typically used in electronic instruments, point-of-sale terminals, weighing scales, digital clocks, televisions, and appliances. The colors available are standard red, high efficiency red, yellow, and green. The standard red product is made from Gallium Arsenide Phosphide (GaAsP) on a GaAsP substrate. Both the high efficiency red and yellow seven segment displays are made from GaAsP on a Gallium Phosphide (GaP) substrate. The green seven segment displays are made from GaP on a GaP substrate. The increased efficiency of the GaP material results in the high efficiency red, yellow, and green displays having 3 to 5 times the minimum luminous intensity of the standard red displays.

A wide range of character heights varying from 7.6 mm (0.3 inch) to 20.3 mm (0.8 inch) allow the designer to choose the correct size display for the desired viewing range. The information in Figure 2 can be used to determine which character size display should be used for easy readibility. The information has been compiled for a standard viewer (20/20 eyesight) in typical office ambient condition (100-1000 lux) with the displays driven at recommended data sheet values.

Character Size	Maximum Viewing Distance
7.6 mm (0.3 inch)	5 metres
10.9 mm (0.43 inch)	6 metres
14.1 mm (0.56 inch)	7.5 metres
20.3 mm (0.8 inch)	9 metres

Figure 2. Large Seven Segment Display Viewing Distances

The large LED display devices are manufactured using the concept of stretching the light from an LED by diffusion and reflection. The LED chips are mechanically supported and electrically connected by a lead frame. A cone shaped reflecting cavity is cast inside a rectangular package above each LED. This is done using glass filled epoxy with the top of this cavity forming the stretched segment. The plastic housing, called a "scrambler," forms the display package and contains the segment cavities. The stretched segment displays offer a variety of colors, sizes, and good on/off contrast.

These seven segment display products are available in either common anode or common cathode configuration with either right hand or left hand decimal point. The displays can be either dc driven or operated in the strobed mode. The low forward voltage of the LEDs makes the displays inherently IC compatible. The ±1 overflow digit in the 14.1 mm (0.56 inch) package style is available in both common anode and common cathode configurations. For all other large seven segment displays, a universal overflow ±1 digit with right hand decimal point is available. The ±1 overflow digit has each LED anode and cathode present on external pins for ease of use.

MONOLITHIC SEVEN SEGMENT DISPLAYS

The monolithic seven segment displays are small, low cost, low power, multi-digit LED devices. They are typically used in desktop calculators, hand held instruments, metering devices, and various consumer products. With character heights ranging from 2.5 mm (0.1 inch) to 4.4 mm (0.175 inch), the monolithic products provide a flexible family of seven segment displays. The 2.5 mm (0.1 inch) character height displays are designed for hand held applications, whereas the 4.4 mm (0.175 inch) displays can be easily read at distances up to 2 metres.

Monolithic displays differ from other types of LED displays in that the individual light emitting segments are formed by diffusing separate LED junctions on a single chip of GaAsP. Because GaAsP is relatively expensive, most monolithic displays are magnified to keep chip sizes small. In most cases, the monolithic display is magnified by an external lens to attain a viewable character size.

Monolithic displays can be classified into two basic categories according to whether the lens is of the immersion or non-immersion type. Immersion lenses are formed by molding a lens directly over the LED chip. Non-immersion lenses have at least one layer of air between the LED chip and the lens assembly. Monolithic displays constructed with immersion lenses (Figure 3a) are manufactured by die attaching the monolithic GaAsP chips to the lead frame. The die attach pad also forms the common cathode electrical connection to the monolithic chip. The aluminum contact for each segment on the monolithic chip is then wire bonded to the appropriate anode contact. The completed device is then fully encapsulated in epoxy. The magnifying lens is formed during encapsulation.

Monolithic displays with non-immersion lenses (Figure 3b) are usually constructed by epoxy die attaching the monolithic GaAsP chips to a special high temperature printed circuit board. The electrical contact for each segment on the monolithic chip is wire bonded to the appropriate anode trace on the printed circuit board. A precision injection molded lens is then aligned and attached to the printed circuit board. This attachment is done using holes that were drilled during fabrication of the printed circuit board to ensure alignment.

Hewlett-Packard's monolithic displays are of common cathode configuration since the GaAsP substrate is n doped material and each LED junction is formed by a P+ diffusion. Due to the monolithic display's low dynamic resistance in the forward region, multiplexing at relatively high peak current is possible while keeping forward voltage typically less than 1.8 volts. For this reason, long strings can be easily strobed.

Figure 3a. Immersion Lens Monolithic Display

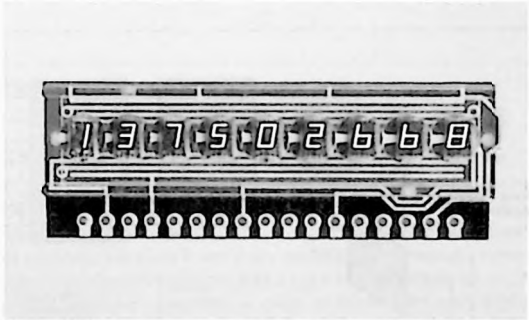


Figure 3b. Non-Immersion Lens Monolithic Display

DC DRIVE TECHNIQUES (Large Seven Segment Displays Only)

When seven segment displays are dc driven, each character is continuously illuminated. This is usually done with one decoder/driver per character and is commonly used for short display strings. If the display length is sufficiently short, the cost of dc decoding may be less than that of strobing circuitry. The fact that the drivers need not handle high current levels is a distinct advantage of dc operation.

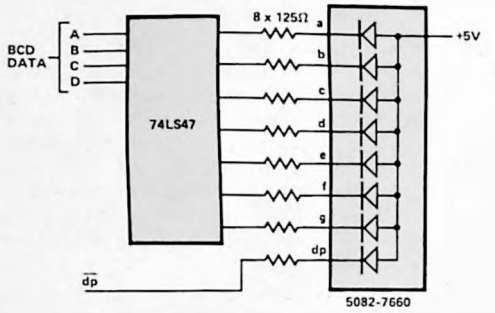


Figure 4a. DC Drive Circuit for the 5082-7660 Common Anode Display

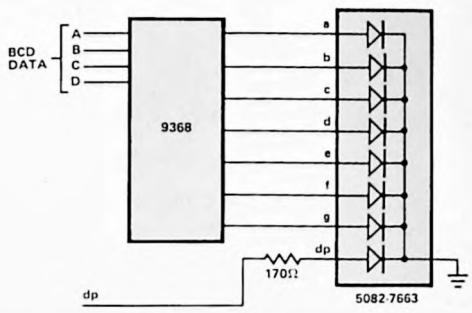


Figure 4b. DC Drive Circuit for the 5082-7663 Common Cathode Display

Figure 4a shows the standard configuration for a common anode display. The current level, set here at 20 mA per segment, is determined by the relation

$$R = \frac{V_{CC} - V_F - V_{O(ON)}}{I_F} = \frac{5.0V - 2.2V - 0.35V}{20\ mA} = 125\Omega$$

where

V_{CC} = voltage supply potential
V_F = forward voltage of LED at desired I_F
$V_{O(ON)}$ = ON state output voltage of display driver (74LS47)
I_F = desired forward current (20 mA)

An analogous circuit is shown in Figure 4b for a common cathode display. The Fairchild 9368 is a seven segment decoder/driver incorporating input latches and constant 15 mA current outputs to directly drive common cathode LED displays.

MULTIPLEXED DRIVE TECHNIQUES

When multiplexing drive circuitry is used, the decoder is timeshared among digits in the display. The digits are electrically connected with like segments wired in parallel. This forms a seven (seven segments) by N (number of digits) array. In operation, the appropriate segment enable lines are activated for the particular character to be displayed. Simultaneously, a digit enable line is selected so that the character appears at the proper digit location. The strobe then progresses to the next digit position, activating the proper segments and digit enable line for that position. Figure 5 contains a block diagram of a typical five digit multiplexed LED display.

Since the eye is a relatively slow time average sensor, a viewer will perceive a repetitive visual phenomenon to be continuous if it occurs at a rate in excess of about 60 events per second. Therefore, if the refresh rate for each digit is maintained at 100 times or more per second, the perceived display will appear flicker-free and easy to read.

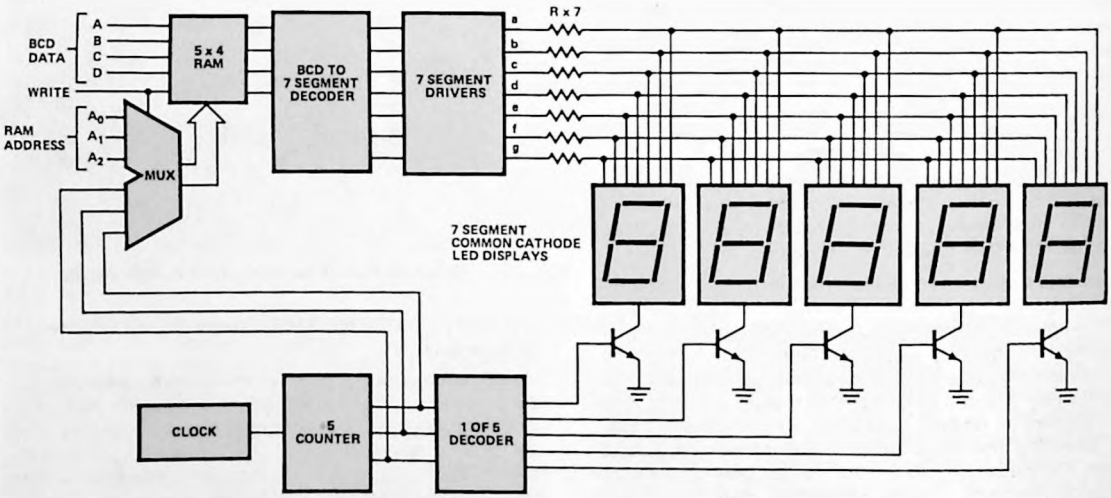


Figure 5. Block Diagram of a Multiplexed Five Digit LED Display

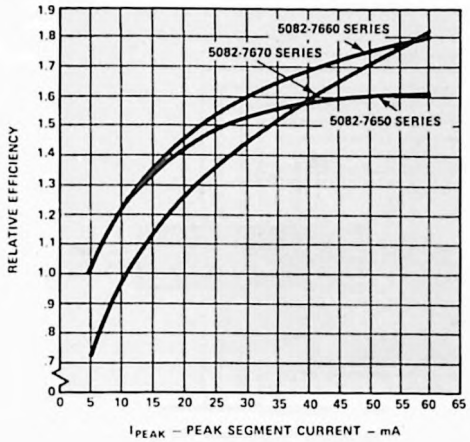


Figure 6a. Relative Luminous Efficiency (Luminous Intensity per Unit Current) vs. Peak Segment Current

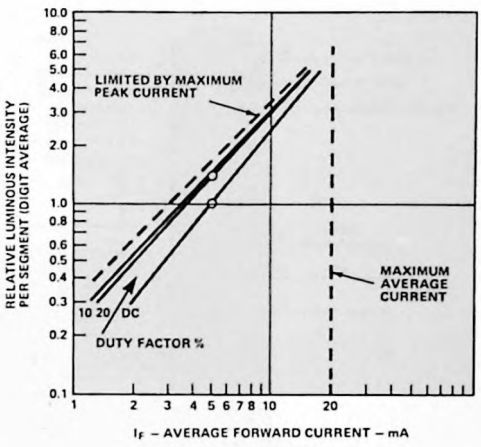


Figure 6b. Relative Luminous Intensity per Segment vs. Average Current (5082-7650)

In displays subject to vibration, a minimum strobe rate of five times the vibration frequency should be maintained.

In addition to reducing the number of decoders and drivers, strobing requires less power than dc drive to achieve the same display intensity. This is due to a basic property of GaAsP where luminous efficiency (light output/unit current) increases with the peak current level (see Figure 6a). Thus, for the same average current, the use of lower duty cycles and higher peak current levels results in increased light output. This phenomenon is illustrated in Figure 6b. Notice that the graph is normalized to one at a forward current of 5 mA dc. If this same device were operated at 25 mA peak, 20% duty factor (as if in a five digit strobed display) the time averaged luminous intensity would increase 40%.

For common decoder/driver circuits, a series resistor is placed in each segment line to limit the LED current. This is done to prevent uneven current distribution among segments. Referring to Figure 7, the current limiting resistor values may be calculated using the following formula:

$$R = \frac{V_{CC} - V_{CE\,(SEG)} - V_F - V_{CE\,(DIG)}}{I_{PEAK}}$$

where

V_{CC} = voltage supply potential
$V_{CE\,(SEG)}$ = saturation voltage drop across segment driver at I_{PEAK}
V_F = LED forward voltage at I_{PEAK}
$V_{CE\,(DIG)}$ = saturation voltage drop across digit driver at [I_{PEAK} x 8 (worst case number of segments ON)]
I_{PEAK} = $I_{AVERAGE}$ x number of digits = peak LED segment current

OR

$$I_{PEAK} = \frac{I_{AVG}}{D.F.}$$

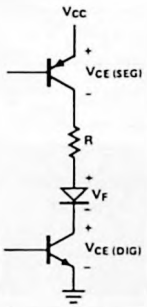
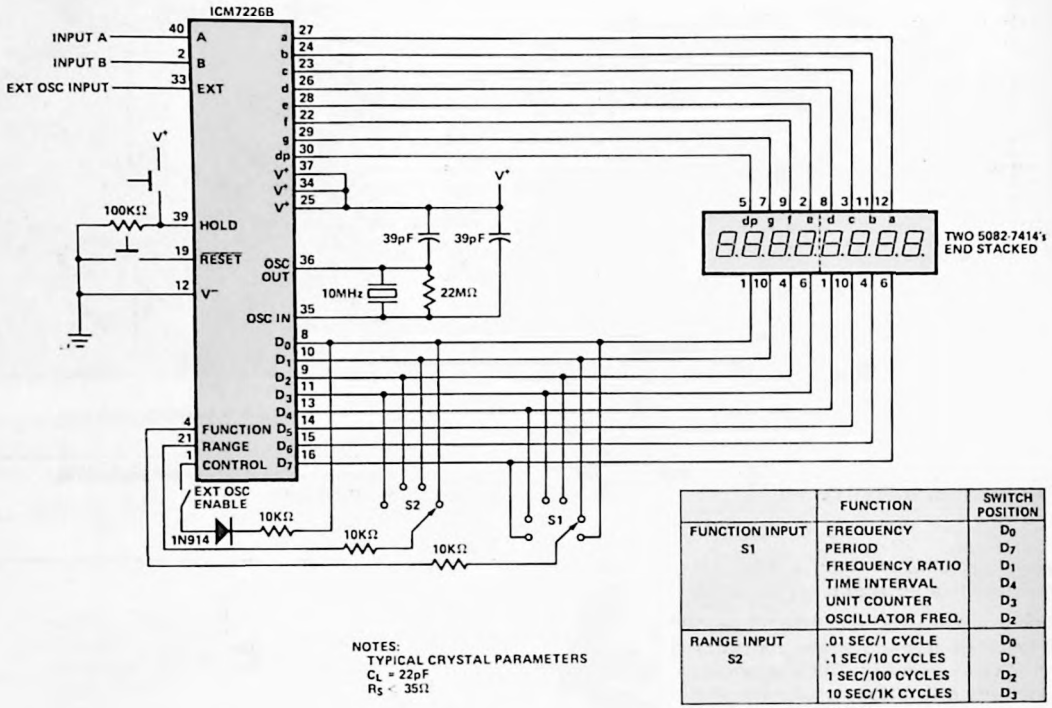


Figure 7. Typical Segment

TYPICAL APPLICATIONS

Figure 8 shows the complete circuitry for a minimum component universal counter. The Intersil ICM7226B is a fully integrated universal counter and LED display driver. It combines a high frequency oscillator, a decade time-base counter, an eight decade data counter with latches, a seven segment decoder, a digit multiplexer, and eight segment and eight digit drivers that drive monolithic LEDs directly. If the designer wishes to use the ICM7226A or B (common anode or cathode) to drive large seven segment products, he should consider his application carefully because higher drive currents are required to produce a readable display.

The ICM7226B updates the segment information and refreshes the common cathode displays at an I_{PEAK} of 15 mA/segment on a 12% duty cycle. This drive current is ideal for the monolithic seven segment family. The circuit in Figure 8 employs two 5082-7414 monolithic devices as the display portion of the counter. Typical devices will exhibit a 30 µcd time averaged luminous intensity, thus



	FUNCTION	SWITCH POSITION
FUNCTION INPUT S1	FREQUENCY	D_0
	PERIOD	D_7
	FREQUENCY RATIO	D_1
	TIME INTERVAL	D_4
	UNIT COUNTER	D_3
	OSCILLATOR FREQ.	D_2
RANGE INPUT S2	.01 SEC/1 CYCLE	D_0
	.1 SEC/10 CYCLES	D_1
	1 SEC/100 CYCLES	D_2
	10 SEC/1K CYCLES	D_3

Figure 8. 10 MHz Universal Counter

providing excellent readability. Combining the compactness of the monolithic displays and the complexity of the single chip universal counter system, an extremely powerful hand held instrument can be realized.

Figure 9 shows the circuitry necessary for a high performance, low power 3-1/2 digit panel meter. The circuit utilizes the Intersil ICL7107 (CMOS) A/D converter, seven passive components, and four large seven segment displays. All necessary active devices are contained on the chip. This includes seven segment decoders, display drivers, a reference voltage, and a clock.

The ICL7107 is designed to dc drive 3 seven segment displays and one overflow digit at a typical forward current of 8 mA per segment. The segment information is decoded and updated continuously by the control logic within the chip. The 7.6mm (0.3 inch) standard red displays (5082-7736/-7740) provide an attractive display for this low cost digital panel meter. For higher light output, the high efficiency red, yellow, or green displays can be used.

MICROPROCESSOR DISPLAY INTERFACE TECHNIQUES

The four basic techniques for interfacing microprocessors to seven segment displays are listed below:

1. The DC Driven Controller statically drives an LED seven segment display from a microprocessor output port. In the standard configuration, each display is assigned a different address so that a Memory or I/O Write to that address changes the contents of the corresponding display digit.
2. The Refresh Controller interfaces the microprocessor to a multiplexed LED display. The controller periodically interrupts the microprocessor and after each interrupt, the microprocessor supplies new display data for the next refresh cycle of the display.
3. The Decoded Data Controller refreshes a multiplexed LED display independently from the microprocessor system. The local RAM stores decoded display data. This data is continuously read from the RAM and then used to refresh the display. Whenever the display message is changed, the microprocessor decodes each character in software and writes the decoded data into the local RAM.
4. The Coded Data Controller also refreshes a multiplexed LED display independently from the microprocessor system. The local RAM stores BCD data which is continuously read, decoded, and used to refresh the display. The display message is changed by writing new BCD characters into the local RAM.

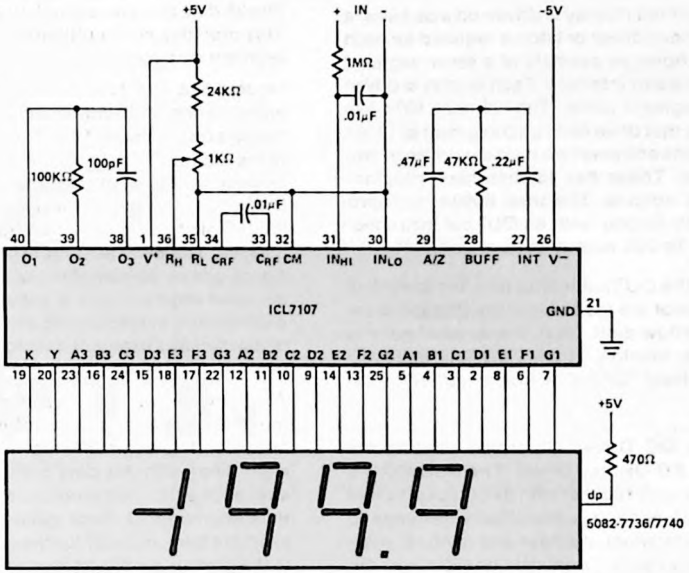
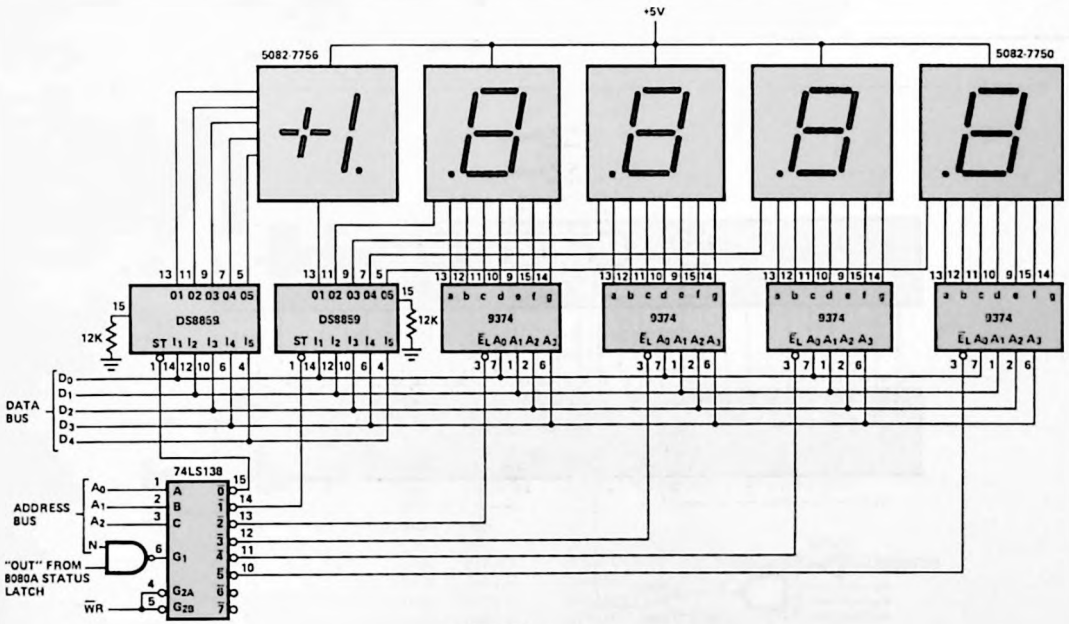


Figure 9. 3-1/2 Digit Voltmeter



X = DON'T CARE

	A_2	A_1	A_0	D_4	D_3	D_2	D_1	D_0
UPDATE OVERFLOW DIGIT	0	0	0	e	d	c	b	a
UPDATE DECIMAL POINT	0	0	1	dp5	dp4	dp3	dp2	dp1
UPDATE DIGIT 1	0	1	0	X	D	C	B	A
UPDATE DIGIT 2	0	1	1	X	D	C	B	A
UPDATE DIGIT 3	1	0	0	X	D	C	B	A
UPDATE DIGIT 4	1	0	1	X	D	C	B	A

Figure 10. DC Driven Controller

APPLICATIONS

DC DRIVEN CONTROLLERS

When the seven segment display is driven on a dc basis, a seven segment decoder/driver or latch is required for each display. Figure 10 shows an example of a seven segment display to microprocessor interface. Each display is driven by its own seven segment driver. The Fairchild 9374 has current sink outputs that drive each LED segment at 15 mA dc. The decimal points and overflow digit are driven by two National DS 8859's. These hex latches have programmable current sink outputs. The Intel 8080A microprocessor updates each display with an OUTput instruction which accesses up to 256 output devices and ports.

Upon execution of the OUTput instruction, the lower five bits of the accumulator are loaded into the DS8859 associated with the overflow digit. Next, the decimal point is updated in a similar fashion. Finally, the four decoder/drivers are sucessively loaded with the correct BCD information.

Figure 11 shows a DC Driven Controller utilizing the National MM5450 LED Display Driver. The MM5450 is a serial in-parallel out shift register with 34 output pins that can sink up to 15 mA each. It is specifically designed to operate with common anode displays and minimal interface with the source of data. Serial data transfer from the data source, in this case the microprocessor, to the display driver is accomplished with two signals. These signals are SERIAL DATA and CLOCK. By using a format of a leading "1" bit followed by the 35 data bits, data transfer is allowed without any additional handshaking signals. The 35 data bits are latched after the 36th bit is complete. This provides non-multiplexed, direct drive to the seven segment displays.

Figures 12a and 12b contain the software necessary to interface the MM5450 to the 6800 and 8080A microprocessors respectively. The serial display data is transferred to the microprocessor via bit 7 of the Data Bus. The data is clocked in each time the microprocessor writes to the MM5450. In the case of the 8080A, this is done with the I/O WRITE signal and a combination of lower ordered addresses. The 6800 accomplishes this task with the VMA signal and a combination of higher address bits. The decoded segment data is assumed to be in four successive memory bytes starting at location $0006. The format of the decoded segment data for all microprocessor interfaces in this note is shown in Figure 13.

The software first outputs a start bit to the MM5450. Next, the first digit's segment information is clocked into MM5450. The segment information is then rotated left eight times with this data being clocked into the display after each shift. This procedure is repeated for each digit, thus providing 33 clock pulses (the start bit plus (4x8) segment bits). In order for the segment data to be latched to the display, a complete set of 36 clocks must occur. For this reason, there are three dummy clocks at the end of the program. The term "dummy" is used because the data that is being clocked into MM5450 never appears on the seven segment display.

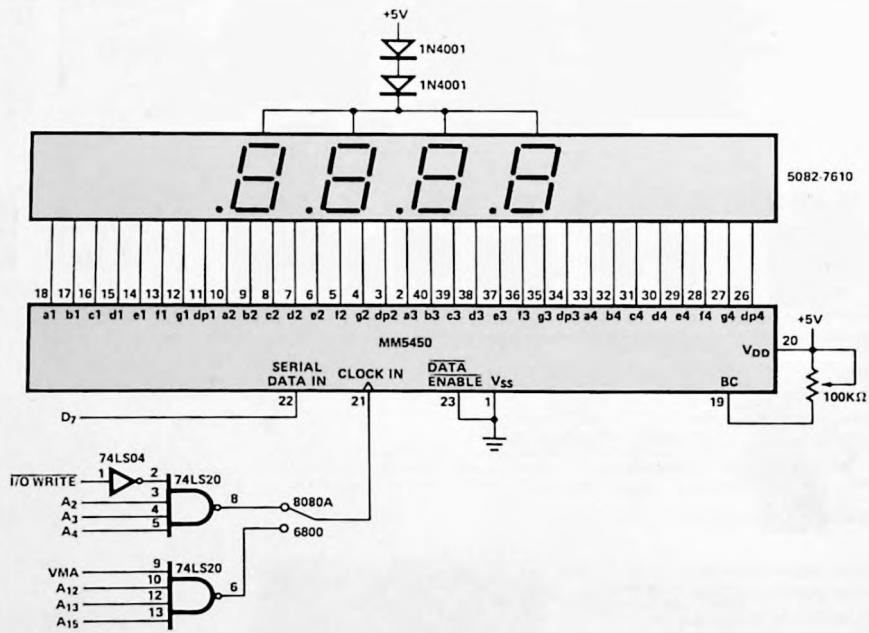


Figure11. DC Driven Controller with Serial Data Interface to 6800 and 8080A

```
                B0 00   DSPLY   EQU   $B000

0006                    DATA    ORG   $0006
0006                            RMB   $4

0400                            ORG   $0400
0400  CE 00 06    LOAD    LDX   I,DATA
0403  86 80              LDA A I,$80     LOAD START BIT
0405  B7 B0 00            STA A E,DSPLY OUTPUT START BIT
0408  C6 08        START   LDA B I,8     INITIALIZE COUNTER
040A  A6 00              LDA A X,0      LOAD DATA
040C  B7 B0 00    LOOP    STA A E,DSPLY OUTPUT DATA TO DISPLAY
040F  49                 ROL A          ROTATE TO NEXT BIT
0410  5A                 DEC B          DECREMENT COUNTER
0411  26 F9              BNE   LOOP     BRANCH IF NOT DONE, ELSE CONTINUE
0413  08                 INX
0414  8C 00 04           CPX   I,$04    LAST WORD?
0417  26 EF              BNE   START    BRANCH IF NOT LAST WORD, ELSE CONTINUE
0419  B7 B0 00            STA A E,DSPLY DUMMY CLOCK 1
041C  B7 B0 00            STA A E,DSPLY DUMMY CLOCK 2
041F  B7 B0 00            STA A E,DSPLY DUMMY CLOCK 3, SEG DATA LATCHED
0422  39                 RTS
```

Figure 12a. 6800 Interface to DC Drive Controller Shown in Figure 11

```
E000                    DSPLY   EQU   001CH

E000                            ORG   0E006H
E006                    DATA    DS    4

E00A                            ORG   0E400H
E400  3E 80        LOAD    MVI   A,80H    LOAD START BIT
E402  D3 1C                OUT   DSPLY    OUTPUT START BIT
E404  21 06 E0             LXI   H,DATA   GET ADDRESS OF SEG DATA
E407  06 08        START   MVI   B,08H    INITIALIZE COUNTER
E409  7E                   MOV   A,M      LOAD SEG DATA
E40A  D3 1C        LOOP    OUT   DSPLY    OUTPUT SEG DATA TO DISPLAY
E400  07                   RLC           ROTATE TO NEXT BIT
E40D  05                   DCR   B        DECREMENT COUNTER
E40E  02 0A E4             JNZ   LOOP     JUMP IF NOT DONE, ELSE CONTINUE
E411  2C                   INR   L
E412  7D                   MOV   A,L
E413  FE 0A                CPI   0AH      LAST WORD?
E415  C2 07 E4             JNZ   START    JUMP IF NOT LAST WORD, ELSE CONTINUE
E418  D3 1C                OUT   DSPLY    DUMMY CLOCK 1
E419  D3 1C                OUT   DSPLY    DUMMY CLOCK 2
E41C  D3 1C                OUT   DSPLY    DUMMYCLOCK 3, SEG DATA LATCHED
E41E  C9                   RET
```

Figure 12b. 8080A Interface to DC Driven Controller Shown in Figure 11

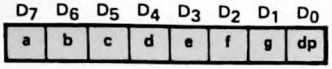


Figure 13. Format for Decoded Segment Data

The 5082-7610 7.6mm (0.3 inch) high efficiency red displays driven at 15 mA/segment dc provide a large, easy to read, four digit display. The 100 KΩ potentiometer sets a reference current for the LEDs and provides brightness control for applications in varying ambients.

REFRESH CONTROLLER

The Refresh Controller uses the microprocessor to actively strobe the display. This strobing is accomplished via an interrupt that causes the microprocessor to service the refresh subroutine. The refresh program provides new segment and digit information for the display. This application note shows two types of Refresh Controllers. The basic difference between the controllers is the nature of data that is transferred from the microprocessor to the controller. The first type (Figure 14) requires eight data lines to transfer the decoded segment and decimal point information. The second type of Refresh Controller (Figure 15) requires only five data lines to interface to the microprocessor. The data is transferred using BCD data and a decimal point bit. The technique for digit strobing also is slightly different due to the difference in display length.

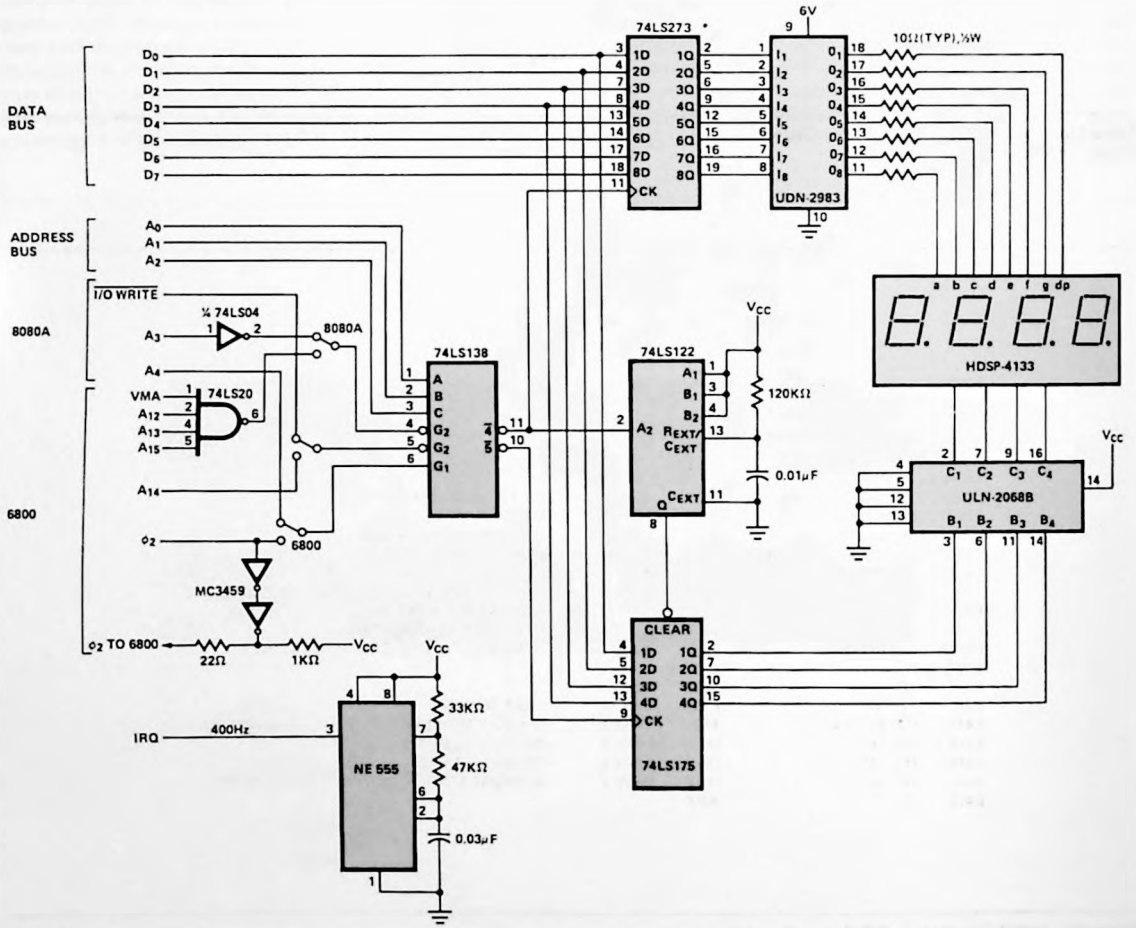


Figure 14. Sunlight Viewable Refresh Controller

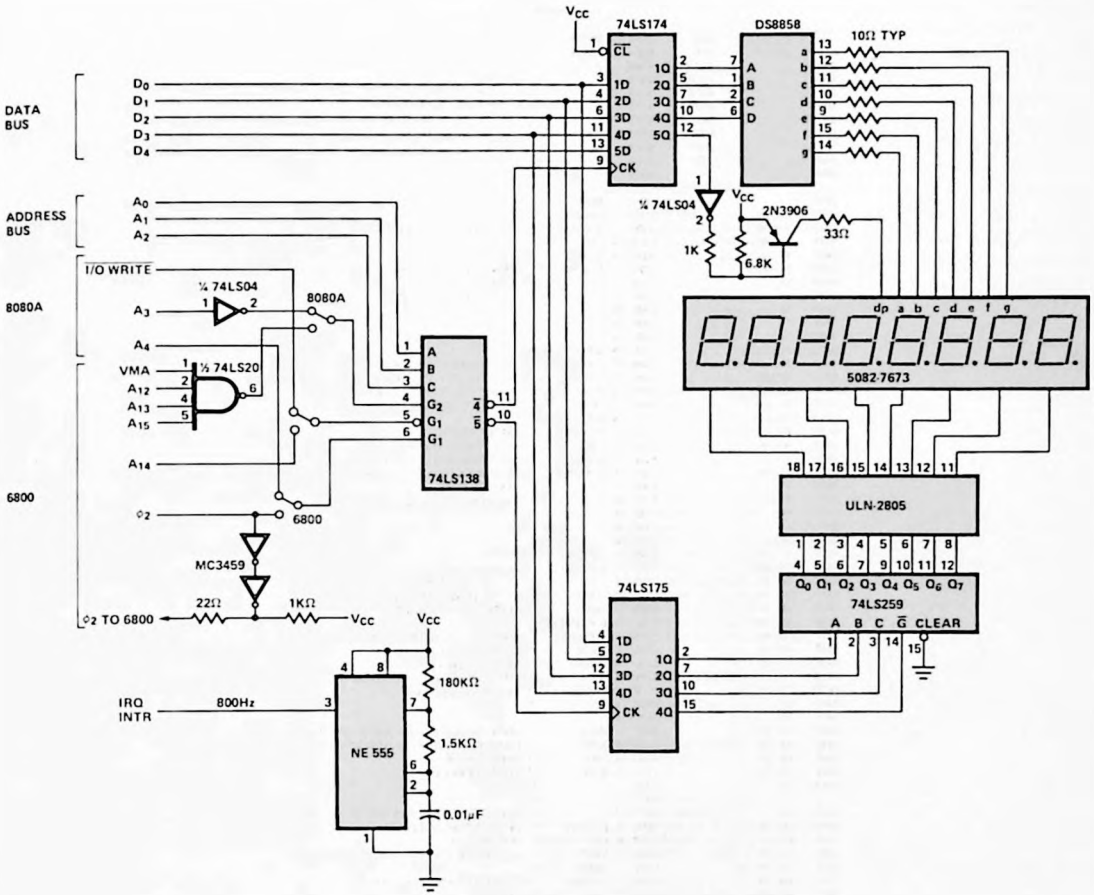


Figure 15. Refresh Controller

The circuit in Figure 14 utilizes the 10.9mm (0.43 inch) yellow HDSP-4133 seven segment displays. These displays are readable in direct sunlight when driven near the data sheet maximums as they are in Figure 14. The Sprague segment drivers are sourcing 120 mA peak on a 1/4 duty factor. The ULN-2068B can sink a maximum of 1.75A and therefore is an excellent digit driver as the maximum digit current is (120 mA) (8 segments) ≅ 1 Amp. The retriggerable monostable multivibrator (74LS122) senses strobing activity on the segment lines. If the strobing stops for any reason (microprocessor crash, etc.), the digit drivers are turned off immediately. This protects the displays from the 120 mA dc they would pass if the strobing ceased.

Figure 16a and 16b contain the software necessary to interface the Refresh Controller in Figure 14 to the 6800 and the 8080A microprocessors respectively. The programs consist of two subroutines. The first subroutine LOAD is called by the user's main program. LOAD should be called the first time data is to be displayed and any time when new display data is desired. This subroutine assumes the user has stored three consecutive bytes of BCD data and decimal point information in locations WORD1, WORD2, and DP. The subroutine unpacks the coded data stored in these locations, decodes it into segment data, and stores it in locations DD1, DD2, DD3, and DD4. Figure 16c graphically shows the effect of the subroutine LOAD.

LOAD uses a segment data lookup table located in ROM. The lookup table consists of sixteen successive locations that contain the segment information for displaying numbers 0-9 and letters A-F. A 1 bit corresponds to an ON segment and a 0 bit to an OFF segment. All dp bits have been programmed to a logical 0 in the lookup table. Subroutine LOAD assumes that only one decimal point will be ON in the four digit string. The code beginning with label DCPT determines which digit should display a decimal point and changes the dp bit to a logical 1. The subroutine is now complete and control returns to the main program.

```
                BF 04       SEG     EQU     $BF04
                BF 05       DIG     EQU     $BF05
0000                        POINT   RMB     2
0002                        DIGIT   RMB     1
0003                        WORD1   RMB     1
0004                        WORD2   RMB     1
0005                        DP      RMB     1
0006                        DD1     RMB     1
0007                        DD2     RMB     1
0008                        DD3     RMB     1
0009                        DD4     RMB     1

0400                        ORG     $0400
0400  CE 06 00      LOAD    LDX     I,$0600
0403  DF 00                 STX     D.POINT     INITIALIZE POINTER
0405  86 01                 LDA A   I,$01
0407  97 02                 STA A   D.DIGIT     INITIALIZE DIGIT
0409  96 03                 LDA A   D.WORD1     LOAD 2 BCD WORDS
040B  16                    TAB                 MAKE A COPY
040C  54                    LSR B               RIGHT JUSTIFY BCD1
040D  54                    LSR B
040E  54                    LSR B
040F  54                    LSR B
0410  D7 01                 STA B   D.POINT+1
0412  DE 00                 LDX     D.POINT     POINT TO DIGIT 1 SEG. DATA
0414  E6 00                 LDA B   X,0         LOAD DIGIT 1 SEG. DATA
0416  D7 06                 STA B   D.DD1       STORE DIGIT 1 SEG. DATA
0418  84 0F                 AND A   I,$0F       MASK LEAVING BCD2
041A  97 01                 STA A   D.POINT+1
041C  DE 00                 LDX     D.POINT     POINT TO DIGIT 2 SEG. DATA
041E  A6 00                 LDA A   X,0         LOAD DIGIT 2 SEG. DATA
0420  97 07                 STA A   D.DD2       STORE DIGIT 2 SEG. DATA
0422  96 04                 LDA A   D.WORD2     LOAD NEXT 2 BCD WORDS
0424  16                    TAB                 MAKE A COPY
0425  54                    LSR B               RIGHT JUSTIFY BCD3
0426  54                    LSR B
0427  54                    LSR B
0428  54                    LSR B
0429  D7 01                 STA B   D.POINT+1
042B  DE 00                 LDX     D.POINT     POINT TO DIGIT 3 SEG. DATA
042D  E6 00                 LDA B   X,0         LOAD DIGIT 3 SEG. DATA
042F  D7 08                 STA B   D.DD3       STORE DIGIT 3 SEG. DATA
0431  84 0F                 AND A   I,$0F       MASK LEAVING BCD4
0433  97 01                 STA A   D.POINT+1
0435  DE 00                 LDX     D.POINT     POINT TO DIGIT 4 SEG. DATA
0437  A6 00                 LDA A   X,0         LOAD DIGIT 4 SEG. DATA
0439  97 09                 STA A   D.DD4       STORE DIGIT 4 SEG. DATA
043B  96 05       DCPT      LDA A   D.DP        LOAD DIGIT THAT NEEDS DP (1, 2, 3, 4)
043D  CE 00 00              LDX     I,$0000     CLEAR INDEX REG
0440  08          INCR      INX
0441  4A                    DEC A
0442  26 FC                 BNE     INCR        LOOP TRANSFERS DP DATA TO INDEX REG
0444  A6 05                 LDA A   X,DP        LOAD THE SEG. DATA NEEDING DP
0446  8B 01                 ADD A   I,$01       GIVE IT A DP
0448  A7 05                 STA A   X,DP        STORE IT BACK
044A  39                    RTS

044B  0F          REFRSH    SEI                 DISABLE INTERRUPTS DURING REFRESH
044C  D6 02                 LDA B   D.DIGIT     FIND OUT WHICH DIGIT
044E  C1 01                 CMP B   I,$01       IS IT DIGIT 1?
0450  26 05                 BNE     NEST        BRANCH IF NOT FIRST, ELSE CONTINUE
0452  CE 00 06              LDX     I,$0006
0455  DF 00                 STX     D.POINT     INITIALIZE POINTER TO DD1
0457  86 00       NEST      LDA A   I,$00       CLEAR A
0459  B7 BF 05               STA A   E.DIG       BLANK DISPLAY
045C  DE 00                 LDX     D.POINT     POINT TO SEG. DATA
045E  A6 00                 LDA A   X,0         LOAD SEG. DATA
0460  B7 BF 04               STA A   E.SEG       OUTPUT SEG. DATA TO DISPLAY
0463  F7 BF 05               STA B   E.DIG       OUTPUT DIGIT DATA TO DISPLAY
0466  C1 08                 CMP B   I,$08       IS IT THE LAST DIGIT?
0468  27 08                 BEQ     LOOP1       BRANCH IF LAST, ELSE CONTINUE
046A  78 00 02              ASL     E.DIGIT     SHIFT TO NEXT DIGIT
046D  7C 00 01              INC     E.POINT+1   POINT TO NEXT SEG. DATA
0470  0E                    CLI                 RE-ENABLE INTERRUPTS
0471  3B                    RTI                 RETURN
0472  86 01       LOOP1     LDA A   I,$01       RE-INITIALIZE TO DIGIT 1
0474  97 02                 STA A   D.DIGIT
0476  0E                    CLI                 RE-ENABLE INTERRUPTS
0477  3B                    RTI                 RETURN

0600                        ORG     $0600
0600  FC                    FCB     $FC         0
0601  60                    FCB     $60         1
0602  DA                    FCB     $DA         2
0603  F2                    FCB     $F2         3
0604  66                    FCB     $66         4
0605  B6                    FCB     $B6         5
0606  3E                    FCB     $3E         6
0607  E0                    FCB     $E0         7
0608  FE                    FCB     $FE         8
0609  E6                    FCB     $E6         9
060A  EE                    FCB     $EE         A
060B  3E                    FCB     $3E         B
060C  9C                    FCB     $9C         C
060D  7A                    FCB     $7A         D
060E  9E                    FCB     $9E         E
060F  8E                    FCB     $8E         F
```

Figure 16a. 6800 Interface to Refresh Controller in Figure 14

```
E000                    SEG     EQU     00ICH
E000                    DIG     EQU     00IDH

E000                            ORG     0E000H
E000                    POINT   DS      2
E002                    DIGIT   DS      1
E003                    WORD1   DS      1
E004                    WORD2   DS      1
E005                    DP      DS      1
E006                    DD1     DS      1
E007                    DD2     DS      1
E008                    DD3     DS      1
E009                    DD4     DS      1

E00A                            ORG     0E400H
E400  21  00  E6        LOAD    LXI     H,0E600H
E403  22  00  E0                SHLD    POINT           INITIALIZE POINTER
E406  3E  01                    MVI     A,01H
E408  32  02  E0                STA     DIGIT           INITIALIZE DIGIT
E40B  3A  03  E0                LDA     WORD1           LOAD 2 BCD WORDS (BCD1, BCD2)
E40E  E6  F0                    ANI     0F0H            MASK OUT LOWER NIBBLE
E410  0F                        RRC                     RIGHT JUSTIFY BCD1
E411  0F                        RRC
E412  0F                        RRC
E413  0F                        RRC
E414  6F                        MOV     L,A             POINT TO DIGIT 1 SEG. DATA
E415  7E                        MOV     A,M             LOAD DIGIT 1 SEG. DATA
E416  32  06  E0                STA     DD1             STORE DIGIT 1 SEG. DATA
E419  3A  03  E0                LDA     WORD1           LOAD SAME 2 BCD WORDS (BCD1, BCD2)
E41C  E6  0F                    ANI     0FH             MASK OUT UPPER NIBBLE
E41E  6F                        MOV     L,A             POINT TO DIGIT 2 SEG. DATA
E41F  7E                        MOV     A,M             LOAD DIGIT 2 SEG. DATA
E420  32  07  E0                STA     DD2             STORE DIGIT 2 SEG. DATA
E423  3A  04  E0                LDA     WORD2           LOAD NEXT 2 BCD WORDS (BCD3, BCD4)
E426  E6  F0                    ANI     0F0H            MASK OUT LOWER NIBBLE
E428  0F                        RRC                     RIGHT JUSTIFY BCD3
E429  0F                        RRC
E42A  0F                        RRC
E42B  0F                        RRC
E42C  6F                        MOV     L,A             POINT TO DIGIT 3 SEG. DATA
E42D  7E                        MOV     A,M             LOAD DIGIT 3 SEG. DATA
E42E  32  08  E0                STA     DD3             STORE DIGIT 3 SEG. DATA
E431  3A  04  E0                LDA     WORD2           LOAD SAME 2 BCD WORDS (BCD3, BCD4)
E434  E6  0F                    ANI     0FH             MASK OUT UPPER NIBBLE
E436  6F                        MOV     L,A             POINT TO DIGIT 4 SEG. DATA
E437  7E                        MOV     A,M             LOAD DIGIT 4 SEG. DATA
E438  32  09  E0                STA     DD4             STORE DIGIT 4 SEG. DATA
E43B  3A  05  E0        DCPT    LDA     DP              LOAD DIGIT NEEDING DP
E43E  01  05  E0                LXI     B,0E005H        SET BC REG PAIR AS A POINTER
E441  03                INCR    INX     B               LOOP TRANSFERS DP DATA TO BC
E442  3D                        DCR     A
E443  C2  41  E4                JNZ     INCR
E446  0A                        LDAX    B               LOAD SEG. DATA NEEDING DP
E447  C6  01                    ADI     01H             GIVE IT A DP
E449  02                        STAX    B               STORE IT BACK
E44A  C9                        RET

E44B  F3                RFRSH   DI                      DISABLE INTERRUPTS
E44C  F5                        PUSH    PSW             SAVE ON STACK
E44D  E5                        PUSH    H
E44E  D5                        PUSH    D
E44F  3A  02  E0                LDA     DIGIT           FIND OUT WHICH DIGIT
E452  FE  01                    CPI     01H             LAST DIGIT?
E454  C2  5D  E4                JNZ     NEST            JUMP IF NOT FIRST, ELSE CONTINUE
E457  21  06  E0                LXI     H,0E006H        HL REG RE-INITIALIZED
E45A  22  00  E0                SHLD    POINT           POINT POINTS TO DD1
E45D  3E  00            NEST    MVI     A,00H
E45F  D3  1D                    OUT     DIG             BLANK DISPLAY
E461  2A  00  E0                LHLD    POINT           POINT POINTS TO SEG. DATA
E464  EB                        XCHG                    SWAP
E465  1A                        LDAX    D               LOAD SEG. DATA VIA DE PAIR
E466  EB                        XCHG                    SWAP BACK
E467  D3  1C                    OUT     SEG             OUTPUT SEG. DATA TO DISPLAY
E469  3A  02  E0                LDA     DIGIT           LOAD DIGIT DATA
E46C  D3  1D                    OUT     DIG             OUTPUT DIGIT DATA TO DISPLAY
E46E  FE  08                    CPI     08H             LAST DIGIT?
E470  CA  E4  80                JZ      LOOP1           JUMP IF LAST, ELSE CONTINUE
E473  07                        RLC                     ROTATE TO NEXT DIGIT
E474  32  02  E0                STA     DIGIT           STORE FOR NEXT DIGIT
E477  23                        INX     H               INCREMENT
E478  22  00  E0        LOOP2   SHLD    POINT           POINT POINTS TO NEXT SEG. DATA
E47B  D1                        POP     D               SAVE IT
E47C  E1                        POP     H
E47D  F1                        POP     PSW
E47E  FB                        EI                      ENABLE INTERRUPTS
E47F  C9                        RET                     RETURN
E480  3F  01            LOOP1   MVI     A,01H
E482  32  02  E0                STA     DIGIT           DIGIT POINTS TO DIGIT 1
E485  C3  78  E4                JMP     LOOP2

                                ORG     0E600
E600  FC                        DB      0FCH            0
E601  60                        DB      060H            1
E602  DA                        DB      0DAH            2
E603  F2                        DB      0F2H            3
E604  66                        DB      066H            4
E605  B6                        DB      0B6H            5
E606  3E                        DB      03EH            6
E607  E0                        DB      0E0H            7
E608  FE                        DB      0FEH            8
E609  E6                        DB      0E6H            9
E60A  EE                        DB      0EEH            A
E60B  3E                        DB      03EH            B
E60C  9C                        DB      09CH            C
E60D  7A                        DB      07AH            D
E60E  9E                        DB      09EH            E
E60F  8E                        DB      08EH            F
```

Figure 16b. 8080A Interface to Refresh Controller in Figure 14

APPLICATIONS

Upon interruption by the 555 timer, the microprocessor is vectored to service the routine RFRSH. This routine uses the register POINT to locate segment information (DD1, DD2, DD3 and DD4) to be output to the display. Label SEG is the address to which segment data is to be written. The label DIG is used in a similar manner to identify the address where digit data is to be written. RFRSH updates the display by first blanking all segments. This interdigit blanking eliminates the phenomenon of partially illuminated segments known as ghosting. Next, segment information is written to the octal latch (74LS273). Finally, the digit information is written to the quad latch (74LS175). Control is then returned to the main program. This process is repeated with the correct segment information for each of the four digits.

With proper display filtering, the circuit in Figure 12 controlled by either the 6800 or 8080A programs provides an excellent four digit, sunlight viewable display.

The Refresh Controller shown in Figure 15 is quite similar to the circuit in Figure 14. However, there are a few minor differences that should be pointed out. The Refresh Controller in Figure 15 utilizes the National DS8858 BCD-to-seven segment decoder driver. This enables the user to write BCD data to the Refresh Controller without utilizing the LOAD subroutine. This saves both RAM space and microprocessor time. The software to interface this Refresh Controller to the 6800 and the 8080A microprocessors is shown in Figures 17a and 17b respectively. The circuit uses the green 5082-7673 large seven segment common cathode displays.

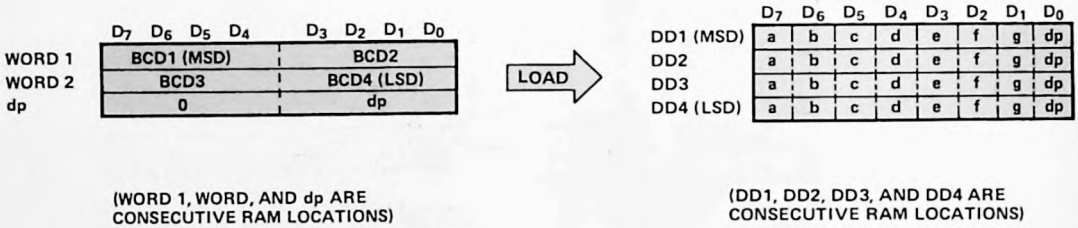


Figure 16c. Subroutine LOAD

```
         BF 04        SEG     EQU   $BF04
         BF 05        DIG     EQU   $BF04
0000                  POINT   RMB   2
0002                  DIGIT   RMB   1
0003                  DATA    RMB   8

0400                          ORG   $0400
0400     CE 00 03     INIT    LDX   I,$0003
0403     DF 00                STX   D,POINT     INITIALIZE POINT
0405     7F 00 02             CLR   E,DIGIT     INITIALIZE DIGIT
0408     0F           RFRSH   SEI               DISABLE INTERRUPTS
0409     DE 00                LDX   D,POINT     GET POINT
040B     E6 00                LDA   B X,0
040D     86 08                LDA   A I,$08
040F     B7 BF 05             STA   A E,DIG     BLANK DISPLAY
0412     F7 BF 04             STA   B E,SEG     OUTPUT SEG. DATA TO DISPLAY
0415     96 02                LDA   A D,DIGIT   GET DIGIT
0417     81 07                CMP   A I,$07
0419     27 0B                BEQ   LOOPI       BRANCH IF LAST DIGIT, ELSE CONTINUE
041B     7C 00 02             INC   E,DIGIT     INCREMENT TO NEXT DIGIT
041E     B7 BF 05             STA   A E,DIG     OUTPUT DIGIT DATA TO DISPLAY
0421     7C 00 01             INC   E,POINT+1   POINT POINTS TO NEXT BCD WORD
0424     0E                   CLI
0425     3B                   RTI
0426     B7 BF 05     LOOPI   STA   A E,DIG     OUTPUT DIGIT DATA TO DISPLAY
0429     CE 00 03             LDX   I,$0003
042C     DF 00                STX   D,POINT     RE-INITIALIZE POINT
042E     7F 00 02             CLR   E,DIGIT     RE-INITIALIZE DIGIT
0431     0E                   CLI
0432     3B                   RTI
```

Figure 17a. 6800 Interface to Refresh Controller Shown in Figure 15

```
E000                  SEG     EQU   001CH
E000                  DIG     EQU   001DH

E000                          ORG   0E000H
E000     03 E0        POINT   DW    DATA
E002                  DIGIT   DS    01H
E003                  DATA    DS    08H

E00B                          ORG   0E400H
E400     21 03 E0     INIT    LXI   H,0E003H
E403     22 00 E0             SHLD  POINT       INITIALIZE POINT
E406     3E 00                MVI   A,0
E408     32 02 E0             STA   DIGIT       INITIALIZE DIGIT
E40B     F3           RFRSH   DI                DISABLE INTERRUPTS
E40C     F5                   PUSH  PSW         SAVE
E40D     E5                   PUSH  H           SAVE
E40E     2A 00 E0             LHLD  POINT       GET POINT
E411     3E 08                MVI   A,08H
E413     D3 1D                OUT   DIG         BLANK DISPLAY
E415     7E                   MOV   A,M
E416     D3 1C                OUT   SEG         OUTPUT SEG. DATA TO DISPLAY
E418     3A 02 E0             LDA   DIGIT       GET DIGIT
E41B     D3 1D                OUT   DIG         OUTPUT DIGIT DATA TO DISPLAY
E41D     FE 07                CPI   07H
E41F     CA 2E E4             JZ    LOOPI       BRANCH IF LAST, ELSE CONTINUE
E422     3C                   INR   A
E423     32 02 E0             STA   DIGIT       INCREMENT TO NEXT DIGIT
E426     23                   INX   H
E427     22 00 E0     LOOP2   SHLD  POINT       POINT POINTS TO NEXT BCD WORD
E42A     E1                   POP   H
E42B     F1                   POP   PSW
E42C     FB                   EI                ENABLE INTERRUPTS
E42D     C9                   RET
E42E     3E 00        LOOPI   MVI   A,0
E430     32 02 E0             STA   DIGIT       RE-INITIALIZE DIGIT
E433     21 03 E0             LXI   H,0E003H    RE-INITIALIZE POINT
E436     C3 27 E4             JMP   LOOP2
```

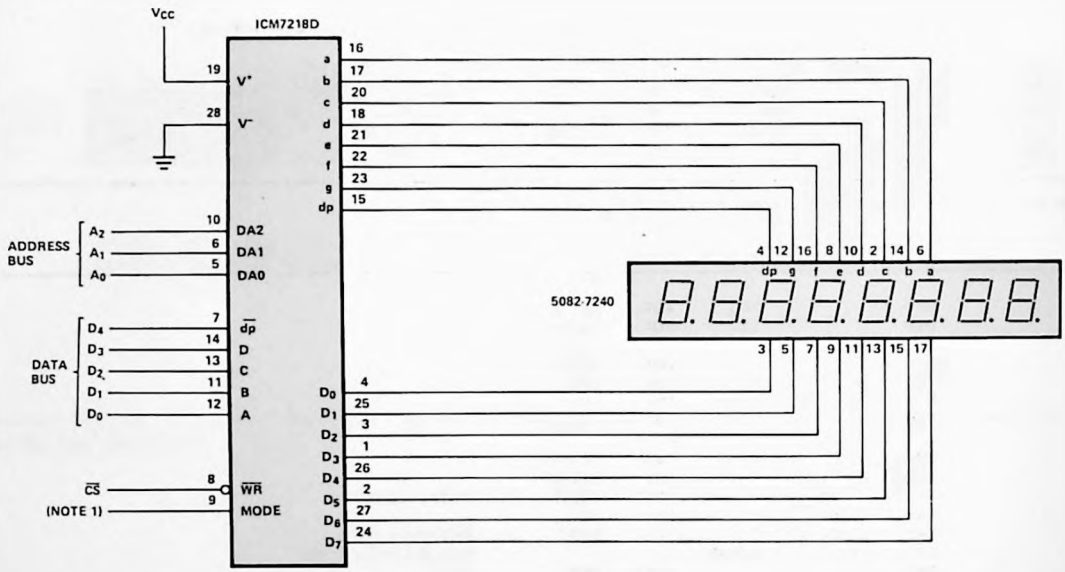
Figure 17b. 8080A Interface to Refresh Controller Shown in Figure 15

APPLICATIONS

CODED DATA CONTROLLER

Figure 18 shows a Coded Data Controller designed for an eight character monolithic seven segment display. The circuit uses the Intersil ICM7218D to provide BCD data storage and display multiplexing. The ICM7218D is designed to drive common cathode LED displays at 10 mA I_{PEAK}/segment (minimum) on a 12% duty cycle.

The circuit illustrated in Figure 18 uses the ICM7218D to drive an eight digit 5082-7240 monolithic LED display. The common anode version (ICM7218C) is rated at 20 mA I_{PEAK}/segment (minimum). If higher drive currents are needed and a four digit display is acceptable, the eight digit lines on the ICM7218D can be paralleled to drive four digits at twice the minimum current. The microprocessor interfaces to the ICM7218D through five Data Inputs (BCD and $\overline{dp}$), three digit address lines (DA0, DA1, and DA2), a MODE input, and a $\overline{WRITE}$ input. Data can be written in to the eight memory locations in the static memory of the ICM7218D via a three bit binary code on the digit address inputs. When the digit address lines are valid, a negative going $\overline{WRITE}$ pulse clocks the BCD and dp data into the RAM. This method of memory addressing allows the user to update the display information only where it is necessary.



(NOTE 1) MODE IS A TRISTATE INPUT SUCH THAT WHEN MODE = HIGH, THE 7218 PROVIDES HEXIDECIMAL DECODING; WHEN MODE = FLOATING, THE 7218 PROVIDES CODE B DECODING; AND WHEN MODE = LOW, THE 7218 BLANKS THE DISPLAY.

Figure 18. Coded Data Controller

DECODED DATA CONTROLLER

Figure 19 shows a Decoded Data Controller designed for use with 20.3mm (0.8 inch) seven segment displays. The circuit utilizes the National MM74C911 to directly drive four of the large seven segment displays. The MM74C911 is used to provide segment data storage and display multiplexing. The MM74C911 is designed to drive common cathode displays at 100 mA I_{PEAK}/segment on a 25% duty cycle. The circuit illustrated in Figure 17 uses the MM74C911 to drive four HDSP-3403 20.3 mm (0.8 inch) standard red common cathode displays.

The microprocessor interfaces to the MM74C911 through eight data lines (a, b, c, d, e, f, g, dp), two address inputs K_1 and K_2, $\overline{\text{CHIP ENABLE}}$, and $\overline{\text{WRITE ENABLE}}$. The desired segment data is written into the register selected by the address information when $\overline{\text{CE}}$ and $\overline{\text{WE}}$ are low. This data is latched when either $\overline{\text{CE}}$ or $\overline{\text{WE}}$ return high. Data hold time is not required.

An internal oscillator sequentially presents the stored data to the output drivers which directly drive the LED display. The drivers are active when the control pin labelled SEGMENT OUTPUT ENABLE ($\overline{\text{SOE}}$) is low, and are tri-stated when $\overline{\text{SOE}}$ is high. This feature allows duty cycle brightness control for varying ambient light conditions. Also, $\overline{\text{SOE}}$ can be used to disable the output drivers for power conservation. The digit outputs directly drive the base of the digit transistor when the control pin labelled DIGIT INPUT OUTPUT ($\overline{\text{DIO}}$) is low.

INTENSITY MATCHING

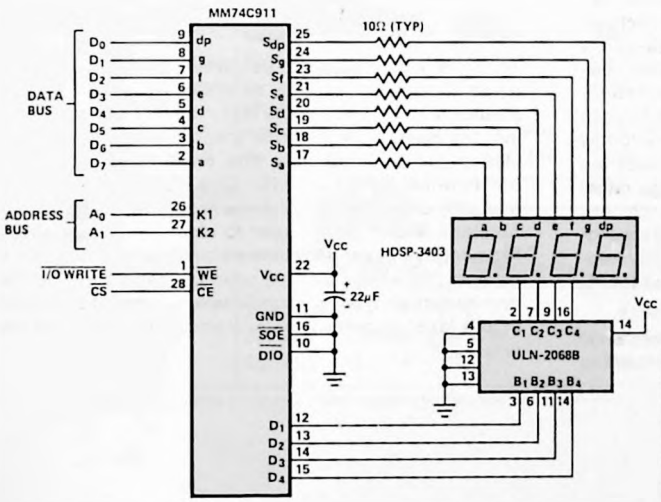
All Hewlett-Packard seven segment displays are tested for luminous intensity to ensure that data sheet values are met. All displays which can be end stacked are categorized according to their intensity levels. The eye can detect roughly a 2:1 change in luminous intensity and, therefore, this is the criterion for intensity categories. This categorization allows end stacking of the displays, thereby providing a panel with a pleasing, uniform appearance.

The large seven segment displays are individually tested and categorized for luminous intensity. The intensity category is designated by a single or double letter located on the right hand side of the package. When end stacking, it is preferable that the user choose devices from a single category to provide uniform intensity across the display panel.

The monolithic seven segment display clusters are inherently intensity matched digit to digit in one display package. The immersion type monolithic displays which are designed for end stacking are categorized for intensity. The category is designated by a letter on the back side of the package. The user should choose devices from a single category when end stacking the displays.

COLOR MATCHING

Color uniformity of the large seven segment displays is an important consideration. The standard red and high efficiency red displays have inherent color uniformity and need not be categorized. However, the eye is more sensitive to color differences in the yellow and green regions. Therefore, displays of these color types are categorized by dominant wavelength. This category is denoted by a number on the right hand side of the package. The user should choose units from a single category to achieve a display panel with optimal color uniformity.



INPUT CONTROL

$\overline{\text{CE}}$	DIGIT ADDRESS K2	DIGIT ADDRESS K1	$\overline{\text{WE}}$	OPERATION
0	0	0	0	WRITE DIGIT 1
0	0	0	1	LATCH DIGIT 1
0	0	1	0	WRITE DIGIT 2
0	0	1	1	LATCH DIGIT 2
0	1	0	0	WRITE DIGIT 3
0	1	0	1	LATCH DIGIT 3
0	1	1	0	WRITE DIGIT 4
0	1	1	1	LATCH DIGIT 4
1	X	X	X	DISABLE WRITING

X = DON'T CARE

OUTPUT CONTROL

$\overline{\text{DIO}}$	$\overline{\text{SOE}}$	DIGIT LINES D4	D3	D2	D1	OPERATION
0	0	R	R	R	R	REFRESH DISPLAY
0	1	R	R	R	R	DISABLE SEGMENTS
1	0	0	0	0	0	DIGITS ARE INPUTS
1	0	0	0	0	1	DISPLAY DIGIT 1
1	0	0	0	1	0	DISPLAY DIGIT 2
1	0	0	1	0	0	DISPLAY DIGIT 3
1	0	1	0	0	0	DISPLAY DIGIT 4
1	1	0	0	0	0	POWER SAVER MODE

R = REFRESH (DIGIT LINES SEQUENCIALLY PULSED)

Figure 19. Decoded Data Controller

APPLICATIONS

SUNLIGHT VIEWABILITY

The rapid growth of sophisticated electronic systems for use in avionic, automotive, machine, and military equipment has created the need for an electronic information display that is viewable in bright sunlight. By combining the newest LED product design technology and the most recent techniques for contrast enhancement, Hewlett-Packard can now provide the display system designer with devices that are useable in direct 107,000 lumens per square meter (10,000 foot candle) sunlight.

The HDSP-3530/-3730/-4030/-4130 series of large seven segment displays optimize the following parameters that contribute to the readability of the LED display in bright sunlight:

a. LED Color
b. Luminance Contrast
c. Chrominance Contrast (color difference)
d. Front Surface Reflections

These sunlight viewable display devices are assembled with Gallium Arsenide Phosphide (GaAsP) LED chips on a Gallium Phosphide (GaP) substrate. These materials produce the needed light output when driven with peak currents up to 120 mA. High current LED chips are used to allow high peak and average current in the display. The high efficiency red and yellow displays provide the most light output for a given input current and can easily be made visible in bright sunlight. The package configuration uses a neutral gray body and untinted segments to allow the display system designer to achieve readability by obtaining an optimum combination of both luminous and chrominance contrast. When placed behind a 20% to 25% neutral density gray filter, the illuminated segments provide a distinctly visible chrominance contrast with respect to the gray package.

MOUNTING CONSIDERATIONS

The large segment display devices are constructed utilizing a lead frame in a standard DIP package. All 7.6mm (0.3 inch) and 10.9mm (0.43 inch) displays are manufactured with leads on 2.54mm (0.10 inch) centers with a row-to-row spacing of 7.6mm (0.3 inch). The 20.3mm (0.8 inch) displays are also on 2.54mm (0.10 inch) centers but the row-to-row spacing is 15.2mm (0.6 inch). The 14.1mm (0.56 inch) displays are on 2.54mm (0.10 inch) centers with row-to-row spacing of 15.2mm (0.6 inch). However, the leads are aligned along the top and bottom of the package rather than down the sides. Both the 14.1mm (0.56 inch) and 20.3mm (0.8 inch) displays can be socketed using a standard 24 pin IC socket or strip sockets. All large seven segment devices are end stackable and are designed for PC board mounting and wave soldering.

If the large segment devices are to be wave soldered, Sn60 or Sn63 solder is recommended. The solder wave is recommended to be at 245° C with a dwell time of 1-1/2 to 2 seconds. The 20.3mm (0.8 inch) displays have a small tab at each corner to establish a 1mm (0.040 inch) seating plane above the printed circuit board. The other large seven segment displays have a shoulder on the lead frame to achieve a similar seating plane above the printed circuit board.

The non-immersion type monolithic displays may be mounted either by use of pins which may be soldered into the plated holes at the connector edge of the PC board or by insertion into a standard PC board connector (Table IV). The devices may be soldered for up to three seconds per tab at a maximum soldering temperature of 230°C. Heat should be applied only to the edge connector tab areas of the PC board. Heating other areas of the board to temperatures in excess of 85° C can result in permanent damage to the lens. It is recommended that a rosin core wire solder or a low temperature deactivating flux and solid wire be used in soldering operations.

The immersion type monolithic displays are designed for insertion into 12 or 14 pin DIP sockets or soldering into PC boards. All of these type of displays are manufactured on 2.54mm (0.100 inch) centers with a row-to-row spacing of 7.6mm (0.300 inch). If the displays are to be soldered into a PC board, the solder temperature must be kept at or below 245° C, 1/16 inch below the seating plane, for a maximum of five seconds. The shoulders of the lead frame pins are intentionally raised above the bottom of the package so that the display can be mounted at an angle to the PC board. Mounting angles up to 20° are often necessary in hand held or desk top applications and are easily attainable with immersion type monolithic displays. Refer to Application Note 937 for further instructions concerning installation of these devices.

LED displays, as well as all electronic components, operate more reliably at lower temperatures. Thermal considerations are important, and any method of cooling or heat sinking the displays will result in more reliable operation. Under no conditions should the absolute maximum temperature ratings be exceeded.

To optimize device optical performance, specially developed plastics are used in all display products. These plastics restrict the solvents that may be used for cleaning. Tests have demonstrated that the only fluorocarbon cleaner that is compatible with plastic LED devices is trichloro-fluoroethane (F113). This cleaner is sold commercially under the trade names Freon, Genesolv D, and Arkalone. Water can be used to clean both large seven segment displays and the immersion lens type monolithic displays. Water can also be used for hand cleaning the non-immersion type monolithic seven segment displays if care is taken to prevent water from collecting under the lens.

TABLE I. BCD to Seven Segment Decoder/Drivers

Part Number	Vendor*	Output Structure	Output Current	Output Active State	Features
74LS47	TI, Fairchild, National	Open Collector	24 mA	Low	Auto Zero-Blanking, Lamp Test, 0-9
74LS48	TI, Fairchild, National	2K Pull-Up	6 mA	High	Auto Zero-Blanking, Lamp Test, 0-9
74LS49	TI, National	Open Collector	8 mA	High	Auto Zero-Blanking, Lamp Test, 0-9
8T04	Signetics	Open Collector	40 mA	Low	Auto Zero-Blanking, Lamp Test, 0-9
8T06	Signetics	Open Collector	40 mA	High	Auto Zero-Blanking, Lamp Test, 0-9
9368	Fairchild	Open Emitter	-19 mA	High	Constant Current, Latch, Auto Zero-Blanking, 0-9, A-F
9370	Fairchild	Open Collector	40 mA	Low	Latch, Auto Zero-Blanking, 0-9, A-F
9384	Fairchild	Current Mirror	15 mA	Low	Constant Current, Latch, Auto Zero-Blanking, 0-9, E,H,C,D
DS8669	National	Open Collector	25 mA	Low	2 Digit (14 Outputs), 0-9, C,A,P,E,H,J,L,F,-
MC14511	Motorola	NPN Bipolar Emitter	-25 mA	High	Latch, Lamp Test, Blanking Input, 0-9
MC14547	Motorola	NPN Bipolar Emitter	-65 mA	High	Latch, Blanking Input, 0-9

*This is a partial list of vendors. Other suppliers for the same part may exist.

TABLE II. Display Drivers

Part Number	Vendor*	Number of Drivers	Input Compatibility	Output Current (mA)	Features
DS8859	National	6	TTL	0-40 (Max)	Programmable Constant Current
DS8867	National	8	7V MOS	-14 (Typ)	Constant Current
DS8877	National	6	MOS, TTL	50 (Typ)	Low Current Version of 75492
DS8874/76/79	National	9	9V MOS	50 (Min)	Serial Input, Low Battery Indicator
ULN-2031/33	Sprague	7	TTL, 5V-15V CMOS	±80 (Max)	NPN or PNP Darlington Pair
75497/498	TI	7	MOS, TTL	125 (Max)	
75492	TI, Fairchild, Motorola, National	6	9 MOS	250 (Max)	Darlington Pair
DS8870	National	6	9V MOS	350 (Max)	
DS8863/8963	National	8	9V MOS	500 (Max)	
ULN-2003A (MC1413)	Sprague, TI Motorola	7	TTL, 5V CMOS	500 (Max)	2.7 kΩ Series Resistance to Darlington Pair
ULN-2981A	Sprague	8	TTL, 5V CMOS	-500 (Max)	
ULN-2068B	Sprague	4	TTL, 5V CMOS	1500 (Max)	Predriver Stage to Darlington Pair

1 OF N DECODERS

Part Number	Vendor*	Number of Drivers	Input Compatibility	Output Current (mA)	Features
74LS259	TI, Signetics	8	TTL	8 (Max)	Active High, Four Mode Operation
DS8665	National	14	9V MOS	-20 (Max)	Active Low, Oscillator Output
NE590	Signetics	8	TTL	250 (Max)	Active Low, Four Mode Operation

*This is a partial list of vendors. Other suppliers for the same part may exist.

TABLE III. Multifunction Display Drivers

COUNTERS

Part Number	Vendor	Function	Drive Conditions
MM74C925/6/7/8	National	CMOS counter with internal output latch and self-contained internal oscillator and scanning circuitry	4 Digit Common Cathode 40 mA pk (typ) 1 of 4 D.F.
MK50395-9	MOSTEK	Six decade counter/display decoder; look ahead carry or borrow, loadable counter	6 Digit Common Anode segment and digit drivers required
MK5002/517	MOSTEK	Four decade counter, latch, decoder with leading zero blanking	4 Digit Common Anode or Common Cathode segment and digit drivers required
ICM7217 ICM7227	Intersil	CMOS up/down counter, presettable start/count and compare register; for hard-wired microprocessor control applications; cascadable	4 Digit Common Cathode (A,C) 12.5 mA pk (typ), 10 mA pk (min) 1 of 4 D.F. Four Digit Common Anode (B) 40 mA pk (typ), 25 mA pk (min) 1 of 4 D.F.
ICM7208	Intersil	Seven decade counter with scanning circuitry, display blanking, reset	7 Digit Common Cathode 15 mA pk (typ) 1 of 8 D.F.
ICM7225	Intersil	High speed (25 MHz typ) counter/ decoder/driver	4-1/2 Digit Common Anode 8 mA dc (typ), 5 mA dc (min)
ICM7216 ICM7226	Intersil	Universal Counter that measures frequency, period, frequency ratio, time interval, units	8 Digit Common Anode (A/C) 35 mA pk (typ), 25 mA pk (min) 1 of 8 D.F. 8 Digit Common Cathode (B/D) 15 mA pk (typ), 10 mA pk (min) 1 of 8 D.F.
ZN1040E	Ferranti Packard	Universal Up/Down Synchronous Counter, with separate memory latches, look ahead or borrow, internal oscillator, and scanning circuitry	4 Digit Common Anode or Common Cathode 80 mA pk (typ), 50 mA pk (min) 1 of 4 D.F.

DISPLAY CONTROLLERS

Part Number	Vendor	Function	Drive Conditions
8279 8279-5	Intel	Programmable Keyboard/Display Interface; scanned keyboard, sensor mode, strobed input mode, right or left entry mode	16 Digit Common Anode or Common Cathode segment and digit drivers required
MM74C912 (BCD-7 Segment) MM74C917 (Binary-Hex)	National	Display Controller Driver with 6 x 8 RAM, internal oscillator and scanning circuit, internal segment decoder	6 Digit Common Cathode 100 mA pk (typ), 60 mA pk (min) 1 of 4 D.F.
MM74C911	National	Expandable Segment Display Controller with 4 x 8 RAM, self-contained internal oscillator and scanning circuit	4 Digit Common Cathode 100 mA pk (typ), 60 mA pk (min) 1 of 4 D.F.
MM5450 MM5451	National	Serial Input Display Driver; two line interface to microprocessor, continuous brightness control, data enable	39 or 35 Segment Common Cathode 25 mA dc (max), 15 mA dc (min)
ICM7218	Intersil	Display driver system with 8 x 8 memory; Hex decode, code B, or no decode	8 Digit Common Anode (A, C, E) 25 mA pk (typ), 20 mA pk (min) 1 of 8 D.F. 8 Digit Common Cathode (B) 25 mA pk (typ), 10 mA pk (min) 1 of 8 D.F.
ICM7212	Intersil	Display Decoder Driver	4 Digit Common Anode 8 mA dc (typ), 5 mA dc (min)

CLOCKS AND STOPWATCHES

Part Number	Vendor	Function	Drive Conditions
ICM7045A	Intersil	Complete industrial stopwatch, precision decade timer to count seconds, minutes or hours by relation of suitable oscillatory frequencies	7 Digit Common Cathode 15 mA pk (typ), 10 mA pk (min) 1 of 8 D.F.
ICM7215	Intersil	Split and Taylor time stopwatch circuit	6 Digit Common Cathode 13.2 mA pk (typ), 9 mA pk (min) 1 of 8 D.F.
S1998A1B	AMI	Digital Alarm Clock with snooze and sleep timer	4 Digit Common Anode 16 mA dc (typ)
MSM5523	OKI	Multifunction clock and radio, frequency counter; five time modes, four frequency modes, AM/FM indicator	4-1/2 Digit Common Anode or Common Cathode segment and digit drivers required
MSM5929	OKI	Auto Clock; 12 or 24 hour format, blinking colon, leading zero blanking	4 Digit Common Anode or Common Cathode segment and digit drivers required

TABLE III. Multifunction Display Drivers (Continued)

A/D CONVERTERS

Part Number	Vendor	Function	Drive Conditions
ICL7107	Intersil	A/D Converter with decoder/drivers and clock	3-1/2 Digit Common Cathode 8 mA dc (typ), 5 mA dc (min)
ADD3501/3701	National	DVM with pulse modulation A-D conversion, internal or external clock overflow displayed	3-1/2 Digit Common Cathode 50 mA pk (typ) 1 of 4 D.F. digit drivers required
LD130	Siliconix	CMOS A/D Converter; BCD outputs	3-1/2 Digit Common Anode or Common Cathode required BCD-7 segment decoder and digit drivers

TABLE IV. Connectors for Non-Immersion Lens Monolithic Seven Segment Displays

Vendor	Part Number	Description
Teledyne Kinetics 410 South Cedros Avenue P.O. Box 427 Solano Beach, CA 92075 (714) 755-1181	Model S4050 Model S4200	Glass filled thermoplastic polyester with spring contacts. Parallel and 90° mounting as well as high and low profile available. Model S4200 is available with up to 40 contacts.
Precision Concepts, Inc. 1595B Ocean Avenue Bohemia, NY 11716 (516) 567-0995	1255 90-1255	Snapper connector. Any number of contacts can be supplied on a strip with any of the following angles from horizontal (0°, 45°, 60°, 90°). Solder plug pins also available.
William Prym-Werke KG 519 Stolberg/Rheinland (02402) 14331/14465	Specify Contact Pin	Contact pin with knurling. Standard dimensions with special designs done on request.
J.A.V. Manufacturing, Inc. 125 Wilbur Place Bohemia, NY 11716 (516) 567-9030	Series 022-002	Snap in friction fit. Available in 30° angle from horizontal. Up to 17 contacts. Solder plug pins also available.

TABLE V. Filter Materials

LED Color	Panelgraphic	SGL Homalite	3M Company	Glarecheq	Rohm and Haas	Schott	OCLI	Polaroid
Standard Red	Ruby Red 60 Dark Red 63 Purple 90	H100-1600 H100-1605 H100-1804 (Purple)	R6510 P7710	Spectrafilter 112 Spectrafilter 118	Plexiglass 2423 Oroglass 2414	RG-645 RG-630		
High Efficiency Red	Scarlet Red 65 Neutral Gray 10	H100-1670	R6310 N0220 (Neutral Gray)	Spectrafilter 110 Spectrafilter 105 (Neutral Gray)		RG-610	Sunguard™ (Neutral Gray)	HNCP10 (Neutral Gray)
Yellow	Yellow 27 Neutral Gray 10	H100-1720	A5910 N0220 (Neutral Gray)	Spectrafilter 106 Spectrafilter 105 (Neutral Gray)			Sunguard™ (Neutral Gray)	HNCP10 (Neutral Gray)
Green	Green 48 Neutral Gray 10	H100-1440	G5610 N0220 (Neutral Gray)	Spectrafilter 107 Spectrafilter 105 (Neutral Gray)			Sunguard™ (Neutral Gray)	HNCP10 (Neutral Gray)

Addresses for companies listed above.

Panelgraphic Corporation
10 Henderson Drive
West Caldwell, NJ 07006
(201) 227-1500

SGL Homalite
11 Brookside Drive
Wilmington, DE 19804
(302) 652-3686

3M Company
Visual Products Division
3M Center, Bldg. 220-10W
St. Paul, MN 55101
(612) 733-0128

Glarecheq
Chequers Engraving Ltd.
1-4 Christina Street
London EC2A P4A
England
(01) 739-6964

Rohm and Haas
Independence Mall West
Philadelphia, PA 19105
(215) 592-3000

Schott Optical Glass
Duryea, PA 13642
(717) 457-7485

Optical Coating Labs, Inc. (OCLI)
2789 Griffen Avenue
Santa Rosa, CA 95401
(707) 545-6440

Polaroid Corporation
Polarizer Division
20 Ames Street
Cambridge, MA
(617) 577-2000/3655

HEWLETT PACKARD

APPLICATION NOTE 1007

Bar Graph Array Applications

INTRODUCTION

The need for converting analog information into a visual display exists in many applications. Historically, the designer has had two possible solutions: the traditional panel meter or discrete indicators aligned in an array. There are serious drawbacks with both solutions. Analog panel meters with inherently mechanical movements have been plagued with low tolerance for mechanical shock. Also, there is a strong customer demand for a more aesthetically pleasing display medium. Discrete indicators cause problems due to high parts count, difficult mechanical and optical alignment, as well as intensity and color variations across a display panel. Hewlett-Packard has solved many of these typical problems by introducing the HDSP-4820/-4830/-4840 series of 10 element LED bar graph arrays. The 10 element bar graph array series, available in standard red, high efficiency red, and yellow, offers the designer ultimate flexibility and ease of use in designing a display system.

This application note begins with a description of the manufacturing process used to construct the 10 element array. Next is a discussion of the package design and basic electrical configuration and how they affect designing with the bar graph array. Mechanical information including pin spacing and wave soldering recommendations are made.

Display interface techniques of two basic types are thoroughly discussed. The first of these two drive schemes is applicable in systems requiring display of analog signals in a bar graph format. The second major drive technique interfaces bar graph arrays in systems where the data is of a digital nature. Examples of microprocessor controlled bar graph arrays are presented.

Summarized for the design engineer are tables of available integrated circuits for use with bar graph arrays. Finally, a list of recommended filters is included.

DEVICE CHARACTERISTICS

The 10 element bar graph array devices are manufactured using the concept of "stretching" the light from an LED by diffusion and reflection as shown in Figure 1. The LED chips are mechanically supported and electrically connected by a lead frame. The plastic housing, called a "scrambler", contains reflective cavities which act as light pipes. These cavities are filled with a diffusant epoxy to provide uniform illumination at the emitting surface.

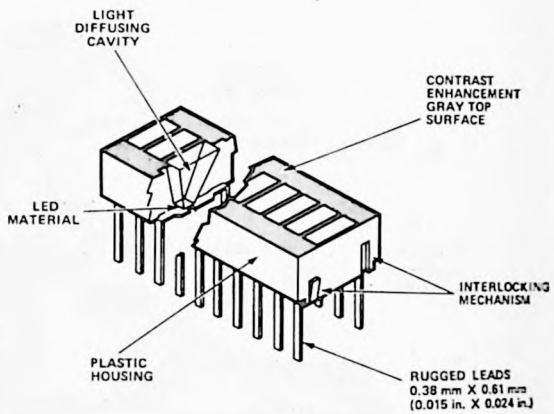


Figure 1. 10 Element Bar Graph (Cutaway)

All bar graph arrays are manufactured in standard DIP packages with leads on 2.54 mm (0.100 inch) centers with a row-to-row spacing of 7.6 mm (0.300 inch). As shown in the device schematic in Figure 2, each LED anode and cathode is present on external pins for ease of use.

Each of the 10 elements within the device is matched for luminous intensity. The effect of this matching is that users of a single ten element array need not worry about element-to-element matching within the package. The average luminous intensity for the device is coded by a letter on the side of the package. In applications requiring two or more bargraph arrays end stacked, the user merely chooses devices from a single light intensity category to provide uniform brightness across the display panel.

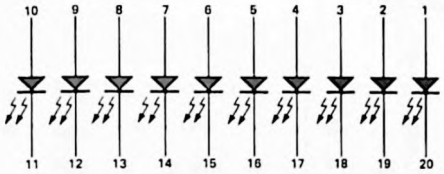


Figure 2. 10 Element Bar Graph Array Schematic

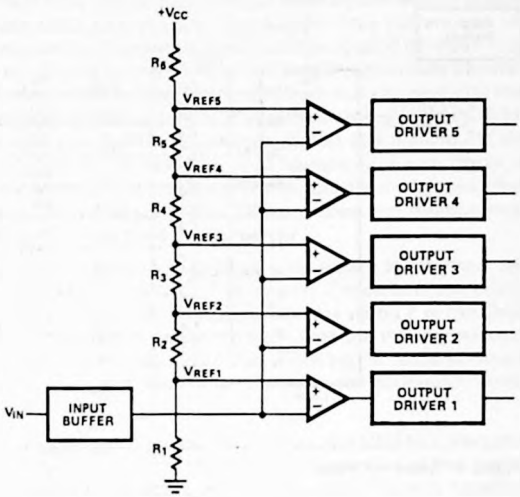
Color uniformity of the bar graph arrays is an important consideration. The standard red and high efficiency red displays have inherent color uniformity and need not be categorized. However, the eye is more sensitive to color differences in the yellow region. Therefore, the yellow bar graph arrays are categorized by dominant wavelength. These categories are coded by a number on the side of the package. The user should choose units from a single color category to achieve a display panel with optimal color uniformity.

The bar graph arrays have a neutral gray top surface and untinted segments to ensure maximum color difference between on and off segments. To maximize contrast enhancement, specially developed filters should be used in conjunction with the bar graph arrays. A list of recommended filters is contained in Table I.

The bar graph arrays offer substantial improvement over discrete devices in the area of mechanical alignment. Because the ten light emitting cavities are molded in a single package, element-to-element consistency as well as mechanical and optical alignment are vastly improved. The package also has a unique interlocking mechanism that eases alignment in applications requiring arrays to be end stacked.

If the bar graph arrays are to be wave soldered, Sn60 or Sn63 Solder is recommended. The solder wave temperature should be no greater than 260°C with a maximum dwell time of 3 seconds. The devices have a 1 mm (0.040 inch) standoff which provides clearance above the printed circuit board to facilitate flux removal.

To optimize optical performance, specifically developed plastics are used in the bar graph arrays. These plastics restrict the solvents that may be used for cleaning. It is recommended that only mixtures of Freon (F113) and alcohol be used for vapor cleaning processes. The immersion time in the vapors should be less than two (2) minutes. Some suggested vapor cleaning solvents are Freon TE, Genesolv DI-15 or DE-15, Arklone A or K. A 60°C (140°F) water cleaning process may also be used, which includes a neutralizer rinse (3% ammonia solution or equivalent), a surfactant rinse (1% detergent solution or equivalent), a hot water rinse and a thorough air dry. Room temperature cleaning may be accomplished with Freon T-35 or T-P35, Ethanol, Isopropanol or water with a mild detergent.



$V_{IN} > V_{REF1}$ OUTPUT DRIVER 1 ENABLED
$V_{IN} > V_{REF2}$ OUTPUT DRIVERS 1, 2 ENABLED
$V_{IN} > V_{REF3}$ OUTPUT DRIVERS 1, 2, 3 ENABLED
$V_{IN} > V_{REF4}$ OUTPUT DRIVERS 1, 2, 3, 4 ENABLED
$V_{IN} > V_{REF5}$ OUTPUT DRIVERS 1, 2, 3, 4, 5 ENABLED

Figure 3. Typical Analog Input Bar Graph Decoder

ANALOG INPUT INTERFACE TECHNIQUES

Many applications for bar graph arrays are in systems where the analog signal needs to be displayed with little or no conditioning. Several analog input IC decoders are available from different manufacturers and are listed in Table II. Although these decoders differ somewhat from manufacturer to manufacturer, the principle upon which they all operate is the same. A block diagram of a typical five element analog input bar graph decoder is shown in Figure 3. Within each IC is a reference voltage network and a set of comparators to detect the level of the analog input signal. When the input signal is greater than the reference voltage for the first comparator, the first output is enabled. As the input signal is increased, subsequent outputs are also enabled. Some manufacturers have incorporated two types of input signal decoding. The first type of decoding turns on all LEDs with voltage thresholds below the analog input (standard bar graph). The second type of decoding turns on only one output at any given time. When the analog input lies within the active region of a particular comparator ($V_{REF\ N} \leq V_{IN} < V_{REF\ N+1}$), that output is enabled and all others are disabled. This is known as position indicator mode. Since only one LED is on at any time in the position indicator mode, power dissipation is significantly reduced. Examples of both types of decoding are discussed in this section.

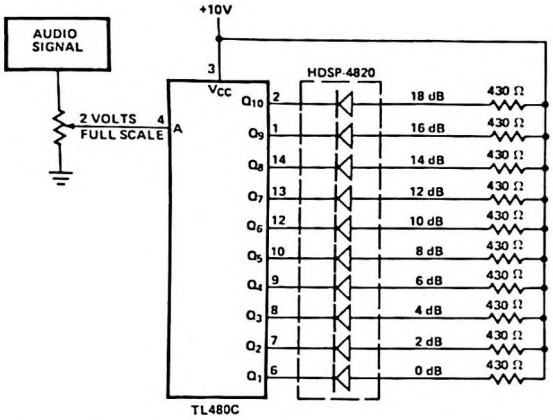


Figure 4. Audio VU Meter

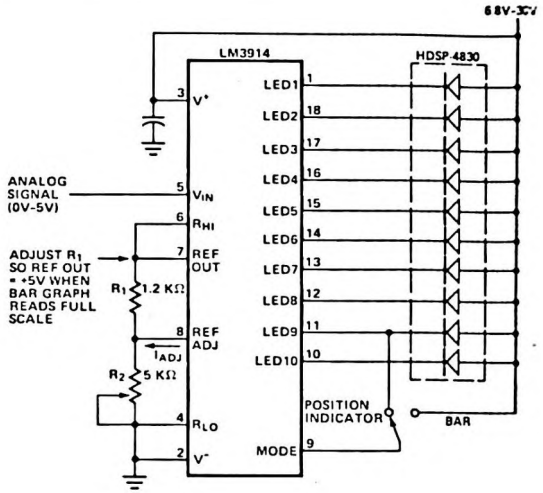


Figure 5. 0V-5V Bar Graph/Position Indicator Meter

The circuit shown in Figure 4 uses the Texas Instruments TL480C and the HDSP-4820 to form a low cost audio system VU meter. The ten comparators combined with the voltage reference network within the TL480C detect the level of an analog input signal at the A input. Output Q1 is switched to a logic low at a typical input voltage of 203 millivolts. Due to the logarithmic scaling within the part, as the input signal is increased by 2 dB increments, the subsequent outputs are switched to logic low levels and the LEDs are illuminated. If the TL480C is set to display full scale when the analog input is at 2.0 volts, 0 dB to 18 dB can be displayed on the bar graph array.

The circuit shown in Figure 5 utilizes the National LM3914 and the HDSP-4830 to form a flexible, ten element bar graph. The LM3914 is a versatile decoder in that it can operate in two distinct modes. The state of MODE (pin 9) determines the display format. When it is tied directly to V_{CC} (pin 3), full bar graph decoding occurs. But when MODE is tied to pin 11 the LM3914 operates in position indicator mode. This MODE pin can also be used to cascade additional LM3914s to form bar graphs of greater resolution.

The circuit in Figure 5 displays a 0V to 5V signal on the HDSP-4830 high efficiency red bar graph array. The full scale reading is determined by the adjustable voltage at the REF OUT node. The LM3914 forces a nominal 1.25V constant voltage between REF OUT (pin 7) and REF ADJ (pin 8). In Figure 5 this voltage is applied across resistor R1. Since this voltage is constant, a constant current flows through R1 giving an output voltage REF OUT as calculated below.

$$\text{REF OUT} = 1.25V\ (1 + R2/R1) + I_{ADJ}(R2)$$

The value of R1 also determines the LED current. Approximately ten times the current that flows from REF OUT (pin 7) is drawn by each lighted LED. The calculation of LED current is shown below.

$$I_{LED} = (1.25V/R1)\ (10)$$

Therefore, by choosing R1 for the desired LED brightness, and using the value of I_{ADJ} stated in the LM3914 data sheet (75 μA typical), R2 can be determined. By using a potentiometer for R2, the value of REF OUT can be adjusted to the precise level desired.

The LED current in Figure 5 has been set nominally to 10 mA DC using the techniques described above. When operated in position indicator mode with V_{CC} = 6.8V, the power dissipation is approximately 110 mW. The worst case power dissipation when operated in bar mode (10 elements on) is approximately 720 mW.

If low power dissipation and full bar graph decoding is desired, the LM3914 can be operated as shown in Figure 6. The LM3914 is again operated in position indicator mode. However, the ten LEDs are driven in series from a +24V power supply. The REF OUT voltage is adjusted so the bar graph reads +5V full scale. When V_{IN} lies between 0V and +0.5V, no LEDs will be on. When V_{IN} lies between +0.5V and +1.0V, Output 1 is enabled and LED 1 is illuminated. Each time the input voltage increases 0.5V, the 10 mA sink moves to the next output pin, illuminating an additional LED. When the input voltage is +5V or more (+35V maximum), all ten LEDs are illuminated with the same 10 mA. To the observer the bar graph appears to operate identically to the one in Figure 5 when in BAR mode. However, the worst case power dissipation has been reduced by approximately one half to 380 mW.

DIGITAL INPUT INTERFACE TECHNIQUES

Many applications for bar graph arrays are in digital systems. While the data being displayed may relate directly to an analog signal, it often will be converted to a digital format for processing. This conversion can be accomplished by a microprocessor and/or dedicated hardware. Several interface techniques that have been developed for displaying this

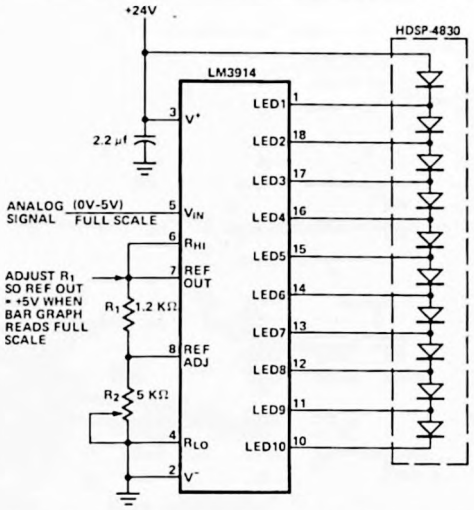


Figure 6. Low Power 0V-5V Bar Graph Meter

digitized data in bar graph form are covered in this section. A list of digital input integrated circuits suitable for use as bar graph drivers is compiled in Table III.

Binary Coded Decimal (BCD) is one commonly used method for coding display data in digital systems. Figures 7 and 8 contain circuits designed for interfacing BCD systems to a ten element bar graph. In each case a 1-of-10 decoder (7442) is used to convert the BCD information to the display format. The circuit in Figure 7 drives the bar graph in position indicator mode. That is, only the one LED corresponding to the BCD input is on at any one time. The circuit in Figure 8 has additional hardware to provide a true bar graph display. Therefore, when any output is decoded and turned on, that LED and all the LEDs below it are illuminated. The circuits in Figures 7 and 8 use the HDSP-4840 yellow bar graph with the forward current set nominally at 10 mA DC.

Figure 9 shows a thirty element, DC driven bar graph array utilizing the National MM5450 LED Display Driver. The circuit uses 3 HDSP-4830 high efficiency red bar graphs end stacked to form the display portion of the circuit. The MM5450 is a serial in-parallel out shift register with 34 output pins that can sink up to 15 mA each. This current can be adjusted by an external potentiometer applied between V_{DD} (pin 20) and Brightness Control (pin 19). Serial data transfer from the data source, in this case the microprocessor, to the display driver is accomplished with the two signals SERIAL DATA and CLOCK. By using a format of a leading "1" bit followed by 35 data bits, data transfer is allowed with a minimal hardware interface. The 35 data bits are latched after the 36th bit is complete. This provides non-multiplexed, direct drive to the bar graph array.

Figure 10 contains the software necessary to interface the MM5450 to the 6800 microprocessor. The serial display data is transferred from the microprocessor via bit 7 of the Data Bus. The data is clocked in each time the microprocessor writes to the MM5450. The clocking is accomplished through a combination of higher order addresses, R/W, VMA and ϕ_2.

The software first outputs a start bit to the MM5450. Next, the binary number corresponding to the number of bar graph elements to be displayed is loaded from memory location BINARY. This value is subtracted from $34_{10} = 22_H$, leaving the number of OFF elements to be clocked. These OFF bits are clocked first, followed immediately by the ON bits. Finally, the 36th clock pulse is generated, and the bar graph is illuminated. This display will remain illuminated without the need for microprocessor interaction until the data needs changing.

The user should ensure that the correct number of clock pulses are always applied to the MM5450. If this condition is violated once, the bar graph will display erroneous data until it is reset. Due to the lack of an external reset pin on the MM5450, the chip must then be turned off and subsequently repowered to reset and initialize correctly.

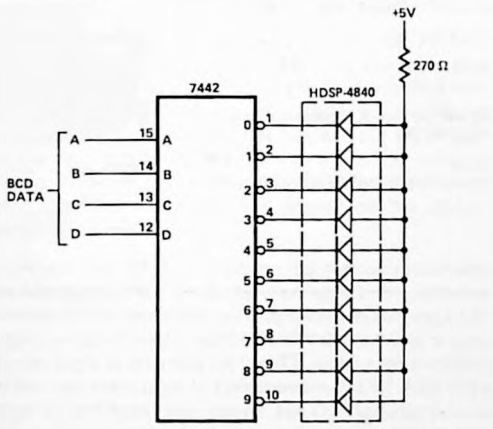


Figure 7. 1 of 10 Position Indicator

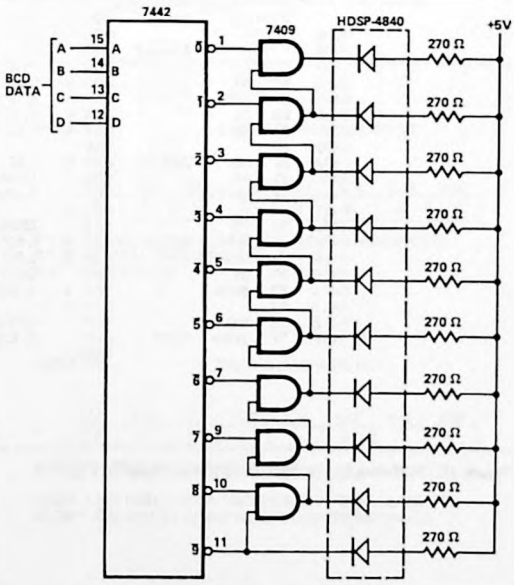


Figure 8. BCD to 10 Element Bar Graph Array

APPLICATIONS

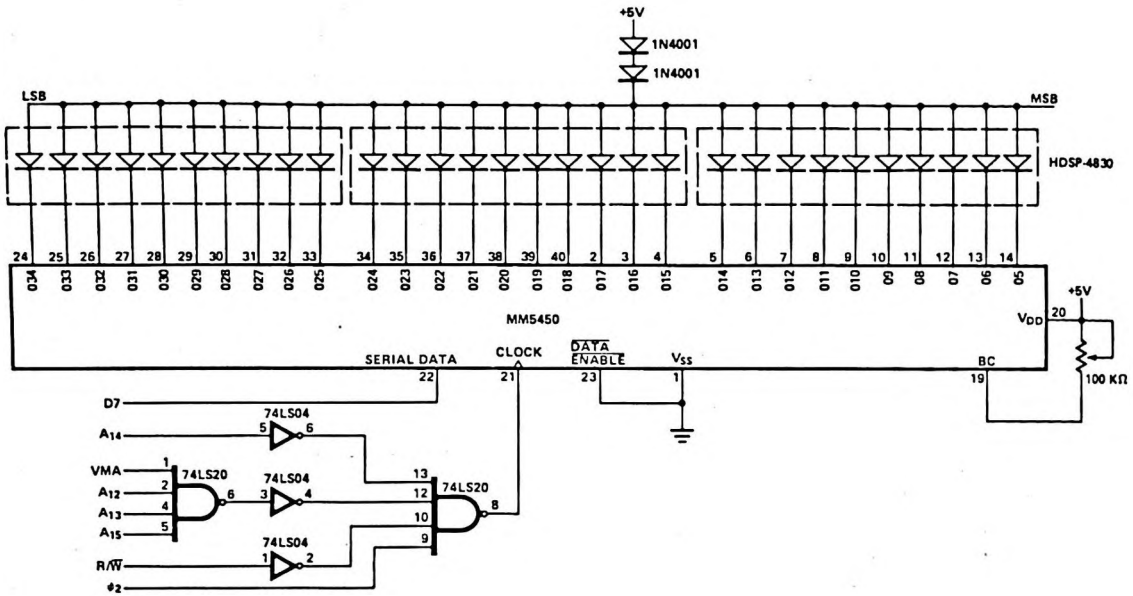


Figure 9. Serial Data Interface Between 6800 and 30 Element Bar Graph Array

```
                        ASMB, A, L
        B000    DSPLAY  EQU     $B000
0006            ORG     $0006
0006            BINARY  RMB     $1          NUMBER OF ELEMENTS ON (30₁₀ = 1E_H OR LESS)
0400            ORG     $0400
0400  86  80            LDA A   I, $80
0402  B7  B000          STA A   E, DSPLY    OUTPUT START BIT
0405  D6  06            LDA B   D, BINARY   GET BINARY
0407  86  22            LDA A   I, $22
0409  10                SBA                 DETERMINE NUMBER OF ZEROS
040A  81  00    ZEROS   CMP A   I, $0       NO ZEROS THEN BRANCH, ELSE CONTINUE
040C  27  06            BEQ     ONES
040E  7F  B000          CLR     E, DSPLY    OUTPUT ZERO
0411  4A                DEC A
0412  20  F6            BRA     ZEROS       LOOP
0414  86  80    ONES    LDA A   I, $80      LOAD ONES
0416  C1  00            CMP B   I, $00
0418  27  07            BEQ     QUIT        BRANCH IF DONE, ELSE CONTINUE
041A  B7  B000          STA A   E, DSPLY    OUTPUT ONE
041D  5A                DEC B
041E  7E  0416          JMP     ONES + 2    LOOP
0421  7F  B000  QUIT    CLR     E, DSPLY    FINAL CLOCK, DATA LATCHED
                        END
```

Figure 10. Software to Interface 6800 to the Circuit in Figure 9.

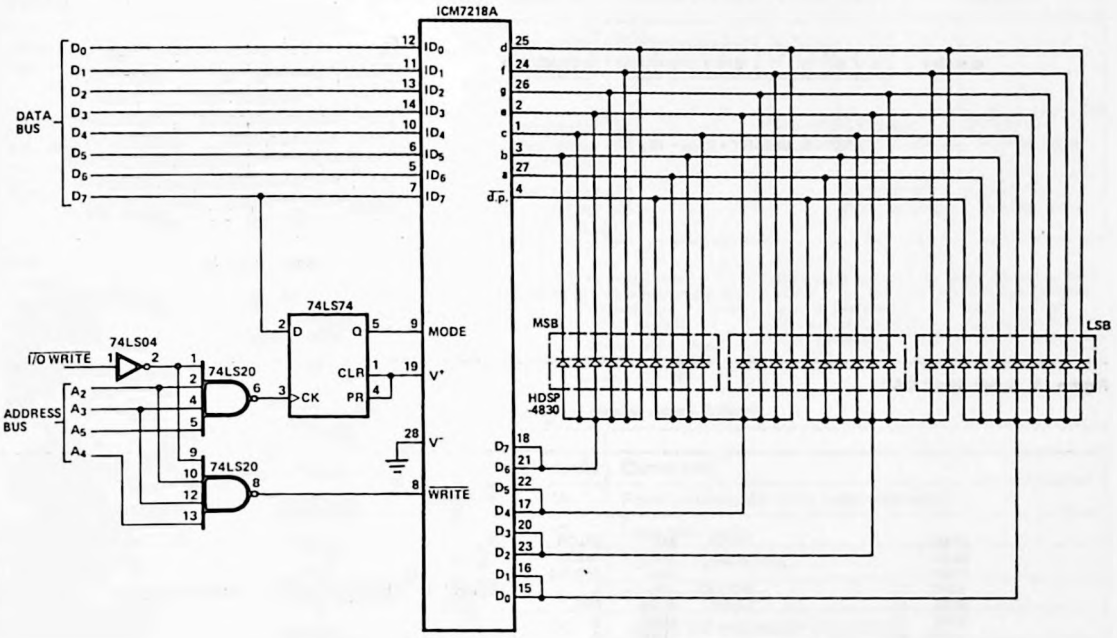


Figure 11. Parallel Data Interface Between 8080A and 30 Element Bar Graph Array

Figure 11 shows an 8080A microprocessor to bar graph interface utilizing the Intersil ICM7218A. This display driver has an 8 x 8 static RAM to store display data, sourcing and sinking drivers, and refresh timing for interfacing up to 64 LED elements to a microprocessor. However, the ICM7218A drives these elements at 20 mA $I_{PEAK/ELEMENT\ (MINIMUM)}$ on a 12% duty factor which may result in unacceptably low average current and brightness. For this reason, the eight digit drivers are paralleled in pairs in Figure 11. This results in a thirty element bar graph array operating at 20 mA $I_{PEAK/SEGMENT\ (MINIMUM)}$ with a duty factor of 24%.

The software to interface the 8080A to the ICM7218A is shown in Figure 14. With the MODE input at a logic, high WRITE is pulsed low. This clocks a control word from the data bus to the ICM7218A. This control word is decoded as described in Figure 12. Inputs ID_4, ID_5, and ID_7 are all logic highs which initialize the device into the proper mode of operation. This means that the next eight data words that are clocked into the ICM7218A will appear on the strobed outputs.

Memory location BINARY contains the number of elements in the bar graph that are to be illuminated. The software converts this information to bar graph form by rotating a 1 bit through the accumulator until BINARY decrements to zero. Since the logic is inverted for the $\overline{d.p.}$ output, an exclusive OR mask has been used to complement this bit. Also since the digit drivers have been paired, two OUTput instructions are required for each byte decoded. The software is graphically depicted in Figure 13. When the ICM7218A has received nine words (control word and eight data words), the information is displayed on the bar graph. This bar graph array will remain illuminated without the need for microprocessor interaction until the data needs changing.

MODE = 1 CONTROL WORD FORMAT

ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
1	X	1	C	X	X	X	X

C = 0 BLANK DISPLAY (RAM CONTENTS UNCHANGED)
C = 1 NORMAL OPERATION
X = DON'T CARE

MODE = 0 DATA WORD FORMAT

ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
$\overline{d.p.}$	a	b	c	e	g	f	d

UNCODED SEGMENT INFORMATION

LOGIC 1 REPRESENTS AN ON SEGMENT FOR ALL INPUTS EXCEPT $\overline{d.p.}$, WHERE LOGIC 0 REPRESENTS AN ON $\overline{d.p.}$

Figure 12. MODE and DATA Words for the ICM7218A

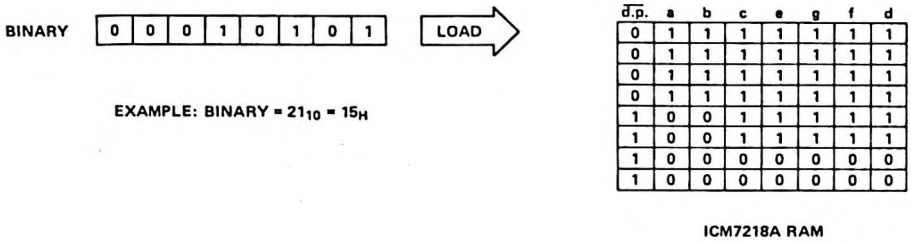


Figure 13. Subroutine LOAD

```
001C                        DSPLY   EQU     001CH
002C                        MODE    EQU     002CH
0000                                ORG     0E000H
E000  01                    BINARY  DB      1           ;NUMBER OF ELEMENTS ON (30₁₀ = 1E_H OR LESS)
E001  F5                    LOAD    PUSH    PSW
E002  C5                            PUSH    B
E003  E5                            PUSH    H
E004  3E F0                         MVI     A, 0F0H
E006  D3 2C                         OUT     MODE        ;MODE IS ONE
E008  D3 1C                         OUT     DSPLY       ;CLOCK CONTROL WORD
E00A  3E 00                         MVI     A, 00H
E00C  D3 2C                         OUT     MODE        ;MODE IS ZERO
E00E  06 08                         MVI     B, 08H      ;BIT COUNTER
E010  0E 04                         MVI     C, 04H      ;BYTE COUNTER
E012  21 00 E0                      LXI     H, BINARY   ;GET BINARY
E015  7E                            MOV     A, M
E016  FE 00                         CPI     00
E018  CA 33 E0              JZ      LOOP 1      ;JUMP IF ZERO, ELSE CONTINUE
E01B  3E 00                 CLEAR   MVI     A, 00
E01D  37                    SET     STC         ;SET CARRY
E01E  17                            RAL         ;ROTATE ONE BIT
E01F  35                            DCR     M
E020  CA 33 E0                      JZ      LOOP 1      ;JUMP IF ZERO, ELSE CONTINUE
E023  05                            DCR     B           ;DECREMENT BIT COUNTER
E024  C2 1D E0                      JNZ     SET         ;JUMP IF NOT ZERO, ELSE CONTINUE
E027  EE 80                         XRI     80H         ;COMPLEMENT BIT 7
E029  D3 1C                         OUT     DSPLY       ;CLOCK DISPLAY
E02B  D3 1C                         OUT     DSPLY       ;CLOCK DISPLAY
E02D  0D                            DCR     C           ;DECREMENT BYTE COUNTER
E02E  06 08                         MVI     B, 08H      ;RESET BIT COUNTER
E030  C3 1B E0                      JMP     CLEAR       ;START NEW BYTE
E033  EE 80                 LOOP 1  XRI     80H         ;COMPLEMENT BIT 7
E035  D3 1C                         OUT     DSPLY       ;CLOCK DISPLAY
E037  D3 1C                         OUT     DSPLY       ;CLOCK DISPLAY
E039  0D                            DCR     C           ;DECREMENT BYTE COUNTER
E03A  CA 42 E0                      JZ      QUIT        ;JUMP IF ZERO, ELSE CONTINUE
E03D  3E 80                         MVI     A, 80H      ;ENSURE BIT 7 CORRECT
E03F  C3 35 E0                      JMP     LOOP 1 + 2
E042  E1                    QUIT    POP     H
E043  C1                            POP     B
E044  F1                            POP     PSW
E045  C9                            RET
E046                                END
```

Figure 14. Software to Interface 8080A to the Circuits in Figure 11.

Table I. Filter Materials

LED Color	Panelgraphic	SGL Homalite	3M Company	Glarecheq	Rohm and Haas	Schott	OCLI	Polaroid
Standard Red	Ruby Red 60 Dark Red 63 Purple 90	H100-1600 H100-1605 H100-1804 (Purple)	R6510 P7710	Spectrafilter 112 Spectrafilter 118	Plexiglass 2423 Oroglass 2414	RG-645 RG-630		
High Efficiency Red	Scarlet Red 65 Neutral Gray 10	H100-1670	R6310 N0220 (Neutral Gray)	Spectrafilter 110 Spectrafilter 105 (Neutral Gray)		RG-610	Sunguard™ (Neutral Gray)	HNCP10 (Neutral Gray)
Yellow	Yellow 27 Neutral Gray 10	H100-1720	A5910 N0220 (Neutral Gray)	Spectrafilter 106 Spectrafilter 105 (Neutral Gray)			Sunguard™ (Neutral Gray)	HNCP10 (Neutral Gray)

Addresses for companies listed above.

Panelgraphic Corporation
10 Henderson Drive
West Caldwell, NJ 07006
(201) 227-1500

SGL Homalite
11 Brookside Drive
Wilmington, DE 19804
(302) 652-3686

3M Company
Visual Products Division
3M Center, Bldg. 220-10W
St. Paul, MN 55101
(612) 733-0128

Glarecheq
Chequers Engraving Ltd
1-4 Christina Street
London EC2A P4A
England
(01) 739-6964

Rohm and Haas
Independence Mall West
Philadelphia, PA 19105
(215) 592-3000

Schott Optical Glass
Duryea, PA 13642
(717) 457-7485

Optical Coating Labs, Inc. (OCLI)
2789 Griffen Avenue
Santa Rosa, CA 95401
(707) 545-6440

Polaroid Corporation
Polarizer Division
20 Ames Street
Cambridge, MA
(617) 577-2000/3655

Table II. Analog Input Bar Graph Array Drivers

Part Number	Vendor*	Drive Conditions	Scale	Elements	Comments
UAA170	Siemens	≤ 50 mA DC	External	16	Position indicator only, user sets scale
UAA180	Siemens	10 mA DC (typ)	External	12	User sets scale
TL489	TI	≤ 40 mA DC	Linear	5	200 mV increments
TL487	TI	≤ 40 mA DC	Log	5	3 dB increments
TL490	TI	≤ 40 mA DC	Linear	10	50-200 mV adjustable increments
TL480	TI	≤ 40 mA DC	Log	10	2 dB increments
TL491	TI	≤ -25 mA DC	Linear	10	50-200 mV adjustable increments
TL481	TI	≤ -25 mA DC	Log	10	2 dB increments
LM3914	National	2 ≤ I ≤ 30 mA DC	Linear	10	Position indicator/bar option
LM3915	National	2 ≤ I ≤ 30 mA DC	Log	10	Position indicator/bar option
LM3916	National	2 ≤ I ≤ 30 mA DC	Log	10	Position indicator/bar option
U237B	AEG-Tel.	20 mA (typ)	Linear	5	200 mV increments (200 mV-1000 mV)
U244B	AEG-Tel.	20 mA (typ)	Linear	5	180 mV increments (200 mV-1000 mV with overlap)
U247B	AEG-Tel.	20 mA (typ)	Linear	5	200 mV increments (100 mV-900 mV)
U254B	AEG-Tel.	20 mA (typ)	Linear	5	100 mV increments (110 mV-900 mV with overlap)
U257B	AEG-Tel.	20 mA (typ)	Log	5	-15 dB to +6 dB
U267B	AEG-Tel.	20 mA (typ)	Log	5	-20 dB to +3 dB
XR-2277	Exar	≤ 18 mA DC	Log	12	-30 dB to +6 dB, position indicator/bar option
XR-2278	Exar	≤ 18 mA DC	Log	12	-20 dB to +8 dB, position indicator/bar option
XR-2279	Exar	≤ 18 mA DC	Log	12	3 dB increments, position indicator/bar option

*This is a partial list of vendors. Other suppliers may exist.

Table III. Digital Input Bar Graph Drivers

Part Number	Vendor*	Drive Conditions	Elements	Comments
MM74C911	National	100 mA pk, 25% DF	32	Software decode, parallel interface
MM5450/51	National	≤ 15 mA DC	34/35	Software decode, serial interface
ICM7218A	Intersil	20 mA pk, 12% DF	64	Common Anode, software decode, parallel interface
8243	Signetics	13 mA DC	8	n of 8 decoder
7442	TI, Fairchild, et al	16 mA DC	10	1 of 10 decoder

HEWLETT PACKARD

APPLICATION NOTE 1008

Optical Sensing for the HEDS-1000

Introduction

The rapid growth of the digital processing used in commercial, industrial and consumer products, has created the need for sensors that convert physical parameters into electrical signals which may directly interface to a digital system. Optical sensors have utility in each of these areas, in that they provide a quick non-contact response to the parameters sought as a data source. Commercial applications include bar code scanning, paper edge sensing, end of tape sensing, and position and magnetic tape loop stabilizing. Industrial uses may consist of optical tachometry, assembly line monitoring, and safety interlocks, while the consumer uses of the optical sensor may be found in audio products, entertainment products, and video games.

This application note describes the electrical and optical design considerations for using discrete optoelectronic devices, or the HEDS-1000 High Resolution Optical Reflective Sensor. The application areas addressed include non-contact transmittive, or reflective sensor systems.

Each of these application areas includes an optical emitter, a transmission path, and a detector to perform the sensing function. The sensing may occur by having the object obstruct the transmission path, or complete it by reflecting the emitter beam to the detector. In either the transmissive or reflective sensing configuration, there are optical, electrical, and mechanical considerations that must be addressed in order to insure optimum performance of the emitter/detector system.

System Elements

Every optical sensor system includes a source of optical flux, a transmission path, and a receiving detector. In most sensor system analysis, the available flux and the responsivity of the receiver are considered to be constant and consequently the dynamic incidance change found at the receiver results from modifications of the transmission path. Figure 1 shows a paper tape reader and densitometer examples of transmissive sensor systems. The presence or absence of the paper hole results in a binary

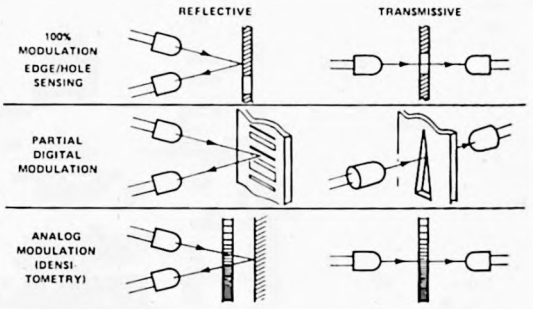


Figure 1. Different Techniques of Flux Path Modulation.

ON-OFF transmission path attenuation. The densitometer functions by causing an analog modulation of the transmission path. Bar code scanning and paper edge sensing are applications of reflective sensor techniques shown in Figure 1. The bar code provides a reflective contrast between the background and the bars. It is the reflective differential that modulates the transmission path. In paper edge sensing applications, the paper edge creates a digital responding transmission system. When the paper edge is not present in the reflecting field of the sensor, the flux transmission will be zero, and the transmittance will increase when the edge is in the field.

Optical Transfer Function

The characteristics of the transmission path can be estimated through the use of an optical transfer function, OTF. The function is the ratio of the total optical flux available, ϕ_e, to the incident flux arriving at the receiver, $\phi_e(R)$. This function allows the designer to calculate the amount of photocurrent available for the detector amplifier.

$$OTF = \frac{\phi_{e(RECEIVED)}}{\phi_{e(AVAILABLE)}} \quad (1)$$

The optical flux attenuation comes from a number of causes. One cause is the transmission loss as the flux is incident upon and passes through the transmission media. These losses come about because of reflection at the surface of the material, and scattering and absorption within the material. For the calculation of the optical transfer function, it is customary to describe these losses, τ, in terms of a transmittance, T, of the material for the wavelength of the source. The transmittance is equal to:

$$T = (1 - \tau) \qquad (2)$$

Another cause of attenuation is the incomplete coupling of the flux from the source to the receiver caused by the mismatch of the receiver relative aperture to the source relative aperture.

Coupling Fundamentals

The general case of source flux coupled to a receiver is dependent upon the source radiation pattern, the source-receiver spacing, and the receiver area. The following analyses show how these parameters affect the OTF.

Figure 2 shows a source which is located at the center of a hemisphere with a receiver of an area A located at a distance, **d**, from the apex. The ratio of the receiver area to the distance squared defines the solid angle, ω, subtended by the area, A. The total flux, ϕ_e, being radiated is the integral of the flux incident within the hemisphere. The radiation pattern of a Lambertian source is shown in Figure 3. The pattern describes the ratio of the radiant intensity at an off-axis angle, $I_e(\theta)$ to the axial radiant intensity, $I_e(0)$. The radiation pattern for a Lambertian source (or the reception pattern for a Lambertian receiver) is described by the cosine of the off-axis angle. The Lambertian radiation pattern function is:

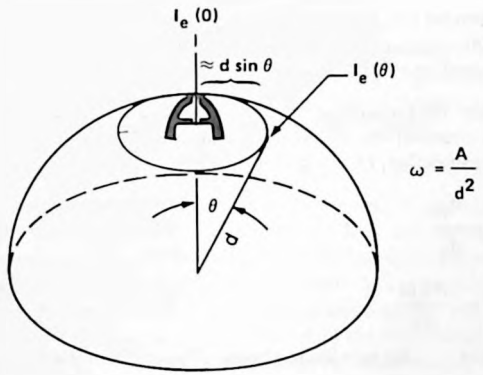


Figure 2. Definition of the Solid Angle, ω.

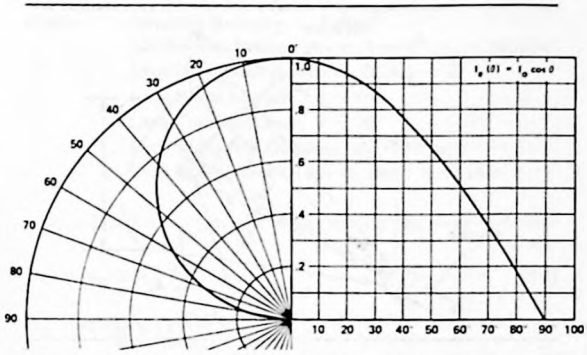


Figure 3. Radiation Pattern of a Lambertian Source.

$$I_e(\theta) = I_e(0) \cos\theta \qquad (3)$$

When the radiation pattern, $I_e(\theta)/I_e(0)$, and the axial radiant intensity, $I_e(0)$, are known, Equation (4) can be used to determine the total flux into the hemisphere, ($\theta = 90°$) or the flux into a cone created by the area, A.

$$\phi_e(\theta) = I_e(0) \int_0^{\theta} \frac{I_e(\theta)}{I_e(0)} 2\pi \sin\theta \, d\theta \qquad (4)$$

When a Lambertian radiator is used as a source, the flux into the cone specified by the off-axis angle, θ, is calculated from Equations (3) and (4).

$$\phi_e(\theta) = I_e(0) \int_0^{\theta} 2\pi \cos\theta \sin\theta \, d\theta$$

$$\phi_e(\theta) = I_e(0) \, \pi \sin^2\theta \qquad (5)$$

The total flux, ϕ_e, of the Lambertian source is obtained from Equation (5) when $\theta = 90°$. Thus, the total flux ϕ_e is π times the axial radiant intensity, $I_e(0)$.

The amount of flux coupled into the receiver area A relates to the relative aperture of the receiver. The relative aperture, also known as the numerical aperture, N.A., defines the ability of the receiver to accept flux arriving at off-axis angles. When a source with a specific radiation pattern is considered, a receiver with a large numerical aperture will capture more flux than one with a smaller N.A. The numerical aperture is defined as the sine of one-half the included angle of the receiver cone. Thus,

$$\text{N.A.} = \sin\theta \qquad (6)$$

where θ = ½ cone angle.

As seen in Figure 4, when small angles of θ are considered, the numerical aperture can be calculated as:

APPLICATIONS

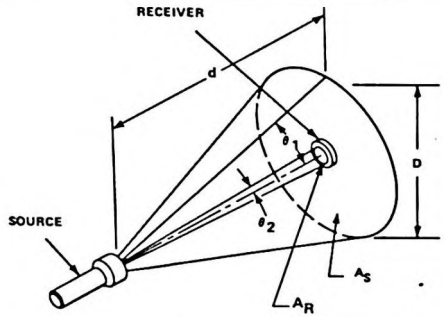


Figure 4. Illustration of Numerical Aperture Relationships.

$$N.A. = \sin\theta \approx D/2d$$

$$N.A. = \sin\theta \approx (A/\pi)^{1/2}/d$$

$$N.A.^2 = \sin^2\theta \approx A/\pi d^2 \qquad (7)$$

In Figure 4 are shown a source and a receiver separated by a distance, d. At that distance, the cone (θ_1) of radiation from the source irradiates an area, A_S. Clearly, the receiver having an area, A_R, much smaller than A_S, describes a smaller cone (θ_2) and will receive only a fraction of the flux radiated by the source. This fraction describes the Optical Transfer Function (OTF) for this simple situation, and a good estimate of the value of this fraction is the ratio of the areas A_R/A_S. Then, applying the relationship derived in Equation (7), the OTF can be defined in terms of the cones for source and receiver which are described by numerical apertures:

$$OTF = \frac{\phi_R}{\phi_S} = \frac{A_R}{A_S} = \frac{\pi d^2 N.A._R{}^2}{\pi d^2 N.A._S{}^2} \qquad (8)$$

$$= \left(\frac{N.A._R}{N.A._S}\right)^2 = \left(\frac{\sin\theta_2}{\sin\theta_1}\right)^2$$

In estimating OTF, it is necessary only to recognize and evaluate such cones of coupling — exit cone (or N.A.) and acceptance cones. As a general rule, the cone angle, θ, is defined as the angle at which coupling is 0.1 (10%) of the axial value ($\theta = 0$). A case of special interest is that of a Lambertian emitter having a radiation pattern varying as cos θ. The angle at which cos θ = 0.1 is 84.26°, at which sin θ = N.A. = 0.995; thus, for practical purposes, a Lambertian source is regarded as having N.A. = 1. If, in Figure 4, a Lambertian source were used, the relationship in Equation (8) reduces:

$$OTF = \left(\frac{N.A._R}{N.A._S}\right)^2 = \left(\frac{N.A._R}{1}\right)^2 = (N.A._R)^2 \qquad (9)$$

This simplification is important as it is used extensively in the sections to follow. Notice, however, that OTF cannot exceed unity, so that if $N.A._R > N.A._S$, then OTF = 1. This occurs when the acceptance cone of the receiver is larger than the exit cone of the source.

Lens Fundamentals

In practical sensor applications, the source-receiver distance might be ten or more times the diameter of the receiver. If the receiver area is small relative to d, then by Equation (7), the receiver numerical aperture will be small. If the source is Lambertian, the total flux coupling will then relate to the square of this small numerical aperture.

Through the use of lens, more efficient coupling will result. In order to understand how this is accomplished, it is helpful to present a few rules of optics. The first is the basic lens equation. Referring to Figure 5 a double convex condensing lens is shown relaying an image from the source to the receiver. The source is located a distance, d_S, from the lens and the real image is located at a distance, d_R, which is related to the focal length of the lens. Thus, the relationship of d_S, d_R, f is called the basic lens equation.

$$\frac{1}{f} = \frac{1}{d_S} + \frac{1}{d_R} \qquad (10)$$

where f = Focal Length

d_S = Source Lens Distance

d_R = Received Image Distance

This relay lens system is focused when the receiver is placed at the distance, d_R, [from Equation (10) when f and d_S are known] from the lens.

Under the focused condition, the image of the source (at the plane of the receiver) is magnified. The degree of magnification, m, is equal to the ratio of d_R to d_S.

$$m = \frac{d_R}{d_S} \qquad (11)$$

$$m^2 = \frac{A_{S,M}}{A_S} \qquad (12)$$

where $A_{S,M}$ = Source Image (Source Magnified)

A_S = Source Area

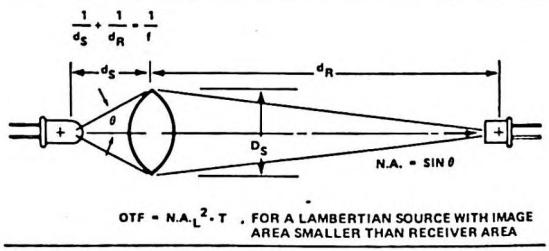


Figure 5. Focused Emitter Detector System Using a Double Convex Lens.

Using Equations (10) and (11), the magnification can be represented in terms of the focal length and source to lens distance, d_S.

$$A_{S,M} = m^2 A_S = \left(\frac{f}{d_S - f}\right)^2 \cdot A_S \qquad (13)$$

When the source-lens distance, d_S, is twice the focal length, f, the image will appear at $d_R = 2f$ on the other side of the lens. Under a 2f focused condition, the area of the image $A_{S,M}$, is equal to the area of the source A_S. This configuration is termed a 1:1 magnification or 2f system.

Lenses also have relative aperture qualities. The relative aperture may be specified as either a numerical aperture, N.A., or as an f-number, f/. The f-number is equal to the ratio of the focal length to the diameter of the lens. The f-number and the numerical aperture are inversely related, such that a smaller f-number will result in a proportionately larger N.A.

In Figure 5, the effective diameter of the lens is D_L, and relative to this, the numerical aperture is approximately $D_L 2d_S$ as in Equation (7). Comparing the definitions of f/no and N.A.:

$$\text{f/no} = \frac{f}{D_L} \qquad \text{N.A.} \approx \frac{D_L}{2d_S}$$

$$\text{f/no} = \frac{1}{2\text{N.A.}}\left(\frac{f}{d_S}\right) \qquad (14)$$

When $d_S = f$, the source is focused at infinity, making N.A. = 1/2(f/no); when $d_S < f$, there is no real image, but a virtual image of the source lying on the same side of the lens, and the lens is less effective in improving the coupling.

Lens Coupling

The amount of flux coupled into the lens is dependent upon the numerical aperture of the lens and the exit aperture of the source. When a focused lens system is considered such as that shown in Figure 5, the flux that arrives at the received image point is equal to the ratio of the square of the numerical aperture of the lens divided by the square of the exit numerical aperture of the source, this total times the transmittance, T, of the lens. Thus, the lensed OTF is equal to:

$$\text{OTF} = \frac{\phi_R}{\phi_S} = \left[\frac{\text{N.A.}_L}{\text{N.A.}_S}\right]^2 \cdot T \qquad (15)$$

When the source is Lambertian, the equation simplifies to:

$$\text{OTF} = \frac{\phi_R}{\phi_S} = \text{N.A.}_L^2 \cdot T \qquad (16)$$

The following will illustrate a practical example:

Given: Detector Area $A_D = .1\ mm^2$
Lambertian Source $A_S = .1\ mm^2$, $\phi_S = 100\mu W$
Lens Numerical Aperture $\text{N.A.}_L = .5$
Lens Focal Length, f = 5 mm
Lens Transmittance, T = .95
Lens to Source Distance, $d_S = 20$ mm
Lens to Receiver Distance, $d_R = 6.67$ mm

Using Equation (15), the flux at the receiver will be:

$$\phi_R = \phi_S \text{N.A.}_L^2 \cdot T \qquad (17)$$

$$\phi_R = 100\mu W\,(.5)^2 \cdot .95$$

$$\phi_R = 23.75\mu W$$

The received area is determined by Equation (12).

$$A_{S,M} = \left(\frac{f}{d_S - f}\right)^2 \cdot A_S$$

$$A_{S,M} = \left(\frac{5\ mm}{20\ mm - 5\ mm}\right)^2 \cdot .1\ mm^2 = .011\ mm^2 \qquad (18)$$

Thus, into an area of .011 mm^2, a flux of 23.75μW is concentrated. Using the basic lens equation, (10), the received image lies 6.7 mm from the lens. If a photodiode with an area, A_D, were placed at this distance, d_R, the fraction of this flux that couples the detector is the ratio of A_D to $A_{S,M}$ if the detector area lies entirely within the source image area. In general, this fraction is the ratio of that portion of the source image that overlaps the receiver, divided by the total source image area, and therefore cannot exceed unity, even when the detector area A_D is much larger than the source image area, $A_{S,M}$.

$$\text{Detector Coupling} = K_D = \frac{A_D}{A_R} \leq 1 \qquad (19)$$

When a lens coupling is compared with non-lens coupling, the improvement is described by:

$$\frac{\phi_L}{\phi_{n-L}} = \frac{\text{N.A.}_L^2 \cdot T}{\text{N.A.}_R^2} \quad ; \quad \text{N.A.}_R^2 = A_D/[\pi\,(d_S + d_R)^2]$$

where N.A._R is found from Equation (7) with $d = d_S + d_R$

$$\frac{\phi_L}{\phi_{n-L}} = \frac{(.5)^2 \cdot .95}{4.47 \times 10^{-5}} = 5.3 \times 10^3$$

Thus, this simple example using a lens improves the coupling gain by 37dB.

Reflector Fundamentals

Sensor applications, such as bar code scanning, paper edge detection, and optical tachometry, use the reflective properties of the object or element that they sense.

The reflection of the incident flux may either be specular or diffuse. A specular reflector is one where the angle of the reflected ray of flux is equal to the incident ray of flux. Thus, if a ray of flux was incident to the reflector at 20° from the normal, the reflected ray would also be 20° from the normal and 40° from the incident. A first surface mirror or a highly polished code wheel are examples of specular reflectors. They are characterized as having reflection coefficients, ρ, of almost unity. It has a numerical aperture, $N.A._{R\text{-}S}$, equal to the N.A. of the source that is incident upon it. The reflected flux would be equal to incident flux times the reflection coefficient.

$$\phi_{OUT} = \phi_{IN} \frac{N.A._L^2}{N.A._{R\text{-}S}^2} \cdot \rho; \quad \text{where } N.A._{RS} = N.A._L$$

$$\phi_{OUT} = \phi_{IN}\rho \tag{20}$$

The reflection coefficient is assumed to be constant over the wavelengths of interest. If this is not true, then a correction coefficient, $k\rho(\lambda)$ must be introduced to correct for this spectral property.

A perfectly diffuse reflector is characterized as having a Lambertian radiation pattern. The flux that is coupled from the reflector is equal to:

$$\frac{\phi_{OUT}}{\phi_{IN}} = \frac{N.A._{RECEIVER}^2}{N.A._{REFLECTOR}^2} \cdot \rho \tag{21}$$

In typical applications, the numerical aperture of the receiver will be that of the receiving lens. Also, the N.A. of the diffuse surface is unity; therefore, Equation (21) can be rewritten as:

$$\frac{\phi_{OUT}}{\phi_{IN}} = N.A._L^2 \cdot \rho \tag{22}$$

Most reflectors are neither perfectly specular or diffuse, but a combination of the two. A typical diffuse reflector may appear more specular at one wavelength and more diffuse at another. Also, the angle of incidence may modify the reflection properties.

It may be desirable in reflective sensor applications to compute the relative ratio of reflection between a specular and a diffuse reflector. Assuming both applications have the same ϕ_{IN} and the same receiving lens, and using Equations (20) and (21), this ratio becomes:

$$\frac{\phi_{OUT\ (SPECULAR)}}{\phi_{OUT\ (DIFFUSE)}} = \frac{\rho_S}{N.A._L^2 \rho_D} \tag{23}$$

Thus, if the receiving lens had a $N.A._L = .3$, the effective gain of using a specular over a diffuse reflector would be 10.45dB.

Confocal Coupling

It was shown in the lens coupling section that the area of the source could be reduced or magnified through the use of a lens. The technique of reducing the image of the receiver and the source, such that they lie on the same plane located a distance between the source and sensor can be accomplished by using two confocally spaced pair of lenses.

Figure 6 shows two plano-convex lenses positioned so that they are confocally focused. Using the coupling concept developed in the coupling fundamentals the overall OTF can be developed in the following steps.

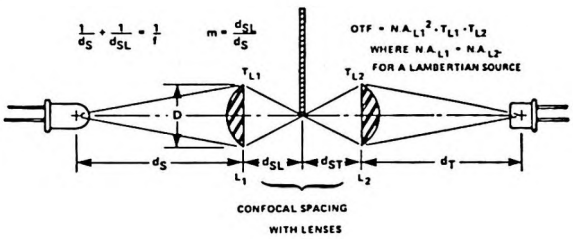


Figure 6. Confocal Spaced Emitter Detector System Employing Two Plano Convex Lenses.

Step 1. Flux into Lens 1.

$$\frac{\phi_{LI}}{\phi_S} = \frac{\text{entrance } N.A._{L1}^2}{N.A._S^2} \cdot T_{LI} \tag{24}$$

Step 2. Flux into Lens 2 from Lens 1.

$$\frac{\phi_{L2}}{\phi_{L1}} = \frac{\text{entrance } N.A._{L2}^2}{\text{exit } N.A._{L1}^2} \tag{25}$$

Step 3. Total OTF.

$$OTF = \frac{\phi_{L2}}{\phi_S} \tag{26}$$

$$= \frac{\text{entrance } N.A._{L1}^2}{\text{exit } N.A._S^2} \cdot \frac{\text{entrance } N.A._{L2}^2}{\text{exit } N.A._{L1}^2} \cdot T_{L1} \cdot T_{L2}$$

The convenient fact about such a transfer function is that each element of the linear system can be evaluated and then the total function is the product of the individual terms.

In a practical application, the exit N.A. of lens 1 and the entrance N.A. of lens 2 will be equal. If a Lambertian

source were used in Equation (24), it would reduce to $N.A._{L1}^2 \cdot T_{L1}$. These two conditions allow the following.

$$\text{Confocal OTF} = \frac{\phi_{L2}}{\phi_S} = N.A._{L1}^2 \cdot T_{L1} \cdot T_{L2} \qquad (27)$$

The image size appearing equidistant between the two lens surfaces is determined by the magnification factor, $m = d_{SL}/d_S$. Thus, a large source and receiver can be focused down to a point in space, and when confocally coupled, the imaged source-receiver area can become the interruption point for a hole edge, or paper edge sensor.

Lens Reflective Coupling

If one of the lenses of a confocally coupled lens system were placed adjacent to the other lens element and skewed so that the two images in front of the lenses intersected, a lensed reflective sensor would result. This is shown in Figure 7.

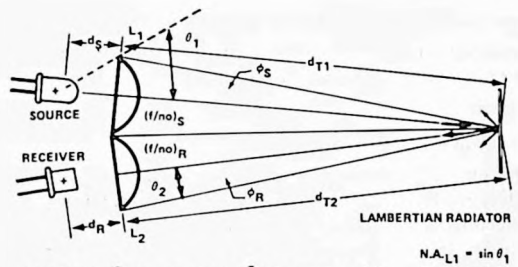


Figure 7. Reflective Coupling Employing Confocally Spaced Lenses.

Every mechanical system has alignment tolerances which may allow the two images at the focused point to move with respect to one another so that the area of the source and receiver images do not totally overlap. The ratio of the image overlap is termed the overlap fraction, OF.

$$O.F. = \frac{\left(\begin{array}{c}\text{AREA OF SOURCE IMAGE}\\ \text{WHICH IS OVERLAPPED}\\ \text{BY RECEIVER IMAGE}\end{array}\right)}{\left(\begin{array}{c}\text{TOTAL AREA OF}\\ \text{SOURCE IMAGE}\end{array}\right)} \leqslant 1 \qquad (28)$$

This fraction can vary from zero to unity. When it is zero, no coupling occurs and at unity, maximum coupling results. If the receiver image overlaps the entire source image, the O.F. will have its maximum value of unity. Having a larger receiver image provides a more consistent O.F. by reducing variability due to alignment difficulty.

The amount of flux coupling would be dependent upon the type and reflectance of the reflector placed at the image intersection, as well as on the N.A.'s of the lenses.

Using Equations (26) or (27), along with (22), and (28), the optical transfer function for a diffuse reflector can be determined.

$$OTF = N.A._{L1}^2 \cdot T_{L1} \cdot T_{L2} \cdot N.A._{L2}^2 \cdot \rho_D \cdot O.F. \qquad (29)$$

where ρ_D = reflection coefficient of a diffuse reflector and other terms are as defined in Figure 28.

In a similar manner, the OTF for the specular reflector may be determined.

$$OTF = N.A._{L1}^2 \cdot T_{L1} \cdot T_{L2} \cdot \rho_S \cdot O.F. \qquad (30)$$

where ρ_S = reflectance coefficient of a specular reflector

The conclusions to be drawn here are that a specular reflector will provide a much larger received flux. However, it suffers from a coupling problem where a movement of the normal of the reflecting plane, with respect to the normal of the confocally spaced lens system, causes the incident flux upon the reflector to be reflected outside of the aperture of the receiving lens. This is shown in Figure 8.

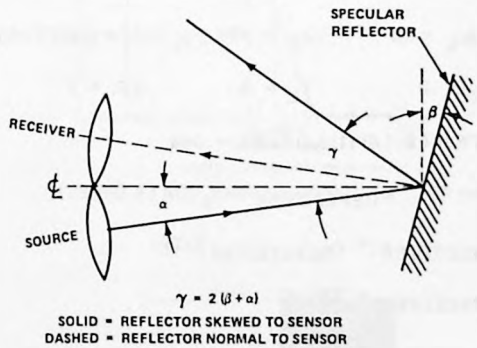


Figure 8. Positioning Sensitivity Caused by the Use of a Specular Reflecting Surface.

HEDS-1000 Reflective Coupling

Many of the alignment problems found in discrete confocally spaced reflective sensor systems can be eliminated with the use of the HEDS-1000 High Resolution Optical Reflective Sensor. This sensor includes a source and receiver focused with 2f optics. The optics system is a bifurcated aspheric lens with an effective numerical aperture of .3. These elements are housed in a TO–5 package with a glass window which is shown in Figure 9.

In the data sheet, radiant flux, ϕ_e, is specified as the flux coupled by the source lens to the image. This means that to develop the optical transfer function, only the receiving lens OTF need be described. The OTF for the HEDS-1000 and a diffuse reflector will appear very similar to that of a single lens system with the addition of the transmittance of the glass window, T_G, and the OTF of the reflector.

$$OTF = \frac{\phi_{RECEIVER}}{\phi_{REFLECTOR}} = T_L \cdot T_G \cdot O.F. \cdot OTF_{REFLECTOR} \quad (31)$$

The HEDS-1000 receiver area A_R is .160mm^2, and the source area A_S is .023mm^2. The ratio of A_R/A_S is greater than one which means that for focused operation, the overlap fraction O.F. is equal to one.

The following example shows the expected flux at the receiver photodiode from a diffuse reflector.

Step 1. Diffuse Reflector OTF. (32)

$$OTF = N.A._L^2 \cdot \rho_D$$

Step 2. Total OTF for HEDS-1000 Using Step 1 and Equation (31).

$$OTF = T_L \cdot T_G \cdot O.F. \cdot N.A._L^2 \cdot \rho_D$$

Step 3. Using the Following:

$N.A._L = .3$ $\rho_D = 98\%$, ϕ_e (DATA SHEET)=9μW

$T_G = .9$ $T_L = .8$ O.F. = 1

$OTF = (.8)(.9)(1)(.3)^2(.98) = .064$

Step 4. $\phi_{RECEIVER} = \phi_e$ (DATA SHEET)

$\phi_{RECEIVER} = \phi_{REFLECTOR}$ (OTF)

$\phi_{RECEIVER} = 576$ nW

If a specular reflector were used, the flux at the receiver would be the product of the transmittance of the glass and lens, the overlap fraction, O.F., and the reflectance of the specular reflector ρ_S. This is shown in Equation (33).

$$\phi_{RECEIVER} = \phi_{REFLECTOR}(T_L)(T_G)(O.F.)(\rho_S) \quad (33)$$

$\rho_S = .95$

$\phi_{RECEIVER} = 9\mu W\,(.8)\,(.9)\,(1)\,(.95) = 6.16\mu W$

Through the use of the numerical aperture of the receiver lens, it is possible to determine the Optical Transfer Function, and using this OTF, the radiant flux that appears at the receiver surface. From the responsivity of the receiver diode, the photocurrent can be estimated

OPTICAL SENSOR PARAMETERS

Introduction

Bar code scanning, paper edge sensing, and optical tachometry applications place specific requirements on optical resolution and electrical performance of a reflective sensor system.

This section will describe the expected optical resolution and electrical performance of the HEDS-1000 as the object being sensed is placed at a location other than the optical focus point.

Modulation Transfer Function

The optical resolution of a reflective sensor system is determined by the overlap area of the images focused at the reflector surface. This may be limited by either source or receiver image size, whichever is the smaller. Optical resolution of a reflective sensor system is defined as the ability to discriminate the reflection of closely spaced lines with unequal reflectances. Figure 10 shows a series of reflectors and bars, and the response to this pattern as the imaged source and receiver, are moved laterally across the surface. The assumption is made that the reflector reflectance, $\rho_{REFLECTOR}$, is much greater than the reflectance of the bar between the reflectors. The conclusion that can be drawn from this illustration is that the ability of the sensor to discriminate between reflectors spaced a distance, s, apart increases as the space, s, increases.

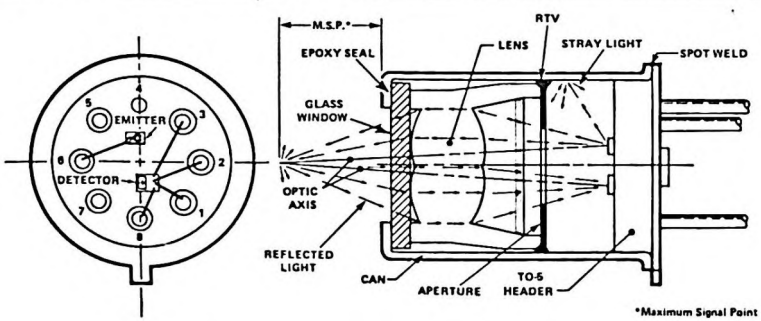


Figure 9. Elements of the HEDS-1000 High Resolution Optical Reflective Sensor.

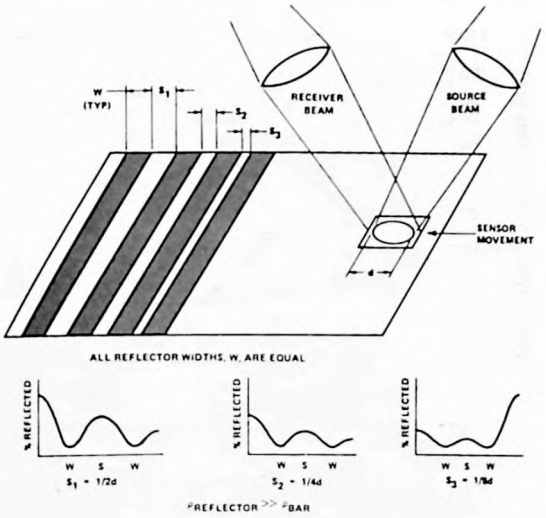


Figure 10. Resolution of an Optical Reflective Sensor System.

$$\text{Resolution } \alpha \frac{s}{d} \qquad (34)$$

Figure 11a, b shows a reflector object with a reflecting surface composed of equal width reflecting (white), and non-reflecting (black) lines. When a receiver with a circular image with a diameter, d, is positioned over the reflector so that the image area totally intersects the white line, a maximum or 100% peak reflected response will result. In a similar manner, when the image is positioned over the black line, a minimum or 0% peak reflected response will occur. The difference between maximum and minimum response specifies the peak amplitude response under these line width-image diameter conditions.

If this scanning spot were scanned laterally across the black-white transition, the response would be a ramp with a slope (% RESPONSE/lateral distance) determined by the image diameter. This is shown in Figure 12a. The 50% response point shown in Figure 12b indicates that the image area is equally intersecting the black-white reflecting areas. If the lateral scanning were continued across the surface, the reflected response for Figure 11a would be a trapezoidal wave form. This is shown in Figure 11b.

If an image is used to scan a black-white pattern where the line width is much smaller than the image diameter, the minimum to maximum response will be reduced from the response obtained when the line width is much larger than the image size.

An example of this is shown in Figure 13. A total 0 – 100% response occurs for a $W_2 = 3$ condition, while

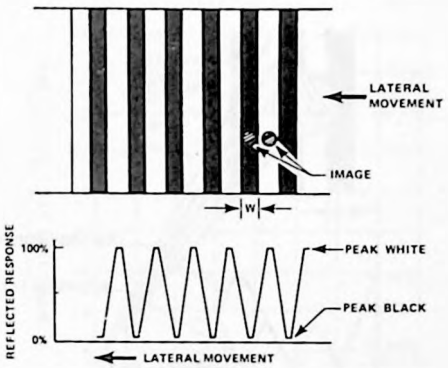


Figure 11. a,b. Image Response for Equally Spaced White and Black Lines.

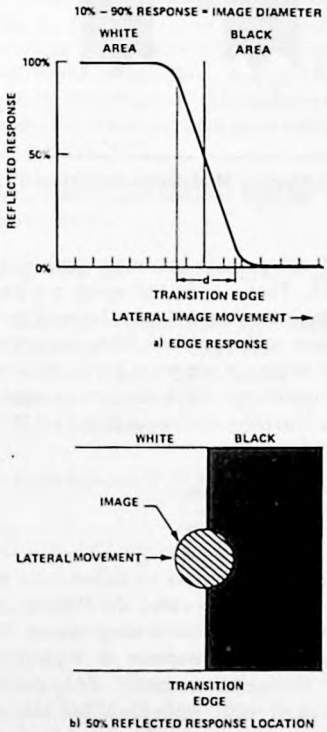


Figure 12. Image Transition Response.
a) Edge Response
b) 50% Reflected Response Location

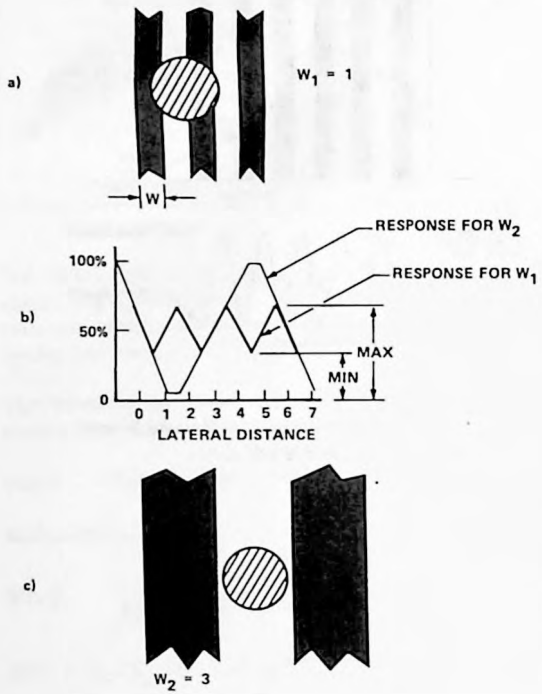


Figure 13. Reflection Modulation for Different Line Widths.

only a 33% minimum to maximum response is obtained when $W_1 = 1$. Thùs, as the line width gets smaller with respect to the image, the difference between the minimum and maximum is also reduced. When the performance at smaller line widths is compared to the performance for line widths resulting in 100% response, a modulation ratio is obtained. This ratio is shown in Equation (35) using data from Figure 13.

$$\text{Modulation} = \frac{\text{MAX} - \text{MIN}}{\text{MAX} + \text{MIN}} \qquad (35)$$

The modulation performance for different line pair widths for a fixed image size is called the Modulation Transfer Function, MTF, of the optical image system. The MTF is specified as a percent response at a particular spatial frequency. The spatial frequency, F, is defined as the number of equal width white-black line pairs per lateral distance. The common units for spatial frequency is line pairs per millimeter, ln pr/mm. The spatial frequency is determined by Equation (36).

$$F = \text{ln pr/mm} = \frac{1}{2 \text{ line width (mm)}} \qquad (36)$$

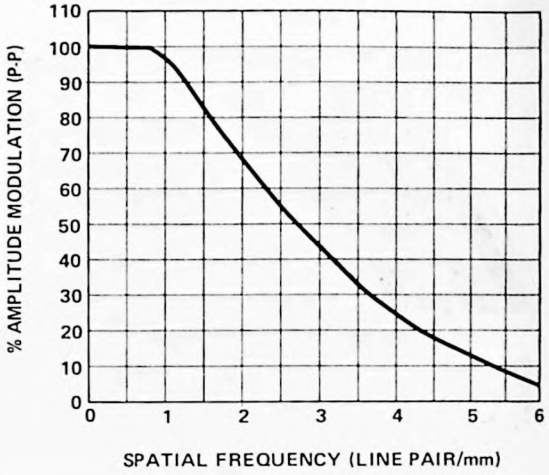


Figure 14. Modulation Transfer Function of the HEDS-1000.

Figure 14 shows the modulation transfer function, MTF, for the HEDS-1000. In applications such as bar code scanning and optical tachometry, the spatial frequency can be calculated with Equation 36. If a black-white line pattern with a line width of .254 mm (.01 in.) were to be scanned by the HEDS-1000, the performance can be determined through the use of Figure 14 and Equation (36). The spatial frequency is determined to be 1.97 ln pr/mm which results in an MTF response of 70%.

The MTF performance indicates that when a line pattern is scanned by the HEDS-1000, the reflected flux is degraded from the amount of flux obtained from a non-patterned reflector. Thus, the MTF response becomes another element to be added to the optical transfer function, OTF, as given in Equations (32) and (33).

Depth of Field

The optical transfer function, OTF, of a reflective sensing system was presented in the Lens Reflective Coupling, and the HEDS-1000 Reflective Coupling Sections. In each case, the assumption was that the source and the received image were focused on the same plane. In most applications, the mechanical alignment of the sensor to the reflecting element will not be at the fixed focused point.

As the reflecting object moves away from the focus point, the image will become defocused resulting in a blurred image. In a reflective sensor system, the defocusing will occur for both the source and received image. The ratio of the intersection of the two image areas determines an overlap fraction, O.F.. As the system is defocused, the overlap, O.F., decreases.

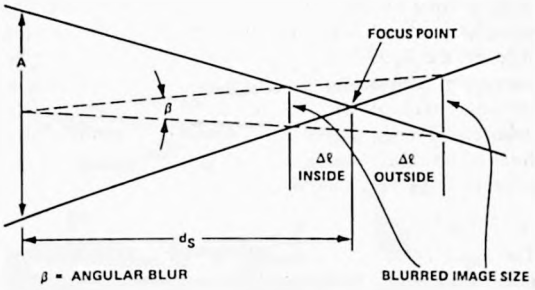


Figure 15. Defocusing Versus Depth of Field.

The defocused coupling response versus reflector distance is referred to as the depth of field, $\Delta\ell$. Figure 18 shows the relative response versus reflector distance. One will note an assymetrical response on either side of the maximum signal point. There is a much sharper $\%I_P(\Delta\ell)$ response roll-off for the distance between the reference plane to the maximum signal point, MSP, than from the MSP, to distances further away. This is due to the fact that the amount of blurring on the near side of the MSP is less than that on the far side. This is shown in Figure 15. The blurred image at $\Delta\ell$ inside is smaller than the blurred image at $\Delta\ell$ outside. When a reflective type of lensed system, as shown in Figure 9, is considered, the overlap fraction, O.F., is smaller at a $\Delta\ell$ inside than that for the same $\Delta\ell$ outside.

The defocusing of the optical system also impacts the modulation transfer function. As the system is defocused, the image size will increase causing a reduction in the MTF for a specified line pair per millimeter.

HEDS-1000 Total Transfer Function

The optical transfer function for the HEDS-1000 was developed in the HEDS-1000 Reflective Coupling Section. This development specified the performance of the reflective sensor as a ratio of flux incident at the receiver ϕ_R to the flux ϕ_e incident at the reflector, $OTF = \phi_R / \phi_e$. The electrical designer needs to know the relationship of the current supplied to the emitter, I_F, which produces a photocurrent, I_{PR} in the detector. This relationship will be referred to as the sensor electrical transfer function or total transfer function, TTF.

The TTF is the product of the optical transfer function, the flux from the emitter, ϕ_e, and the flux responsivity, R_ϕ, of the photodiode. This is shown in Equation (37).

$$TTF = \frac{I_{PR}}{I_F} = R_\phi \cdot OTF \cdot \phi_e(I_F) \cdot K \qquad (37)$$

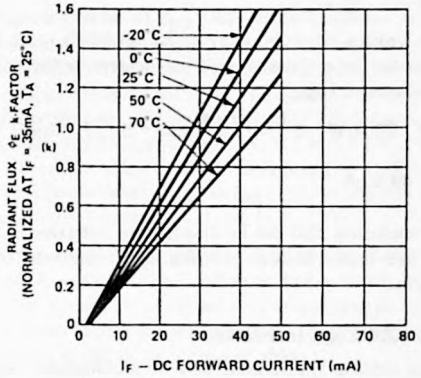


Figure 16. K-factor of ϕ_e Versus LED DC Forward Current.

The flux responsivity, R_ϕ, of the photodiode at 700 nm is specified as .22A/W. The flux responsivity, R_ϕ, will be considered a constant throughout the calculations. The radiant flux, ϕ_e, from the source is dependent upon the current through the LED emitter. The K-factor relationship of the output flux, ϕ_e, to LED forward current, I_F, is shown in Figure 17. This graph is normalized at 35mA and 25°C. Thus, the data sheet typical of 9μW occurs at 35 mA and 25°C.

The following example will illustrate how the TTF is used for a bar code scanner.

Given: I_F = 45 mA ϕ_e (35 mA) = 9μW
T_A = 25°C
Reflector = Lambertian, ρ_D = .85 @ 700 nm
Bar Width = .01", =0.254 nm
Depth of Field = $\Delta\ell$ = .6 mm
N.A.$_L$ = .3 T_G = .9 T_L = .8
R_ϕ = .22 A/W

The total transfer function, TTF, is:

$$TTF = \frac{I_{PR}}{I_F} = R_\phi \cdot T_L \cdot T_G \cdot N.A._L^2 \cdot \rho_D \cdot O.F.(\Delta\ell) \times MTF \cdot \phi_e \cdot K \qquad (38)$$

The first step is to evaluate the overlap fraction, $O.F.(\Delta\ell) = \%I_{PR}(\Delta\ell)$, a function of the depth of field, $\Delta\ell$. From Figure 19, the $\%I_{PR}(\Delta\ell) = 50\% = .5$. Thus, the O.F. is equal to .5.

The second step is to determine the MTF response for a bar width of .254 mm, for a depth of field of .6 mm. Equation (36) is used to arrive at an F(APP) = 1.97 In pr/mm. Figure 14 is used to determine the MTF (APP) of 70%. Thus, MTF (1.97 In pr/mm) is equal to 70%.

The third step is to determine the K-factor. This is can be found from Figure 16. The K-factor for an $I_F = 45$ mA is equal to 1.3 at 25°C.

These values of O.F. ($\Delta\ell$), MTF(APP), and K are substituted into Equation (38) to determine the reflected photocurrent, I_{PR}.

$$I_{PR} = .22\ A/W \bullet .8 \bullet .9 \bullet (.3)^2 \bullet .85 \bullet .5 \bullet .7 \bullet 9\mu W \bullet 1.3$$

$$I_{PR} = 49.6\ nA$$

The conclusion that can be drawn from this example is that there are many factors contributing to the total transfer function.

HEDS-1000 Logic Interfacing

Optical sensing applications may be accomplished with the HEDS-1000 High Resolution Reflective Optical Sensor. This device includes a 700 nm emitter, a bifurcated aspheric lens, and a photodetector. The cathode of the LED emitter and the substrate of the photodetector are electrically connected to the mechanical package. The photodetector may be interconnected as a discrete photodiode or a photodiode-transistor amplifier.

Photodiode Interconnection

The photodiode, within the integrated photodetector, is isolated from the substrate-case by substrate diodes. These diodes appear from the common substrate-case to the transistor collector, and to the cathode of the photodiode.

Figure 17 shows recommended interconnection of the unused terminals of the sensor when discrete photodiode operation is desired. Care should be taken to ensure that these substrate diodes are always reverse biased so that they do not create a conductive path that may damage the substrate or other circuit elements.

The photodiode behaves like a current source, such that when optical flux falls on the device, it will generate a photocurrent in relationship to its responsivity, R_ϕ, of approximately .22μA/μW at 700 nm. The total photocurrent, I_P, generated by this photodiode is the summation of two currents, the reflected photocurrent, I_{PR}, and a stray photocurrent, I_{PS}. Thus, $I_P = I_{PR} + I_{PS}$.

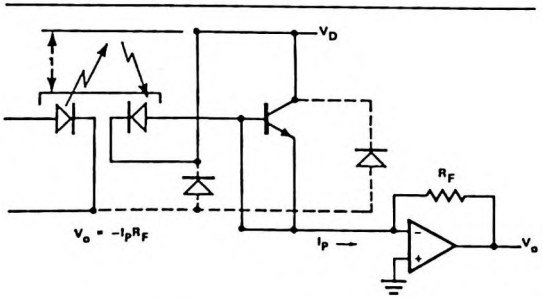


Figure 17. Photodiode Transresistance Amplifier.

Stray Photocurrent — I_{PS}

The stray photocurrent, I_{PS}, results from flux falling on the detector from sources other than the reflector surface. The principle source of stray photocurrent is from the scattered flux of the LED emitter that is reflected within the mechanical package. Ambient light can also be a source of the stray photocurrent, but this source has been greatly minimized by the use of an optical long wave filter. This filter action is provided by the red coloration found in the bifurcated lens.

$I_{PR} - I_{PS}$ Ratio

The magnitude of the stray photocurrent resulting from internal scattering is directly proportional to the forward current, I_F, through the LED and the emitter relative efficiency. DC operation of the emitter will result in a steady state stray photocurrent that will range in direct relationship to the specifications and the worst case or typical value of $I_{P(MIN)}$ and $I_{P(MAX)}$ related to the stray photocurrent ratio, I_{PR}/I_{PS}. The photocurrent specified for the HEDS-1000 is the total photocurrent, I_P, which is equal to the sum of I_{PR} and I_{PS}. The ratio of I_{PR} to I_{PS} is designated a quality or Q-factor of the sensor. Thus, as Q increases for a given I_P, the value of stray photocurrent, I_{PS}, decreases. A worst case analysis for I_{PS} under the condition of minimum Q = 4, and an LED current of 35 mA results in an $I_{PS(MIN)} = 20$ nA for $I_{P(MIN)} = 100$ nA, and $I_{PS(MAX)} = 50$ nA for $I_{P(MAX)}$ 250 nA. A typical value of Q = 6.5 would cause I_{PS} to range from 13 nA to 33 nA.

The quality factor, Q, relationship to I_P, I_{PS}, and I_{PR} is shown in Equation (39).

$$Q = \frac{I_{PR}}{I_{PS}} \qquad I_P = I_{PS} + I_{PR} \tag{39}$$

$$I_{PR} = I_P\,[Q/(Q+1)] \qquad I_{PS} = I_P\,[1/(Q+1)]$$

where
- Q = Quality Factor
- I_P = Total Photocurrent
- I_{PR} = Reflected Photocurrent
- I_{PS} = Stray Photocurrent

Depth of Field With Respect to Maximum Signal Point

Figure 18 shows that the 100% maximum reflected photocurrent, I_{PR}, response occurs at the location from the reference plane defined as the Maximum Signal Point, MSP. It also shows that the value of the reflected photocurrent I_{PR} is reduced as the reflector is moved in either direction away from the maximum signal point. The HEDS-1000 has a relatively symetrical response of I_{PR} versus the distance, ℓ, from the MSP. The depth of field of this optical system is defined as the distance, $\Delta\ell$, between two equal percentage response points on either side of the MSP. The 50% I_{PR} response is referred to as the depth of field full width half maximum, FWHM. The depth of field, $\Delta\ell$, FWHM shown in Figure 18 is found to be 1.2 mm. Thus, if the

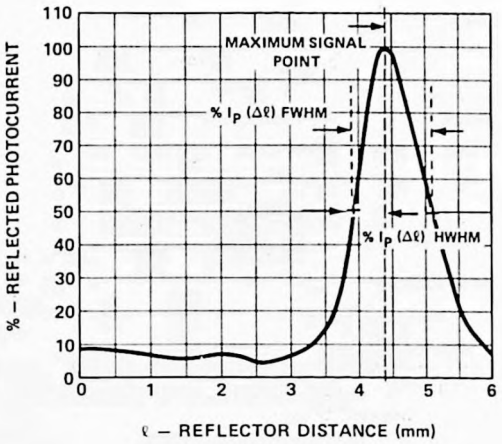


Figure 18. Depth of Field vs. Maximum Signal Point.

reflector were moved one half of the total FWHM distance, Δℓ, from the MSP, the 50% I_{PR} point would occur approximately .6 mm on either side of the MSP location. The reflected photocurrent, I_{PR}, response at a specific depth of field is referred to as the $\%I_{PR}$ (Δℓ). This value is always less than or equal to 100%.

The specific value of the I_{PR} is dependent upon the flux from the emitter and the type and reflection coefficient, p, of the reflector. The reflector fundamentals section presented the characteristics of the reflectors, and demonstrated that a specular reflecting surface offers and order of magnitude improvement in the reflecting photocurrent when compared to a diffuse surface.

When a diffuse reflector is used, the expected value of the reflected photocurrent, at a specific depth of field, I_{PR} (Δℓ), is the product of the percent response of I_{PR} at the depth of field $\%I_{PR}$ (Δℓ), the reflection coefficient, ρ, of the reflector, the total photocurrent measured at the MSP from a diffuse reflector at a specific LED current I_P (I_F), and the quality ratio Q/Q + 1. This relationship is shown in Equation (40).

$$I_{PR}(\Delta\ell) = \%I_{PR}(\Delta\ell) \cdot \rho \cdot I_P(I_F) \cdot Q/(Q+1) \quad (40)$$

When a specular reflector is used, an additional coefficient is introduced. The HEDS-1000 I_{PR} performance is specified for a diffuse reflector; thus, when a specular reflector is used, an improvement factor dictated by Equation (23) is obtained. This factor indicates the I_{PR} improvement, for $p_S = p_D$, is inverse of the lens numerical aperture squared. The $I_{PR}(\Delta\ell)$ response for a specular reflector is shown in Equation (41).

$$I_{PR}(\Delta\ell) = \%I_{PR}(\Delta\ell) \cdot \rho \cdot I_P(I_F) \cdot Q/(Q+1) \cdot 1/N.A._L^2 \quad (41)$$

The expected value of I_{PR} (Δℓ) using a diffuse reflector with a relector having a reflectance of 75%, a total depth of field of 1.2 mm (.6 mm each way), and LED emitter current of 35 mA, and quality factor Q = 6.5, can be deter- mined from Equation (40). The depth of field of 1.2 mm is equal to a 51_{PR} (Δℓ) of 50%, and typical I_P (35 mA = 140 nA. The I_{PR} (Δℓ) under these conditions is equal to 45.5 nA. If a specular reflector were used, an I_{PR} (Δℓ) = 506 NA would be found from Equation (41), for $N.A._L = 0.3$.

These two equations are useful in determining the expected range of I_{PR} for a given reflector and a depth of field. These two system elements are very important in bar code scanning and paper edge sensing where the type of reflector and specific depth of field are variables.

Amplifier Considerations

Each sensor application will generally specify the electrical interface required and the range of the types of reflectors which will be utilized. The magnitude of the photocurrent generated by the photodiode is normally too small to interface directly to a logic gate. This condition indicates that an amplifier is needed. The amplifier electrical performance parameters, such as current and voltage gain, and the type of coupling are determined by the logic family to be interfaced, the application, and the magnitude of the reflected photocurrent.

Applications using specular reflectors include tachometry and optical limit sensing, while diffuse reflectors are more generally found in paper edge sensing and bar code reading. An ac coupled amplifier is acceptable in tachometry and bar code reading, while a dc coupled amplifier is required for steady state applications such as paper edge sensing and optical limit sensing.

The relationship of the reflected photocurrent, I_{PR}, to stray photocurrent, I_{PS}, has a large effect on the type of dc amplifier design selected. The initial step in amplifier design is to determine the worst case magnitude of the stray photocurrent, I_{PS}. It is this worst case value of I_{PS} that becomes the input quiescent bias current, which sets the threshold for the dc amplifier output voltage.

Transresistance – TTL Interface

A very common dc amplifier used with photodiodes is the transresistance type of amplifier. The simplest form is shown in Figure 15.4.1-1. The circuit configuration described by the electrical transfer function, $V_o = -I_P R_F$, is often called a current to voltage converter. A single power supply transresistance amplifier is shown in Figure 20 Here the photodiode is connected to the inverting input, and an offset voltage derived from V_{cc} is determined by a resistive voltage divider, $1 + R_2/R_1$ and is applied to the non-inverting input. The electrical transfer function is:

$$V_o = \frac{V_{cc}}{1 + R_2/R_1} - I_P R_F \quad (42)$$

where $I_P = I_{PR} + I_{PS}$

APPLICATIONS

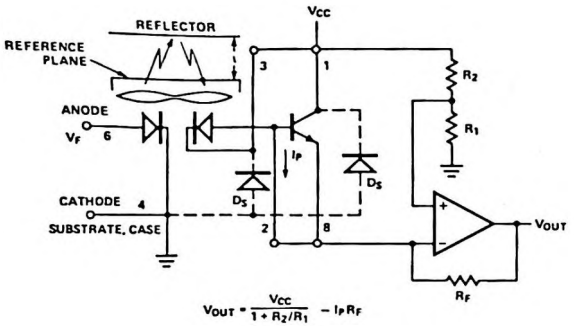


Figure 19. Photodiode Transresistance Amplifier with Offset Voltage.

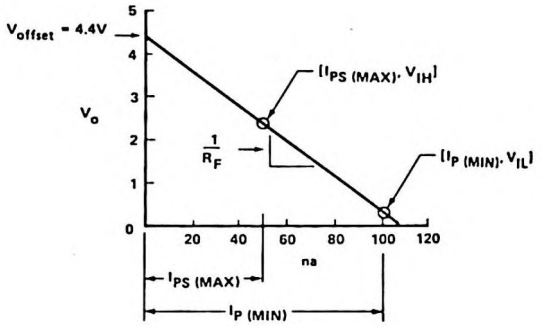


Figure 20. Graphical Solution of Transresistance Amplifier Design.

Equation (43) indicates that under the condition of zero reflected photocurrent, $I_{PR} = 0$, the output voltage, V_o, will be the offset voltage less the voltage developed by the stray photocurrent, I_{PS}, times the transresistance, R_F. Thus, the relationship for $I_{PR} = 0$ is:

$$V_o = \frac{V_{cc}}{1 + R_2/R_1} - I_{PS} R_F \qquad (43)$$

When the transresistance amplifier shown in Figure 19 is used to interface the photodiode to a TTL logic device, the output voltage, V_o, of the amplifier must change from a logic high, V_{IH}, of 2.0V to a logic low, V_{IL}, of .8V. To improve the noise immunity of the interface, it is desirable to broaden the range of V_{IH} to V_{IL} to 2.4V and .4V. The offset voltage and the value of the transresistance resistor, R_F, is selected to insure that the maximum value of stray photocurrent, $I_{PS\,(MAX)} = 50$ nA, does not cause the output voltage, V_o, to fall below V_{IH} of 2.4V, and the minimum total photocurrent, $I_{P\,(MIN)} = 100$ nA, will cause the V_o to be equal to a $V_{IL} = .4V$.

It is very unlikely that an $I_{PS\,(MAX)}$ 50 nA and $I_{P\,(MIN)} = 100$ nA will occur simultaneously for a single device. A device that has an $I_{PS\,(MAX)}$ of 50 nA would also have an $I_{P\,(MIN)}$ of 250 nA. In a similar manner, a device that has an $I_{P\,(MIN)}$ of 100 nA would most likely have an $I_{PS\,(MAX)}$ of 20 nA.

Figure 20 shows the graphic construction of the electrical transfer function for Equation (42). The interface conditions of $[I_{PS\,(MAX)}, V_{IH}]$ and $[I_{P\,(MIN)}, V_{IL}]$ describe a line whose y intercept dictates the offset voltage, V_{offset}, and whose slope determines the transresistance, R_F. Using Equations (44) and (45), the offset voltage, V_{offset}, and the transresistance can be determined.

$$V_{offset} = \frac{V_{IL}\, I_{PS\,(MAX)} - V_{IH}\, I_{P\,(MIN)}}{I_{PS\,(MAX)} - I_{P\,(MIN)}} \qquad (44)$$

$$R_F = -\frac{V_{IH} - V_{IL}}{I_{PS\,(MAX)} - I_{P\,(MIN)}} \qquad (45)$$

The value of V_{offset} and R_F which satisfy the TTL interface conditions can be determined from Equations (44) and (45). For the example, V_{offset} = 4.4V, and $R_F = 40\,M\Omega$.

This example of photodiode-logic interfaces places parametric demands on the instrumentation operational amplifier selected. This amplifier should have a very low input offset current, thus allowing sensing of I_P at very low levels. It should have a gain greater than that required for the interface. For example, the required current gain for the photodiode-TTL amplifier is approximately 85dB; thus, an amplifier with an open loop gain of 100dB would be desirable. The slew rate of a transresistance amplifier may be slower than that required for TTL logic interconnection; thus, it may be necessary to specify a Schmitt trigger gate as the interconnecting logic element.

CMOS Interface

The internal transistor of the HEDS-1000 may also be used as a gain element in a single or multiple stage amplifier. Figure 21 shows an example of interconnecting the photodiode to a CMOS buffer gate, CD4049, using the internal transistor as a gain element.

It was shown previously that the value of I_{PS} and I_P can vary from unit to unit under similar conditions of I_F, reflector type and distance, ℓ. There will also be variations

of the h_{FE} of the transistor from unit to unit. The design of the photodiode-transistor amplifier to CMOS logic gate must take into consideration the variations of I_{PS}, I_P, and h_{FE} when a direct coupled interconnection is desired. Figure 21 presents a design for an HEDS-1000 CMOS interface. The first step is to calculate the worst case stray photocurrent, $I_{PS\,(MAX)}$. The $I_{PS\,(MAX)}$ becomes the transistor base current which, when multiplied by the $h_{FE\,(MAX)}$, will determine the maximum collector current resulting from stray photocurrent. It is a requirement of this circuit that the collector current resulting from $I_{P\,(MAX)}$ does not cause the collector output voltage to fall below the input logic high level, V_{IH}, of 4 volts. Thus, the maximum value of the load resistor is selected based on the $I_{PS\,(MAX)}$ and $h_{FE\,(MAX)}$ of the sensor.

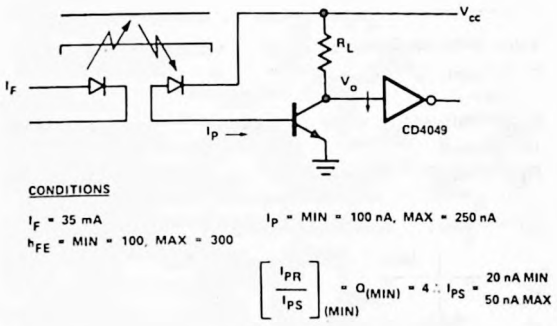


Figure 21. HEDS-1000 Interface to a CMOS Gate.

It is desirable in this type of interface to have at least a two to one difference between the $I_{PS\,(MAX)}$ and the $I_{P\,(MIN)}$. Such a stipulation will place constraints on the type of reflector, the depth of field, and the allowable spread between $h_{FE(MIN)}$ to $h_{FE(MAX)}$. Equations (40) and (41) are used to calculate the $I_P\,(\Delta\ell)$ for worst case conditions of $I_{P\,(MIN)}$ when a depth of field of 1.2 mm is desired. Thus, a diffuse reflector would cause 37.5 nA $I_{P\,(MIN)}$ and a specular reflector would result in an $I_{P\,(MIN)}$ of 416 nA. Using the criteria of $I_P(\Delta\ell)/I_{PS\,(MAX)} \geq 2$ [where $I_P(\Delta\ell)$ is evaluated for $I_{P\,(MIN)}$] indicates that a reflector with specular properties should be used.

The next step is to determine the minimum value of R_L for the minimum value of $I_P\,(\Delta\ell)$ and $h_{FE\,(MIN)}$ which causes the transistor collector voltage to fall below the V_{IL} of the CMOS gate.

This worst case analysis of Table 1 indicates that there is a very narrow range between the $R_{L\,(MAX)}$ and $R_{L\,(MIN)}$. If a smaller depth of field $\Delta\ell$ were selected, the range would be larger, thus giving a greater design margin.

Table 1. HEDS-1000 to CMOS Interface Design Procedure.

Step 1. Maximum Stray Photocurrent

$$I_{PS\,(MAX)} = \frac{I_{P\,(MAX)}}{Q_{MIN} + 1} = \frac{250\text{ nA}}{4+1} = 50\text{ nA}$$

$$Q_{MIN} = \frac{I_{PR\,(MIN)}}{I_{PS\,(MAX)}}$$

Step 2. $R_{L\,(MAX)}$ for V_{IH}

$$R_{L\,(MAX)} = \frac{V_{cc} - V_{IH}}{h_{FE\,(MAX)} \cdot I_{PS\,(MAX)}} = \frac{5.0 - 4.0}{300 \cdot 50 \times 10^{-9}}$$

$$= 66.7\text{k}$$

Step 3. Minimum Photocurrent from Specular Reflector at $\Delta\ell$ = 1.2 mm

From Equation (41):

$$I_P\,(\Delta\ell) = \%I_P\,(\Delta\ell) \cdot \rho \cdot I_P \left[\frac{\text{N.A.(SURFACE)}}{\text{N.A. (LENS)}}\right]^2$$

$$I_P\,(\Delta\ell) = .5 \cdot .75 \cdot 100\text{ nA} \left[\frac{1}{.3}\right]^2 = 416\text{ nA}$$

ρ = 75%
N.A.$_{(SURFACE)}$ = 1
N.A.$_{(LENS)}$ = .3
$I_{P\,(MIN)}$ @ I_F = 35 mA = 100 nA
$\%I_P\,(\Delta\ell)$, $\Delta\ell$ 1.2 mm = .5

Step 4. $R_{L\,(MIN)}$ for V_{IL} at $\Delta\ell$

$$R_L = \frac{V_{cc} - V_{IL}}{h_{FE\,(MIN)} \cdot I_P\,(\Delta\ell)} = \frac{5.0 - 2.25}{100 \times 416\text{ nA}} = 66.1\text{k}$$

Step 5. Select R_L = 66.2k 1%

Current Feedback Amplifier

Another common design problem is to interface the photodiode-transistor amplifier to a differential comparator such as the LM311 family. Here the design goals are similar to those specified in Figure 21 but an even greater

APPLICATIONS

degree of output voltage, V_o, stability is desired. By using a simple current feedback amplifier such as the one shown in Figure 22, the variations of V_o caused by Δh_{FF} and ΔI_{PS} will be minimized. In this amplifier design, the trade-offs are between voltage/current gain, stability, and amplifier speed. As the ratio of R_F to R_L approaches unity, the V_o stability improves, but there is a loss in signal gain. The difference between the I_{PS} and $I_P(\Delta\Omega)$ will specify a current that will cause a change in the output voltage, V_o. When a larger swing in V_o is desired, the value of R_L is increased, such that $\Delta V_o \alpha (I_P - I_{PS}) R_L$. However, as R_L increases, the speed of the circuit decreases. Tables 2 and 3 show a design example using an R_L = 100k, R_F = 10MΩ. In Figure 22, the differential comparator threshold is set by the resistor ratio R_1, R_2 and should be equal to 1.25V. This is below the minimum quiescent, V_o, of 1.3V caused by the variations of h_{FE} and I_{PS}. The change of the quiescent voltage caused by the variation of h_{FE} can be calculated through the use of the stability factor defined as s". This factor is the incremental change of I_C caused by an incremental change in h_{FE}. Specifically,

$$s'' = \left(\frac{\Delta I_C}{\Delta h_{FE}}\right)_{I_P = 0} \qquad (46)$$

The V_o stability is improved as the value of s" is reduced. The incremental V_o change of the circuit shown in Figure 22 can be calculated from the following relationship:

$$\Delta V_o = -\Delta h_{FE}\left[s'' R_L + \frac{\delta^2 V_o}{\delta h_{FE}\,\delta I_P}\right] \qquad (47)$$

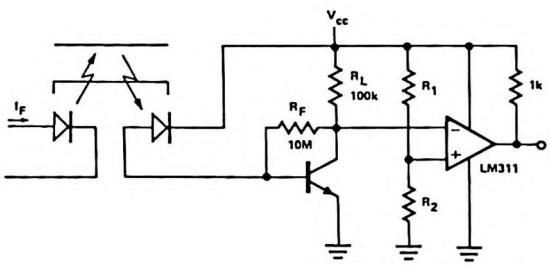


Figure 22. Current Feedback Amplifier Interface to an Analog Comparator.

Table 2 Current Feedback Amplifier Design Procedure.

OUTPUT VOLTAGE, V_o

$$V_o = \frac{V_{CC}\left(\frac{R_F}{h_{FE}R_L}\right) + V_{BE}\left(1 + \frac{1}{h_{FE}}\right) - R_F I_P}{\left(\frac{R_F}{h_{FE}R_L}\right) + \left(1 + \frac{1}{h_{FE}}\right)}$$

STABILITY FACTOR, $s'' = \dfrac{\Delta I_C}{\Delta h_{FE}}$

$$s'' \approx \frac{(R_L + R_F)\,(V_{cc} - V_{BE})}{(R_F + R_L + R_L h_{FE})^2}$$

Table 3 Practical Example of a Current Feedback Amplifier Design.

h_{FE} MIN = 100 MAX = 300 $I_{PS(MAX)}$ = 41 nA

R_L = 100kΩ R_F = 10MΩ V_{cc} = 5.0V , V_{BE} = .6V

	h_{FE} = 100	h_{FE} = 300
V_o	2.60V	1.39V
s"	1.1×10^{-7}	

The s" parameter is important in dc coupled amplifier circuits because the change in V_o caused by the Δh_{FE} may result in the succeeding gain stages being driven into saturation.

Current–Voltage Feedback Amplifier

When even greater output voltage stability is desired, a modified current-voltage feedback amplifier may be necessary. This bias approach uses R_F and R_N as shown in Figure 23, to force a V_B which sets I_C to a level determined by V_B/R_E. This circuit can offer an s" ten times better than the current beedback amplifier. The design is such that an h_{FE} variation of 100 – 300 will cause a 0.3V change in V_o in the current-voltage feedback configuration, while this same Δh_{FE} for Figure 22 will cause a 1.2V change.

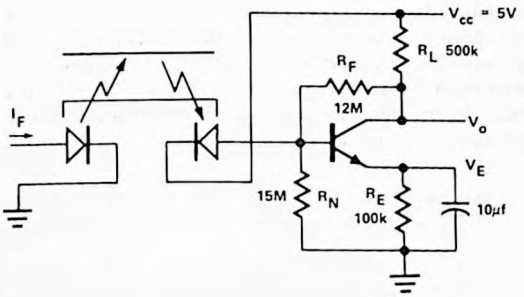


Figure 23. Current-Voltage Feedback Amplifier.

The design example given in Table 4 sets the V_o at 2.5V and offers an s" of 7.5×10^{-9}. The output voltage V_o will be reduced from a design center of 2.5V to a worst case ($V_o - s'' \Delta h_{FE} R_L$) = 2.25V. This implies that the threshold of the comparator should be set to a level of 1.55V. This amplifier offers a transresistance of 8MΩ which means for a 100nA I_P ($\Delta\ell$), the output voltage V_o will fall to 1.5V which is a sufficient differential to cause the LM311 output to change logic states.

Table 4. Design Equations for the Current-Voltage Feedback Amplifier.

Step 1. Select R_L Given: V_o and I_C

$$R_L = \frac{(V_{cc} - V_o)}{I_C} = \frac{2.5V}{5\mu A} = 500k$$

Step 2. Select R_E Given: V_E and I_E

$$R_E = \frac{V_E}{I_E} = \frac{.5}{4.91 \times 10^{-6}} = 101k \approx 100k$$

Step 3. Select R_N Given: I_N

$$R_N = \frac{V_E + V_{BE}}{I_N} = \frac{.5 + .6}{75\ nA} = 14.6M\Omega \approx 15M\Omega$$

Step 4. Select R_F Given: I_N and I_B

$$R_F = \frac{V_o - V_E - V_{BE}}{I_N + I_B} = \frac{2.5 - .5 - .6}{75\ nA + 50\ nA}$$

$$= 11.2M\Omega \approx 12M\Omega$$

Step 5. Stability Factor, s"

$$s'' = \frac{\left[V_{CC} - V_{BE}\left(1 + \frac{R_F + R_L}{R_N}\right)\right](g+1)}{R_F\,[1 + (1 + h_{FE})g]^2}$$

where $g = \frac{R_E}{R_N}\left(1 + \frac{R_L}{R_F}\right) + \frac{R_E + R_L}{R_F}$

$s'' = 7.5 \times 10^{-9}$

LSTTL Interface

The previous circuits dealt with CMOS and comparator type interfaces. Figure 24 shows a two transistor amplifier to LSTTL interface. This circuit can either be ac or dc coupled, only the direct coupled configuration will be presented. The design approach is similar to that of Figure 21 with the additional analysis of the second stage.

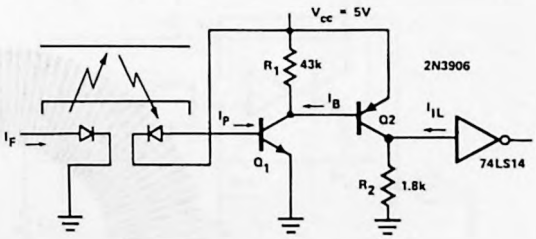


Figure 24. DC Coupled HEDS-1000 to LSTTL Interface.

The first transistor, Q_1, is biased by the photodiode in a common emitter configuration. Under the conditions of $I_{PS(MAX)}$, the collector of Q_1 is pulled up to within .5V of V_{cc}, thus insuring that Q_2 is not conducting. This condition sets the maximum value of R_1. When a reflected

APPLICATIONS

photocurrent is present, the resulting I_C of Q_1 is the combination of current through R_1 and the I_B of Q_2. Thus, R_1 must be large enough that the current sinking capability of Q_1 (dictated by h_{FE} and I_P) will result in sufficient I_B in Q_2 to cause Q_2 to saturate.

In the absence of reflected photocurrent, both Q_1 and Q_2 are normally off. Under this condition, the load resistor, R_2, must be able to sink the I_{IL} of the LSTTL gate at the desired V_{IL}. To satisfy the desired logic condition, R_2 must be less than V_{IL}/I_{IL}. The minimum value of R_2 is determined by the current sourcing capability of Q_2 produced by I_B. The collector current of Q_2 must generate a voltage drop across R_2 greater than the V_{IH} of the gate. It is recommended that a high gain, low leakage PNP transistor, such as a 2N3906, be selected for Q_2.

The rate at which the output voltage of Q_2 changes is directly related to the speed at which the reflecting surface is moving into the reflection plane of the sensor. In many applications, the rate of change of V_o through the switching region of the LS gate is so slow that it may cause logic level chatter at the output of the gate. If this chatter is observed, it is recommended that a Schmitt trigger gate, such as the 74LS14, be used.

REFLECTIVE SENSOR APPLICATIONS

Rotary Tachometry

A reflective sensor can be used as the transducer to determine the rotary speed of a motor shaft. This can be accomplished by utilizing a disc with equally spaced reflective and non-reflective lines placed around the circumference of the disc. The number of line pairs per revolution will then give a specific pulse count per revolution. In many applications, it is desired to have a very high density of line pairs around the perimeter of a small diameter disc. The performance of the reflective sensor is determined by the MTF for the spatial frequency, F, of line pairs on the disc. The spatial frequency for a disc is determined by Equation (48).

$$F = \frac{\text{lines/rev.}}{4\pi r} \qquad (48)$$

Using Figure 25, the spatial frequency can be determined assuming the radius is to the center point of the line pattern. Given the radius, r = 10 mm, and 220 lines/revolution, a spatial frequency of 1.75 ln pr/mm is calculated. When an HEDS-1000 is used as the sensor for this code wheel, an MTF response of 75% is obtained from Figure 14.

The code wheel is afixed to a hub which is placed on the rotating shaft. The reflective sensor is positioned perpendicular to the disc and at a distance such that the maximum signal point, MSP, is at the plane of the code pattern. The highest reflected photocurrent, I_{PR}, is obtained from a specular reflecting code pattern. This can be implemented by photolithographing a pattern of opaque bars on a shiny metallic wheel-hub assembly. A diffuse code wheel assembly should be used when the mechanical tolerance of the axial alignment of the HEDS-1000 to the normal of the code wheel exceeds 10°.

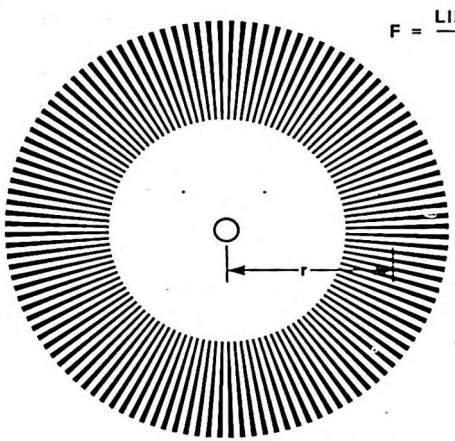


Figure 25. Spatial Frequency of a Code Wheel.

Tachometry applications allow an ac coupled amplifier to be used, such as the current feedback type in Figure 22. AC coupling the output of the HEDS-1000 eliminates the dc output offset voltage variations caused by the stray photocurrent.

HEDS-1000 Analog Tachometer

The HEDS-1000 can be used as the transducer in high speed rotary tachometry applications. Figure 26 shows a circuit diagram that uses the reflective sensor as a pulse source input to a frequency to voltage converter.

The HEDS-1000 is configured as a current feedback amplifier and ac coupled to an LM2907 frequency to voltage converter. The transistor Q_1 is used as a current source to supply the I_F to the LED emitter.

The reflective sensor generates n pulses per revolution, where n is the number of line pairs per revolution. The magnitude of the frequency, f, applied to the F-V converter is n times the number of revolutions per minute. This is the relationship shown in Equation (49).

$$n = \frac{\pi r}{\text{line width}} = \frac{2\pi r}{\text{ln pr width}} \qquad (49)$$

$$f = n \ \text{rev/min} \times \frac{1}{60} \cdot \frac{\text{min}}{\text{sec}} \qquad \text{where f = Hz}$$

The capacitor, C, is the dominant factor in determining the maximum output voltage for a required full scale frequency indication. The capacitor required to determine a full scale output voltage for a specific full scale frequency is shown in Equation (50).

$$C = \frac{V_{OUT\ FULL\ SCALE}}{R \cdot V_{cc} \cdot f_{FULL\ SCALE}} \qquad (50)$$

A $V_{OUT\ FULL\ SCALE}$ = 1V, 0–25,000 rev/min tachometer can be designed using a code wheel with a radius of 20 mm and a line width of .63 mm. The approach is to determine maximum full scale frequency from Equation (49), and then using Equation (50), the full scale frequency

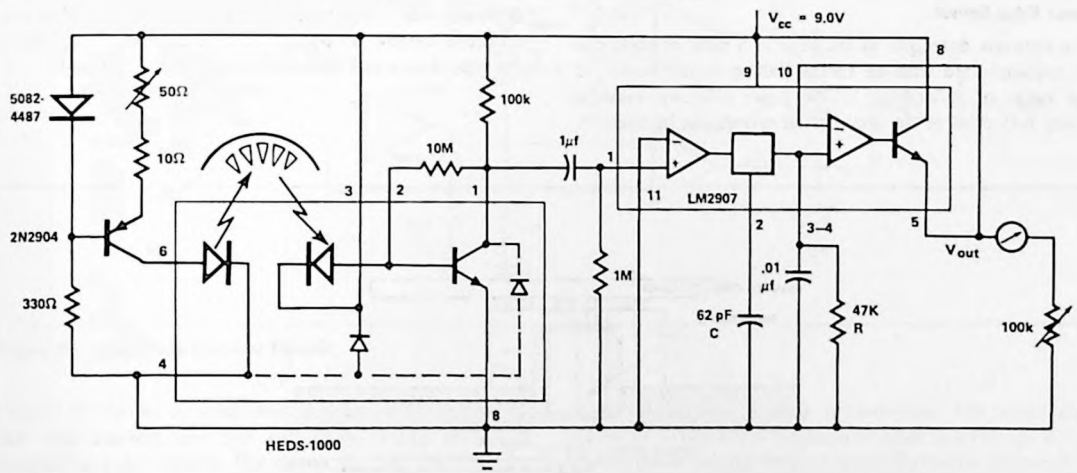


Figure 26. Analog Tachometer Circuit.

APPLICATIONS

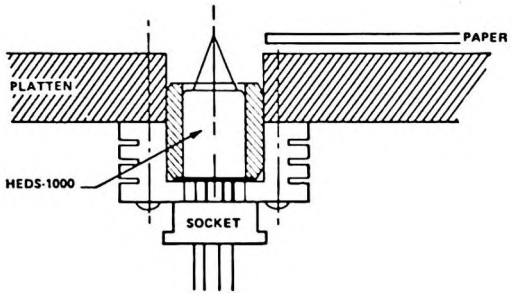


Figure 27. Reflective Type Paper Edge Sensor.

is 41.5kHz and C is calculated to be 57pF. A 62pF capacitor is used for this example.

The F-V converter will respond to a minimum input signal swing of 250mV. This input level can be insured through the use of a specular reflector. In the HEDS-1000 Total Transfer Function Section it was shown that the I_{PR} increases by 10.45dB when a specular reflector is used over a diffuse reflector. The limitation of a specular reflecting code wheel is that the HEDS-1000 alignment to the code wheel must not be greater than 10° from the normal. If the deviation is greater than 10° the image of the source will not be reflected to the detector.

Paper Edge Sensor

The accurate detection of the edge of a piece of paper can be accomplished with an HEDS-1000 reflective sensor. If the range of reflectivity of the paper is known, either a paper reflective or an obscuration system can be selected. When a paper type which is highly reflective is considered, it is desirable to utilize a reflective system of the type that positions the sensor so that the maximum signal point lies at the surface of the paper platten. This approach is shown in Figure 27. When a low reflectance paper type is being sensed, the obscuration type system may be more suitable. Such a system is shown in Figure 28.

The edge position sensing accuracy is dependent on the spot location as referenced to the mechanical system. The HEDS-1000 offers a reflective sensing spot location of ±.51 mm with respect to the package center line.

When an obscuration sensor system is used, the two transistor amplifiers shown in Figure 24 provide a convenient dc coupling to a 74LS logic family. When the reflective system is applied, a transresistance amplifier of the type shown in Figure 19 should be considered.

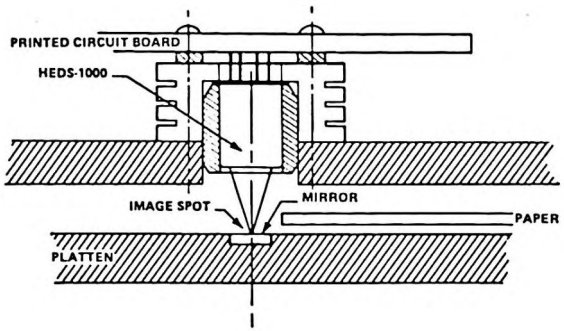


Figure 28. Obscuration Type Paper Edge Sensor.

Bar Code Scanner

A reflective optical sensor can be used as the transducer in a bar code scanner application. The bar code is an encoded form of binary data storage. The relative width difference bar to bar, and space to space, describe the typical encoding scheme of Differential Width encoding. This is the data format used in the Universal Product Code. UPC.

The sensor provides an electrical output signal with a pulse width determined by the bar and space widths, and signal amplitude dependent upon the bar and space reflection coefficients.

The Differential Width encoding scheme requires that output pulse width, bar to bar, or space to space, be an accurate representation of the distance per unit time. The accuracy of the scanning output improves when the reflecting spot size is smaller than the minimum bar or space width. The smaller the scanning image, the more abrupt the transition from bar to space.

The output signal amplitude is determined by the difference between the bar reflectance and space reflectance. The minimum output signal to maximum output signal ratio is directly proportional to the bar to space reflectance.

The signal amplifier that is interconnected to the sensor must have a large dynamic operating range to accomodate the variations of reflector types, and also provide adequate signal differential for the bar to space reflectivity difference.

Figure 13 shows the trapezoidal pulse train that is obtained from scanning a bar code of equal width bars and spaces. As the image size increases due to defocusing, the pulse train amplitude is reduced and the waveform becomes triangular. It is desirable that the amplifier provides the signal amplitude change at the same scanning location as the bar to space transition.

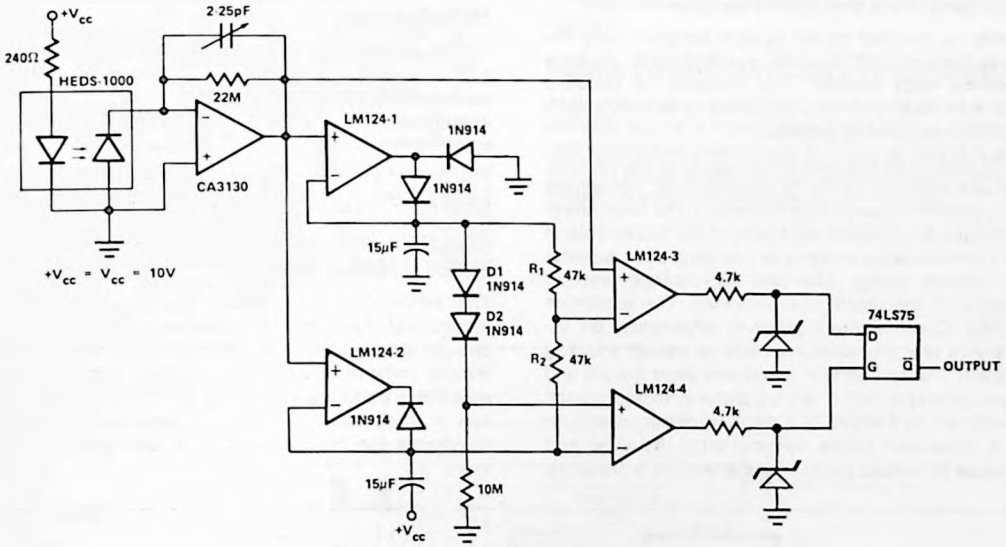


Figure 29. Bar Code Scanner Circuit.

Figure 29 shows a schematic for an amplifier system that will convert the bar and space widths into TTL compatible logic signals. The circuit uses the CA3130 as a transresistance amplifier for the HEDS-1000 photodiode. The output of the amplifier is applied to positive peak (LM124-1) and negative peak (LM124-2) detectors. The resistors R_1 and R_2 set the reference (negative-going) input to the code comparator (LM124-3) at a voltage which is halfway between the positive peak and the negative peak, so the switching threshold is therefore at 50% of the peak-to-peak modulation. The noise gate (LM124-4) compares the negative peak to a voltage which is two diode voltage drops (D_1 and D_2) below the positive peak, so unless the peak-to-peak amplitude exceeds two diode drops, the G input of the 74LS75 remains low and $\overline{Q}$ cannot change. This ensures that the $\overline{Q}$ output of the 74LS75 will remain fixed unless the excursions at the output of the CA3130 are of adequate amplitude (two diode drops) that noise will not interfere.

APPLICATIONS

HEWLETT PACKARD

APPLICATION NOTE 1011

Design and Operational Considerations for the HEDS-5000 and HEDS-6000 Incremental Shaft Encoders

INTRODUCTION

A shaft encoder is a component which translates the rotational movement of a shaft into an electrical waveform.

This note is directed to the system designer using the Hewlett-Packard HEDS-5000 or HEDS-6000 modular incremental shaft encoder. The contents are therefore specific and require initial understanding of shaft encoders and their associated systems.

The first section of this note briefly analyzes the theory of design and operation of the HEDS-5000/6000. The second section, covering Design Considerations and Error Analysis, provides an in-depth treatment of the relationship of motor mechanical parameters to encoding error accumulation. Several design examples demonstrate practical utilizations of the techniques presented. The section on Operating Considerations presents information on assembly and test procedures as well as trouble shooting and repair. The last section introduces some circuits and software concepts which will be useful in interfacing the shaft encoder to a digital or a microprocessor based system. A selection guide summarizing the uses and advantages of various encoder characteristics is presented in the Appendix. Also included is a selection of motors suitable for mating with the HEDS-5000/6000 encoders.

DESCRIPTION

A shaft encoder used in a system such as a servo motor control enables the use of digital components in the loop, i.e., a microprocessor instead of servo amplifier, thus lowering the total system cost. A typical digital control loop is shown in Figure 1.

The optical shaft encoder offers several advantages over other encoder types. It is noncontacting, thus it does not burden the system with added inertia and friction, and is inherently more reliable. The encoding speed is high and it offers high noise immunity.

The HEDS-5000/6000 series are families of modular incremental shaft encoders. Two similar channels whose outputs are in quadrature (90 degrees phase difference) provide velocity and direction information. An optional third index pulse channel can provide an absolute indication of shaft rotation once per revolution. The output waveforms are digital and compatible with TTL/LSTTL logic.

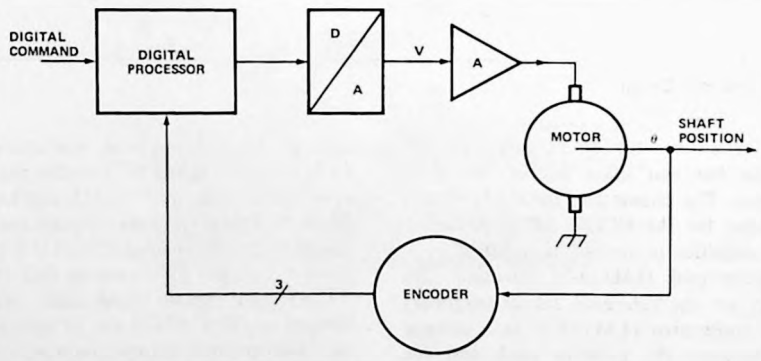


Figure 1. Digital Motor Control Block Diagram

Hewlett-Packard HEDS-5000/6000 series encoders are offered in a large number of standard resolutions and shaft sizes. The HEDS-5000/6000 data sheets describe standard available products. Other resolutions, shaft diameters, and output waveforms are possible and may be designed upon custom request. Consult the factory or your local HP Sales Office for assistance.

The modular encoder kit is assembled from three parts:

1. The Encoder Body, which contains the phase plate, detectors, and integrated circuits.
2. The Code Wheel, which is mounted on the system's shaft.
3. The Emitter End Plate, containing the light source (LED), which snaps onto the body to form a dust resistant unit.

The assembled HEDS-5000 is approximately 28 mm in diameter and 18 mm high. The HEDS-6000 is approximately 56 mm in diameter and 19.5 mm high. Both have a 0.6 metre flat cable providing the electrical connections.

Further physical and parametric information on the products are provided in the HEDS-5000 and HEDS-6000 data sheets.

THEORY OF OPERATION

A light beam interrupted by a rotating code wheel is the essence of an optical shaft encoder. To allow for higher resolution at a given diameter than that achievable by a simple direct beam interruption method, a mask or "Phase Plate" is placed in the light path above the photo detectors. Both the code wheel and the phase plate display a similar pattern of slits and bars, and when viewed together they form what is known as a Moire pattern. The light from the LED can only reach the detectors when the code wheel slits are aligned with the slits on the phase plate, and since the code wheel is rotating, the detector receives alternating periods of light and dark.

As the resolution of the encoder is increased and the line spacing of the code wheel is decreased, satisfactory operation becomes very sensitive to the collimation of the light transmitted through the code wheel and phase plate, as well as sensitive to the gap spacing between the code wheel and phase plate. To increase the reliability of operation, the HEDS-5000/6000 employs an aspherical lens system and miniature point source emitter which highly collimates the light beam. This highly collimated light allows the code wheel and phase plate separation to be much greater than that achieved in existing discrete component encoders, and also reduces the encoder's sensitivity to shaft axial end play.

Each channel contains two photodetectors with corresponding phase plate patterns spaced in a manner that causes one detector to be dark while the other is fully illuminated. The currents produced by the photodetectors are amplified by a differential amplifier (push-pull). The differential configuration reduces the sensitivity to LED light level changes and thus eliminates the need for any electrical gain adjustments. Digitizing for each channel is accomplished by a comparator which switches when the analog values are equal. The output of the comparator provides TTL/LSTTL compatible logic signals.

A block diagram of the HEDS-5000/6000 is presented in Figure 2.

DESIGN CONSIDERATIONS & ERROR ANALYSIS

As in most measurement systems, the encoding process is not error free. It is important to know the causes of errors and understand their effects in order to select a suitable encoder and to define the mechanical requirements of the system on which the encoder will be mounted.

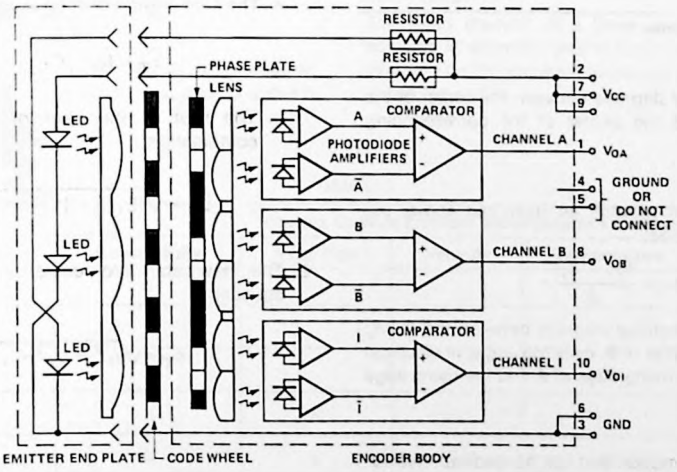


Figure 2. HEDS-5000 and HEDS-6000 Block Diagram

DEFINITIONS

Angular Degree:
The mechanical unit of shaft rotation, i.e., one shaft rotation = 360 degrees.

Code Wheel Count (N):
The number of bar and space pairs around the code wheel, i.e., N=500 in the HEDS-5000 — AXX.
N=1000 in the HEDS-6000 — BXX.

Cycle:
The portion of the output waveform which corresponds to the occurence of a full light and dark period on one detector pair, i.e., there are N cycles in one complete shaft rotation.

Electrical Degree:
The units of the output waveform: 1 cycle = 360 Electrical Degrees = 360/N angular degrees.

Pulse and State Widths:
Portions of the quadrature output of the encoder. See Figure 3 for definitions.

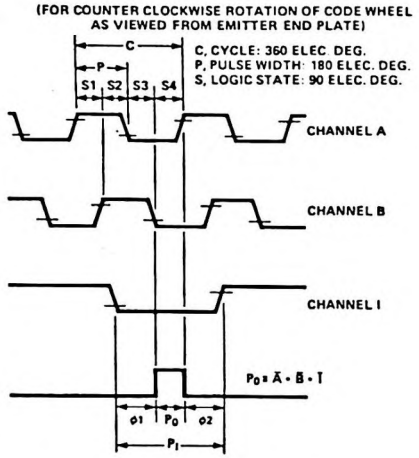


Figure 3. Output Waveforms

Phase:
The angle in electrical degrees between the center of the channel A pulse and the center of the corresponding channel B pulse.

Index Phase:
For counter clockwise rotation as illustrated above, the Index Phase is defined as:

$$\Phi_I = \frac{(\phi_1 - \phi_2)}{2}.$$

ϕ_1 is the angle, in electrical degrees between the falling edge of I and falling edge of B. ϕ_2 is the angle, in electrical degrees, between the rising edge of A and the rising edge of I.

Resolution:
The smallest angular motion that can be resolved. Resolution can be expressed as either the number of output transitions in one complete revolution or as the angle of shaft rotation between two consecutive transitions.

ENCODING CHARACTERISTICS

Since there are N cycles per each shaft revolution, there are N values for each encoding parameter. In the HEDS-5000/6000 data sheet encoding errors are defined in the following manner:

- Typical Error: The average value (over a large batch of encoders) of the maximum error observed in a complete shaft revolution of each encoder.
- Maximum Error: The largest error that should be observed in any batch.

STATISTICAL NATURE OF ERRORS

In a modular encoder, the encoding characteristics of a particular unit cannot be measured directly until the unit is assembled on a system. It would be useful to be able to predict its performance, but, while the errors of any particular unit cannot be predicted with certainty, a statistical treatment will usually result in a good approximation to the behavior of a large batch. The distribution of component characteristics is usually Gaussian and can be described by its mean ($\bar{E}$) and standard deviation (σ). In the case of encoder errors, $\bar{E}$ is defined to be the average of the absolute value of the errors.

When two (or more) factors combine to form a third parameter, their errors can combine vectorially or algebraically. In a vectorial combination, the resultant error could be smaller or larger than the original errors (and sometimes zero). For example, the eccentricity resulting from the random assembly of a code wheel (which has an eccentricity error) and an eccentric shaft is a vectorial combination. An algebraic combination occurs when the two errors always make the resultant error larger as is the case when the pulse width error combines with the phase error to produce state width error.

When estimating the distribution of an error derived from such combinations, the following formulas are used:

1. The new mean is either:
   a. The sum of means in an algebraic combination

$$\bar{E}_T = \bar{E}_1 + \bar{E}_2 + \ldots\ldots \bar{E}_n$$

   b. The root of the sum of squares in a vectorial combination

$$\bar{E}_T = \sqrt{(\bar{E}_1)^2 + (\bar{E}_2)^2 + \ldots\ldots (\bar{E}_n)^2}$$

2. The new standard deviation is derived from the equation:

$$\sigma_T = \sqrt{\sigma_1{}^2 + \sigma_2{}^2 + \ldots\ldots \sigma_n{}^2}$$

DESIGN CONSIDERATIONS

The performance of a modular shaft encoder is affected by assembly and shaft tolerances to a much greater degree than in a pre-assembled encoder with self-contained shaft and bearings. Those factors plus shaft velocity, temperature, and others combine with the intrinsic encoder characteristics to yield the resultant accuracy. A quantitative discussion of the relationship between environmental conditions and accuracy can only be made for a specific encoder type, (i.e., the HEDS-5000/6000), although the general concepts can be extended to others.

Table 1 summarizes the relationships between the encoding parameters and the environmental factors that affect them.

The check mark indicates that the factor listed affects the corresponding encoding characteristics. As can be seen, cycle uniformity is virtually unaffected by factors outside the encoder, while the state width which is the sum of all the encoder transitions will be affected by most of these factors.

Eccentricity and Radial Play

Eccentricity primarily affects position, phase and state width errors. A quantitative discussion of this factor is presented in the specific Encoder Errors section.

The shaft eccentricity which affects the encoder performance is actually a combination of four separate and independent factors:

- Eccentricity: the cyclic off-axis motion of the shaft.
- Radial Play: the random motion due to bearing tolerance and uneven loading.
- Shaft Undersize Tolerance: the cyclic off-axis motion of the code wheel caused by off center mounting of the hub on an undersize shaft.
- Code Wheel/Hub Assembly: the cyclic off-axis motion of the code wheel caused by off center mounting of the code wheel with respect to the hub bore.

Shaft Axial Play

The shaft axial play affects mainly the phase (or quadrature) between the two encoder channels, and to a much lesser degree the pulse width. Aside from phase jitter considerations, the axial play should be restricted to less than 0.5 mm for the HEDS-5000 and 0.58 mm for the HEDS-6000, due to the physical constraints of the encoder. The recommended assembly procedure protects the code wheel and phase plate by holding the shaft at its closest point to the phase plate when setting the code wheel. The axial motion is therefore always in the direction of increasing separation, which increases reliability without deteriorating the pulse width performance. When the maximum allowable play is exceeded, the top of the code wheel hub can hit the Emitter End Plate, which is not necessarily catastrophic but certainly undesirable.

Velocity and Temperature

Both position and cycle accuracy are measured between similar transitions of the output waveform and are virtually unaffected by the velocity of rotation. Since counting cycles (by toggling a TTL counter or a similar device) require only a very small time between the logic transitions, the count frequency can typically reach 200 kHz before losing count.

On the other hand, the pulse width is measured between two different transitions and the accuracy will be limited by any difference in the propagation delay of the transitions. This time difference becomes a greater portion of the Pulse Width as the frequency is increased. Propagation delays are also slightly affected by temperature variations.

Assembly

The only adjustment necessary during the assembly of a two channel HEDS-5000/6000 is optimization of the phase between channels. The phase adjustment aligns the axial center of the phase plate pattern to match that of the code wheel. The average phase between channels A and B should be adjusted to 90 degrees. The error in the adjustment process can be limited to about 10 degrees using an oscilloscope presentation of the output. Tighter adjustment tolerances can be achieved by using an averaging phase meter as described in the assembly procedure section, Figure 11.

The index channel of a three channel encoder is also adjusted at assembly and is typically aligned so that P_I is centered on the low state combinations of channels A and B (see Figure 3).

Table 1

Encoding Characteristic	Factors Outside Encoder Manufacturer's Control				
	Eccentricity	Axial Play	Velocity	Temperature	Assembly
Position Accuracy	X				
Cycle Uniformity	X				
Pulse Width			X	X	
Phase	X	X			X
State Width	X	X	X	X	X

ENCODER ERRORS

Each encoder characteristic contains errors resulting from the relationship between the internal encoder components and the environment. As previously shown, more than one environmental factor affects any encoding error. The discussion below will define these encoder errors, discuss the primary factors contributing to the errors and provide sample calculations as necessary.

Position Error

Position error expressed in minutes of arc or electrical degrees is defined as the difference between the actual shaft position and the position as determined by the output of the shaft encoder. Figure 4 illustrates position error for a code wheel with 8 cycles per revolution.

Position error is primarily caused by off-axis rotation of the code wheel with respect to the phase plate and detectors. The effect of eccentricity is inversely proportioned to the code wheel radius. The position error, $\Delta\theta$, resulting from eccentricity is calculated as follows:

$$\Delta\theta = \frac{kE}{R} \text{ (degrees)}$$

where

$$k = \frac{360}{2\pi}$$

E = eccentricity (mm TIR)

R = code wheel radius

= 10.9 mm for the HEDS-5000

= 22 mm for the HEDS-6000

A sensitivity factor Q_p can be defined in order to estimate the contribution of eccentricity to position error.

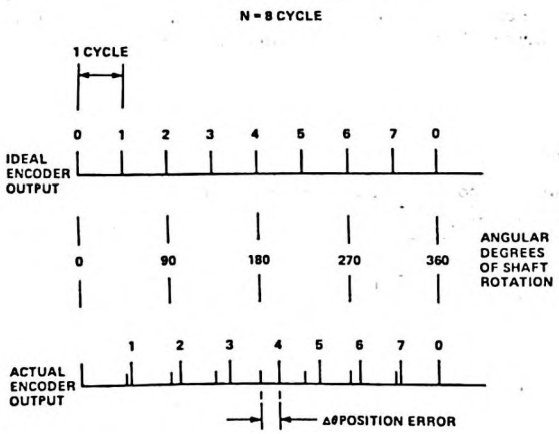


Figure 4. Shaft Encoder Transitions vs. Angle of Rotation

$$Q_p = \frac{k}{R} = 5.3 \text{ angular degrees/mm of eccentricity for the HEDS-5000}$$

$$= 2.6 \text{ angular degrees/mm of eccentricity for the HEDS-6000}$$

Code wheel and phase plate artwork contribute to position error; however, the magnitude is small and can be neglected. Note that position error is inversely related to the radius of the code wheel. Therefore, the HEDS-6000 will have a smaller position error than the HEDS-5000.

Position error is a concern for high resolution positioning systems. The following example estimates position error of the HEDS-5000 based upon eccentric motion of the code wheel pattern. Calculations for the HEDS-6000 are similar. Such eccentric movement affecting the encoder is actually a combination of the four separate and independent factors discussed earlier.

To Calculate Position Error

1. List the contributing factors. Table 2 presents data which is consistent with the recommended operating conditions as specified in the HEDS-5000 Data Sheet. Code wheel/hub assembly data presented is impirically determined for the HEDS-5000.

Table 2

Contributing Factor	Mean $\bar{E}$	Std Dev. σ
Code Wheel/ Hub Assembly	0.040 mm	0.015 mm
Shaft Eccentricity	0.020 mm	0.005 mm
Shaft Undersize	0.015 mm	0.010 mm

Note that shaft radial play is not included due to the random nature of the contribution. The three factors listed cause predictable cyclic error that are combined vectorially. Radial play contributes to phase and state width error as explained in the following sections.

2. Combine the errors as outlined in the section on the statistical nature of errors to calculate the vector sum of the mean:

$$\bar{E}_T = \sqrt{(\bar{E}_1)^2 + (\bar{E}_2)^2 + (\bar{E}_3)^2}$$

$$= 4.7 \times 10^{-2} \text{ mm}$$

Compute the standard deviation

$$\sigma_T = \sqrt{\sigma_1^2 + \sigma_2^2 + \sigma_3^2}$$

$$= 1.9 \times 10^{-2} \text{ mm}$$

3. To estimate the encoder accuracy it is necessary to multiply by the total eccentricity factor Q_p which denotes the contribution to position error. Recall that

Q_p = 5.3 angular degrees/mm eccentricity

for the HEDS-5000, N = 500. The average position error, $\Delta\theta$, is:

$$\Delta\overline{\theta} = \overline{E}_T Q_p$$

$$= (4.7 \times 10^{-2}\,\text{mm})\ (5.3 \text{ angular degrees/mm})$$

$$= 0.25 \text{ angular degrees}$$

$$= 15 \text{ minutes of arc}$$

The standard deviation $\sigma(\Delta\theta)$ is:

$$\sigma(\Delta\theta) = \sigma_T Q_p$$

$$= (1.9 \times 10^{-2}\,\text{mm})\ (5.3 \text{ angular degrees/mm})$$

$$= 0.1 \text{ angular degrees}$$

$$= 6 \text{ minutes of arc}$$

The maximum position error $\Delta\theta_{max}$ is approximately:

$$\Delta\theta_{max} = \Delta\overline{\theta} + 2\,[\sigma(\Delta\theta)]$$

$$= 0.25 + 2\,(0.1) \text{ angular degrees}$$

$$= 27 \text{ minutes of arc}$$

$$= 225 \text{ electrical degrees}$$

($\overline{x} + 2\sigma$ will contain 98 percent of a normal distribution)

The relationship between shaft eccentricity and position accuracy is illustrated in Figure 5 for the HEDS-5000 and HEDS-6000. The residual position error (where shaft eccentricity = 0 in Figure 5) denotes the code wheel/hub assembly contribution to position error. The remainder of the graph includes contribution from both shaft eccentricity and shaft undersize. $E_T + 2\sigma_T$ from our example yields 0.085 mm for maximum eccentricity which corresponds to about 27 minutes of arc on the typical curve for the HEDS-5000. The 99 percentile curve is an indication of the manufacturing process distribution giving rise to the residual position error.

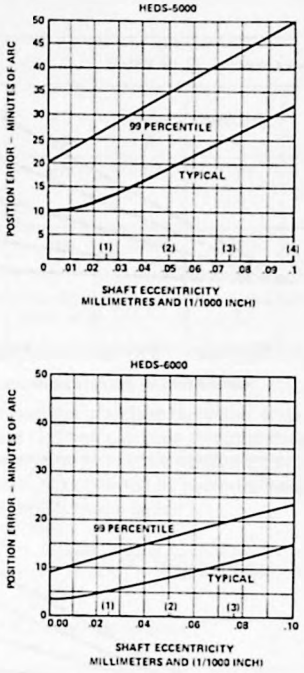


Figure 5. Position Error vs. Shaft Eccentricity

Cycle Error

All cycles will contain 360 electrical degrees; however, the number of mechanical degrees represented by each cycle may vary from the ideal of 360/N. Cycle error, ΔC, is usually expressed in electrical degrees, hence the equivalent angular error:

$$\text{Angular Cycle Error} = \frac{\Delta C}{N}$$

The quality of the code wheel and phase plate artwork is the main factor affecting the cycle error. Data on this parameter is presented in the data sheet. Eccentricity has a minor affect on cycle error and need not be calculated as a significant contribution.

Pulse Width Error

Pulse width error is the maximum deviation of the pulse from the nominal value of 180 electrical degrees.

Although the use of a differential amplification greatly reduces the sensitivity to component and circuit variables, some pulse error will result from a non-uniform light pattern impinging on the differential detectors or an imbalance of the differential elements. An additional error can be observed if, over the temperature range, the encoder is run at high velocities. This is caused by the unequal propagation delays of the falling and rising edges of the digital pulse trains. As with most I.C. parameters, this propagation delay differential is temperature dependent. At 25 degrees centigrade the propagation delays are nearly equal but with increasing or decreasing temperature the delays become unequal.

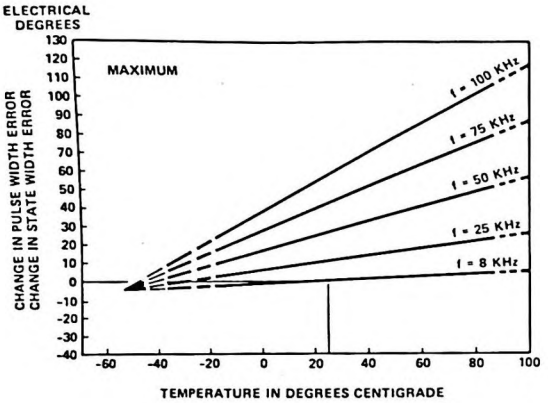
Figure 6 shows maximum and typical values to expect in pulse width error due to changes in temperature and velocity.

Phase Error

Phase error is the maximum deviation from the nominal value of phase (90 electrical degrees) between channel A and channel B.

Since phase does not extend between two output transitions, strictly speaking it is not an encoding parameter. But since phase error is a direct contributor to State Width Error, it is important to understand the mechanism by which phase error arises.

The average phase of most encoder systems is adjusted during the assembly procedure to be as close as possible to the nominal value of 90 degrees. This helps to average out cyclic variations in phase during a shaft rotation. Therefore the design concern is primarily with respect to the amount that the phase varies as the shaft moves randomly during its rotation.



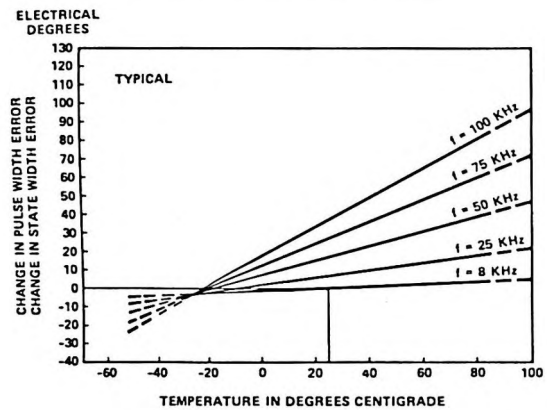


Figure 6. Typical and Maximum Changes in Pulse Width Error and State Width Error vs. Temperature

A shift of the phase between the two encoder channels occurs due to the axial, radial and eccentric movement of the code wheel pattern with respect to the phase plate.

Phase Error Due To Radial Play

The radial play and eccentricity will change the phase in an amount inversely proportional to the square of the code wheel radius, and proportional to code wheel count N.

$$\Delta\phi_R = \frac{K_2\,NE}{R^2}\cdot$$

A phase sensitivity factor can be defined in order to estimate the contribution of radial play and eccentricity to phase error.

$$Q_e = \frac{K_2 N}{R^2}$$

= 520 electrical degrees/mm (typical for the HEDS-5000, N = 500)

= 227 electrical degrees/mm (typical for HEDS-6000, N = 1000)

The contribution that phase error has on state width error is calculated in the state width error design example and is divided between cyclic eccentricity and random shaft radial play.

Phase Error Due to Axial Movement

Axial movement will also result in a change of phase if the light beams illuminating the two channels are not perfectly parallel. The equation governing phase change due to axial movement is:

$$\Delta\phi_A = \Delta G \cdot Q_{ma}$$

where:

ΔG = change in gap due to axial play (mm)

Q_{ma} = misalignment factor (electrical degree/mm)

A typical value for Q_{ma} as observed in a sample of a HEDS-5000/6000 production run is:

$$Q_{ma} = 20 \text{ degree/mm}$$

Total Phase Error

Phase error contributions due to radial play and axial movement are summed vectorially to give total Phase Error:

$$\Delta\phi_T = \sqrt{\Delta\phi_R{}^2 + \Delta\phi_A{}^2}$$

State Width Error

State Width Error is the maximum deviation of the state width from its nominal value of 90 electrical degrees.

Since the State Width is the combination of all the encoder's transitions, all of the factors which contribute to pulse width and phase error will also contribute to state width error. These error contributions can best be thought of as falling into three categories. The first includes eccentricity contributions resulting in cyclic errors as outlined in the preceding position error section. The second category is factors creating random errors. The third category includes those factors that are due to the intrinsic design of the encoder such as lens quality, I.C. switching characteristics, and I.C. hysteresis. For the HEDS-5000/6000, this collective error is 5 electrical degrees on the average.

A quantitative discussion of the effect that these factors have on state width error is presented in the following design examples.

DESIGN EXAMPLES

In the following examples the state width error of a hypothetical production batch will be estimated. State width is crucial in providing direction information. Thus a minimum state width must be maintained over the whole range of operating conditions. The value of that minimum can range from 1 to 20 electrical degrees or more, and is dependent upon the type of counting circuitry used where directional information must be obtained. Two approaches to the analysis will be discussed. First, state width error at room temperature will be estimated without considering

velocity extremes. The second example will answer the question, "What should the test limit at room temperature be to ensure a minimum state width at the extremes of the temperature and velocity ranges?"

Not all of the numbers required in the procedure are available in the data sheet. HEDS-5000/6000 data sheet values are used where possible, and the other encoder values were empirically derived from testing of production assemblies. The numbers relating to shaft variables must be estimated or measured by the designer. The values used below are only for a particular set of motor parameters within the recommended operating conditions of the HEDS-5000/6000. The examples also assume that a phase error adjustment has been made during assembly so that average phase error over 360 mechanical degrees is nearly zero.

Any error in phase results in a corresponding error in state width of equal magnitude. Therefore the sensitivity factors established for phase are used in calculating state width error.

Room Temperature Analysis Example

ECCENTRICITY, ΔS_1

Total code wheel pattern eccentricity was estimated in the position error example.

Mean eccentricity = 4.7×10^{-2} mm

Standard deviation of eccentricity = 1.9×10^{-2} mm

The effect of eccentricity on the state width is obtained by multiplying the total expected eccentricity by the phase sensitivity factor Q_e = 520 electrical degrees/mm.

Since eccentricity is measured as a peak-to-peak value (TIR) and average phase error has been preadjusted to be nearly zero, then the maximum expected movement of the code wheel with respect to the phase plate should be less than or equal to 1/2 the TIR values specified for eccentricity. Hence the mean and standard deviation values for eccentricity used in calculating ΔS_1 are divided by two.

The following calculations are for the HEDS-5000, N = 500. Calculations for the HEDS-6000 are similar.

The eccentricity contribution ΔS_1, is:

$$\overline{\Delta S_1} = \left(\frac{4.7 \times 10^{-2}\,\text{mm}}{2}\right) (520 \text{ electrical degrees/mm})$$

$$= 12.2 \text{ electrical degrees}$$

$$\sigma(\Delta S) = \frac{(1.9 \times 10^{-2}\,\text{mm})}{2} (520 \text{ electrical degrees/mm})$$

$$= 4.9 \text{ electrical degrees}$$

RANDOM PHASE, ΔS_2

The contributing factors to random phase should be estimated in conjunction with a Q factor relating to their contribution to state width error. Table 3 summarizes these factors. The shaft axial play and radial play in this example were derived from a typical 31.75 mm (1-1/4 in.) motor with ball bearings. Again, the phase sensitivity factors, Q_e and Q_{ma} which were presented earlier, are used to establish error contribution. The number presented for assembly errors were derived from a typical production run using a phase meter (see "Test Procedures" section) as an adjustment aid.

Table 3

Factor	Units	Mean $\overline{E}$	Std. Dev. σ	Phase Sensitivity Factor, Q
Shaft Axial Play	mm	0.1	0.06	Q_{ma} 20 elect. deg./ mm
Shaft Radial Play	mm	0.006	0.003	Q_e 520 elect. deg./ mm
Assembly Adjustment	Elect. Deg.	3	3	none

Multiply the mean and standard deviation of each factor by the appropriate Q. Then calculate the total mean contribution by vectorially combining the weighted means. The total standard deviation is obtained by vectorially combining the standard deviation for each factor.

$$\overline{\Delta S_2} = \sqrt{[(0.1)\ 20]^2 + [(0.006)\ 520]^2 + [3]^2}$$

$$= 4.7 \text{ electrical degrees}$$

$$\sigma(\Delta S_2) = \sqrt{[(0.06)(20)]^2 + [(0.003)\ (520)]^2 + [3]^2}$$

$$= 3.5 \text{ electrical degrees}$$

INTERNAL ERRORS, ΔS_3

The combination of errors intrinsic to the HEDS-5000 and not directly affected by shaft and assembly tolerances are a result of lens quality, IC switching characteristics and miscellaneous tolerances. These affects summed are approximately the following:

$$\overline{\Delta S_3} = 5 \text{ electrical degrees}$$

$$\sigma(\Delta S_3) = 8.4 \text{ electrical degrees}$$

This data was obtained from sample production lots.

Error Distribution

The state width error distribution is computed by algebraically summing* the means of Eccentricity, Random Phase, and Internal Errors. The standard deviations are combined vectorially.

Mean State Width Error $\overline{\Delta S_T} = 12.2 + 4.7 + 5$

$$= 21.9 \text{ electrical degrees}$$

Standard Deviation of State Width Error $\sigma(\Delta S_T) = \sqrt{(4.9)^2 + (3.5)^2\ (8.4)^2}$

$$= 10.3 \text{ electrical degrees}$$

*The error contributions are algebraically summed in order to obtain a worst case performance.

The example above predicts the mean state width error for an encoder batch would be less than 25 electrical degrees when parameters are kept within the recommended operating conditions as specified in the HEDS-5000 data sheet. The state width error for 99% (2.3 σ) of the batch is computed as follows:

$$\Delta\overline{S}_T = \Delta S_T + 2.3\ [\sigma\Delta(S_T)]$$

$$= 21.9 + (2.3)\ (10.3)$$

$$= 45.5 \text{ electrical degrees}$$

and is approximately 45 electrical degrees. Note: these figures agree with the state width error as specified in the HEDS-5000 data sheet.

Encoders and motors with characteristics resembling the example have been assembled and tested. The resultant state width error histogram is illustrated in Figure 7.

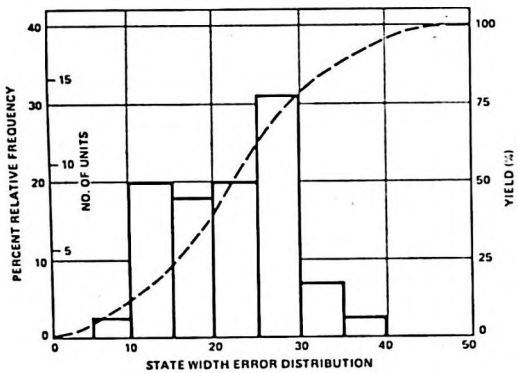


Figure 7. State Width Error Distribution Sample Manufacturing Batch

Designing for Temperature Range

To ensure decoding over the full temperature range the HEDS-5000/6000 data sheets are complete with graphs similar to Figure 6 showing maximum and typical pulse width and state width errors vs. temperature and velocity.

OPERATING CONSIDERATIONS

Assembly Mounting Surface

The encoder may be mounted directly on a motor which has a two-sided shaft extension or on a remote bearing support at the end of a shaft.

In either case, the mounting surface should be flat and smooth. No special operations are required for the surface finish except removal of burrs that might interfere with the phase adjustment operation which entails sliding the encoder over the mounting surface. The HEDS-5000 is attached by means of three screws, two for the HEDS-6000. The mounting surface for each encoder should therefore be drilled as shown in Figure 8 below and tapped with metric or English threads as required.

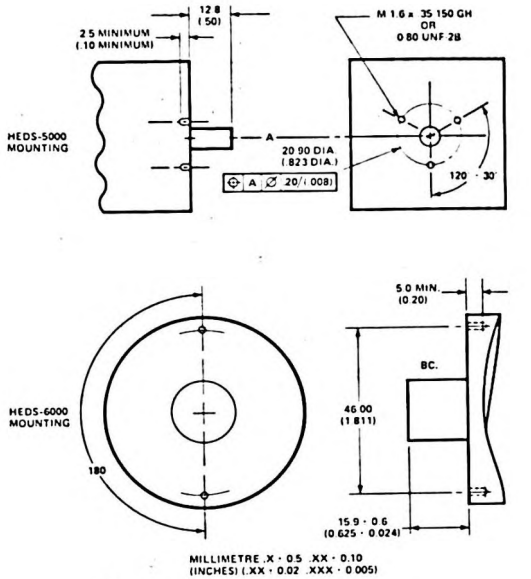


Figure 8. Mounting Requirements

Adhesives

Two different kinds of adhesives are used in the assembly of the encoder.

R.T.V. (silicone rubber) is used on the mounting surface to fill the following functions:

1. Provide a lubricating medium to ease the sliding of the encoder while adjusting phase.
2. Provide a flexible adhesive to accommodate differentials in expansion coefficients between the encoder and its mounting surface.

Dow Corning 3145 (or GE 162) was chosen because in addition to meeting the criteria above, they are non-corrosive and do not emit corrosive vapors.

The Hysol epoxy used in mounting the code wheel onto the shaft was selected to provide a rigid bond when set, and it presents a reasonable compromise between initial viscosity necessary for holding the code wheel in position before setting, setting time, and useful pot life. R.T.V. can be used with success on shaft sizes greater than 1/4 inch. However, the use of R.T.V. on shaft sizes smaller than 1/4 inch is not recommended since the smaller contact area results in a smaller initial holding force and a weaker bond.

ASSEMBLY PROCEDURE

CAUTION: The shaft encoder circuitry may be damaged by an electrostatic discharge. The cable extremities are the susceptible areas. Normal precautions such as ground straps for assembly personnel should eliminate any damage due to electrostatic discharge.

The HEDS-5000/6000 data sheet describes in detail a typical assembly procedure. While the exact procedure in any manufacturing environment will differ due to the variety of applications, it is worthwhile to understand the underlying rationale in the assembly before establishing a specific procedure. There are three steps which may affect the encoder's performance: centering, gap setting and phase adjustment.

Centering the HEDS-5000 encoder around the shaft using the cone tipped tool (HEDS-892X) provides easier screw insertion and a good starting point for the final phase adjustment. Centering the HEDS-6000 can be done by sight.

Although the HEDS-5000/6000 is very tolerant of variations in gap between the code wheel and the fixed phase plate, only a correct initial gap setting will assure full benefits from this feature. It is essential that the code wheel does not touch the phase plate through its rotation, axial movement and vibration. The HEDS-5000 makes use of a gap setter which sets the code wheel/phase plate gap to approximately 0.63 mm, referenced from the top of the encoder body. The code wheel/phase plate gap of the HEDS-6000 is set by leveling the code wheel hub to the encoder body top. Applying R.T.V. on the emitter end plate is recommended as a dust shield but is not required in dust-free environments.

The final step in the assembly is the phase adjustment which can also serve as the final inspection. As mentioned before, in most applications this is a necessary step to provide the required encoding characteristics. Since it is a contributor to state width error, the average phase should be adjusted to a value as close as possible 90 electrical degrees. A plus or minus 10 degree adjustment can be easily achieved using a phase meter as described in the "Test Procedures" section. Adjustment according to an oscilloscope trace of the output is less accurate and demands more training, but the above requirements can be achieved with the proper care and attention.

Where phasing between channels is not of concern (tachometer applications) or if a large initial deviation from proper phasing can be tolerated and corrected, phase adjustment may be modified or omitted.

TEST PROCEDURES

All piece parts of a modular encoder are tested at the factory prior to shipment. Testing the piece parts at the customer's location is difficult since it requires specialized test fixtures. The encoder can best be tested after it is assembled, although some simple tests can be incorporated if an incoming inspection is required.

INCOMING INSPECTION

For Encoder Piece Parts:

Code Wheel: Visually check for shipping damage, i.e., bending or dents which exceed the data sheet limits (code wheel part drawing).

Emitter End Plate: The LEDs can be turned on by passing current through the emitter end plate leads. See Figure 9. The current should be limited to 10 mA and the supply voltage compliance should not exceed 10V for the protection of the LEDs.

Encoder Body: When the 5V supply and ground are connected through the 10 pin connector, the outputs can be observed on a scope. Moving the encoder body in front of an illumination source (e.g., light bulb) will cause the outputs to toggle.

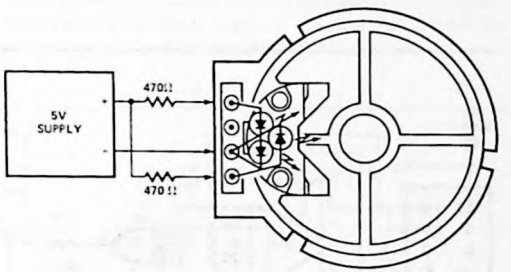


Figure 9. Emitter End Plate Test Configuration

For Motors:

Shaft: For shaft tolerance definitions and testing see Appendix C.

Assembly: The gap at which the code wheel was set cannot be measured directly but with some practice a visual estimate can be made by observing, with proper magnification, the parallax between the code wheel slits and the phase plate pattern.

Phase Adjustment/Final Test: The final step in assembly is the phase adjustment. It can be achieved using a scope or an averaging phase meter. The set up and waveform for the scope test are presented in Figure 10. When setting the phase, it is advisable to turn the shaft in both directions and adjust for minimum phase error.

Figure 11A is a schematic for an averaging phase meter which makes the task of adjusting the phase between channels easier and more accurate.

Operating Instructions:

1. Observe the LEDs on the phase meter to verify that the shaft rotation and LED director indication correspond.
2. Recheck shaft direction or adjust the phase until correct.
3. Adjust the encoder (see assembly instructions in data sheet) for zero reading on the phase meter.

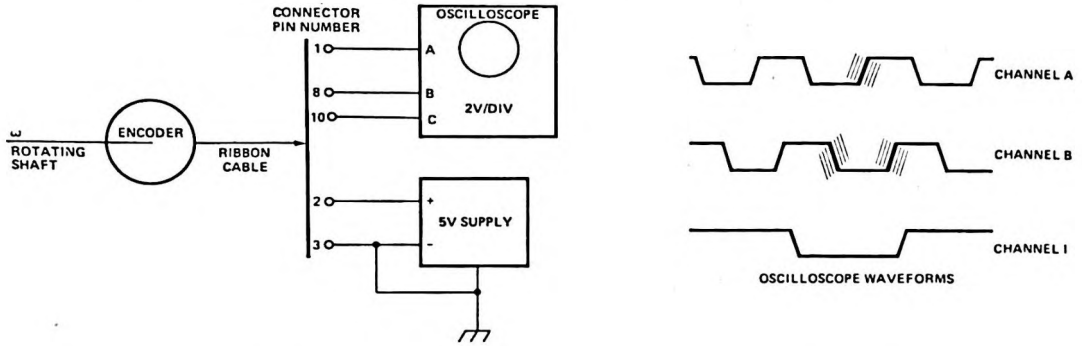
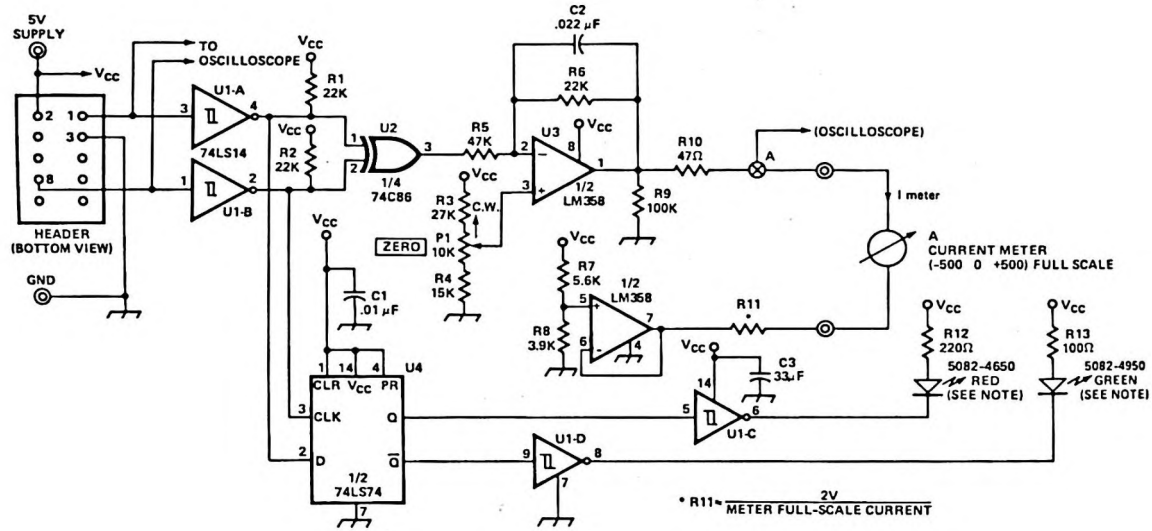
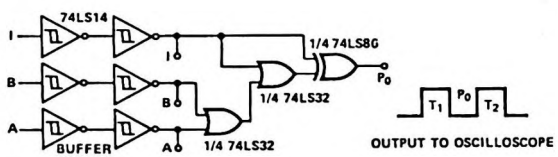


Figure 10. Scope Test Set-Up



NOTE: THE RED L.E.D. IS LIT WHEN CHANNEL A (PIN 1) IS THE LEADING WAVEFORM.

A. Phase Meter Circuit



B. Index Pulse Positioning Circuit

Figure 11. Phase Meter Circuit and Index Pulse Positioning Circuit

If the index channel is to be used, some applications require that it be aligned with the main data channels. The index pulse position and the phase must be adjusted simultaneously. This procedure sets the index phase to zero.

After channel A and B have been phased using an oscilloscope or phase meter circuit, use an oscilloscope and the circuit shown in Figure 11B, and set the trigger for the falling edge of the I output. Adjust the index pulse so that T_1 and T_2 are equal in width. The physical adjustment is a side motion (see assembly instructions in data sheet).

Repeat the process until both phase and index pulse positions are as desired.

Note: Occasionally due to statistical variations in the pieceparts, a high pulse width or phase error may be observed and can be improved by replacing the emitter end plate with another. The original end plate can subsequently be used on another unit, usually without causing the problematic symptoms.

TROUBLE SHOOTING AND REPAIR

The HEDS-5000/6000 does not require any adjustments after it is assembled, thus minimizing the need for field service. The emitter end plate can be removed, but care must be exercised to prevent bending the wire leads on the encoder body. Pry slots are provided on the end plate circumference for easy opening. When the end plate is removed, a light source can be directed towards the encoder body and the shaft rotated to observe the change of state in the output channels. If the encoder body checks OK, and the wire leads are inspected, a new end plate can be snapped into place and the encoder retested. The removed end plate can then be inspected as described in incoming inspection procedures.

OPERATING ENVIRONMENT

Certain operating environments could have an adverse affect on the materials used in the manufacture of the HEDS-5000/6000. To allow the user to evaluate these situations, the following information on the generic material constituents of the encoder is supplied.

Piece Part	Material
Encoder Body & End Plate	Glass Filled Nylon
Emitter & Detector Lenses	Polycarbonate
Cable Jacket	Polyvinylchloride
Code Wheel	Nickel Alloy
Adhesives	RTV, Silicone

INTERFACE

For the encoder to serve as a useful function in a system, it must be interfaced correctly both mechanically and electrically.

HARDWARE

The flat ribbon cable supplied with the encoder is a cost effective cable for most applications. An unshielded cable can sustain relatively high levels of electromagnetic interference without affecting the encoder's performance. On the other hand, this cable is constructed of solid copper wire which is not designed for repeated flexing or relative motion between the encoder body and connector. Figure 12 illustrates the location of stress concentration during flexture. To avoid stress concentrations during relative movement or in a high vibration environment, it is recommended that the cable be tied down as shown in Figure 13. The remainder of the cable should be mounted to minimize repeated flexture in any specific area. Consult the factory for further information involving relative movement of the encoder.

The standard HEDS-5000/6000 is supplied with a 10-pin female insulation displacement type connector mounted on the ribbon cable. Table 4 lists a few of the available mating connectors which may be utilized to interconnect the encoder to external circuitry. Consult the factory for alternative cable and connector options.

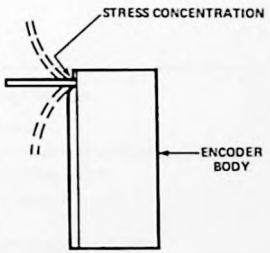


Figure 12.

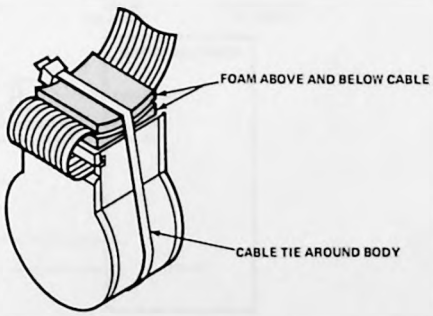


Figure 13.

CIRCUITS

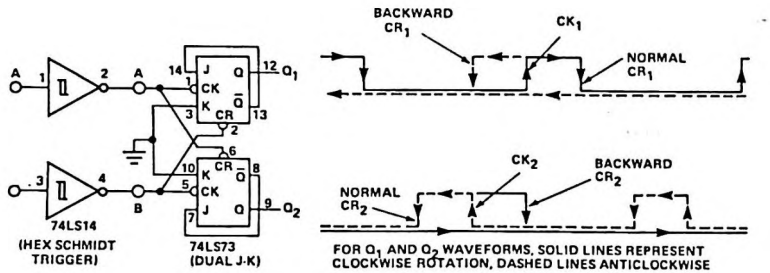
Although some applications require the use of only one channel, i.e., tachometers or a unidirectional shaft rotation, the most common application will involve the integration (count) of the shaft position, and thus require the information from both channels to determine the direction of rotation. The basic circuit counts cycles, while a slightly more complex version which counts both transitions of a channel (2x) is sometimes useful. In all cases it is recommended that the digital output of the encoder be buffered by an LSTTL Schmitt trigger (74LS14). The use of a Schmitt trigger gate increases the fan out capabilities while lowering the system's susceptibility to errors caused by slow transition times of the encoder's output.

Table 4

Manufacturer	Part Number
AMP	102154-1 102160-1
Molex	10-56-2101 10-55-2101
3M	3446-2002 3446-1002
Berg	65962-001
Robinson-Nugent	IDH-10-S1 IDH-10-SR1

The circuit depicted in Figure 14 provides an up or down pulse for every cycle. Due to the latched hysteresis configuration, the circuit avoids the multiple count problem which can occur in the event of a stationary shaft oscillating slightly about a transition.

By counting each transition of an output channel, the resolution can be increased to enable the distinction between the high and low states of the channel. The edge detection circuit shown in Figure 15 provides a pulse for each transition of channel A. The Exclusive OR gate toggles at twice the channel frequency of each channel, but when observed coincident with the negative slope of the edge detector output, its state corresponds to the direction of rotation. These two outputs can be used to drive the clock and control inputs of an Up/Down counter such as the 74' S168.



BASIC DIRECTIONAL SENSING. FOR CLOCKWISE ROTATION, Q_1 PULSATES; FOR ANTICLOCKWISE ROTATION, Q_2 PULSATES.

Figure 14. Cycle Count (1X) Circuit

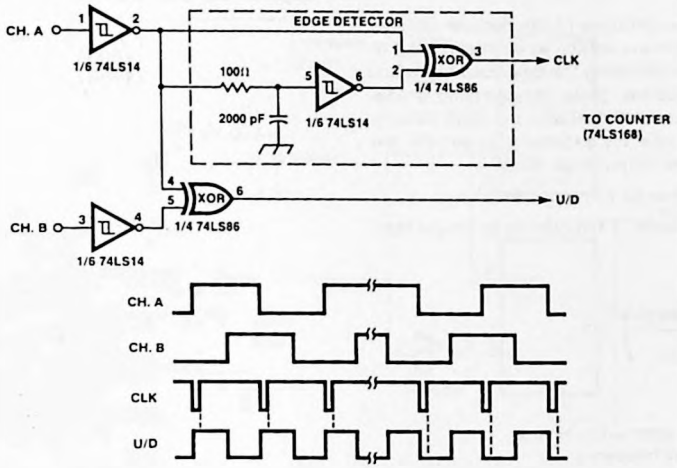


Figure 15. 2X Count Circuit

MICROPROCESSOR INTERFACE

The approach used for interfacing to a microprocessor could vary depending on the design requirements. An interrupt driver routine is simple to implement and is suitable for lower speeds. Using a programmed input routine can lead to a minimum hardware design and can accommodate higher rotational velocities. For very high velocities the encoder output can be buffered to a hardware counter before being input to the microprocessor.

Interrupt Driver Design

Interrupt Routine:
- Input channel A & B into Accumulator.
- Mask all but bits 0 & 1.
- IF Accumulator = 1 or 2.
- THEN
  - Increment count register.
- ELSE
  - Decrement count register.

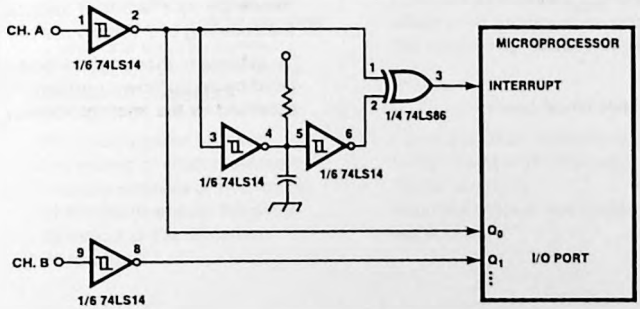


Figure 16. Interrupt Interface

Utilization of the overflow flag enables the designer to increase the effective counter width to fill his maximum count requirement.

Programmed Input: The sampling of the decoder outputs and the decode algorithm are written as an integral part of the program flow thus eliminating the time overhead associated with interrupt routines. Since the sampling is now independent of the encoder transitions, the shaft velocity must be limited, to enable the processor to sample the encoder at least once per output logic state.

The maximum velocity can be computed as follows:

1. The minimum state width is required to be longer than the program cycle.

$$T_s \left(1 - \frac{\Delta S_{max}}{90}\right) > T_p$$

where:

T_s = Nominal state width time at maximum frequency

T_p = Program Sampling Period

ΔS_{max} = Maximum State Width error

2. Substituting T_S from above, the maximum frequency is:

$$f_{max} = \frac{1}{4T_S} = \left(\frac{1 - \frac{\Delta S_{max}}{90}}{4T_p}\right) \text{ Hz}$$

ΔS maximum is estimated using the methods outlined in the "Design Considerations" section. Since ΔS is also a function of frequency, a first guess at the frequency should be assumed and a second iteration might be required (for very fast program cycles) to converge the result and the assumption.

The maximum allowed velocity is derived from f_{max}:

$$\omega_{max} = (2\pi f_{max}/N) \text{ rad/sec}$$

where:

N = Code Wheel count

Example: A motor which is required to run at speeds up to 600 R.P.M.: The estimated state width error is 45 electrical degrees. Compute the maximum sampling period.

$$f = \left(\frac{600}{60}\right) 500 = 5 \text{ KHz}$$

$$T_S = \frac{1}{4f}$$

$$= 0.05 \text{ msec}$$

$$T_p \leq T_S \left(1 - \frac{\Delta S_{max}}{90}\right)$$

$$\leq 0.05 \left(1 - \frac{45}{90}\right) \text{ msec}$$

$$\leq 25 \ \mu\text{sec}$$

The maximum allowable time between input samples is 25 μsec. The total program cycle should not exceed that number if none of the encoder's counts are to be missed.

DECODE ROUTINE

A programmed decode routine should have the previous state stored in memory. After the present state is input, a decision can be made on the direction of rotation (if any). This can be handled by accessing a look up table at a location determined by the two bit word representing the previous state, and whose content is the expected word for the next state in a clockwise rotation.

BUFFERED DESIGN

The level of buffering will depend upon the ratio of the encoder's frequency and the microprocessor sampling frequency.

The single stage memory element (Flip-Flop) described in Figure 15 will increase the maximum allowable encoder frequency by a factor of approximately 2.5 and still enable the counting of 2 transitions per cycle.

To achieve higher shaft velocities, the encoder can be buffered by an up/down counter. The parallel counter word is accessed by the microprocessor.

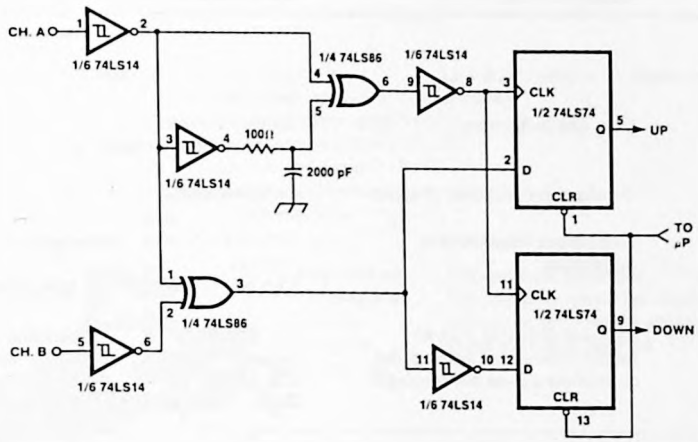


Figure 17. 2X Up/Down Buffer

SHAFT POSITION COUNTER

An optical incremental shaft encoder is a cost effective, reliable component for measuring shaft position. Since its output is a pulse for every increment of rotation, external circuitry is required to integrate the pulse train and indicate the shaft's position.

The circuitry presented in Figure 17 translates the encoder's output into the inputs required by an Up/Down counter. The count resolution is two times the code wheel count.

APPENDIX A
ENCODER SELECTION

PARAMETER	DESCRIPTION	MAIN ADVANTAGES
TYPE:		
ABSOLUTE	Provides a binary "word" for each position. Each bit requires a separate optical channel. The resolution is equal to the number of output bits.	Constantly retains the correct position information for one revolution. Not affected by power shut-off.
INCREMENTAL	Provides a pulse for each increment of shaft movement. Usually consists of two optical channels to enable the determination of the direction of rotation.	Lower cost than absolute due to the limited number of channels. Higher reliability. Encoded position not limited to one revolution.

PARAMETER	DESCRIPTION	MAIN ADVANTAGES
NO. OF CHANNELS:		
1 CHANNEL	Only one pulse train.	All the information required for unidirectional applications.
	Timing is proportional to speed.	Least expensive electronics.
2 CHANNEL	Two output waveforms in quadrature.	Provides information on direction of rotation. Can be integrated to obtain position.
3 CHANNEL	As in two channel, plus an output providing a single pulse or multiple pulses per revolution.	Provides an absolute indication of shaft position once per revolution. Can be used to reset position counters. Can be used as a third data channel.
CONSTRUCTION:		
SELF-CONTAINED	The encoder is supplied as a functional unit containing its own bearings and shaft.	Easy to use. Less assembly and testing required. Less affected by shaft eccentricity and loading.
MODULAR	The encoder is supplied in kit form and assembled by the user on the system's shaft.	Lower cost. Smaller size. Less inertia and friction due to the elimination of the internal bearing. Does not require alignment of two shafts. Does not add torsional resonance between encoder and motor due to long shaft.
ENCODING:		
DIRECT	A slotted wheel interrupts the light path between a light source and a photo-detector. The spokes and slots on the wheel are as wide as the light beam, thus limiting the maximum resolution.	Simple. Low cost.
MOIRÉ	A mask of a bar/slot pattern is placed on the photodetector. A code wheel which has a similar pattern is rotated in the light path. The light reaches the detector only when the slots on the code wheel and the mask line up. The resolution is therefore limited only by the slot spacing on the mask and code wheel and not by the light beam diameter.	High resolution can be achieved without sacrificing detector size.

PARAMETER	DESCRIPTION	MAIN ADVANTAGES
OPTICS:		
NOT LENSED	The light beam is allowed to diverge from the source. In this configuration the separation (gap) between the code wheel and the masked detector has to be very small in order to maintain sufficient light modulation on the detector.	Low cost, suitable for lower resolution encoder.
FOCUSED	A lens focuses the emitted light on the code wheel. Any shaft play will move the code wheel from the optimal position increasing the beam size and thus reducing the modulation contrast.	Efficient light collection. Allows higher resolution than the non lensed design — when not using the Moiré encoding method.
COLLIMATED	A lens collects the light from a small source and transforms it into a parallel pencil of light directed towards the code wheel and the masked detector. The light modulation is not sensitive to the code wheel-mask separation, allowing wider gap at higher resolution.	Wider gap. Allows looser shaft play specifications. Allows higher resolution. Efficient light collection.
LIGHT SOURCE:		
INCANDESCENT	A small light blub.	High output power.
SOLID STATE	A light emitting diode provides red or near infra-red light.	Lower current consumption. Better reliability. Smaller, more consistent source enables better collimation.
CODE WHEEL:		
GLASS	The bar pattern is printed on a glass wheel.	More resolution capability. Better cycle accuracy. Flat.
METAL	The pattern is composed of slots in a metallic disc.	Lower inertia. Higher Resolution/Inertia ratio. Pattern is scratch resistant. Rugged.

PARAMETER	DESCRIPTION	MAIN ADVANTAGES
SIGNAL CONDITIONING:		
SINGLE ENDED	A single detector per channel collects the modulated light. The resultant photo current is amplified by a single ended amplifier. Digitization is accomplished by comparing the amplifier output to a reference level (usually at half the peak value). Any change in the light path, i.e., source degradation, will affect the symmetry of the digitized waveform.	Low cost.
DIFFERENTIAL (PUSH-PULL)	The mask pattern of two adjacent detectors is spaced so that a light period on one corresponds to a dark period on the other detector. The resultant currents are amplified by a differential amplifier. Digitization is accomplished by comparing the outputs to each other.	Stable waveform. Less affected by time, temperature, or alignment changes.
OUTPUT:		
ANALOG	The amplified triangular waveform is output to be digitized by external circuitry.	The output can be used for interpolated analog position feedback. Sometimes used also in velocity feedback.
DIGITAL	The digitization occurs within the encoder.	Interfaces directly to digital circuitry. Higher noise immunity. Simpler interconnect cable requirements.

APPENDIX B
SUITABLE DC MOTORS

The use of encoded motors in position control applications often requires that the motor be specially fabricated to meet particular requirements with respect to torque, speed, diameter, shafts, housings, etc. It is not, therefore, practical to list to any significant extent all of the motors which may be utilized in conjunction with the HEDS-5000/6000.

There are four mechanical motor shaft parameters which must be held within specified limits in order for the encoder to operate properly. These parameters are:

Axial End Play
Shaft Perpendicularity
Shaft Eccentricity (run out)
Radial Play

Absolute maximum values for these parameters, along with recommended operating conditions, are specified in the HEDS-5000/6000 data sheet.

As a resource for those who wish to obtain motors for evaluation of the HEDS-5000/6000 performance, the vendors as listed in Table 5 have been evaluated and samples have been found to meet the required data sheet specifications. There are many other manufacturers of motors suitable for use with the HEDS-5000 and the HEDS-6000, as well as other motors from the listed manufacturers which are equally suitable.

Servo-Tek	Hawthorne, NJ	Superior Electric	Bristol, CT
Electro Craft	Hopkins, MN	Honeywell	Rockford, IL
Pittman	Harleysville, PA	Harowe	West Chester, PA
Portescap	West Caldwell, NJ or 2300 La Chaux-de-Fonds, Switzerland	Maxon Faulhaber	Burlingame, CA or or Sachseln, Germany Germany
Transcoil	Worcestor, PA	Inland Motors	Sierra Vista, AZ
Clifton Precision	Clifton Heights, PA	Dynetic Systems	Elk River, MN

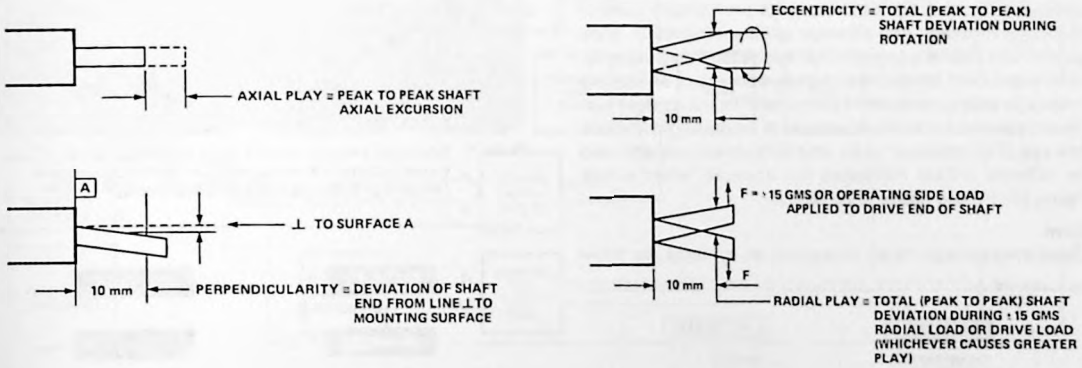
In reviewing motor data sheets, it will be found that size is well specified; however, motor vendors rarely specify the previously mentioned mechanical parameters in their data sheets. Dialog with the manufacturer will be necessary in order to obtain data on motor shaft parameters.

Some suppliers offer sleeve bearings or pre-loaded ball bearings for securing the shaft. Pre-loaded ball bearings improve the shaft parameter values and may be required in order to achieve the desired specifications.

The encoder mounting requirements must be communicated to the motor vendor to ensure correct alignment of the encoder. This may require that an additional mounting plate with screw holes be machined for the motor.

Testing for axial end play, shaft perpendicularity, shaft eccentricity, and radial play is necessary to determine acceptance of motors to incoming inspection criteria. The user should be sure that the test conditions represent the requirements of the HEDS-5000/6000 encoder. For example the code wheel is placed approximately 10 mm from the mounting surface when the encoder is assembled. Therefore perpendicularity, eccentricity, and radial play measurements should be made 10 mm from the mounting surface.

APPENDIX C
MOTOR SHAFT PARAMETERS



HEWLETT PACKARD

APPLICATION NOTE 1012

Methods Of Legend Fabrication

INTRODUCTION

Hewlett-Packard LED Light Bar Modules inscribed with fixed messages or symbols can be used to construct economical annunciators. Annunciators can be used in a variety of ways; to convey the status of a system, to indicate a selected mode of operation, or to indicate the next step in a sequence. Light bars are available in 5.08 mm x 10.16 mm (0.2 inch x 0.4 inch), 5.08 mm x 20.32 mm (0.2 inch x 0.8 inch), 10.16 mm x 10.16 mm (0.4 inch x 0.4 inch), and 10.16 mm x 20.32 mm (0.4 inch x 0.8 inch) sizes and in either single surface or multi-segmented form. Light bars can be easily installed in front panels using the Hewlett-Packard Panel and Legend Mount (HLMP-2598, -2599, -2898, -2899).

This application note discusses alternative ways the message or symbols (legends) can be designed. A selection matrix is then provided to assist in the selection of the most appropriate method of legend fabrication. Each fabrication method is explained in detail along with mounting and attachment techniques. Finally, prevention of cross-talk is discussed for legend areas of a multi-segmented light bar

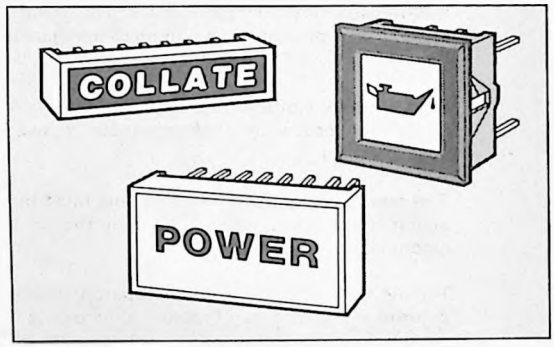
LEGEND DESIGN

Format

The two basic legend formats are shown in Figure 1. Dark field format consists of a transparent message with an opaque surround. Dark field formats are typically used to display a message that conveys routine information, such as the next step in a sequence or a selected mode of operation. Light field format, the inverse, consists of an opaque message with a transparent surround. The transparent surround permits a maximum amount of emitted light to catch the eye of an observer. Light field formats are typically used to indicate critical messages, for example, when a tank nears empty and needs to be refilled.

Font

Easy-to-read bold faced characters or symbols are more desirable than light faced characters or symbols (Figure 2). Suggested type faces are Helvetica, Futura Demi-Bold or Univers 65.



The size of the characters in the legends are directly related to the distance at which they are viewed. The following table, based on normal visual acuity[1], shows character height necessary to comfortably read the display from various distances.

Table 1. Viewing Distance vs. Character Height

Viewing Distance Metres (Feet)	Min. Character Height mm (Inch)
1 (3.3)	1.45 (0.06)
2 (6.6)	2.91 (0.11)
3 (9.9)	4.36 (0.17)
4 (13.2)	5.82 (0.23)

Note: 1. Character Height (mm) = Viewing Distance (m) x 1.454
Visual activity = 5 minutes of arc for 20/20 vision
Tangent of 5 minutes of arc = 1.454×10^{-3}.

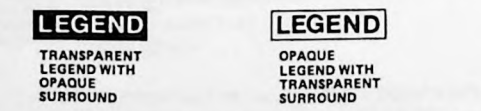


Figure 1. The Two Basic Legend Formats

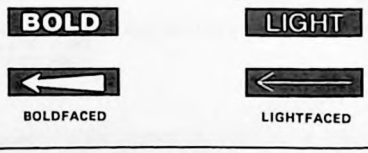


Figure 2. Boldfaced Characters and Symbols Make Legends that are Easy to Read

Front Panel Appearance

If it is desirable to conceal the message when the device is OFF, a Dead Front can be employed. A Dead Front can be achieved by placing a low transmission filter over the display to reduce contrast between off segments and the background of the legend. It may also be necessary to reduce the color difference between off segments and the background by using transparent and neutral density gray areas to form the legend. In this case, the transparent portions of the legend as they reflect ambient light in the OFF condition will appear similar in color to the neutral density gray. In the ON condition, the illuminated transparent areas of the legend will contrast vividly with the neutral density gray.

In many cases it may be desirable for the observer to be aware of the message in both the ON and OFF state. This is achieved by using a higher transmission filter and/or legend areas with a large color difference, such as black and transparent areas. In the OFF state the background area will have a recognizable color difference from the transparent area and the message will be readable.

SUMMARY AND COMPARISON OF LEGEND GENERATION TECHNIQUES

Two basic methods can be used to fabricate legends for light bar modules. The first involves engraving directly on the front surface of the light bar and filling the engraved area with opaque enamel. The second method involves fabricating a thin film legend such as an exposed photographic film, silkscreened polycarbonate film, prefabricated adhesive film or instant lettering. These thin film legends are applied to the light bar with the Hewlett-Packard Panel and Legend Mount, with double sided transparent tape or with adhesive backing. Figure 3 shows the steps required in each fabrication method.

Durability of the legend is often an important factor to the designer. The following tests have ben performed on samples of each of these legend fabrication methods, where applicable:

Temperature Cycling:	100 cycles from -40°C to +85°C 15 min. at extremes, 5 min. transfer
Temperature Storage:	+55°C 1000 hours
Humidity Test:	5 days, 90-98% RH, -10°C to +65°C non-operating
Transmission Test:	Visual inspection
Peel Strength Test:	Maximum dynamometer deflection at constant rate of peel (12"/minute)
Taber Abrasion Test:	500 grams for 1,000 cycles
UV Testing:	2 years simulated UV exposure under QUV® weathering equipment
Solvent Resistance	Freon, Methanol, Isopropanol Alcohol, Water

Table 2 shows results of these tests and also provides information on relative costs.

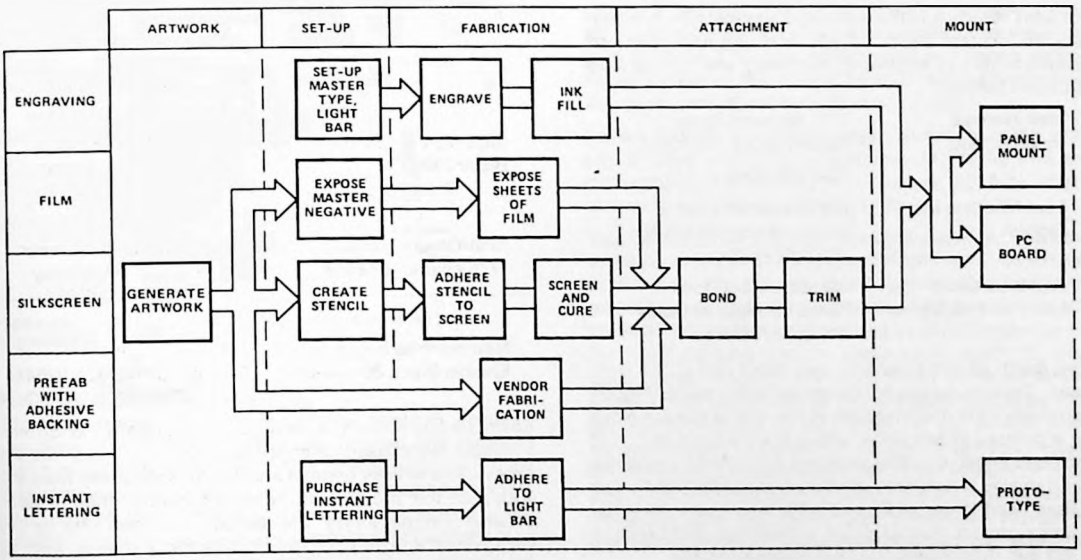


Figure 3. Legend Fabrication Methods

Table 2. Selection Matrix

Legend Fabrication Method	Format/Mounting				Durability				Relative Cost	
	Dark Field	Light Field	Dead Front	HP Panel and Legend Mount	Abrasion Resistance	Temp. Compatibility	Peel Strength	Solvent Resistance	Set-Up Cost	Manufacturing Cost
Engraving		X		X	X	X	Excellent	Good	High	High
Photographic	X	X	X	X	X	X	Good	Good	Low	Med Low
Silkscreen[1]	X	X	X	X	[1]	X	Good	Fair	Med	Med Low
Prefab with[2] Adhesive Backing	X	X	X	X	X	X	Good	Good	Low	Low
Instant Lettering[3]		X		X			Poor	Poor	Low	Med

Set-Up Cost:
Cost of original artwork, tools, equipment necessary to begin legend fabrication.

Manufacturing Cost:
Cost of raw materials, and labor necessary to fabricate and assemble a legend on a light bar.

Notes:
1. Abrasion resistant only when backprinted.
2. For extreme ultra-violet exposure, Brady-Panel® is the recommended fabrication method.
3. Recommended for prototype applications only.

ENGRAVING

Engraving is recommended for high temperature and high humidity applications. It should be noted, however, that engraving is only appropriate for light field formats.

Since small areas are to be engraved, such factors as type font, letter height and spacing between letters is very important. For smaller letters regular master type is recommended and for larger letters condensed master type is recommended. After the master type is set the light bar must be rigidly mounted in a vice which holds three sides in place and prevents the leads from bending.

For best results a calibrated engraving machine is necessary to control depth of cut and alignment. Several manufacturers of engraving machinery and cutting tools are listed below:

New Hermes Incorporated	1711 Monarch Street Garden Grove, CA 92641 (714) 898-9265
Lars Machine Inc. Gorton	1925 Roosevelt Avenue Racine, Wisconsin 53406 (414) 554-8880
Richards Micro-Tool Inc. ("end mills only")	100 Nicks Rock Road Plymouth, Massachusetts (617) 617 746-6900

The depth of cut should be only 0.245 mm (0.010 inch) deep. Carbide cutters are recommended because they are extremely rigid and long lasting. The tool shape can either be a tapered shank cutter with a conical point (65° ± 5° included angle) or a straight shank end mill. For visual balance smaller letters need smaller width end mills and larger letters need larger width end mills. As a guide, for letter heights greater than or equal to 3.06 mm (0.125 inch) a 0.382 mm (0.0156 inch) end mill is recommended.

The end mill, although more fragile than a tapered cutter, offers some advantages. The shape of the end mill allows the operator to be less concerned about variations in cutting depth because the width of cut is dependent only on the width of the end mill. When using the tapered cutter the operator must be careful to engrave at a constant depth because width of cut is dependent on depth of cut. Also, due to its shape, the tapered cutter may need to be resharpened more often than an end mill. If the tip of the tapered cutter becomes dulled the width of cut will increase whereas, if the tip of the end mill becomes dulled the width of cut will remain the same.

Fill the engraved area with a viscous flat black enamel for best results. The following enamels are recommended:

Gliddens 908 Flat Black® All Purpose Enamel	SCM Corporation Gliddens Coatings and Resins Division 801 Cantebury Rd. Westlake, Ohio 44145 (216) 344-8000
Impervo-Flat Enamel® Black 23581	Benjamin Moore Co. 51 Chestnut Ridge Rd. Montvale, NJ 07645 (201) 573-9600
Rust-Oleum Matte Black® 7776 enamel-oil base	Rust-Oleum Corporation 11 Hawthorne Parkway Vernon Hills, IL 60061 (312) 367-7700
New Hermes-Engravers® Enamel Black 30-450-35	1711 Monarch St. Garden Grove, CA 92641 (714) 898-9265

Enamel is applied with a small brush (standard 2 or 3), with a lintless wipe used immediately after to clean off the excess. The excess enamel should be kept away from the edges of the module. If, however, some enamel does become lodged along the border between the epoxy encapsulant and polycarbonate package, a solvent, such as Shell Sol BT-67® manufactured by Shell Oil Company, can be applied with a lintless wipe to clean the edges. Finally, after the enamel is nearly dry, a lintless wipe dipped in methanol or isopropanol alcohol can be used to clean the module.

THIN FILM LEGENDS

Legend Artwork

All thin film methods except "instant lettering" require the generation of photo-reproducible artwork. For best results this artwork layout should be done carefully on an enlarged scale and then reduced. Since legends must be precisely placed on the face of the light bar, alignment marks should be included in the artwork. The legend artwork, shown in Figure 4a, contains alignment marks and notched corners. By making the legend 0.005 inch oversized on each edge, any slight misalignment that might occur during attachment will not be noticeable (Figure 4b).

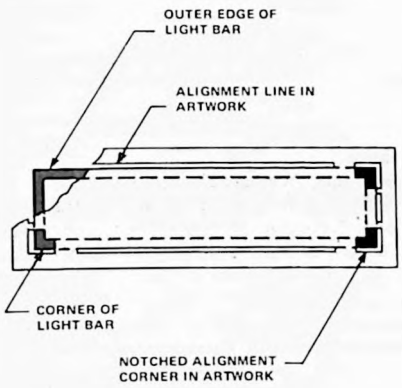


Figure 4a. Legend Artwork with Alignment Marks

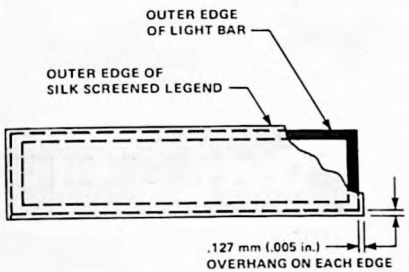


Figure 4b. Legend Artwork with Overhang to Allow for Alignment

PHOTOGRAPHIC PROCESS

The photographic process is fast and relatively inexpensive. First, the artwork is reduced, stepped and repeated onto a master negative. Then, this master negative is used to expose each sheet of film in such a way that the legend is read through the film stock. Thus, when a legend is attached to a light bar the emulsion is in contact with the tape or epoxy encapsulant. Although the film stock protects the fragile emulsion from exposure or abrasion specular reflection off the front surface is increased.

Polyester based films which feature dimensional stability, high contrast, maximum optical density and a very low fog level are recommended. Two polyester based films have been tested and found satisfactory — Kodak Reproduction Film 4566® and Kodalith Ortho Film type 3 4556®. Similar films can also be obtained from other manufacturers, such as Agfa Gavaert, GAF, or Dupont. Both recommended films have the same polyester base but different emulsions and development procedures. Kodak Reproduction Film, traditionally used in line work reproduction, offers greater strength and less susceptibility to pin-holes. The Kodalith-Ortho film is more sensitive to pin-holes or dust, and has been traditionally used in half-tone reproduction.

SILKSCREEN

The Legend Substrate

A thin untinted transparent film of polycarbonate or polyester may be used as the legend substrate. A material that exhibits very good performance is 0.102 mm (0.004 inch) thick LEXAN® Film No. 8010-112 manufactured by General Electric, Plastics Division, Speciality Plastics Department, 1 Plastics Avenue, Pittsfield, Massachusetts 01201. Silkscreening paints and inks adhere very well to LEXAN®. LEXAN® also exhibits very good dimensional stability with temperature variations. Polyester film, such as 0.102 mm (0.004 inch) Formula Type S MYLAR® produced by the E.I. Dupont de Nemours Company, Wilmington, Delaware 19898, may also be used as a legend substrate, although specially formulated inks are required. Epoxy inks and acrylic inks should not be used on Polyester films because the ink does not adhere well to the film.

The Silkscreening Ink

Certain formulated inks, acrylic laquer type inks or epoxy inks may be used in the silkscreening process. Both polycarbonate and polyester may be screened with GF 140®, a formulated ink produced by General Formulations, 350 S. Union, Sparta, Michigan 49345. GF 140® is unusually tough and flexible, but due to its solubility characteristics special caution is required. The ink exhibits an extremely strong affinity for polyester and polycarbonate and other materials such as paper. Therefore, silkscreened film sheets should not be stacked on top of each other or stacked interleaved with paper until after the ink has been cured.

Nazdar 70-111®, a modified acrylic-lacquer type ink, may also be used to print on polycarbonates. Nazdar inks are manufactured by the Nazdar Company, 1087 N. North Branch Street, Chicago, Illinois 60622.

This ink is very easy to handle and to clean up. However, adhesion to the polycarbonate substrate is not as permanent as with the other recommended inks. One epoxy ink recommended for use only on polycarbonate films is the WORNOWINK® Series 50 with #9 catalyst produced by the Hysol Division, Dexter Corporation, 15051 E. Don Julian Road, Industry, California 91749. After screening an epoxy ink will quickly air dry to a semi-hard state that permits the legends to be sheared or cut to size without any smearing, chipping or peeling. With epoxy based ink, care must be taken to add the proper amount of catalyst. If too much catalyst is added the ink may continue to harden after the normal cure cycle. This hardening occurs over a period of several months and may cause the ink to become brittle. Thus, screened sheets may have a limited shelf life and should not be stored for a long period of time prior to light bar adhesion. When cured at elevated temperatures epoxy paints exhibit a high degree of abrasion resistance and chemical resistance.

Screen Mesh

Ink thickness is determined by the screen mesh and to a lesser degree the height of the screen above the polycarbonate sheet. The silkscreening process should produce a controlled ink thickness of 0.025 mm (0.001 inch). A thicker layer of ink may cause the legend substrate to curl or the ink to crack during temperature cycling. For each of the inks listed above the following screen mesh sizes are recommended:

50/9 WORNOWINK	200 mesh
GF 140	200 mesh, 325 mesh
Nazdar 70-111	325 mesh

Printing

Front printed legends are formed by screen printing the ink on the top side of the legends. When the legends are attached to the light bar the ink is exposed. Because the ink is exposed, front printed legends are not suited for abrasive environments. All the inks described above are suitable for front-printing; however, only one ink, GF 140, can be used for back printing.

A back-printed legend is formed by screening the ink on the backside of the legends. Thus, when applied to a light bar, the ink is in contact with the tape, and the polyester film serves as a protective coating. Back-printed legends with GF 140 ink exhibit abrasion resistance and slightly stronger adhesion than front printed GF 140 legends.

PREFABRICATED LEGENDS WITH ADHESIVE BACKINGS

Some manufacturers sell custom constructed polycarbonate or polyester legends backed with an industrial strength adhesive. Brady manufactures Poly-Panel®, a material constructed from second surface printed polycarbonate. Brady Poly-Panel® comes in a variety of colors and textures. A shiny clear texture material transmits the most light, but increases specular reflections. Therefore, this material should only be used behind a filter. A velvet texture, on the other hand, offers a diffused dead front appearance but at the cost of a greater attenuation of light. Brady Poly Panel®, thickness not to exceed 0.010 inch, can be ordered with B-196® adhesive backing, a transparent unsupported acrylic pressure sensitive adhesive backing.

The Brady Poly-Panel® has no loss of properties due to abrasion or UV exposure. Data sheets with extensive reliability testing can be obtained from the manufacturer:

W.H. Brady Co. Nameplate Division 750 West Glendale Avenue P.O. Box 571 Milwaukee, Wisconsin 53201 (414) 332-7620	Poly-panel with polycarbonate substrate B-196 adhesive thickness — 0.005-0.010 inch texture — clear or velvet

INSTANT LETTERING

Instant lettering is a quick method of legend fabrication. It is usually limited to prototype applications, because under extreme temperature cycling and humidity testing noticeable bubbles may form. Also, the adhesive bond between instant lettering and the light bar is weak.

Letraset, a manufacturer of instant lettering, offers a broad line of typefaces and symbols that are easy to apply. The letters or symbols are simply transferred to the light bar with a burnishing tool. To protect Letraset a polycarbonate sheet (see silkscreening section) may be attached over the instant letters.

ATTACHING A LEGEND TO A HEWLETT-PACKARD LIGHT BAR

Using the Legend in a Light Bar Panel and Legend Mount

Hewlett-Packard Panel and Legend Mounts (HLMP-2598, -2599, -2898, -2899), are used to install light bars in front panels. A space has been provided for holding a 0.13 mm (0.005 inch) thin film legend over the front surface of the light bar. Legends should be trimmed to the size of the light bar prior to installation.

Panel and legend mounts are convenient because no adhesive or tape is required to hold the legend in place. For more specific instructions on mounting techniques refer to the Hewlett-Packard Panel and Legend Mount data sheet.

Tape

All thin film legends, except those with adhesive backings can be bonded to the face of a light bar with an optically transparent tape. Two tapes which have been tested and found satisfactory are M69®, produced by the Connecticut Hard Rubber Company, 407 East Street, New Haven, Connecticut 06509, and POLYKEN 126® produced by the Kendall Company, Polyken Division, 1 Federal Street, Boston, Massachusetts 02101. These optically transparent tapes consist of a polyester film carrier with acrylic adhesive on each side and a release backing. The thickness of the adhesive and carrier combination is typically 0.102 mm (0.004 inch). Both tapes can be purchased slit to desired width and of the two tapes M69® exhibits slightly stronger adhesion to the film substrate.

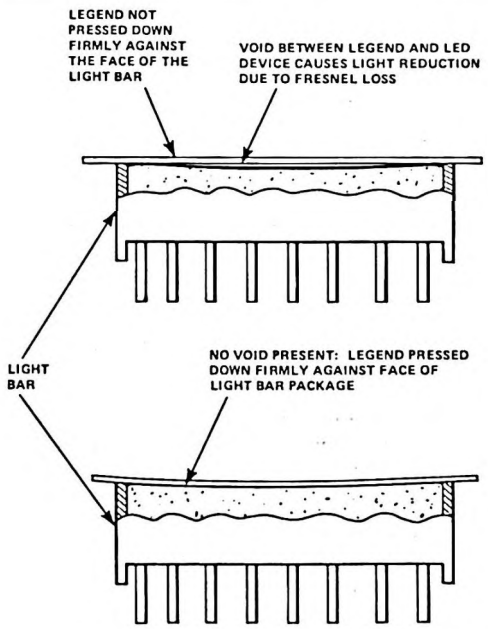


Figure 5. Securely Attached Legend Prevents Reduction of Light Due to Fresnel Loss

Bond

The steps to bond legends without adhesive backings to the face of the light bar are:

1. With release backing intact, apply the exposed adhesive side of the tape to the back side of the legend or front surface of the light bar with firm pressure.

2. Remove the release backing. Align the legend to the face of the light bar and apply with firm pressure. It is important to ensure that there are no voids in the adhesive/legend and adhesive/light bar interfaces. Voids in the adhesive interfaces, as illustrated in Figure 5, reduce light transmission through the legend due to Fresnel loss and do not permit a secure bond to take place.

3. Trim the legend to size with a pair of scissors or a small shear. (Figure 6)

4. For increased adhesion, oven cure the assembly at a temperature of 115°C (240°F) for 4 hours.

Note: For legends with adhesive backings follow steps 2 and 3 only.

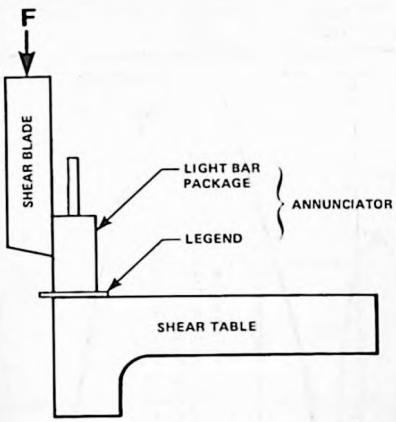


Figure 6. Shearing Legend to Size

REDUCTION OF CROSS-TALK IN A MULTI-FUNCTION ANNUNCIATOR

Some Hewlett-Packard Light Bars provide more than one light emitting surface within the same package. Each light emitting surface may be illuminated independently. A single multi-function legend may be applied to a multi-segmented light bar to form a small annunciator that is capable of displaying as many as four independent messages or symbols.

However, the legend substrate and the acrylic adhesive tend to act as light pipes. Some light travels from an illuminated area of the multi-function legend to adjacent non-illuminated areas, as illustrated in Figure 7. This light leakage, called cross-talk, if severe enough can cause confusion between the ON and OFF status of the adjacent functions displayed by the legend areas.

Cross-talk can be reduced by using dark field format and by printing on the back side of the legend substrate. Back side printing reduces the amount of emitted light that enters the substrate. Thus, the amount of light than can leak into adjacent legend areas is decreased.

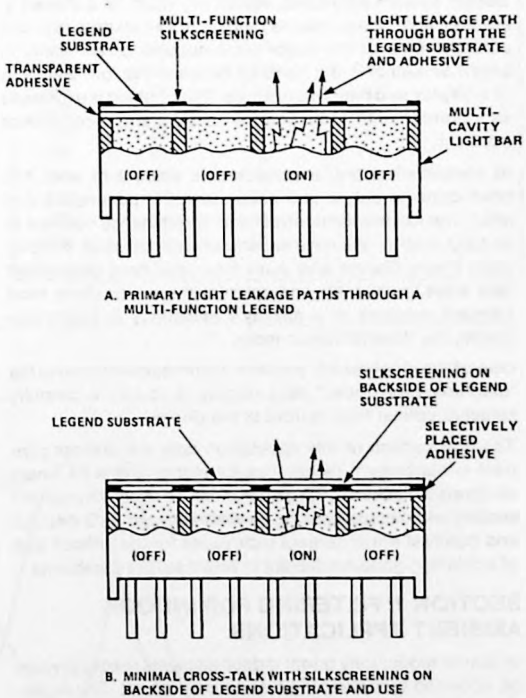


Figure 7. Light Leakage (Cross-Talk) Between Illuminated and Non-Illuminated Porsions of a Multi-Function Legend Bonded in a Multi-Cavity Light Bar

HEWLETT PACKARD

Application Note 1015

Contrast Enhancement Techniques For LED Displays

GENERAL INTRODUCTION

Readability is the most important feature of an electronic display system. Moreover, readability must be achieved in ambient lighting conditions ranging from darkness to bright sunlight. One of the major contributions to readability in bright ambients is the contrast between the "on" elements of a display and their background. This contrast is expressed as a combination of luminance contrast and chrominance contrast.

At Hewlett-Packard, a considerable amount of work has been done to define and understand the parameters that affect the luminance contrast and chrominance contrast of an LED display. We have expanded upon the work done by Jean Pierre Galves and Jean Brun and have determined new ways to calculate and optimize the values of the most relevant measure of a display's readability in bright ambients, the "discrimination index".[1]

One of the most readily available techniques to improve the "discrimination index" of a display is to use a carefully selected optical filter in front of the display.

The first section of this application note will discuss contrast enhancement techniques for indoor ambients where all Hewlett-Packard LED displays can be used. The second section will discuss specific Hewlett-Packard LED displays and contrast enhancement techniques for the difficult task of achieving good readability in bright sunlight ambients.

SECTION 1: FILTERING FOR INDOOR AMBIENT APPLICATIONS

In dim to moderately bright indoor ambients readability can be obtained by optimizing luminance contrast. The objective is to maximize the luminance contrast between the light emitting elements and the background while minimizing the luminance contrast between the non-illuminated elements and the background. For LED displays, this can be achieved by:

1. Designing the display package for low reflectance so that the luminance of the non-illuminated elements matches the luminance of the display package.
2. Choosing a filter that transmits a maximum amount of LED light while attenuating the reflected light off the display package.
3. Choosing a filter with low front surface reflectance for a given ambient lighting condition.

On the other hand, to obtain readability in bright indoor and sunlight ambients the optimization of chrominance contrast as well as luminance contrast becomes important. Chrominance contrast refers to the color difference between the light emitting elements and the background. The optimization of chrominance contrast is more fully explained in section two while this section concentrates on the optimization of luminance contrast.

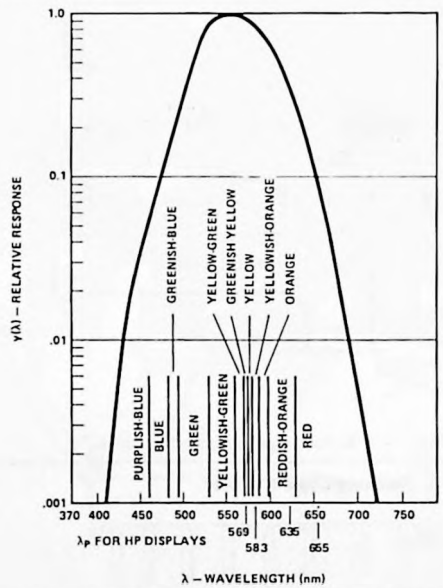


Figure 1. CIE Standard Observer Eye Response Curve (Photopic Curve), Including CIE Vivid Color Ranges.

First, to obtain a better understanding of filtering, the more commonly used terms in contrast enhancement will be defined. Next, specific filter transmission recommendations for each LED color will be presented. Also, plastic versus glass filter materials and the effects of ambient lighting on luminance contrast will be discussed. Finally, recommended filter manufacturers and the materials they offer will be listed.

DEFINITIONS

Eye Response - Standard Observer Curve

The Standard Observer Curve is important in contrast enhancement because the eye's sensitivity to light emitting sources, ambient lighting and display backgrounds is very dependent on the wavelengths of emitted or reflected visible light. The eye response of a standard observer to various wavelengths of light is shown in Figure 1. The Standard Observer Curve was established in 1931 by the CIE (Commision Internationale De L'Eclairage) as the industry standard for relating the total power (radiant flux) emitted from a source to the amount of power to which the eye is sensitive (luminous flux). The curve is on a logarithmic scale and for reference various wavelengths of energy are labeled by color. As can be seen, the eye's response peaks in the yellow-green region, which means that per watt of radiated power a source in this region will have more lumens than sources of other wavelengths. The exact conversion factor at the peak (555 nm) is 680 lumens of luminous flux (lm) per watt of radiated power (W).

Peak Wavelength and Filter Transmission

The wavelength at the peak of the LED radiated spectrum is called peak wavelength (λp). Figure 2 and Table 1 show the typical LED radiated spectrum for four standard colors; red ($\lambda p = 655$ nm), high efficiency red ($\lambda p = 635$ nm), yellow ($\lambda p = 583$ nm) and green ($\lambda p = 569$ nm). All four standard colors fall in the region of visible light. The appropriate filter

Table 1. LED Spectrums Normalized To One At Typical Peak Wavelengths

Wavelength (nm)	Standard Red	High Efficiency Red	Yellow	Green
540			.01	.03
545			.02	.05
550			.03	.13
555			.05	.33
560			.12	.65
565			.24	.87
570			.47	1.00
575			.73	.85
580			.92	.67
585			1.00	.55
590		.01	.94	.42
595		.03	.78	.33
600		.04	.62	.26
605	.01	.12	.48	.18
610	.01	.20	.37	.14
615	.03	.40	.28	.11
620	.05	.61	.17	.08
625	.13	.78	.13	.07
630	.20	.96	.11	.05
635	.37	1.00	.08	.04
640	.55	.91	.07	.03
645	.75	.81	.06	.03
650	.94	.71	.05	.02
655	1.00	.58	.05	.02
660	.96	.45	.04	.01
665	.84	.36	.04	.01
670	.72	.27	.03	
675	.60	.21	.01	
680	.47	.15		
685	.36	.12		
690	.25	.09		
695	.21	.05		
700	.16	.01		

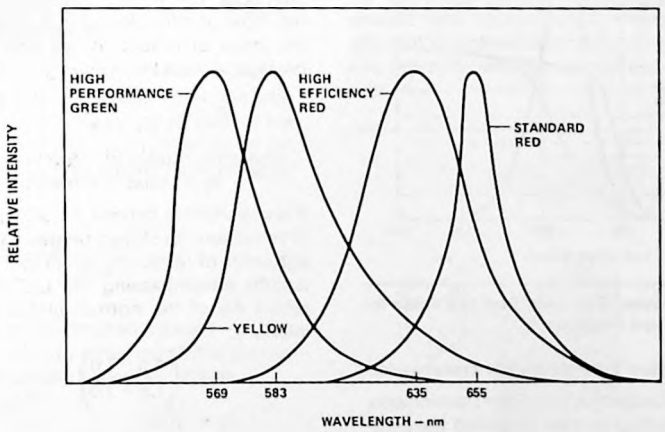


Figure 2. Relative Intensity vs. Wavelength.

for use with any of these four colors is chosen according to its published transmission curve. Filter transmission curves exhibit relative transmittance vs. wavelength over the region of visible wavelengths. The relative transmittance of a filter with respect to any particular wavelength is defined as:

$$\text{Relative Transmittance } T(\lambda) = \frac{\text{Luminous Flux with Filter at Wavelength } \lambda p}{\text{Luminous Flux without Filter at Wavelength } \lambda p}$$

If a particular optical filter has a fairly constant transmission over the LED radiated spectrum, then the transmission at the peak wavelength may be used to estimate the amount of display emitted light that passes through the filter. For example, if a filter has a relatively flat transmittance of 60% at a given λ_P, then approximately 60% of the display emitted light will pass through the filter to the observer and 40% will be absorbed. In actuality, the display emitted light passing through a filter (L) is an integral that is the product of several functions. As defined by the following equation, the Standard Observer Curve and LED Spectrum must be integrated with the filter transmission curve.

$$L = \int \ell(\lambda) Y(\lambda) T(\lambda)\, d\lambda \qquad (1)$$

Where $\ell(\lambda)$ = radiated spectrum of the illuminated light emitting element (See Table 1)

$Y(\lambda)$ = the 1931 CIE photopic curve (See Wyzecki & Stiles, *Color Science*)

$T(\lambda)$ = relative transmission characteristic of the filter (Supplied by Filter Manufacturer)

As shown in Figure 3, if the slope of the filter transmission curve changes rapidly in the region of the LED radiated spectrum, then the transmission at the peak wavelength will no longer be an accurate estimate of display emitted light that passes through the filter. On the other hand, for a more constant transmission, as also shown in Figure 3, the estimate is fairly accurate.

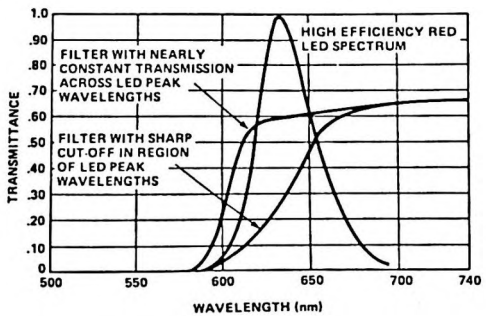


Figure 3. Comparison Between Two Long Pass Red Filters for Use with High-Efficiency Red Displays.

Filter Characteristics Which Determine Light Transmission

As mentioned in *Peak Wavelength and Filter Transmission*, filters are chosen according to their published transmission curves which exhibit relative transmittance vs. wavelength over the region of visible light.

For any filter, the total transmitted light is equal to the LED emitted light less the light absorbed within the filter and the light reflected at the filter-to-air interfaces.

The relative absorption characteristics are determined by the dye color and dye concentration while the reflectance characteristics are determined by the index of refraction of the filter material. Since the index of refraction is nearly a constant, dye coloring and dye concentration are varied to obtain the appropriate transmission at any given wavelength.

When choosing a filter or molding your own material, it is important that the dye color and dye concentration are carefully controlled so that the internal transmission characteristics are consistent from one filter to another. Internal transmittance can be considered the LED emitted light minus the light absorbed within the filter material. Thus, the formula for the LED light transmitted through the filter becomes:

Luminous flux with filter at wavelength λp	=	Luminous flux internally transmitted through the filter	−	Luminous Flux reflected at filter-to-air interfaces
$T(\lambda)$	=	$Ti(\lambda)$	−	$R(\lambda)$ (2)

If the dye coloring is held at a constant density, the internal transmission through the filter material at any given wavelength $Ti(\lambda p)$, is an exponential function of the thickness of the material

(Internal Transmission) $\qquad Ti = e^{-ax} \qquad (3)$

where: x = The quantity of unit thicknesses of filter material.
e = 2.71828
a = Absorbtion coefficient and is equal to $-\ln(t)$ where t is the internal transmission for a unit thickness.

As shown in Figure 4, the internal transmission through 1.0 mm thickness of filter material is 0.875 at a wavelength of 655 nm. The same filter material at a thickness of 2.5 mm has a relative transmission of 0.716.

$-\ln(0.875) = 0.1335 = a$

$T = e^{-(.1335)(2.5)} = 0.716$

Light that is not internally transmitted through the filter or absorbed within the filter material is reflected at the filter-air interfaces. The amount of reflected light is dependent upon the index of refraction of the filter material as compared to the index of refraction for air. Mathematically, the percentage of reflected light is given by the following ratio:

$$R = \left(\frac{n_1 - n_2}{n_1 + n_2}\right)^2 \qquad (4)$$

where: n_1 = Index of refraction of the filter material.
n_2 = Index of refraction for air = 1.0.

It is important to choose a filter with a homogeneous index of refraction. As shown below, a plastic filter with an average index of refraction equal to 1.5, for the range of wavelengths encompassing the LED's radiated spectrum will reflect 4% of the normal incident light at each filter/air interface.

$$R = \left(\frac{1.5 - 1.0}{1.5 + 1.0}\right)^2$$

$$R = 0.04$$

Since there are two filter-air interfaces, the percentage of LED light lost due to reflection for a filter with an internal transmittance of 0.875 is 7%. Therefore, the total transmittance through the filter according to equation (2) is 0.805 (0.875 − 0.07 = 0.805).

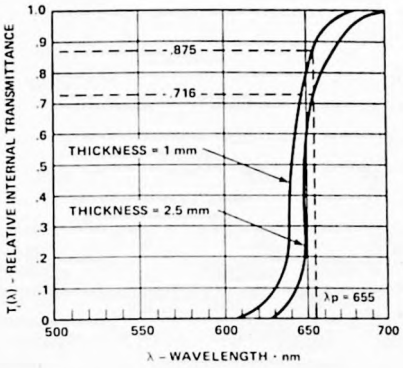


Figure 4. Variation in Relative Transmittance vs. Thickness for a Constant Density Filter Material.

$$\begin{aligned}\text{LED emitted light lost due to reflection} &= \text{loss at 1st interface} + \text{loss at 2nd interface}\\ &= 0.04 + (0.96)(0.875)(0.04)\\ &= 0.04 + 0.03\\ &= 0.07\end{aligned}$$

In addition to attenuating a portion of the light emitted by the display, a filter also shifts the perceived color of the LED. For a given LED spectrum, the color shift depends on the cut-off wavelength and shape of the filter transmission curve. A choice among available filters must be made on the basis of which filter and LED combination is most pleasing to the eye.

Luminance Contrast

Conceptually, the luminance contrast is the observed brightness of the illuminated element compared to the brightness of the surround. The brightness of the illuminated element is the combination of the emitted light and the ambient light reflected off the element, while the brightness of the background is due only to reflected ambient light.

Display Luminance Contrast

For a display without a filter, the luminance contrast ratio can be considered the sterance (intensity/unit area) of the illuminated element plus the ambient light reflected off the element divided by the sterance of the ambient light reflected off the background.

$$\text{Luminance Contrast Ratio} \quad CR = \frac{L_vS + L_vOFF}{L_vB} \qquad (5)$$

Where L_vS = Sterance of illuminated element
L_vOFF = Sterance of light reflected off the element
L_vB = Sterance of light reflected off the background

Mathematically:

$$L_vS = \int \ell(\lambda)Y(\lambda)\,d\lambda$$

$$L_vOFF = \int X(\lambda)Y(\lambda)R_\ell(\lambda)d\lambda$$

$$L_vB = \int X(\lambda)Y(\lambda)R_B(\lambda)d\lambda$$

where $\ell(\lambda)$ = radiated spectrum of the illuminated light emitting element (See Table 1)

$Y(\lambda)$ = the 1931 CIE photopic curve (See Wyzecki & Stiles, *Color Science*)

$X(\lambda)$ = radiated spectrum of the ambient light source (See Wyzecki & Stiles, *Color Science*)

$R_\ell(\lambda)$ = relative reflection characteristic of the light emitting element (See Figures 24 and 35)

$R_B(\lambda)$ = relative reflection characteristic of the surrounding background (See Figures 24 and 35)

When designing a display for optimum luminance contrast, two conditions must be considered. First, it is desirable to have as large a contrast ratio as possible between the illuminated elements and the surrounding background ($C_{ON} = L_vS/L_vB \gg 1$). This is achieved by choosing a background with low reflectance. Second, it is desirable to minimize the contrast ratio between the non-illuminated light-emitting elements and the background, both of which reflect ambient light ($C_{off} = L_vOFF/L_vB = 1$). This second condition is achieved by choosing a background that nearly matches the reflective characteristics and color of the non-illuminated elements. Thus, the non-illuminated elements will blend into the background in the off condition and in the on condition the eye will not be confused as to which elements are illuminated. For example, HP stretched segment displays for indoor applications are designed such that the painted surrounding package matches the reflected luminance and color of the tinted epoxy segments. Another type of stretched segment display has been designed for high ambient applications. This display package is painted gray to match the luminance and color of the untinted segments.

Enhancement of Luminance Contrast — Filtering

The purpose of filtering is to create a high value of luminance contrast by reducing the luminous sterance of the background to a level that is far less than the luminous sterance of the illuminated segments. Wavelength filters increase contrast by passing the wavelengths of LED emitted light while partially absorbing other wavelengths of ambient light. Neutral density filters increase contrast by attenuating ambient light twice, as it enters the filter and after reflection, whereas the LED emitted light is attenuated only once.

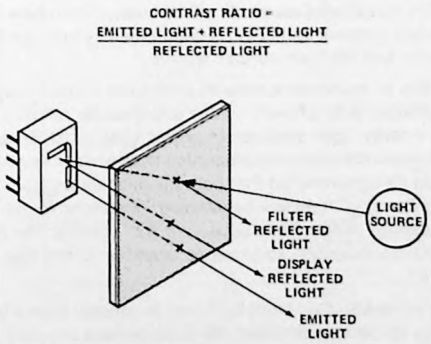


Figure 5. Luminance Contrast for a Light-Emitting Display with a Filter.

When a filter is placed in front of a display, the luminance contrast equation (5) is altered due to two effects. First, the sterance of the illuminated elements and the background is attenuated by the filter. Second, the eye adds the ambient light reflected off the front surface of the filter to both the illuminated elements and the background. Therefore, as shown in Figure 5, the luminance contrast ratio for a light emitting display with a filter can be expressed as:

$$\text{Luminance Contrast Ratio} \quad CR = \frac{L_vS + L_vOFF + L_vF}{L_vB + L_vF} \qquad (6)$$

Where L_vS = Sterance of illuminated element through the filter

L_vOFF = Sterance of light reflected off the element through the filter

L_vB = Sterance of light reflected off the background through the filter

L_vF = Sterance of light reflected off the filter

Mathematically:

$$L_vS = \int \ell(\lambda)Y(\lambda)T(\lambda)\,d\lambda$$

$$L_vOFF = \int X(\lambda)Y(\lambda)T(\lambda)^2R\ (\lambda)d\lambda$$

$$L_vB = \int X(\lambda)Y(\lambda)T(\lambda)^2R_B(\lambda)d\lambda$$

$$L_vF = \int X(\lambda)Y(\lambda)R_F(\lambda)d\lambda$$

where $\ell(\lambda)$ = radiated spectrum of the illuminated light emitting element (See Table 1)

$Y(\lambda)$ = the 1931 CIE photopic curve (See Wyzecki & Stiles, *Color Science*)

$T(\lambda)$ = relative transmission characteristic of the filter (Supplied by Filter Manufacturer)

$X(\lambda)$ = radiated spectrum of the ambient light source (See Wyzecki & Stiles, *Color Science*)

$R_\ell(\lambda)$ = relative reflection characteristic of the light emitting element (See Figures 24 and 35)

$R_B(\lambda)$ = relative reflection characteristic of the surrounding background (See Figures 24 and 35)

$R_F(\lambda)$ = relative reflection characteristic of the filter front surface (See Table 5 and Figure 37)

As exhibited by the luminance contrast equation display readability is greatly affected by the amount and direction of ambient light reflected back into the observer's eyes (L_vF). If too much ambient light is reflected back into the observer's eyes, the luminance contrast ratio will approach a value of 1 and the illuminated elements will be masked from view. The reflected ambient light, L_vF, is determined by both the filter material and the front surface texture.

For dim to moderate ambients a textured surface may be advantageous to diffusely scatter any specular reflectances from nearby light sources. However, care must be exercised when choosing the amount of front surface texture. It should be remembered that both the incident ambient and display emitted light will be diffused. Therefore, to prevent the display image from appearing too blurred, the filter should be mounted as close as possible to the display. (d<1/4")

If higher levels of ambient light may be present from a light source or nearby window, the front surface should have only a very slightly textured finish. Due to the larger quantities of incident ambient light, too coarse a texture will create a large amount of scattered diffuse glare and obscure view of the display. As explained later in *Front Surface Reflectance* and *Filters for Contrast Enhancement-Seven Segment LED Displays*, the other option in higher ambient light levels is to use an untextured surface and cant the filter slightly forward such that specular reflectances are directed downward, away from the eyes of the observer.

Typical Lighting Levels

The level and spectrum of ambient lighting affects the luminance contrast of any display and filter assembly. According to the IES lighting handbook, the following illumination standards are typical for tasks performed indoors; 25-75 footcandles for passageways and active storage rooms, 75-200 footcandles for desk work and up to 1000 footcandles for extra fine bench or machine work. [2] In this application note, 25-75 footcandles ambient illumination will be referred to as dim ambients, 75-200 footcandles as moderate ambients and 250-1000 footcandles as bright ambients. Illumination levels can be easily measured with a calibrated color corrected light meter. Some commercially available light meters are the *Gossen Panlux Electronic Luxmeter*, the *Spectra Lumicon* and the *Sekonic L398*. For indoor applications, the spectrum of ambient lighting can vary from fluorescent to incandescent or even sunlight from a nearby window.

RECOMMENDATIONS FOR WAVELENGTH FILTERING

Figure 2 shows the radiated spectrum for a typical standard red, high efficency red, yellow and green LED and Figures 6 through 10 along with Table 2 summarize the recommended filter transmission curves for each of these colors. Filters with similar characteristics are commercially available and specific manufacturers are listed in Tables 3 and 4. For all colors there are three recommended curves: one for dim ambients, another for moderate ambients and finally a third curve for bright ambients. The curves for moderate and bright ambients have a lower transmission to further reduce the greater amount of reflected ambient light off the display background. In the following section the reasons for specifying a particular transmission curve for each LED color are explained.

Filtering Standard Red Displays (λ_P = 655 nm)

In dim to moderate ambients, filtering out reflected ambient light from red displays is easily accomplished with a long wavelength pass filter having a sharp cut-off in the 600 nm to 630 nm range (see Figure 6). This long wavelength pass filter absorbs the shorter yellow, green and blue wavelengths while passing the red wavelengths and those longer wavelengths to which the eye is not very sensitive. In brighter ambients, above 200 footcandles a gray filter with 18-25% transmission is recommended (See Figure 10). As explained later in *Filtering in Bright Sunlight Ambients*, the gray filter increases readability in brighter ambients by enhancing the color contrast between the illuminated elements and the background.

Filtering High Efficiency Red Displays (λ_P = 635 nm)

In dim to moderate ambients, the use of a long wavelength pass filter with a cut-off in the 570 to 600 nm gives essentially the same results as obtained when filtering red displays (see Figure 7). The resulting color is a deep reddish orange. If several displays are to be assembled in a line, the particular red filter should be chosen carefully. Many red filters have a sharp cut off in the 610-640 nm range, which

falls in the same region as the peak wavelengths of high efficiency red LEDs. As explained in *Peak Wavelength and Filter Transmission* this sharp cut-off may cause an LED with a peak wavelength of 640 nm to pass much more LED emitted light through the filter when compared to an LED with a peak wavelength of 630 nm. If the cut-off is too sharp, the eye may perceive intensity mismatches between these light emitting elements. Two possible filtering techniques can be employed to minimize intensity variations. First, a red filter can be used which exhibits 35-50% transmission and a relatively flat transmission curve in the 620-640 nm wavelength range (see Figure 7). Or, second, a gray filter that has a constant 18-25% transmission across the visible spectrum can be used (see Figure 10). Gray filters with 18-25% transmission are also recommended for bright ambients above 200 footcandles. As explained later in *Filtering in Bright Sunlight Ambients* the gray filter increases readability in brighter ambients by enhancing the color contrast between the illuminated elements and the background.

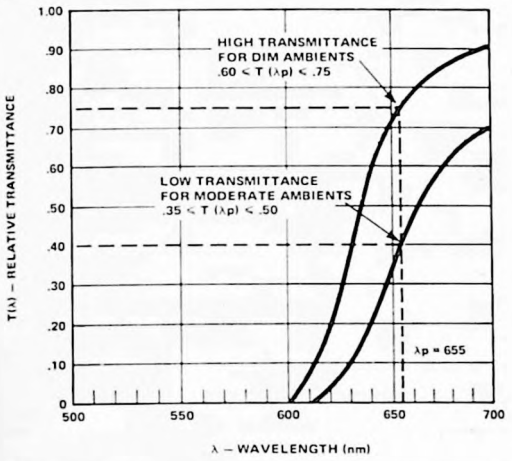


Figure 6. Typical Transmittance Curves for Filters to be Used with Standard Red Displays.

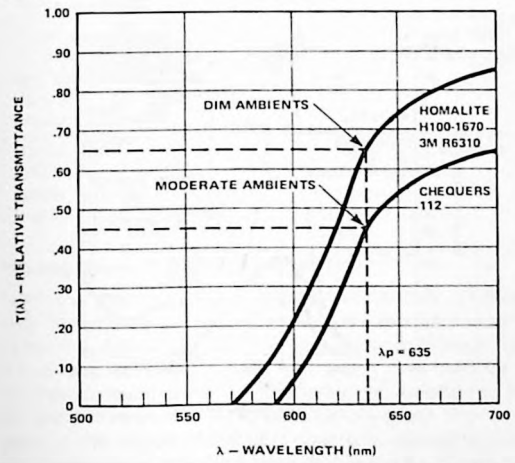


Figure 7. Typical Transmittance Curves for Filters to be Used with High-Efficiency Red Displays.

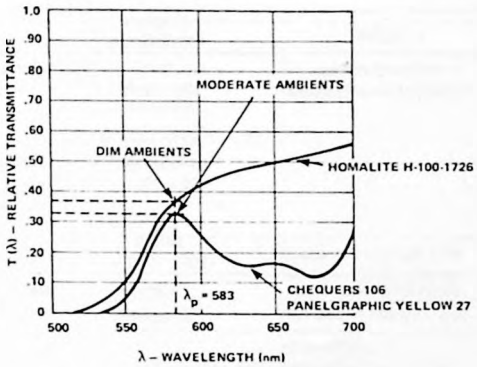


Figure 8. Typical Transmittance Curves for Filters to be Used with Yellow Displays.

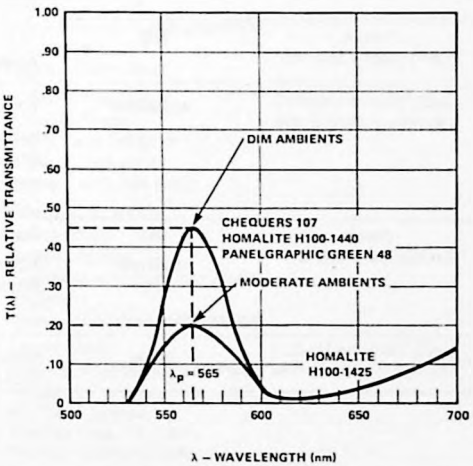


Figure 9. Typical Transmittance Curves for Filters to be Used with Green Displays.

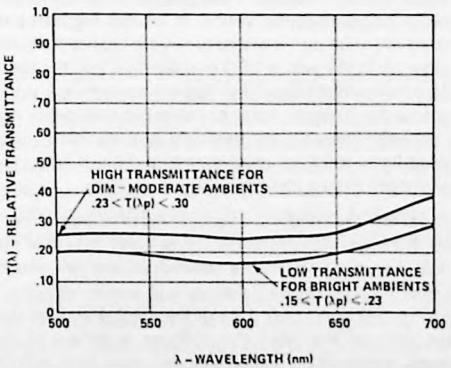


Figure 10. Typical Transmittance Curves for Filters to be Used with All Colored Displays.

APPLICATIONS

Table 2. Filter Recommendations For Various Display Colors And Levels of Ambient Illumination

Color	Ambient Illumination	Recommended Filter Type	Comments
Standard Red (λ_p Typical = 655 nm)	Dim (25 - 75 fc)	Red Long Pass (70%T) with cut-off in 600-630 nm region	Red Filters will save power because a maximum amount of LED light is transmitted through the filter
	Moderate (75 - 200 fc)	Red Long Pass (45%T) Neutral Density Gray or Bronze (20-25%T)	
	Bright (200 - 1000 fc)	Neutral Density Gray or Bronze (18-23%T)	Gray or Bronze filters enhance color contrast
High Efficiency Red (λ_p Typical = 635 nm)	Dim	Red Long Pass (65%T) with cut-off in 570-600 nm region	Red Filters will save power because a maximum amount of LED light is transmitted through the filter
	Moderate	Red Long Pass (40%T) Neutral Density Gray or Bronze (20-25%T)	Red filters with sharp cut-off in the 610-640 nm range may cause intensity mismatches
	Bright	Neutral Density Gray or Bronze (18-23%T)	Gray or Bronze filters enhance color contrast
Yellow (λ_p Typical = 583 nm)	Dim	Yellow Band Pass (30%T) Amber Long Pass (40%T)	Most effective filter is amber although a yellow band pass filter may be used
	Moderate	Amber Long Pass (40%T)	
	Bright	Neutral Density Gray or Bronze (18-23%T) Neutral Density Gray (30%T)/ Light Amber (80%T) combination	Gray, Bronze, or Gray/Amber combination filters enhance color contrast
Green (λ_p Typical = 569 nm)	Dim	Green Band Pass (45%T)	
	Moderate	Neutral Density Gray or Bronze (20-25%T)	Gray recommended for moderate-bright ambients because the eye is very sensitive to background reflected light in the green region
	Bright	Neutral Density Gray or Bronze (18-23%T)	Gray or Bronze Filters enhance color contrast

Filtering Yellow Displays (λ_p = 583 nm)

In dim ambients, amber filters or yellow band pass filters are recommended for filtering yellow displays (see Figure 8). It is more difficult to achieve a high contrast when filtering yellow displays because yellow is in the region of the standard observer curve where the eye is most sensitive. In this case, both the yellow LED emitted light and the yellow ambient light reflected off the display background will be passed by the filter. In order to achieve a noticeable contrast between the LED emitted light and the background reflected light, the filter must absorb a greater amount of ambient light than a red filter.

The most effective filters are dark yellow or orange (amber), although a lower transmittance yellow band pass filter may be used. Figure 11 shows the effect of such a yellow band pass filter on a yellow LED display with a peak wavelength of 583 nm. Although only 27% of the display emitted light passes through the filter, the contrast is enhanced. For moderate ambients an amber filter or a gray filter with 20-25% transmission is recommended. And as recommended for red displays in brighter ambients above 200 footcandles a gray filter with 18-23% transmission should be used.

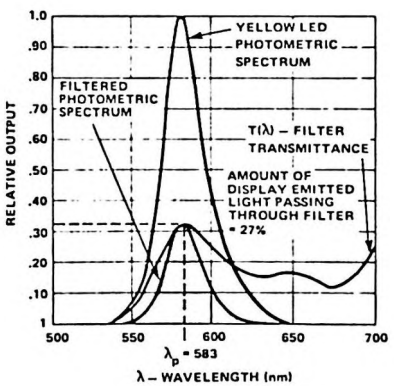


Figure 11. Effect of a Wavelength Filter on a Yellow LED Display.

Table 3. Plastic and Glass Filter Manufacturers

PLASTIC FILTER MANUFACTURERS

Manufacturer	Product
SGL HOMALITE 11 Brookside Drive Wilmington, DE 19804 Phone: (302) 652-3686 SGL International 76 Euclid Avenue Haddonfield, NJ 08033 Phone: (609) 429-7400	Polyester wavelength and neutral density filters; two optional anti-reflection surfaces and three different grades of polyester available.
Rohm and Haas Independence Mall West Philadelphia, PA 19105 Phone: (215) 592-3000 Rohm and Haas Canada, Ltd. 2 Manse Road West Hill, Ontario MIE 3T9 Phone: (416) 284-4711 Rohm and Haas Company European Operations Chesterfield House, 4th Floor Barter Street London WC 1A2TP Phone: 01-242-4455	Plexiglas®; sheet and molding powder; wavelength and neutral density filters.
Chequers Engraving, Ltd. 1-4 Christina Street, London EC2A 4PA Phone: 01-779-6964/5	Spectrafilter®; wavelength and neutral density filters with optional glarecheq anti-reflection surface.
3M-Company Industrial Optics Carbonless/Related Prod. Div. 225-35 3M Center St. Paul, MN 55144 Phone: (612) 733-4403	Panel Film® and Louvered Light Control Film®; wavelength and neutral density filters with abrasion-resistant and anti-reflection surfaces available.
Panelgraphic Corporation 10 Henderson Drive West Caldwell, NJ 07006 Phone: (201) 227-1500 Thorne/Panelgraphic Great Cambridge Road Enfield, Middlesex England Phone: 01-366-1291	Chromafilter®; wavelength and neutral density filters with scratch-resistant and anti-reflection surfaces available.
Polaroid Corporation Polarizer Division One Upland road Norwood, MA 02062 Phone: (617) 769-6800	Circular Polarizing filters with an optional anti-glare surface.
Duralith Corporation 525 Orange Street Milville, New Jersey 08332 Phone: (609) 825-6900	Polyester, Polycarbonate or Acrylic laminated display panels and membrane switch panels

Glass Filter Manufacturers

Manufacturer	Product
Schott Optical Glass Inc. Duryea, PA 18642 Phone: (717) 457-7485 Schott Glass Vlaswerke Hattenbergstrasse No. 10 6500 Mainz W. Germany Phone: 49-61-31-661	Glass wavelength and neutral density filters.
Hoya Optics U.S.A., Inc. 3400 Edison Way Fremont, CA 94538 Phone: (415) 490-1880	Glass wavelength and neutral density filters.
OCLI Optical Coating Laboratories, Inc. 2789 Northpoint Parkway Santa Rosa, CA 95401-7397 Phone: (707) 545-6440 OCLI Europe 621 London Road High Wycombe, Buckinghamshire England HP11 1ET Phone: (0494) 36286	High-efficiency, anti-reflection (HEA®) coatings for glass filters.
Polaroid Corporation Polarizer Division One Upland Road Norwood, MA 02062 Phone: (617) 769-6800 Polarizers (U.K.) Ltd. Lincoln Road Cressex Estates High Wycombe, Buckinghamshire England Phone: High Wycombe 01-205-025	Optically-coated glass with circular polarizer.
Liberty Mirror Division of Libbey-Owens-Ford Company 851 Third Avenue Brackenridge, PA 15014 Phone: (412) 224-1800	Optically-coated glass with circular polarizer.
Precision Glass Laminations 324 Yolanda Santa Rosa, CA 95404 Phone: (707) 528-9070	Optically-coated glass with circular polarizer.
Marks Polarized Corporation 153-16 10th Avenue Whitestone, NY 11357 Phone: (212) 767-9600	Optically-coated glass with circular polarizer.

Filtering Green Displays (λ_P = 565 nm)

Since the peak wavelength of a green display is typically only 10 nm away from the peak of the standard observer curve, it is difficult to achieve high contrast through filtering. A long wavelength pass filter, such as is used for red and yellow displays, is no longer effective. An effective filter for dim ambients is a band pass yellow-green filter which peaks in the region of the LED spectrum. Similar to yellow band pass filters, the recommended green band pass filter reduces background reflected light (see Figure 9) by having a much lower transmission than a red filter. Figure 12 shows the effect of a green band pass filter on a green LED with a peak wavelength of 565 nm. Although only 33% of LED emitted light passes through the filter, the contrast is enhanced. Due to the increased sensitivity of the eye to background reflected light, a gray filter with 20-25% transmission is recommended for moderate ambients and a lower transmission gray filter of 18-20% for brighter ambients.

Filtering All Display Colors

If displays of different colors are to be placed behind one filter, a neutral density gray filter is the best choice. Neutral density gray filters have nearly constant transmission across the visible spectrum. They enhance contrast by attenuating ambient light twice, both as it enters the filter and after reflection, whereas the LED emitted light is attenuated only once. To maximize the contrast between off elements and

Table 4. Recommended Products and Applications for Plastic and Glass Filters

Filter Products	% Transmission at LED Peak	LED Display Color	Ambient Lighting	Maximum Front Surface Texture If Desired
PLASTIC FILTER PRODUCTS				
SGL Homalite Grade 100				
H100-1650	75%	Stand. Red	Dim Moderate	LR-72 LR-92
H100-1670	71%	High Effic. Red	Dim Moderate	LR-72 LR-92
H100-1720 H100-1726	46% 34%	Yellow	Dim to Moderate	LR-72
H100-1440 H100-1425	40% 25%	Green	Dim	LR-72 LR-92
H100-1266 (Gray) H100-1250 (Gray) H100-1230 (Bronze)	25% 26% 25%	All	Bright or Sunlight	None
Rohm & Haas - Plexiglas®				
2423	65%	Stand. Red	Moderate	
2074 (Gray) 2370 (Bronze) 2538 (Gray)	20% 15% 16%	All	Bright or Sunlight	
Chequers Engraving Ltd. - Spectrafilter®				
118 112	85% 45%	Stand. Red	Dim Moderate	Glarecheq
110 112	80% 20%	High Effic. Red	Dim Moderate	Glarecheq
106	32%	Yellow	Moderate	Glarecheq
107	48%	Green	Dim	Glarecheq
105 (Gray)	23%	All	Bright or Sunlight	None
3M Company - Panel Film® or Light Control Film®				
R6510 P7710 (Purple)	70% 85%	Stand. Red	Dim to Moderate	ABM6
R6310	67%	High Effic. Red	Dim to Moderate	ABM6
A5910	45%	Yellow	Moderate	ABM6
ND0220 (Gray)	27%	All	Bright or Sunlight	Glos
Panelgraphic Corporation Chromafilter®				
Ruby Red 60 Dark Red 63	70% 50%	Stand. Red	Dim Moderate	Anti-Reflection None
Scarlet Red 65	60%	High Effic. Red	Dim	Anti-Reflection
Yellow 27 Amber 23	30% 27%	Yellow	Dim Moderate	Anti-Reflection None
Green 48	48%	Green	Dim	Anti-Reflection
Gray 15 Gray 10	17% 23%	All	Bright or Sunlight	None
Duralith Corporation				
Red Gray	% transmission can be requested	Stand. Red High Effic. Red All		

Table 4. **Continued.**

Filter Products	% Transmission at LED Peak	LED Display Color	Ambient Lighting	Maximum Front Surface Texture If Desired
Polaroid Corporation - Polarizing Filters				
HRCP Red	30%	Stand. Red	Moderate	Non-Glare
HACP Amber HACP 15 (Amber/Gray)	37% 13%	Yellow	Moderate Bright or Sunlight	Non-Glare None
HNCP 37 (Gray)	37%	All	Moderate	Non-Glare
HNCP10 (Gray)	10%	All	Sunlight	Optically-coated glass
GLASS FILTER PRODUCTS				
Schott Optical Glass Inc.				
RG-645 RG-630	80% 97%	Stand. Red	Moderate Dim	
RG-610	95%	High Effic. Red	Dim	
Hoya Optics Inc.				
R-62	90%	Stand. Red	Moderate	
RG-60	85%	High Effic. Red	Moderate	
Polaroid Corporation - Polarizing Filters				
HNCP10 (Gray)	10%	All	Sunlight	Optically-coated glass
Liberty Mirror, Precision Glass Laminations, Marks Polarized				
Polarizing Filters made to customer specification				Optically-coated glass
OCLI Laboratories				
HEA® Coatings placed on glass filters				

the background, 18-25% transmission is recommended (see Figure 10). To minimize the contrast between off elements and the background, a gray bodied display should be used, although colored bodied displays can also be used behind a gray filter. Also, as mentioned in filtering high efficiency red displays, neutral density gray filters with nearly constant transmission offer the advantage of minimizing intensity variations between displays.

In addition, neutral density gray filters with 18-25% transmission are recommended for bright indoor ambients above 200 footcandles and for sunlight ambients. As explained later in Section 2 the gray filter increases readability in bright ambients by enhancing the color contrast between the illuminated elements and the background. The exact transmission is dependent upon the filter front surface reflectance and the level of ambient lighting. In moderate to bright ambients a filter with fairly low diffuse reflectance and 20-25% transmission is recommended. For brighter ambients, above 1000 footcandles, a filter with lower diffuse reflectance and 15-20% transmission is recommended.

Special Wavelength Filters and Filters In Combination

A designer is not limited to a single color wavelength or a neutral density filter to achieve the desired contrast and front panel appearance. Some unique wavelength filters and filter combinations have been successfully developed. One is the purple color filter for use with red LED displays, and another is the use of a neutral density filter in combination with a light amber filter to achieve a dark front panel for yellow LED displays.

The Purple Contrast Filter for Red LED Displays: The filters that have been previously discussed provide a high level of contrast between the illuminated display elements and the surrounding background. Another approach achieves the same contrast ratio, but has a background color quite different than the color of the illuminated LEDs. This color contrast is accomplished by using a dark purple filter with standard red LED displays, as shown in Figure 13. Purple is a mixture of red and blue light which is perceived by the eye as a distinct color from red. Psychologically, a purple contrast filter is more pleasing to many people than a red filter. The reason for this may be that when illuminated, the standard red display stands out vividly against the purple background. Since it is the color difference that enhances the contrast, the purple contrast filter is extremely effective in bright ambients.

Filters in Combination: A neutral density gray filter is often used in combination with other filters to provide a dead front appearance as well as increased contrast in bright ambients. A typical example is given in Figure 14. The resulting filter is the product of the relative transmittance of the light amber, TLA(λ), and the relative transmittance of the neutral density gray, TNG(λ).

$$\text{Filter Transmission } (\lambda) = |TLA(\lambda)\ TNG(\lambda)|$$

The amount of light reaching the eye of a viewer is 24% of the unfiltered LED spectrum.

$$\text{Fraction of Available Light Through a Combination Filter} = \frac{\int \ell(\lambda)\, Y(\lambda)\, |TLA(\lambda)\, TNG(\lambda)|\, d\lambda}{\int \ell(\lambda)\, Y(\lambda)\, d\lambda}$$

Where $\ell(\lambda)$ = radiated spectrum of the illuminated light emitting element (see Table 1)

$Y(\lambda)$ = the 1931 CIE standard observer curve (see Wyzecki & Stiles, *Color Science*)

$TLA(\lambda)$ = relative transmission characteristic of the filter (supplied by filter manufacturer)

$TNG(\lambda)$ = relative transmission characteristic of the filter. (For neutral density gray filters the transmission can be considered a constant across the visible spectrum)

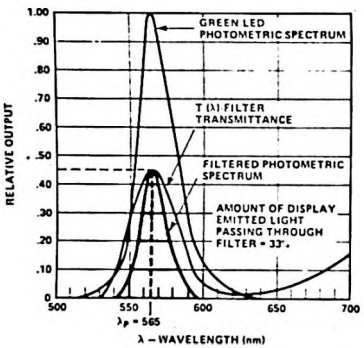


Figure 12. Effect of a Bandpass Wavelength Filter on a Green LED Display.

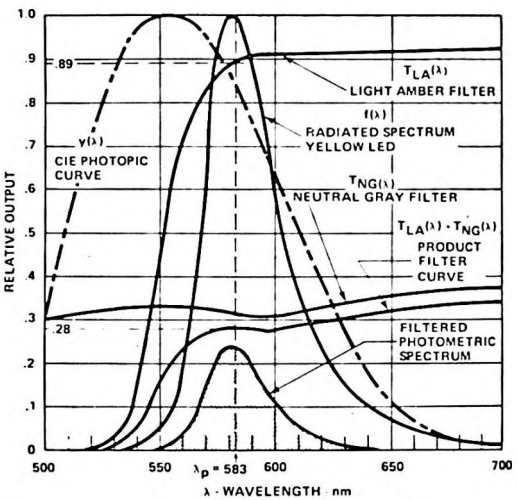


Figure 14. A Neutral Density Gray Filter in Combination with a Light Amber Filter for Use with Yellow Displays.

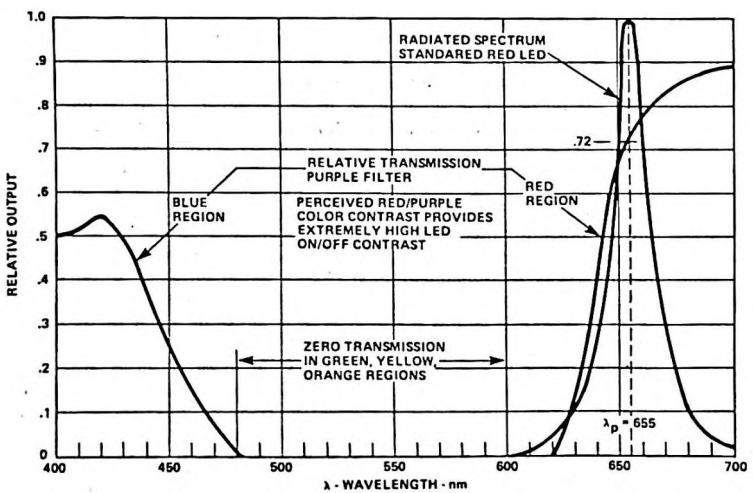


Figure 13. A Purple Color Wavelength Filter for Standard Red LED Displays.

The advantage is a dark gray front panel window with very low luminous sterance (zero transmission below 525 nm) that retains its appearance in bright ambients. The disadvantage is a considerable reduction in the luminous sterance of the display. This is somewhat offset by the distinct color difference between the illuminated yellow segments of the display and the dark gray background.

Another example is a purple or long pass red filter used behind a neutral density gray filter. The recommended transmittance for both of these filter combinations is discussed further in Section 2, *Filter Recommendations for Seven Segment Displays* and *Filter Recommendations for Dot Matrix Displays*.

The disadvantage of using two filters in combination is the added loss of LED emitted light due to four filter air interfaces rather than two interfaces. As shown in *Filter Transmittance*, a single plastic filter with a homogeneous index of refraction equal to 1.5 will lose 4% of LED emitted light at each interface. To avoid any additional loss the two filters should be laminated together with an epoxy that nearly matches the index of refraction of the filter materials.

FILTER MATERIAL AND FILTER REFLECTANCE

Plastic Filters

Due to their low cost, ease in machining to size and resistance to breakage, plastic contrast filters are being used in the majority of display applications. Most manufacturers of plastic filters for use with LED displays provide relative transmission curves similar to those presented in Figures 6 through 10. When selecting a filter, the transmittance curve shape, attenuation at the peak wavelength, wavelength cut off and front surface reflectance should be carefully considered to obtain optimum contrast. As mentioned previously, in dim to moderate ambients, a textured plastic filter can be used. However, in bright ambients an untextured filter with low diffuse reflectance is the best choice.

Four manufacturers of plastic wavelength filters include Rohm & Haas Company (Plexiglas®), Chequers Ltd. (Spectrafilter®), SGL Homalite, 3M-Company (Panel Film®), and Panelgraphic Corp. (Chromafilter®). The LED filters produced by these manufacturers are usable with all LED displays and lamps. Table 3 lists some of the filter manufacturers and where to obtain more information. Table 4 lists specific wavelength and neutral density filters along with recommended applications.

Optical Glass Filters

Optical glass filters are typically designed with constant density, so it is the thickness of the glass that determines the transmission. This is just the opposite of plastic filters which are usually designed such that all material thicknesses have the same transmission.

The primary advantage of an optical glass contrast filter over a plastic filter is its superior performance. This is especially true for red LED filters. Figure 15 illustrates a red optical glass filter for use with high efficiency red LED displays. The relative transmittance is generally higher than that of a comparable plastic filter, and the slope of the relative transmittance curve is usually much steeper and more closely follows the shape of the radiated spectrum of the LED.

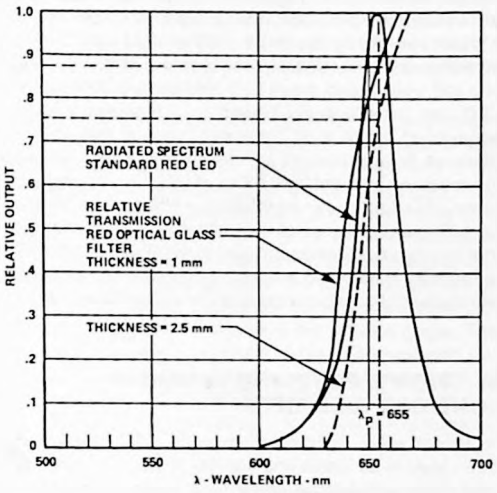


Figure 15. A Red Optical Glass Filter for use with High Efficiency Red LED Displays.

The front surface of an uncoated glass filter typically has 4% specular reflectance and negligible diffuse reflectance. If the filter is to be used in a bright ambient, a High Efficiency Antireflection (HEA) coating can be applied to the front surface. As explained in *Example - Dot Matrix LED Display and Filter*, HEA coatings reduce front surface specular reflectances to 0.25% across the visible spectrum.

Some leading manufacturers of optical glass filters are the Schott Optical Glass, Inc. of Duryea, Pennsylvania and Munich, Germany and Hoya Optics of Fremont, California.

A leading producer of High Efficiency Antireflection (HEA) coated glass is OCLI, Optical Coating Laboratories Inc. of Santa Rosa, California. Table 3 lists some of the filter manufacturers and where to obtain more information. Table 4 lists specific wavelength and neutral density filters along with recommended applications.

EFFECTIVENESS OF A WAVELENGTH FILTER IN AN AMBIENT OF ARTIFICIAL LIGHTING

Contrast is very dependent upon the ambient lighting. Figure 16 reproduces the spectral distribution for fluorescent lighting, incandescent lighting, and sunlight.[3] Fluorescent lighting contains almost no red, yet contains a considerable amount of yellow and long wavelength green. Incandescent lighting is just the opposite. Due to these differences in color content, it is very important to define all lighting spectrums under which the display may be viewed. If a filter is chosen using indoor incandescent lighting, the display may not be readable when used in a sunlight ambient. One frequently encountered example was found in watches and calculators where a high pass red filter was used with a red light emitting display.

If most of the spectral distribution of the artificial lighting is outside of the radiated spectrum of the LED, it is very easy to reduce the reflected ambient light to a very low level without sacrificing too much LED emitted light. Figure 16 also shows the relationship between the peak wavelengths of a red, yellow and green LED and artificial lighting. A red LED can be effectively filtered in a fluorescent ambient because of the lack of red wavelengths in that spectrum. Whereas, in incandescent lighting it is very difficult to reduce the reflected ambient light off a red LED display package. A green LED display can be effectively filtered in an incandescent ambient because of the lack of green wavelengths in that spectrum. Whereas, in fluorescent lighting it is difficult to reduce the reflected ambient light off the display package without significantly decreasing the LED emitted light.

SECTION 2: FILTERING IN BRIGHT SUNLIGHT AMBIENTS

In recent years, light emitting diode (LED) displays have been used in an increasing number of avionics, automotive, and other applications where high levels of ambient light are present. LED displays of the latest package design and with the brightest dye and appropriate contrast enhancement filters, are now being used in ambients up to 107,000 lm/m^2 (10,000 footcandles). In these bright ambients the following parameters effect the readability of an LED display:

a) Luminance contrast
b) Chrominance (color) contrast
c) Front surface reflections

Historically, when determining sunlight readability, most engineers have considered only the luminance contrast - the ratio of sterance between the illuminated element and its background. Unfortunately, this approach neglects the chrominance contrast of the display - the color difference between the illuminated element and its background. Color must be considered because the eye is sensitive to color differences, as well as differences in luminance. Finally, the luminance and chrominance contrast can be combined into a quantitative measure of sunlight readability, known as the discrimination index. This index was first proposed in 1975 by Jean Pierre Galves and Jean Brun[4] at the 29th Agard Avionics Panel Technical meeting in Paris, France and later adapted to LED displays in 1977 by Dave Evans.[5] Discrimination indices determined under similar ambient conditions permit LED displays to be ranked in order of readability.

The effect of ambient reflected light, briefly mentioned in the Discrimination Index theory is more fully defined in this application note. Specifically examined is how light reflected off the front surface of the filter affects the calculation of luminance contrast and how the color of the emitted light mixed with ambient reflected light affects the chrominance contrast. In order to quantify these effects, the sunlight ambient, the reflectance characteristics of the display and filter surfaces, as well as the observer's viewpoint must be defined.

Sunlight is defined according to it's spectrum, intensity and luminous distribution. As shown in Figure 16 the spectrum of bright sunlight is nearly a flat curve across the visible spectrum. The worst case intensity of bright sunlight can range from 5,000 footcandles falling on an automobile dashboard to 7,000 footcandles for commercial aircraft with a fixed overhead, up to 10,000 footcandles for military aircraft. Two worse case sky luminous distributions should be considered; the sun as a single spot source, and a diffuse sunlight ambient. The first condition describes a clear blue

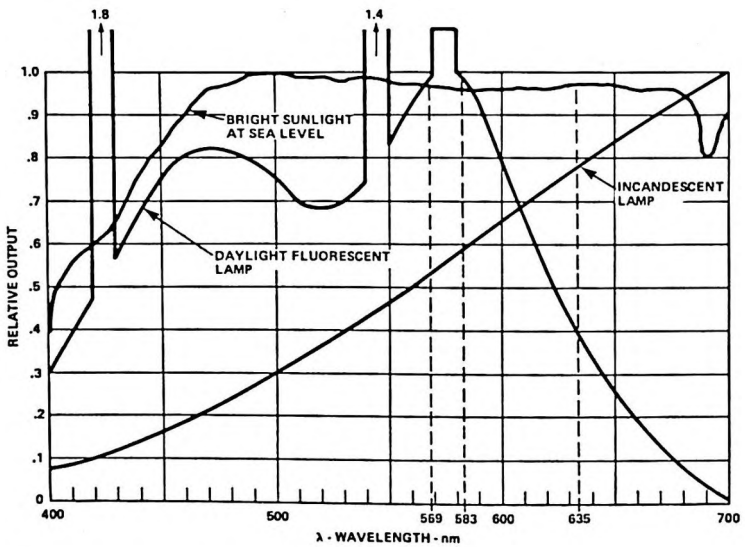


Figure 16. Spectral Distribution for Sunlight, Daylight Fluorescent and Incandescent Ambient Lighting.

sky where the bright glare of the sun's image is reflected back into the observer's view. Because the sterance of the sun's reflected image off of any optical filter is several orders of magnitude greater than the sterance of the illuminated elements, a portion of the illuminated elements will be masked from view. However, it should be remembered that in reality this worst case viewing condition is seldom encountered. Also, with standard mounting techniques the reflected image of the sun can be blocked from the front surface of the filter.

On the other hand, a more commonly encountered worst case viewing condition is a diffuse sunlight ambient that is incident on a filtered display. This condition describes a clear blue sky, ignoring the reflected image of the sun. In the following sections the sky luminous distribution is considered to be a diffuse sunlight ambient.

To understand filtering in bright sunlight ambients according to the Discrimination Index Theory the following topics will be discussed. First, the effectiveness of wavelength filters in diffuse sunlight ambients will be determined. Second, the reflectance of LED display and filter front surfaces will be discussed. Third, the luminance, chrominance and discrimination indices will be defined with special consideration for the effect of ambient reflected light. Fourth, specific filtering techniques will be presented using a seven segment display example and an alphanumeric display example in an ambient of 107,000 lm/m^2. Finally, as a guide for design engineers, specific recommendations for filtering red, yellow, and green displays will be presented along with a list of plastic and glass filter manufacturers.

EFFECTIVENESS OF A WAVELENGTH FILTER IN SUNLIGHT AMBIENTS

Wavelength filters are not recommended for sunlight ambients due to the undesirable affects on luminance and chrominance contrast. Certain high transmission wavelength filters will create insufficient luminance contrast. This occurs when the combination of reflected sterance off the display background, as seen through the filter and off the front surface of the filter, is far greater than the sterance of the light emitting elements.

Also, wavelength filters create little color contrast between the light emitting elements and the background. This is due to the fact that color is determined by the wavelengths of emitted or reflected light. Wavelength filters pass a large amount of reflected background light having the same wavelength as the LED emitted light. Thus, a red display with a red filter in a sunlight ambient will appear to have both red light emitting elements and a red background. Readability will be poor due to the lack of color contrast.

Although wavelength filters are not recommended for sunlight ambients other filters can be used. Actually, LED displays are quite readable in diffuse sunlight ambients if the package design and filtering techniques optimize both luminance and chrominance contrast. Before defining luminance and chrominance contrast, the effect of front surface reflectance should be considered.

DISCRIMINATION INDEX THEORY

Front Surface Reflectance

The Discrimination Index theory can be applied to any display technology. However, it is important to consider the front surface reflectance of the display package and even more importantly the reflectance of the filters which are typically used to enhance contrast. Front surface reflectance will decrease the contrast ratio and also desaturate the color of the display. Color desaturation occurs in bright sunlight when the eye mixes the display emitted light with the reflected ambient light.

The amount of reflected ambient light in a diffuse sunlight ambient is dependent upon the front surface material and also on the viewing condition. As shown in Figure 17 there are two viewing conditions that should be considered. First is a typical viewing condition where the observer sees only diffuse reflectance. Diffuse reflectance refers to scattered light. A highly diffusing surface will appear equally bright from all angles of view because the radiation pattern is nearly lambertian. For a lambertian pattern, the intensity of emitted light varies as the cosine of the off-axis angle. The examples in *LED Seven Segment Display Example* and *Dot Matrix LED Display Example* assume all devices measured are lambertian. Thus, for diffuse reflectance the total percent reflected light is divided by π to arrive at the sterance (cd/m^2).

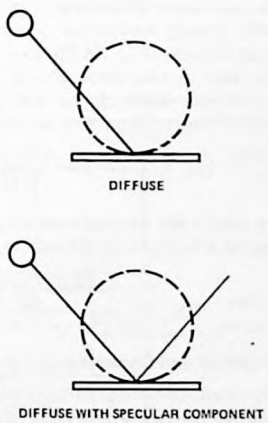


Figure 17. Types of Background Reflections from Display Surfaces — Two Viewing Conditions.

Second, is a worst case viewing condition where the observer sees both diffuse and specular reflectance. Specular reflectance refers to a ray or beam of light that is reflected from a planar surface, such as a mirror, where the angle of reflection equals the angle of incidence. Both angles are measured from a line perpendicular to the surface called the normal. The formulas used to calculate luminance index and chrominance index under conditions of reflected ambient light are derived in the following section. Appendix A shows the integrals used in computation.

Luminance Contrast and Luminance Index[6]

As previously defined in *Enhancement of Luminance Contrast — Filtering*, the luminance contrast ratio for a filtered LED display is given by the following equation:

$$\text{Luminance Contrast Ratio} \quad CR = \frac{L_vS + L_vOFF + L_vF}{L_vB + L_vF} \qquad (7)$$

Luminance difference, EL, can be defined as the eye's response to the contrast ratio. Because the eye responds to changes in light levels logarithmically, EL is defined as

$$\text{(Luminance Difference)} \quad EL = \text{Log } CR \qquad (8)$$

As established in photography and television, the smallest discernable contrast ratio the eye can perceive is 1.05. This contrast ratio of 1.05 inserted in the luminance difference equation (EL) yields a threshold luminance difference (ELTH) of 0.021. However, for comfortable discernability it has been demonstrated in photography and television that a contrast ratio of 1.4 between two pieces of monochrome information is desirable. This yields a luminance difference of 0.15, called a unitary luminance difference (ELU) which is seven times the threshold luminance difference (ELTH).

$$ELTH = \text{Log } 1.05 = 0.021 \qquad (9)$$

$$ELU = \text{Log } 1.4 = 0.15$$

The unitary luminance difference (ELU) can be visually observed by comparing two monochromatic steps on the Kodak gray scale that are four steps apart. On the gray scale each step represents a 10% change in luminance, so two steps, four steps apart, represents a 40% change in luminance.

The ratio of the luminance difference of an actual display compared to the unitary luminance difference (ELU) is called the luminance index (IDL). An IDL value of one would imply a display with a luminance difference just large enough for comfortable discernability. Any value of luminance index greater than or equal to one is desirable.

$$\text{(Luminance Index)} \quad IDL = \frac{EL}{ELU} = \frac{\text{Log } CR}{0.15} \qquad (10)$$

Thus, using the previously defined contrast equation, the luminance index for a filtered LED display becomes:

$$\text{Luminance Index Filtered LED Display} \quad IDL = \text{Log}\frac{\left(\frac{L_vS + L_vOFF + L_vF}{L_vB + L_vF}\right)}{0.15} \qquad (11)$$

Chrominance Contrast and Chrominance Index[7]

Chrominance contrast is a normal part of everyday life. For example, an observer can easily distinguish a gold braid on a purple robe. Even so, the concept of chrominance contrast has only recently been applied to light emitting displays in order to achieve readability in bright sunlight. Before defining chrominance contrast and chrominance index, the determination of LED color and the concept of color difference must be explained.

LED Color: High efficiency red, yellow and green devices of the GaP substrate technology are possible colors for use in sunlight ambients. The GaP (gallium phosphide) substrate LED technology is chosen because its quantum efficiency is significantly higher than the GaAs (gallium arsenide) substrate technology.

The 1931 CIE Chromaticity Diagram is used to objectively determine the color of an LED. The CIE system is based on the concept of additive color mixing as derived from experiments in which colors were matched by mixing colored lights. LED color is defined by the dominant wavelength which is that wavelength of the color spectrum which, when additively mixed with the light from the source CIE illuminant C, will be perceived by the eye as the same color as is produced by the radiated spectrum. CIE illuminant C is a 6500-degree Kelvin color temperature source that produces light which simulates the daylight produced by an overcast sky. A graphical definition of λd and color purity is given on the CIE chromaticity diagram in Figure 18. The dominant wavelength is derived by first obtaining the x,y color coordinates from the radiated spectrum. These color coordinates are then plotted on the CIE chromaticity diagram. A line is drawn from the illuminant C point through the x,y color point intersecting the perimeter of the diagram. The point where the line intersects the perimeter is the dominant wavelength, λd. The dominant wavelengths and corresponding colors for LEDs are shown on the CIE chromaticity diagram in Figure 19.

Also shown in Figure 18 is the color purity, or saturation, which is defined as the ratio of the distance from the x,y color point to the illuminant C point, divided by the sum of this distance and the distance from the x,y point to the perimeter. The x,y color coordinates for LEDs plot very close to the perimeter of the chromaticity diagram. Therefore, the color purity approaches a value of 1, typical of the color saturation obtained from a monochromatic light source. However, as discussed in the following section, this color purity is desaturated by reflected ambient light.

Chromatic Distance and the 1960 CIE-UCS Chromaticity Diagram: The ability of the eye to discern the color difference between the illuminated LED and the background can be evaluated by measuring the distance between their respective color coordinates. In this case, the 1931 CIE color system should not be used because the areas of unitary observed color differences are ellipses which leads to errors when using the distance between two color coordinates in the diagram as a measure of color difference.[8] The 1931 system was reshaped in 1960 so that the areas of observed color difference are nearly circular. Although the 1960 Chromaticity Diagram was again reshaped in 1976 to a more uniform color space, a comparison between these two systems shows rather close agreement in red-green chromaticity difference perception and significant disagreement in blue-purple chromaticity difference perception.

In this diagram the distance between any two chromaticity coordinates in the green to red region can be considered a measure of their color difference. For example, Figure 21 shows the chromatic distance (EC) between a gray background and red LED. According to the Discrimination Index Theory, the chromatic distance between an illuminated element and its background can be calculated using the following equation based on the 1960 CIE UCS Chromaticity Diagram.

$$\text{(Chromatic Distance)} \quad EC = \sqrt{(u_\ell - u_b)^2 + (v_\ell - v_b)^2} \qquad (12)$$

Where (u_ℓ, v_ℓ) = Color of emitted light

(u_b, v_b) = Color of background reflected light

However, in actual practice, this chromatic distance is reduced by desaturation of the display color which occurs when ambient light is reflected off the front surface of the filter and the illuminated LED element. The amount of desaturation depends upon the luminance ratio between the LED emitted light and the reflected ambient light. To account for this effect, the Chromatic Distance (EC) equation must be re-written, where the terms $u_{b\ell}, v_{b\ell}$ are the color coordinates of the mixture of emitted light and reflected light.

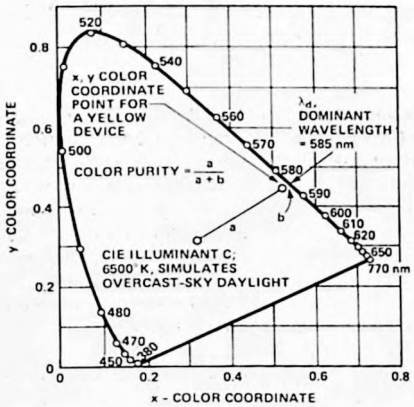


Figure 18. Definition of Dominant Wavelength and Color Purity, Shown on the CIE Chromaticity Diagram.

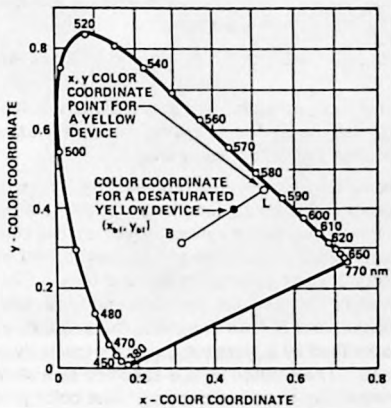


Figure 20. Additive Color Mixture.

SYMBOL	COLOR NAME
R	RED
rO	REDDISH-ORANGE
O	ORANGE
yO	YELLOWISH-ORANGE
Y	YELLOW
gY	GREENISH-YELLOW
YG	YELLOW-GREEN
yG	YELLOWISH-GREEN
G	GREEN
bG	BLUISH-GREEN
BG	BLUE-GREEN
gB	GREENISH-BLUE
B	BLUE
pB	PURPLISH-BLUE
bP	BLUISH-PURPLE
P	PURPLE
rP	REDDISH-PURPLE
RP	RED-PURPLE
pR	PURPLISH-RED
pPK	PURPLISH-PINK
PK	PINK
OPK	ORANGE-PINK
C	CIE ILLUMINATED C

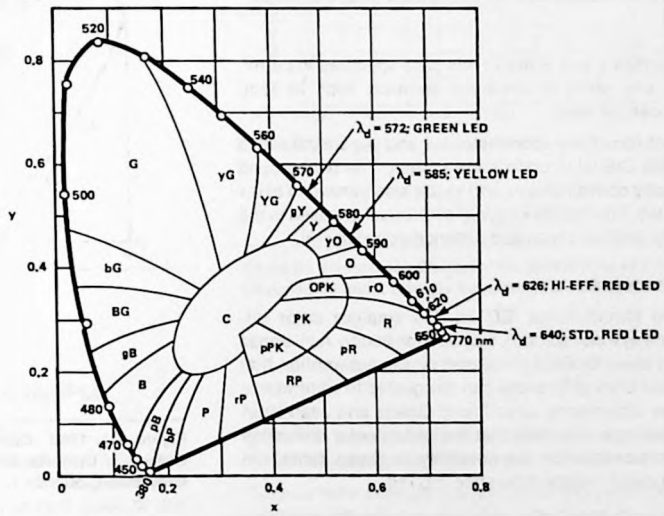


Figure 19. Dominant Wavelengths and Corresponding Colors for LEDs, Shown on the CIE Chromaticity Diagram.

(Chromatic Distance) $EC = \sqrt{(u_{b\ell} - u_b)^2 + (v_{b\ell} - v_b)^2}$ (13)

Where

$(u_{b\ell}, v_{b\ell})$ = Color mixture of emitted light and reflected light

(u_b, v_b) = Color of background reflected light

The u and v coordinates used in the above equations can be calculated using the following principle illustrated in Figure 20, the 1931 Chromacity Diagram.

The chromaticity coordinates representing the mixture of a light source which has luminance L and chromaticity coordinates (x_ℓ, y_ℓ) with a light source which has luminance B and chromaticity coordinates (x_b, y_b) lies at point $(x_{b\ell}, y_{b\ell})$ on the straight line joining (x_ℓ, y_ℓ) and (x_b, y_b). The exact point at which $(x_{b\ell}, y_{b\ell})$ lies depends upon the ratio of the luminances L and B.[9] In this case, the ambient reflected light is specified by a sterance B and chromaticity coordinates x_b, y_b*. The emitted light is specified by a sterance L and chromaticity coordinates x_ℓ, y_ℓ.* The color produced by mixing the emitted light with the reflected ambient light is specified by:[10]

$$x_{b\ell} = \frac{M_\ell x_\ell + M_b x_b}{M_\ell + M_b} \qquad y_{b\ell} = \frac{M_\ell y_\ell + M_b y_b}{M_\ell + M_b} \quad (14)$$

$$M_\ell = \frac{L}{y_\ell} \qquad M_b = \frac{B}{y_b}$$

* Note: See Appendix B for integrals used to calculate x,y chromaticity coordinates of background and illuminated element.

The quantities L and B are in this case specified in cd/m^2, however any units of luminous sterance such as foot-lamberts can be used.

The new chromaticity coordinates $x_{b\ell}$ and $y_{b\ell}$ are translated to the 1960 CIE (U,V) coordinate system. The background chromaticity coordinates x_b and y_b are also translated to u,v coordinates. The results $(u_{b\ell}, v_{b\ell})$ and (u_b, v_b) are used in the previously defined chromatic distance equation (13).

Chrominance Index

Threshold chrominance (ECTH), the smallest color difference the eye can discern, was determined by A.H. Jones in 1968 to equal 0.00384.[11] Based on the assumption that comfortable color differences can be equated to comfortable luminance differences, Jean Pierre Galves and Jean Brun determined experimentally that the unitary color difference (ECU) for comfortable discernability is seven times the threshold chrominance difference (ECTH).

$$ECTH = 0.00384$$
$$ECU = 7 \times 0.00384 = 0.027 \quad (15)$$

The ratio of the chrominance difference of an actual display to the unitary chrominance difference (ECU) is called the chrominance index (IDC). A chrominance index of one would imply a display with a color difference just large enough for comfortable discernability. Any chrominance index greater than or equal to one is desirable.

$$\text{(Chrominance Index) } IDC = \frac{EC}{ECU} = \frac{EC}{0.027} \quad (16)$$

Thus, the chrominance index for the illuminated element becomes:

$$IDC = \frac{EC}{0.027} = \frac{\sqrt{(u_{b\ell} - u_b)^2 + (v_{b\ell} - v_b)^2}}{0.027} \quad (17)$$

Chrominance Contrast of Red, Yellow, Green Displays and a Gray Background: To increase chrominance contrast most Hewlett-Packard sunlight viewable displays are designed with a neutral gray background. Figure 21 shows the color coordinates for a typical gray background and for a red, yellow and green LED. As can be seen, the chromatic distance between the red LED and the gray background is 3 times the chromatic distance between the yellow LED and the gray background. The difference is even greater when the chromatic distance between a red LED and gray background and green LED and gray background are compared. Therefore, for equal sterance a red display has a chrominance contrast advantage over the yellow or green display. However, all displays can be viewable in sunlight ambients when appropriate filtering techniques are employed.

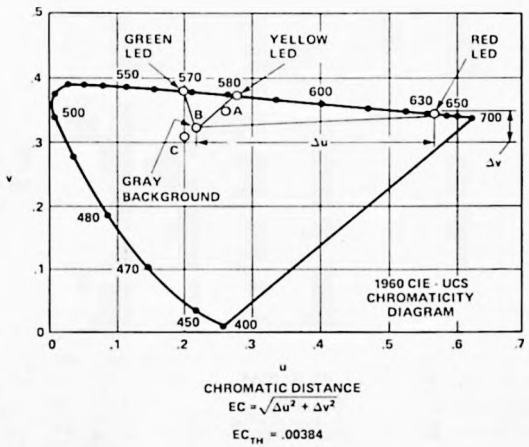


Figure 21. 1960 CIE-UCS Chromaticity Diagram with the Chromatic Distance Between a Green, Yellow or Red LED and a Gray Background.

Discrimination Index[12]

The luminance and chrominance indices can be combined into a figure of merit for readability called the discrimination index. The minimum value of discrimination index for comfortable readability is achieved when either the luminance or chrominance indices are equal to unity.

$$ID = \sqrt{IDL^2 + IDC^2} \qquad IDmin = 1.0 \tag{18}$$

To visualize the total achieved contrast between the illuminated element and its background, the discrimination index may be plotted in the three dimensional 1960 CIE-UCS photocolorimetric space. The photocolorimetric space is defined in the horizontal plane by the 1960 (U,V) Chromaticity System and in the vertical plane by the logarithmic luminance scale.[13] In Figure 22, the luminance index and chrominance index of the illuminated element is plotted as one point and the display background as another. The distance between these two distinct points is the discrimination index.

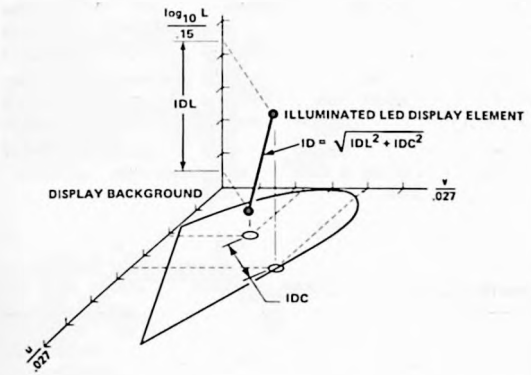


Figure 22. Photocolorimetric Space.

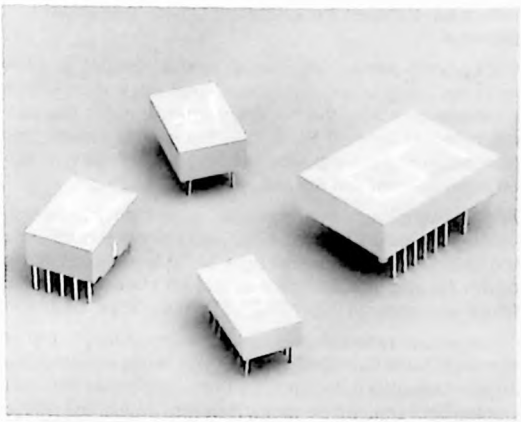


Figure 23. Sunlight Viewable LED Displays.

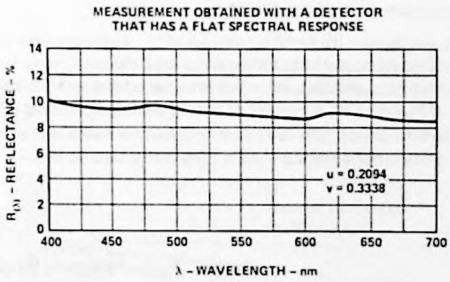


Figure 24. Reflectance Characteristic for the Face of a Gray Body Stretched Segment Sunlight Viewable LED Display.

LED SEVEN SEGMENT DISPLAY EXAMPLE

LED Seven Segment Display Package

Seven Segment LED displays designed for high light ambient conditions can be used to illustrate the discrimination index theory. Figure 23 shows the four sizes of displays which allow for viewing distances of 3,6,7 and 10 meters. These displays are well suited for bright ambient applications due to the chrominance contrast provided by the display package and luminance contrast due to high brightness LEDs. The LEDs are large junction gallium phosphide chips which have high light output and can be driven at increased drive currents. The segment cavities are designed to maximize sterance (intensity/unit area) as well as to maximize chrominance contrast. The color and reflective characteristics of the untinted epoxy segment nearly matches the color and reflectance of the gray painted background. Thus, the off segments blend into the background in the off condition and in the on condition the eye is not confused as to which segment is illuminated.

To determine sunlight readability of this particular display package diffuse and specular reflectance measurements, as defined in *Front Surface Reflectance* were taken on the gray paint and the epoxy. The diffuse measurements were taken using a MacBeth densitometer (RD-100R) which measures at an angle of 45° and the specular measurements were taken using the Hewlett-Packard 8450A spectrophotometer which measures at an angle of 30°.

Figure 24 shows the typical reflectance characteristics for the face of a gray body, seven segment display. The gray paint exhibited less than 0.02% specular reflectance and 9-12% diffuse reflectance. The epoxy was very close with less than 0.02% specular reflectance and 9% diffuse reflectance.

Filters for Contrast Enhancement — Seven Segment LED Displays

Background diffuse reflectances can be reduced to a low level by using a neutral density gray filter with 18-25% transmission across the visible spectrum. Besides attenuating reflected light off the display the neutral density gray filter enhances the chrominance contrast between the illuminated element and the gray display package.

Another consideration is the reflected ambient light, which will significantly reduce the contrast ratio and desaturate the color of the LED emitted light. In Table 5, typical values of diffuse and specular reflectance are shown for plastic filters with textured or untextured front surfaces.

The specular reflectance of either the untextured (4-6%) or textured (2-4%) filter is fairly high. Thus, when viewed at the angle of specular reflectance the glare off the filter will wash out the light emitting elements. However, untextured plastic filters are frequently used in bright sublight. Untextured filters have a smooth front surface and therefore exhibit large amounts of specular reflectance and little diffuse reflectance. As long as the specular reflectances are directed away from the observer's view, the untextured filter will offer the advantage of minimizing diffuse reflectance. For example, the diagram in Table 5 shows how tilting the top of the filter slightly forward will direct specular reflectance downward, away from the observer's eyes.

The particular transmittance [15-25%] is dependent upon the filter front surface reflectance and desired front panel appearance. Plastic filters with low diffuse reflectance (0.3-0.7%) give best results at 18% transmission. This lower transmission of 18% will also produce a more noticeable dead front appearance than a 25% transmission filter.

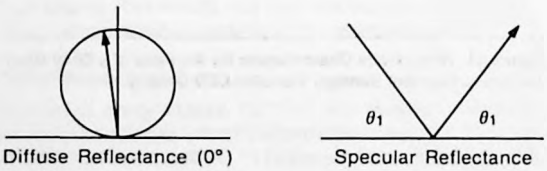
Example — Seven Segment LED Display and Filter

In the following example, a 0.3-inch yellow LED seven segment display (HDSP-4030) is used with an 0.7% diffuse reflectance, neutral density gray untextured plastic filter with 23% transmission in an ambient of 107,000 lm/m^2 (10,000 footcandles). Only diffuse reflectance is considered because the filter has been mounted such that specular reflectances are directed away from the eyes of the observer.

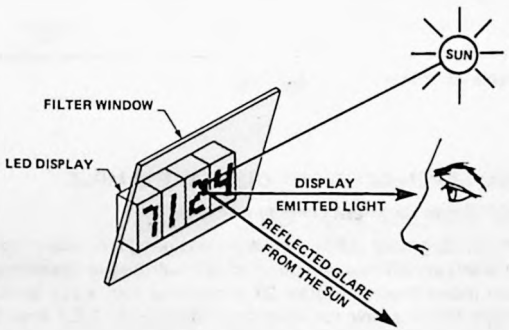
In Figures 25 through 29 luminance, chrominance and discrimination indices are calculated for two conditions. First, with no consideration of front surface reflectance and second, for a typical viewing condition where the observer only sees diffuse reflectance. As can be seen, the value of each index is reduced by front surface reflectance. If an engineer fails to consider front surface reflectance in his calculations, he may be misled in two ways. First, he may believe that a contrast ratio of 1.79:1 can be achieved. However, when diffuse reflectance is considered, the contrast ratio is reduced to 1.42:1. Second, he may also believe that the chromatic distance between the illuminated LED and the background is 0.0853. However, when desaturation due to diffuse reflectance is considered the chromatic distance is reduced to 0.0229.

Finally, when the contrast ratio and chromatic distance are combined into the discrimination index, the consequences of front surface reflectance are evident. The discrimination index without front surface reflectance is 1.58. When front surface reflectance is considered, the discrimination index is reduced to 1.31, which is still above the minimum of 1.0 for comfortable readability. Although the discrimination index of 1.31 is lower than 1.58, it is a more realistic value of the discrimination index perceived by the eye.

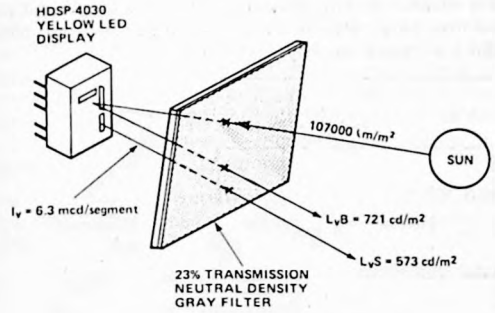
Table 5. Typical Values of Diffuse and Specular Reflectance for Plastic Filters.



Plastic Filter	Diffuse Reflectance at 0°	Specular Reflectance	
		10°	30°
Untextured	.3 - 1.0%	3.0 - 5.0%	4.0 - 6.0%
Textured	.6 - 1.3%	1.0 - 3.0%	2.0 - 4.0%



NOTE:
A FILTER WINDOW CANTED FORWARD WITH RESPECT TO THE PLANE OF THE FACE OF THE DISPLAY DIRECTS REFLECTION AWAY FROM THE EYES OF AN OBSERVER.



$$IDL = \frac{LOG\ CR}{0.15}$$

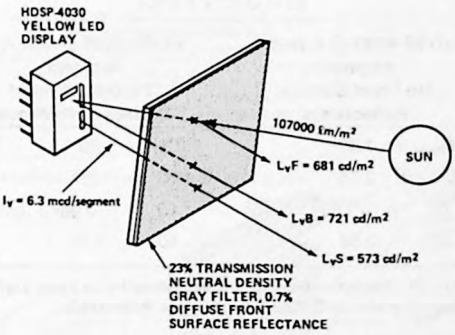
$$CR = \frac{L_vS + L_vB}{L_vB}$$

$$CR = \frac{573 cd/m^2 + 721 cd/m^2}{721 cd/m^2}$$

$$CR = 1.79$$

$$IDL = 1.69$$

Figure 25. Luminance Index — No Front Surface Reflectance.



$$IDL = \frac{LOG\ CR}{0.15}$$

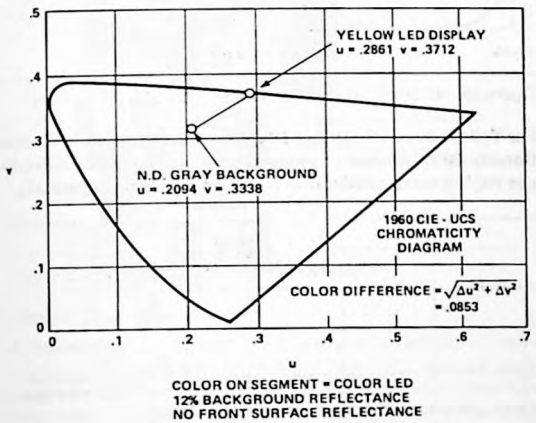
$$CR = \frac{L_vS + L_vB + L_vF}{L_vB + L_vF}$$

$$CR = \frac{573\ cd/m^2 + 721\ cd/m^2 + 681\ cd/m^2}{721\ cd/m^2 + 681\ cd/m^2}$$

$$CR = 1.41$$

$$IDL = 0.99$$

Figure 26. Luminance Index — Diffuse Front Surface Reflectance.



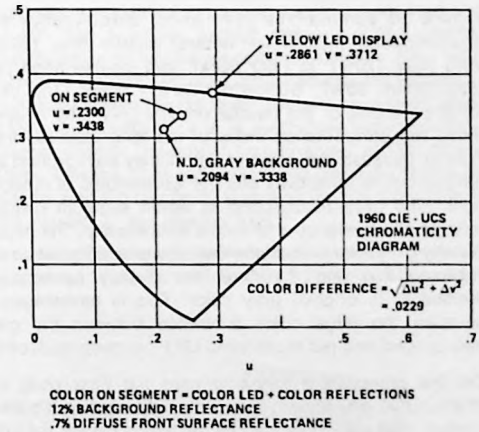
$$IDC = \frac{\sqrt{\Delta u^2 + \Delta v^2}}{0.027}$$

$$\sqrt{\Delta u^2 + \Delta v^2} = 0.0853$$

$$IDC = \frac{0.0853}{0.027}$$

$$IDC = 3.16$$

Figure 27. Chrominance Index — No Front Surface Reflectance.



$$IDC = \frac{\sqrt{\Delta u^2 + \Delta v^2}}{0.027}$$

$$\sqrt{\Delta u^2 + \Delta v^2} = 0.0229$$

$$IDC = \frac{0.0229}{0.027}$$

$$IDC = 0.848$$

Figure 28. Chrominance Index — Diffuse Front Surface Reflectance.

$$ID = \sqrt{IDL^2 + IDC^2}$$

HDSP-4030 @ 6.3mcd/segment No Front Surface Reflectance	HDSP-4030 @ 6.3mcd/segment .7% Diffuse Front Surface Reflectance
IDL = 1.69	IDL = .99
IDC = 3.16	IDC = .85
$ID = \sqrt{1.69^2 + 3.16^2}$	$ID = \sqrt{.99^2 + .85^2}$
ID = 3.58	ID = 1.31

Figure 29. Discrimination Index Calculations for no Front Surface Reflectance and for Diffuse Front Surface Reflectance.

FILTER RECOMMENDATIONS FOR SEVEN SEGMENT DISPLAYS

Plastic, 0.7% Diffuse Reflectance

To obtain filter recommendations for design engineers, three red, yellow, and green seven segment displays were modeled in a computer program in the same fashion as the previous example. A variety of untextured plastic filters, each with a typical diffuse front surface reflectance of 0.7% were also modeled, and discrimination indices calculated in an ambient of 107,000 lm/m² (10,000 footcandles). Based on the discrimination index theory and observation at Hewlett-Packard, the following recommendations are suggested to maximize readability.

For High Efficiency Red Seven Segment Displays, A Neutral Density Gray Filter or Double Band Pass Filter Produces Highest Values of Discrimination Index (see Figure 30).

Figure 30 summarizes luminance, chrominance and discrimination indices for neutral density gray (23%T), long pass (70%T at LED peak), and double band pass (520-560nm 30%T, 610-660nm 30%T) filters. The chrominance index of the neutral density gray filter is seven times the chrominance index of the long pass red filter. This is because the color of the display background is a function of its reflectivity and the wavelengths of reflected light. The gray background of seven segment displays reflects all wavelengths of visible light equally. The neutral density gray filter also attenuates all wavelengths of visible light equally, and therefore, the display background maintains its original gray color. This is advantageous because the large color difference between the gray background and red illuminated LED improves readability.

On the other hand, the long pass red filter does not attenuate all wavelengths of visible light equally. It passes wavelengths only in the red region which causes the gray display background to appear red in color. For this reason, red filters that are perfectly acceptable indoors are difficult to use in bright sunlight, where there is very little color difference between the red background and the red illuminated LED.

A theoretical double band pass filter was also programmed into the computer. The idea was to create a greater chrominance difference between the illuminated element and the background by passing more reflected light at a wavelength other than that of the illuminated LED. In this case, a chrominance index of 4.03 was achieved in comparison to a chrominance index of 3.07 for a neutral density gray filter. The resulting discrimination index of 4.17 is larger than the discrimination index of 3.21 for a neutral density gray filter. This double band pass filter may be achievable by placing a purple filter (50%T) behind a neutral density gray filter (45%T).

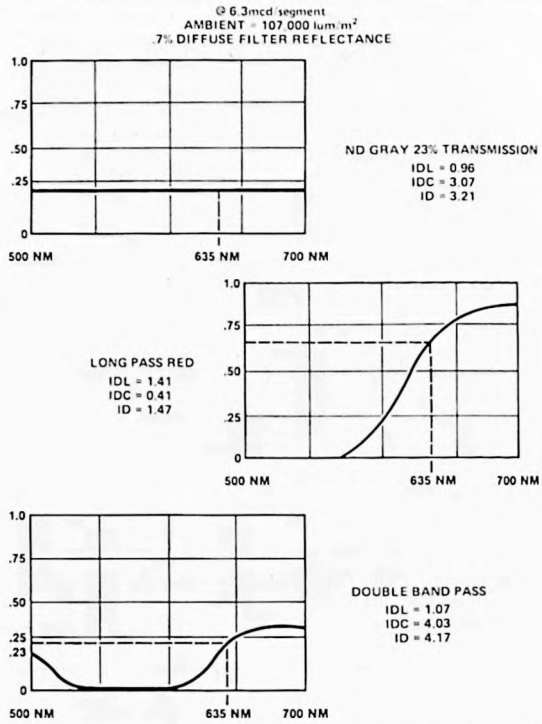


Figure 30. HDSP-3530 High Efficiency Red 0.30-inch Display.

For Yellow Seven Segment Displays a Combination Neutral Density Gray/Amber or Neutral Density Gray Filter Produces High Values of Discrimination Index (see Figure 31).

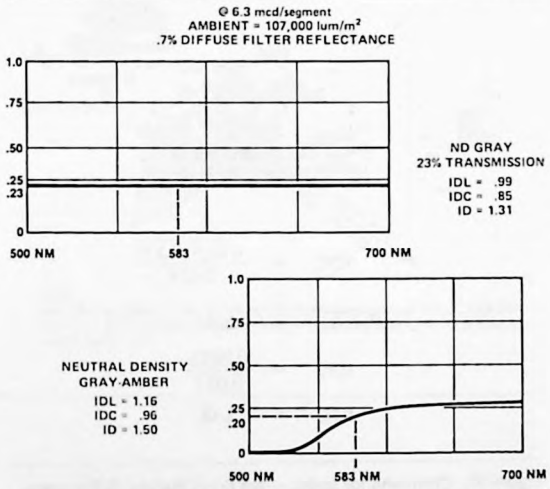


Figure 31. HDSP-4030 Yellow 0.30-Inch Display.

The value of discrimination index for a neutral density gray/amber filter with 20% transmission at the LED peak is 1.50; and for a neutral density gray filter with 23% transmission across the visible spectrum is 1.31. Of these two filters the luminance and chrominance indices of the amber/neutral density gray filter is slightly higher than the luminance and chrominance indices of the neutral density gray filter. Either filter is acceptable depending on the desired front panel appearance.

For Green Seven Segment Displays a Neutral Density Gray Filter Produces Highest Values of Discrimination Index (see Figure 32).

A neutral density gray filter with 23% transmission across the visible spectrum produces a discrimination index of 1.10. Another possibility is a double band pass filter which would increase the chrominance difference between the illuminated LED and the background by passing reflected light of a wavelength other than that of the illuminated LED. However, the feasibility of production and expense of this filter may not warrant its development for use with green seven segment displays.

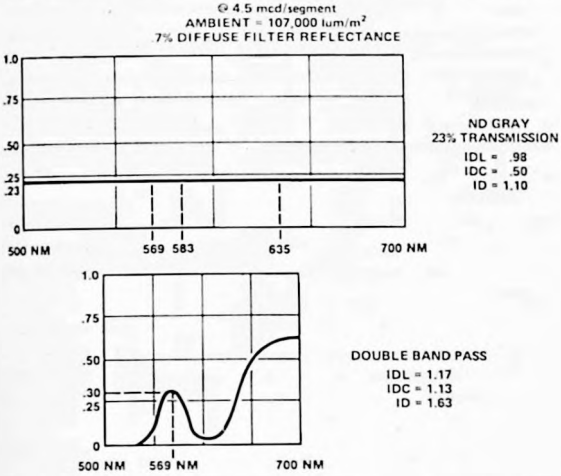


Figure 32. HDSP Green 0.30-Inch Display.

Plastic, Louvered Filters

A louvered filter operates similarly to a venetian blind. As shown in Figure 33, light from the LED display passes between the louvers to the observer. On the other hand, incoming off-axis ambient light is blocked by the louvers and therefore is not reflected off the face of the display back to the observer. Although this results in a very high contrast ratio, the trade-off is a restricted viewing angle. For example, the zero degree louver filter shown in Figure 33 has a horizontal viewing angle of 180°, however, the vertical viewing included angle is 60°. The louver aspect ratio (louver depth/distance between louvers) determines viewing angle.

Some applications require a louver orientation other than zero degrees. For one example, an 18° louvered filter may be used on the sloping top surface of a point of sale terminal. A second example is the use of a 45° louvered filter on overhead instrumentation to block out ambient light from ceiling mounted lighting fixtures.

AVAILABLE OPTIONS FOR LOUVERED FILTERS – ANY COMBINATION IS POSSIBLE

ASPECT RATIO AND VIEWING ANGLE	LOUVER ANGLE	LOUVER COLOR
2.75: 1 = 60°	0°	OPAQUE BLACK
2.00: 1 = 90°	18°	TRANSLUCENT GRAY
3.50: 1 = 48°	30°	TRANSPARENT BLACK
	45°	

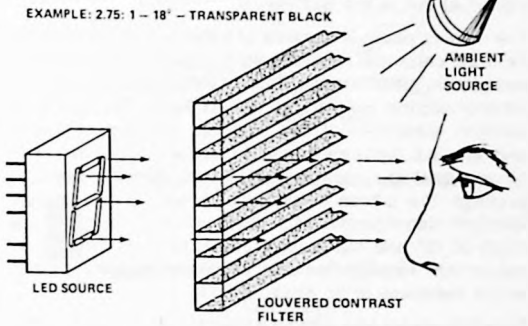


Figure 33. The Operation of a Louvered Filter.

In bright sunlight, neutral density filters with transparent black louvers are most effective. A secondary colored filter may be placed behind the neutral density louvered filters to increase color contrast at the expense of LED emitted light. For sunlight applications, two different louver options are recommended. First a 45° neutral density louvered filter is recommended. This particular filter produces a horizontal and vertical included viewing angle of 60° for a louver aspect ratio of 2.75:1. Another possibility is a neutral density crosshatch filter which increases the contrast but further reduces the vertical and horizontal viewing angle to 40° for a louver aspect ratio of 2.75:1. A crosshatch filter is essentially two zero-degree neutral density louvered filters oriented at 90° to each other. With this filter, red, yellow and green digits mounted side by side will be clearly visible as long as the sunlight is not parallel to the viewing axis.

Louvered filters for LED displays are manufactured by 3M Company, Light Control Division, St. Paul, Minnesota.

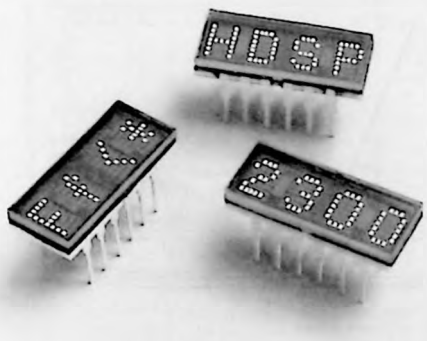


Figure 34. Small Alphanumeric Display.

DOT MATRIX LED DISPLAY EXAMPLE

Dot Matrix LED Display Package

Dot Matrix LED displays can also be used to illustrate the discrimination index theory. Figure 34 shows a particular dot matrix alphanumeric display, with four characters in each package. These displays are well suited for bright ambient applications due to the high sterance of each individual dot in the 5x7 matrix.

The display package consists of a dark ceramic substrate, 140 LED chips and two integrated circuits all covered by a transparent glass window. Each of these materials and the interconnecting gold traces reflect light. To determine sunlight readability of this particular package, specular and diffuse reflectance measurements were taken on each of the package materials. For this particular display package, the diffuse measurements were taken using a MacBeth densitometer (RD-100R) which measures at an angle of 45° and the specular measurements were taken using the Hewlett-Packard 8450A spectrophotometer which measures at an angle of 30°.

Figure 35 shows that without a filter this display has a high amount of specular reflectance due to the traces, LED chips, IC's and the glass window.

Filters for Contrast Enhancement — Dot Matrix Display

Specular reflectances off the display package can be reduced to a very low level by using a circular polarizer. The circular polarizer shown in Figure 36 consists of a linear polarizer and a quarter wave plate laminated together. The linear polarization axis is oriented at 45° to the optical axis of the quarter wave plate. Non-polarized sunlight passing through the linear polarizer is broken into x and y components which emerge from the quarter wave plate, 90° out of phase, circularly polarized. Upon reflection by the specular reflecting display surface, the direction of this circular polarized light is reversed. Passing back through the quarter wave plate, the x and y components are placed back in phase, but since they are linearly polarized at 90° to the linear polarizer, this reflected light is absorbed by the filter.

Another consideration is the ambient light reflected off the front surface of the filter. Too much reflected ambient light will significantly reduce the contrast ratio and desaturate the color of the LED emitted light. Untextured plastic

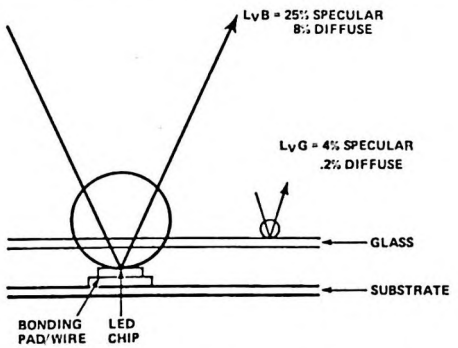


Figure 35. Dot Matrix Alphanumeric Display, Typical Values of Reflectance at 30°.

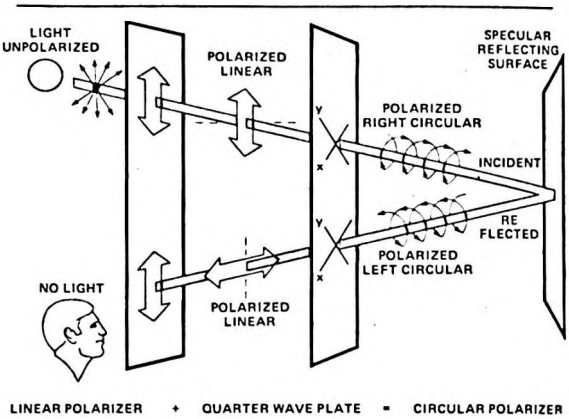


Figure 36. Operation of a Circular Polarizer.

filters are frequently used, and they can perform quite well in bright sunlight if they are mounted in such a way as to direct specular reflectances away from the observer's eyes. For sunlight ambients where specular reflectance cannot be directed away from the observer's eyes, a glass filter with a quarter wavelength, anti-reflection coating can be used. This optical coating minimizes specular reflectances by reducing the apparent index of refraction of the glass filter to a value which closely approximates the index of refraction of air.

This index matching reduces the amount of LED emitted light lost at the glass to air interface and also reduces the amount of ambient light reflected off the front surface of the filter.

The amount of LED emitted light lost at the glass-to-air interface can be calculated by the index of refraction equation discussed in *Peak Wavelength and Filter Transmission.*

$$R = \left(\frac{n_1 - n_2}{n_1 + n_2}\right)^2 \qquad (19)$$

Where n_1 = index of refraction for filter material
n_2 = index of refraction for air

$$\text{Reflection Loss} = 2(R)\ (100\%) \qquad (20)$$

For a clear uncoated glass the reflection loss as calculated below is 10.6%.

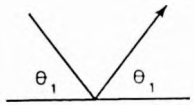
$$R = \left(\frac{1.6 - 1.0}{1.6 + 1.0}\right)^2 = 0.053 \qquad (21)$$

Where n = 1.6, a typical index of refraction for glass
n = 1.0, index of refraction for air

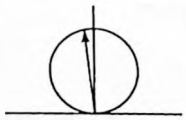
$$\text{Reflection Loss} = 2(0.053)\ 100\% = 10.6\% \qquad (22)$$

In Table 6 typical values of specular and diffuse reflectance are shown for a commercial grade HEA® coating supplied by Optical Coating Laboratories in Santa Rosa, California. The reflectance of the commercial grade HEA® coating (#11-002A) was measured on a Gardner Hazeguard XL-211 Hazemeter (diffuse reflectance) and a

Table 6. Typical Values of Diffuse and Specular Reflectance for HEA Coatings.



Specular Reflectance


Diffuse Reflectance (0°)

Angle of Incidence	Specular Reflectance		Diffuse Reflectance
	Commercial Grade	Military Grade	Both Grades
10°	.10%	.05%	<.02%
30°	.25%	.10%	.02%
45°	.45%	.25%	.04%

Beckman DK2A Spectrophotometer (specular reflectance). As can be observed from the table, HEA coatings are most effective between 0 and 30°. Also shown on Table 6 are reflectance values for a military grade coating — data supplied by manufacturers of anti-reflection coatings. Since the values of specular reflectance are very low (0.20-0.45%), these filters can be used in diffuse as well as specular reflecting viewing conditions. As illustrated in Figure 37, the specualar reflectance of the commercial grade coating (#11-002A) is typically 0.25% for any wavelength in the visible spectrum. For a piece of optically coated clear glass, the amount of LED light lost at the glass-to-air interfaces due to reflection is 0.50%. A reflectance loss of 0.50% through a clear coated glass filter is considerably less than 10.6% for a clear uncoated glass filter.

$$R = \left(\frac{1.105 - 1.0}{1.105 + 1.0}\right)^2 = 0.0025 \qquad (23)$$

Where n = 1.105, a typical index of refraction for optically coated glass

n = 1.0, index of refraction for air

$$\text{Reflection Loss} = 2\,(0.0025)\,(100\%) = 0.5\% \qquad (24)$$

The amount of ambient light reflected off the face of an optically coated glass filter can also be calculated. The luminous sterance of the specular reflected glare in a 107,000 lm/m² ambient is 267 cd/m² for coated glass with 0.25% reflectance, which is considerably less than 2140 cd/m² for an untextured plastic filter with 2.0% reflectance or 4280 cd/m² for an uncoated piece of glass with 4.0% reflectance.

Several manufacturers produce filters consisting of a circular polarizer sandwiched between two pieces of glass, one of which is optically coated. The Polaroid HNCP10, a neutral density gray circular polarizing filter with 10-12% transmission across the visible spectrum is one such filter. Figure 38 is a cut away view of the filter, and Figure 39 portrays its spectral characteristics. The top curve depicts the transmission of unpolarized light (LED emitted light and diffuse reflectances), and the bottom curve the transmission of polarized light (specular reflectances). The bottom curve shows that specular reflectances from the glass window of the display, the top surfaces of the LED's and the on board IC's are reduced to a very low level.

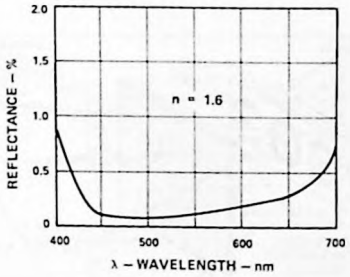


Figure 37. Front Surface Reflectance of Glass with Double Sided 1/4 Wave Optical Coating.

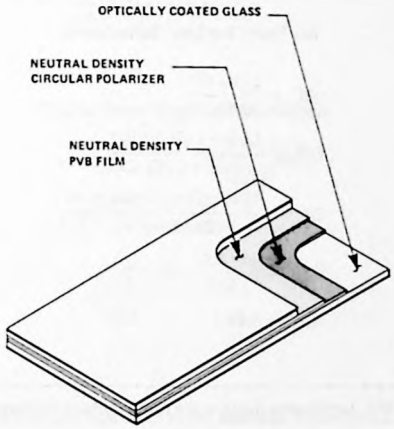


Figure 38. Circular Polarizer Laminated Between a Piece of HEA Coated Glass and a Piece of Uncoated Glass.

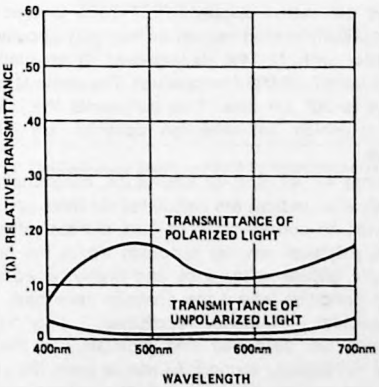
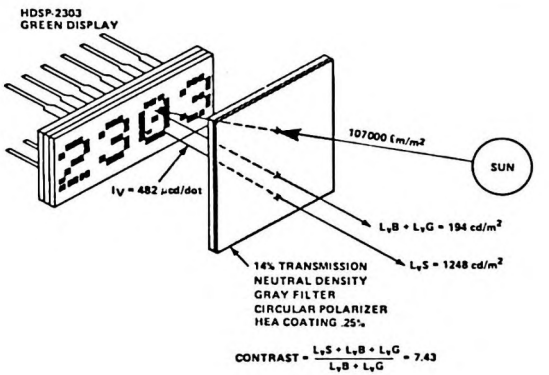


Figure 39. Spectral Characteristics of a Circular Polarizing Optically Coated Glass Filter.

APPLICATIONS



No Front Surface Reflectance

$$IDL = \frac{LOG\ CR}{0.15}$$

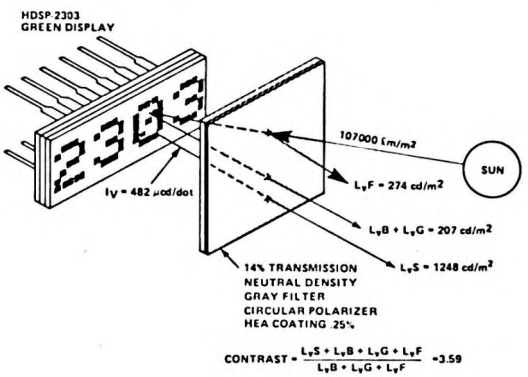
$$CR = \frac{LvS + LvB + LvG}{LvB + LvG}$$

$$CR = \frac{1248cd/m^2 + 194cd/m^2}{194cd/m^2}$$

$$CR = 7.43$$

$$IDL = 5.81$$

Figure 40a. Luminance Index — No Front Surface Reflectance.



Diffuse Front Surface Reflectance

$$IDL = \frac{LOG\ CR}{0.15}$$

$$CR = \frac{LvS + LvB + LvG + LvF}{LvB + LvG + LvF}$$

$$CR = \frac{1248cd/m^2 + 194cd/m^2 + 6.8cd/m^2}{194cd/m^2 + 6.8cd/m^2}$$

$$CR = 7.21$$

$$IDL = 5.72$$

Diffuse and Specular Front Surface Reflectance

$$IDL = \frac{LOG\ CR}{0.15}$$

$$CR = \frac{LvS + LvB + LvG + LvF}{LvB + LvG + LvF}$$

$$CR = \frac{1248cd/m^2 + 207cd/m^2 + 274cd/m^2}{207cd/m^2 + 274cd/m^2}$$

$$CR = 3.59$$

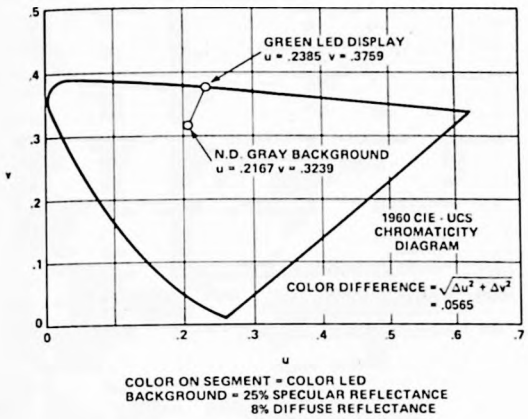
$$IDL = 3.70$$

Figure 40b. Luminance Index — Front Surface Reflectance.

Example — Dot Matrix LED Display and Filter

In the following example, a 0.20 inch green LED alphanumeric dot matrix display (HDSP-2303) is used with a 0.25% optically coated neutral density gray circular polarizing filter with 12-14% transmission in an ambient of 107,000 lm/m² (10,000 footcandles). The angle chosen for analysis is 30° off axis. This represents the maximum angle at which anti-reflection coatings are still very effective.

In Figures 40, 41, and 42 luminance, chrominance and discrimination indices are calculated for three conditions. First, with no consideration of front surface reflectance, second, a typical viewing condition where the observer sees only diffuse reflectance and finally, a worst case viewing condition where the observer sees both diffuse and specular reflectance combined. The last two conditions are described and illustrated in the *Front Surface Reflectance* section. As can be seen, the value of each index is reduced by front surface reflectance. If an engineer fails to consider front surface reflectance in his calculations, he may be misled in two ways. First, he may believe that a contrast ratio of 7.43:1 can be achieved.



COLOR ON SEGMENT = COLOR LED
BACKGROUND = 25% SPECULAR REFLECTANCE
8% DIFFUSE REFLECTANCE

No Front Surface Reflectance

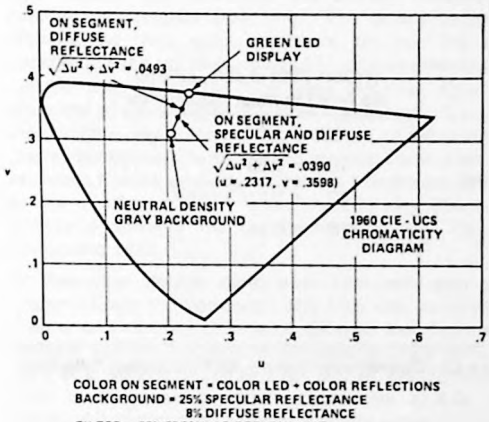
$$IDC = \frac{\sqrt{\Delta u^2 + \Delta v^2}}{0.027}$$

$$\sqrt{\Delta u^2 + \Delta v^2} = 0.0565$$

$$IDC = \frac{0.0565}{0.027}$$

$$IDC = 2.09$$

Figure 41a. Chrominance Index — No Front Surface Reflectance.



COLOR ON SEGMENT = COLOR LED + COLOR REFLECTIONS
BACKGROUND = 25% SPECULAR REFLECTANCE
8% DIFFUSE REFLECTANCE
FILTER = 25% SPECULAR REFLECTANCE
.02% DIFFUSE REFLECTANCE

Diffuse Front Surface Reflectance

$$IDC = \frac{\sqrt{\Delta u^2 + \Delta v^2}}{0.027}$$

$$\sqrt{\Delta u^2 + \Delta v^2} = 0.0493$$

$$IDC = \frac{0.0493}{0.027}$$

$$IDC = 1.83$$

Diffuse and Specular Front Surface Reflectance

$$IDC = \frac{\sqrt{\Delta u^2 + \Delta v^2}}{0.027}$$

$$\sqrt{\Delta u^2 + \Delta v^2} = 0.0390$$

$$IDC = \frac{0.0390}{0.027}$$

$$IDC = 1.44$$

Figure 41b. Chrominance Index — Front Surface Reflectance.

However, when diffuse reflectance is considered, the contrast ratio is reduced to 7.23:1. When both diffuse and specular reflectances are considered, the contrast ratio is significantly reduced to 3.59:1. Second, he may also believe that the chromatic distance between the illuminated LED and the background is 0.0565. However, when desaturation due to diffuse reflectance is considered, the chromatic distance is reduced to 0.0493, and when both specular and diffuse reflectances are considered, the chromatic distance is further reduced to 0.0390.

Finally, when the contrast ratio and chromatic distance are combined into the discrimination index, the consequences of front surface reflectance are evident. The discrimination index without front surface reflectance is 6.18; with diffuse front surface reflectance is 6.0; and when both specular and diffuse reflectances are considered, it is 3.97. Although both 6.0 and 3.97 are lower numbers than 6.18, they represent more realistic values of the discrimination index perceived by the eye.

(HDSP-2303 at 482 μcd/dot)
No Front Surface Reflectance

IDL = 5.81

IDC = 2.09

$ID = \sqrt{5.81^2 + 2.09^2}$

ID = 6.18

Figure 42a. Discrimination Index — No Front Surface Reflectance.

(HDSP-2303 at 482 μcd/dot)
Diffuse Front Surface Reflectance

IDL = 5.72

IDC = 1.83

$ID = \sqrt{5.72^2 + 1.83^2}$

ID = 6.00

(HDSP-2303 at 482 μcd/dot)
Diffuse and Specular Front Surface Reflectance

IDL = 3.70

IDC = 1.44

$ID = \sqrt{3.70^2 + 1.44^2}$

ID = 3.97

Figure 42b. Discrimination Index — Front Surface Reflectance.

FILTER RECOMMENDATIONS FOR DOT MATRIX DISPLAYS (CIRCULAR POLARIZERS, OPTICALLY COATED GLASS)

To determine filter recommendations for design engineers, three green, yellow, and high efficiency red alphanumeric displays were modeled in a computer program in the same fashion as the previous example. A variety of filters each consisting of a circular polarizer sandwiched between optically coated glass were also modeled, and discrimination indices calculated in an ambient of 107,000 lm/m² (10,000 footcandles). Figures 43, 44, and 45 summarize the results for each of the three colors. Based on the discrimination index theory and observation at Hewlett-Packard, the following filter recommendations are suggested to maximize readability.

For Green Displays, a Neutral Density Gray or a Double Band Pass Filter may increase the Discrimination Index (see Figure 43).

A neutral density gray filter with 14% transmission across the visible spectrum produces a discrimination index of 3.97.

To increase the chrominance difference between the illuminated LED and the background by passing reflected light of a wavelength other than that of the illuminated LED, a double band pass filter was also modeled. In this case, a chrominance index of 3.87 was achieved in comparison to the chrominance index of 1.44 for a neutral density gray filter. This particular band pass filter passes 30% of the LED emitted light in a 20 nm bandwidth (560-580 nm) and 60% of the red ambient light in a 40 nm bandwidth (610-650 nm). The final discrimination index is 5.20.

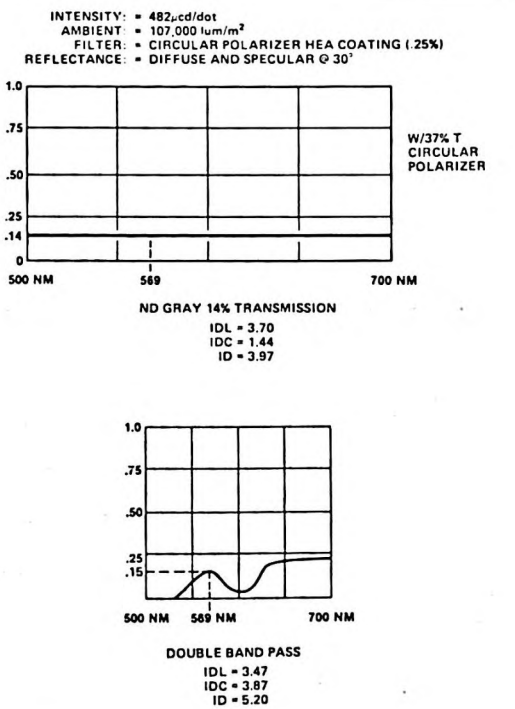


Figure 43. HDSP-2303 Green Alphanumeric 0.20-inch Display.

For Yellow Displays, a Neutral Density Gray/Amber Filter Combination or a Neutral Density Gray Filter Yields High Values of Discrimination Index (see Figure 44).

The value of discrimination index for an amber/neutral density gray filter with 11% transmission at the LED peak is 3.32; and for a neutral density gray filter with 14% transmission across the visible spectrum, the discrimination index is 2.87. Of these two filters, the amber/neutral density gray filter used with a yellow LED display produces the highest values of chrominance and discrimination indices. Another possibility not shown in Figure 44 is a double band pass filter with 35% transmission between 570-590 nm and 60% transmission between 630-660 nm. Although this filter yielded highest values of discrimination index (3.81), it is questionable whether its development would be cost effective and if the added improvement would be significantly noticeable.

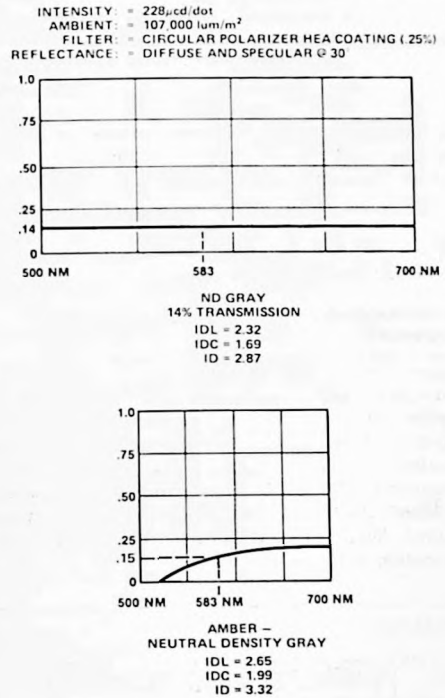


Figure 44. HDSP-2301 Yellow Alphanumeric 0.20-inch Display.

For High Efficiency Red Displays, a Neutral Density Gray Filter Produces High Values of Discrimination Index (see Figure 45).

Figure 45 summarizes luminance, chrominance and discrimination indices for neutral density gray (14%T), long pass (70%T at LED peak), and double band pass filters (520-560 nm 50%T, 610-660 nm 30%T). The chrominance index of the neutral density gray filter is ten times the chrominance index of the long pass red filter. This is because the color of the display background is a function of its reflectivity and the wavelengths of reflected light. The gray background of alphanumeric displays reflects all wavelengths of visible light equally. The neutral density gray filter also attenuates all wavelengths of visible light equally, and therefore, the display background maintains its original gray color. This is advantageous because the large color difference between the gray background and red illuminated LED improves readability. On the other hand, the high pass red filter does not attenuate all wavelengths of visible light equally. It passes wavelengths only in the red region which causes the gray display background to appear red in color. For this reason, red filters that are perfectly acceptable indoors are difficult to use in bright sunlight, where there is very little color difference between the red background and the red illuminated LED.

A theoretical double band pass filter was also programmed into the computer. The idea was to create a greater chrominance difference between the illuminated element and the background by passing more reflected light at a wavelength other than that of the illuminated LED. In this case, a chrominance index of 6.50 was achieved in comparison to a chrominance index of 5.62 for a neutral density gray filter. This double band pass filter may be achievable by placing a purple filter (50%T) behind a neutral density gray filter (30%T).

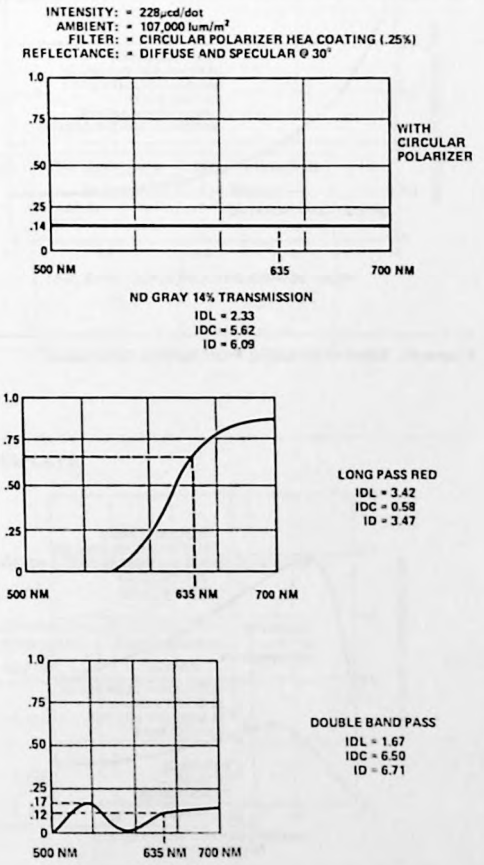


Figure 45. HDSP-2302 High Efficiency Red 0.20-inch Display.

APPLICATIONS

GENERAL CONCLUSIONS

In the previous sections filter recommendations that pertain specifically to seven segment displays and alphanumeric displays have been discussed. There are also some general recommendations that should be followed when choosing *any* LED display and filter for use in a bright sunlight ambient. The four most important general recommendations are discussed in this section.

Front Surface Filter Reflectance Should be Reduced (see Figure 46).

This is important because as the front surface reflectance is reduced, the discrimination index increases. For example, an uncoated neutral density circular polarizing glass filter (14%T) with 4.0% specular reflectance provides a discrimination index of 0.82. This same glass filter with an optical coating of 0.45% provides a discrimination index of 3.23. On the other hand, the same filter with a coating of 0.25% provides a discrimination index of 3.97, while a military grade circular polarizing coated filter of 0.10% provides a discrimination index of 4.86.

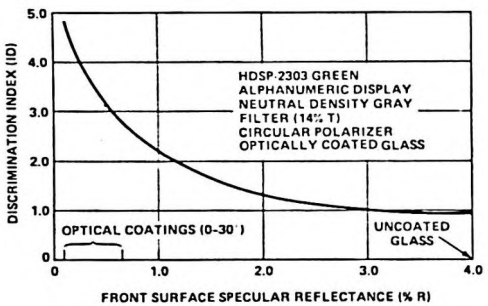


Figure 46. Effect of Reducing Front Surface Reflectance.

For a Given Front Surface Filter Reflectance, The Optimal Neutral Density Gray Filter Transmission Can be Determined (see Figure 47).

The optimal neutral density gray filter transmission is dependent upon the amount of front surface filter reflectance and the reflectance of the materials in the display package.

As an example, a plastic neutral density gray filter with 0.7% diffuse reflectance used with a yellow seven segment display has an optimal transmission of 18-23%. This produces a discrimination index of 1.31 for a 23% transmission filter. A significantly lower transmission filter of 10% will attenuate display emitted light too much in comparison to the amount of front surface reflected light, and its discrimination index will be less than 1.31. On the other hand, a significantly higher transmission filter of 60% will transmit too much background reflected light, so the discrimination index will also be less than 1.31.

As another example, a neutral density gray circular polarizing optically coated glass filter with 0.25% anti-reflection coating used with a green alphanumeric display has an optimal transmission of 10-14%. This produces a discrimination index of 3.97 for a 14% transmission filter. A significantly lower transmission filter of 6% will attenuate display emitted light too much in comparison to the amount of front surface reflected light, and its discrimination index will be less than 3.97. On the other hand, a significantly higher transmission filter of 40% will transmit too much background reflected light, so the discrimination index will also be less than 3.97.

Reduce Incident Ambient Light When Possible (see Figure 48).

As shown in Figure 48, as ambient light is reduced, the discrimination index is increased. As an example, in an ambient of 107,000 lm/m², the background reflected light off a gray bodied seven segment display is 721 cd/m², plastic filter reflected light is 681 cd/m² and the discrimination index is 1.31. If the ambient is decreased to 50,000 lm/m², the background reflected light is reduced to 337 cd/m², filter reflected light to 318 cd/m², and the discrimination index is increased to 2.29.

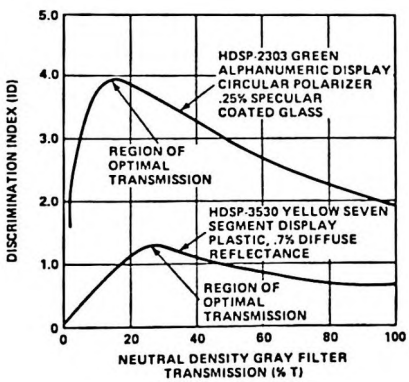


Figure 47. Optimal Neutral Density Gray Filter Transmission.

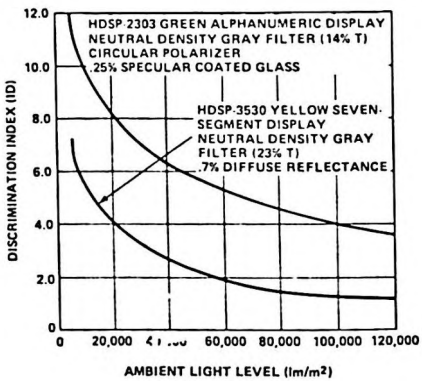


Figure 48. Effect of Reducing Ambient Lighting.

As a second example, in an ambient of 107,000 lm/m², the background reflected light off an alphanumeric display is 207 cd/m², optically coated filter reflected light is 274 cd/m², and the discrimination index is 3.97. If the ambient is decreased to 70,000 lm/m², the background reflected light is reduced to 135 cd/m², filter reflected light to 180 cd/m², and the discrimination index is increased to 4.91.

High Efficiency Red LEDs Product Highest Values of Discrimination Index (see Figure 49).

For high efficiency red, yellow, and green seven segment displays of data sheet typical intensity, all filtered with a 23% transmission neutral density gray filter, discrimination index values are 3.21 for high efficiency red, 1.31 for yellow and 1.10 for green. The difference in discrimination indices is due to differences in chrominance indices. The chrominance index of a high efficiency red display is 3 times greater than the chrominance index of the yellow display. This is shown by referring back to the 1960 CIE chromaticity diagram (see Figure 21). On this diagram, the chromatic distance between the neutral density gray background and a red LED is approximately 3 times as large as the chromatic distance between the neutral density gray background and the yellow LED.

Similarly, for high efficiency red, yellow, and green alphanumeric displays of data sheet typical intensity, all filtered with a 14%T circular polarizing optically coated filter, the discrimination index values are 6.09 for high efficiency red, 2.87 for yellow and 3.97 for green. Again, the high efficiency red display has the greatest chrominance index followed by yellow and green respectively. In this case the discrimination index for the green display is greater than the yellow display due to the higher light output of green LEDs.

.3" SEVEN SEGMENT DISPLAYS

Ambient: 107,000 lm/m²
Filter: Neutral Density Gray Plastic (23%T)
.7% Diffuse Filter Reflectance
Reflectance: Diffuse Only

LED Color	Device Intensity	Background Reflectance	Luminance Index	Chrominance Index	Discrimination Index
High Efficiency Red	6.3 mcd/seg	12%	0.96	3.10	3.21
Yellow	6.3 mcd/seg	12%	0.99	0.85	1.31
Green	4.5 mcd/seg	7%	0.98	0.50	1.10

.20" ALPHANUMERIC DISPLAYS

Ambient: 107,000 lm/m²
Filter: Neutral Density Gray Glass (14%T)
Circular Polarizer, Optically Coated Glass (.25% Specular Reflectance)
Reflectance: Diffuse and Specular at 30°

LED Color	Device Intensity	Luminance Index	Chrominance Index	Discrimination Index
High Efficiency Red	228 µcd/DOT	2.33	5.62	6.09
Yellow	228 µcd/DOT	2.32	1.69	2.87
Green	482 µcd/DOT	3.70	1.44	3.97

Figure 49. Comparison of High Efficiency Red, Yellow, Green LED Displays at Typical Intensity Levels.

SPECIFIC MANUFACTURERS OF NEUTRAL DENSITY PLASTIC AND GLASS FILTERS

Table 7 lists several neutral density filters that can be used with Hewlett-Packard Sunlight Viewable LED Displays. For increased contrast the neutral density filters can be combined with some of the wavelength filters listed in Table 4. For example, an amber filter combined with a neutral density filter can enhance chrominance contrast. In addition, Table 8 lists Hewlett-Packard displays that are specifically designed for Sunlight Ambient Applications.

Table 7. A List of Neutral Density Filters For Use With Sunlight Viewable LED Displays

Filter Product	Manufacturer
H100-1266 Gray H100-1250 Gray H100-1230 Bronze (Plastic)	SGL HOMALITE 11 Brookside Drive Wilmington, DE 19804 (302) 652-3686
Plexiglas® 2074 Gray 2370 Bronze 2538 Gray (Plastic)	Rohm and Haas Independence Mall West Philadelphia, PA 19105 (215) 392-3000
Spectrafilter® Gray 105 (Plastic)	Chequers Engraving, Ltd. 1-4 Christina Street, London EC2A 4PA 01-739-6964/5
Panel Film® Light Control Film® (Louvered) ND0210 50% Gray ND0220 27% Gray (Plastic)	3M-Company Industrial Optics Carbonless, Related Products 225-35 3M Center St. Paul, MN 55144 (612) 733-4403
Chromafilter® Gray 15 Gray 10 (Plastic)	Panelgraphic Corporation 10 Henderson Drive West Caldwell, NJ 07006 (201) 277-1500
Optically Coated Glass HEA® Double Sided Antireflection Coating (Glass)	Optical Coating Laboratories, Inc. 2789 Northpoint Parkway Santa Rosa, CA 95401-7397 (707) 545-6440
Optically Coated Glass With Circular Polarizer HNCP10 Gray (Glass and Plastic) HACP15 Amber/Gray With Circular Polarizer (Plastic)	Polaroid Corporation Technical Polarizer Division 1 Upland Road Norwood, MA 02062 (617) 769-6800
Optically Coated Glass With Circular Polarizer — Made to Customer Specification	Liberty Mirror Division of Libbey-Owens-Ford Company Brackenridge, PA 15014 (412) 224-1800
	Precision Glass Laminations 324 Yolando Santa Rosa, CA 95404 (707) 528-9070
	Marks Polarized 153-16 10th Avenue Whitestone, NY 11357 (212) 767-9600

Table 8. Hewlett-Packard Displays for Sunlight Ambient Applications

Display	Size	Part Number
Seven Segment Displays	0.3 in. 0.3 in. 0.43 in. 0.56 in. 0.80 in.	HDSP-7400,7500,7800 series HDSP-3530,3600,4030 series HDSP-3730,4600,4130 series HDSP-5530,5600,5730 series HDSP-3900,8600,4200 series
Alphanumeric Displays	0.15 in. 0.20 in. 0.27 in.	HDSP-2000 series HDSP-2300 series HDSP-2490 series
Ultra-Bright Lamps	T13/4 T13/4 Lo-Dome T-1	HLMP-3750,3850,3950 HLMP-3390,3490,3590 HLMP-1349,1440,1540

Footnotes and References

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3. Wysecki, Gunter, Stiles, W.S. *Color Science Concepts and* Methods, Quantitative Data and Formulas, 1967. Chpt. 1, pp. 1-43.
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7. Galves, op. cit., p. 5.
8. Judd, D.B. *Estimation of Chromaticity Differences and Nearest Color Temperature on the Standard 1931 (ICI) Colorimetric Coordinate System,* J. Opt. Soc. Am., pp. 421-426 (1936).
9. Hurvich, Leo. *Color Vision,* 1981, p. 292.
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11. *For Color Television Cameras with Three Receptors,* Journal of the SMPTE, Volume 77, February 1968. pp. 108-115.
12. Galves, op. cit., p. 5.
13. Kowalski, P. *Equivalent Luminances of Colors,* Journal of the Optical Society of America, Vol. 59, No. 2, February 1969. p. 129.

APPENDIX A

To calculate contrast ratio of a display the following integrals were used:

$$L_vS = 1/A\int \ell(\lambda)\bar{Y}(\lambda)T_1(\lambda)T_G(\lambda)d\lambda$$

$$L_vOFF = L_vOFF\ Specular + L_vOFF\ Diffuse$$

$$L_vOFF\ Specular = \int |S_B(\lambda)\bar{Y}(\lambda)R_S(\lambda)T_G(\lambda)^2 + S_B(\lambda)\bar{Y}(\lambda)R_{GS}(\lambda)|\ T_1(\lambda)T_2(\lambda)d\lambda$$

$$L_vOFF\ Diffuse = 1/\pi \int |S_B(\lambda)\bar{Y}(\lambda)R_D(\lambda)\ T_G(\lambda)^2 + S_B(\lambda)\bar{Y}(\lambda)\ R_{GD}(\lambda)|T_1(\lambda)^2d\lambda$$

$L_vB = L_vOFF$ for purposes of the program

$$L_vF = L_vFspecular + L_vFdiffuse$$

$$L_vFspecular = \int S_B(\lambda)\bar{Y}(\lambda)R_{FS}(\lambda)d\lambda$$

$$L_vFdiffuse = 1/\pi \int S_B(\lambda)\bar{Y}(\lambda)R_{FD}(\lambda)d\lambda$$

For Seven Segment Displays Only:

L_vOFF specular and $L_vF$specular are ignored

$T_G(\lambda) = T_2(\lambda) = 1$

$R_S(\lambda) = R_{GS}(\lambda) = R_{GD}(\lambda) = R_{FS}(\lambda) = 0$

For Alphanumeric Displays Only:

$T_G(\lambda)$ = Transmission of glass window

$T_2(\lambda)$ = Transmission of filter polarized light

$R_S(\lambda)$ = Specular reflectance of ambient light off element

$R_{GS}(\lambda)$ = Specular reflectance of glass window

$R_{GD}(\lambda)$ = Diffuse reflectance of glass window

$R_{FS}(\lambda)$ = Specular reflectance of filter front surface

For Seven Segment Displays and Alphanumeric Displays:

A = Area of light emitting element

$\ell(\lambda)$ = LED radiometric spectrum

$\bar{Y}(\lambda)$ = 1931 CIE Photopic response curve

$T_1(\lambda)$ = Transmission of filter-unpolarized light

$S_B(\lambda)$ = Spectrum of CIE illuminant B - noon sunlight 4870°K

$R_D(\lambda)$ = Diffuse reflectance of ambient light off element

$R_{FD}(\lambda)$ = Diffuse reflectance of filter front surface

APPENDIX B

To calculate x,y chromaticity coordinates of an illuminated element and the background, the following integrals were used:

$$X_\ell = 1/A \int \frac{K(\lambda)}{\bar{Y}(\lambda)} \bar{X}(\lambda)d\lambda \qquad Y_\ell = L_vS$$

$$X_b = X_{off} = \int \frac{m(\lambda) + n(\lambda)}{\bar{Y}(\lambda)} \bar{X}(\lambda)d\lambda \qquad Y_b = Y_{off} = L_vOFF + L_vF$$

Where $\bar{X}(\lambda)$ = 1931 CIE Tristimulus Weighting Function

$\bar{Y}(\lambda)$ = 1931 CIE Photopic Response Curve

$K(\lambda) = \ell(\lambda)\bar{Y}(\lambda)T_1(\lambda)T_G(\lambda)$

$m(\lambda) = |S_B(\lambda)\bar{Y}(\lambda)R_S(\lambda)T_G(\lambda)^2 + S_B(\lambda)\bar{Y}(\lambda)R_{GS}(\lambda)|\ T_1(\lambda)T_2(\lambda) + 1/\pi\ |S_B(\lambda)\bar{Y}(\lambda)R_D(\lambda)T_G(\lambda)^2 + S_B(\lambda)\bar{Y}(\lambda)R_{GD}(\lambda)|T_1(\lambda)^2$

$n(\lambda) = S_B(\lambda)\bar{Y}(\lambda)[R_{FS}(\lambda) + 1/\pi\ R_{FD}(\lambda)]$

Chromaticity Coordinates

$$x_\ell = \frac{X_\ell}{X_\ell + Y_\ell} \qquad y_\ell = \frac{Y_\ell}{X_\ell + Y_\ell}$$

$$x_b = x_{off} = \frac{X_b}{X_b + Y_b} \qquad y_b = y_{off} = \frac{Y_b}{X_b + Y_b}$$

Finally, x, y chromaticity coordinates are translated to 1960 CIE (U,V) coordinate system

$$u = \frac{4x}{(12y - 2x + 3)} \qquad v = \frac{6y}{(12y - 2x + 3)}$$

APPLICATIONS

HEWLETT PACKARD

APPLICATION NOTE 1016

Using the HDSP-2000 Alphanumeric Display Family

INTRODUCTION

First introduced in 1975, the HDSP-2000 alphanumeric display has been designed into a variety of applications. The HDSP-2000 display was originally designed for commercial, industrial, instrumentation, and business equipment applications. However, the introduction of high efficiency red, yellow, and high performance green devices as well as several display sizes has opened up a multitude of new applications for the HDSP-2000 alphanumeric display family. The high efficiency red, yellow, and high performance green devices use gallium phosphide (GaP) LEDs. The GaP displays are readable in direct sunlight with proper contrast enhancement techniques. For this reason, the HDSP-2000 family displays have been designed into a variety of avionic and process control applications. The HDSP-2000 family displays are available in three character sizes of 3.8mm (0.15"), 4.9mm (0.19"), and 6.9mm (0.27") to allow the designer to optimize display compactness versus long distance readability. Versions of the HDSP-2000 family alphanumeric displays are available with a true hermetic package and an operating temperature range of -55° C to +85° C to allow designers to utilize the proven reliability of LED display technology in military and aerospace applications.

This note is intended to serve as a design and application guide for users of the HDSP-2000 family of alphanumeric display devices. The information presented will cover: the theory of the device design and operation; considerations for specific circuit designs; thermal management, power derating and heat sinking; intensity modulation techniques.

The HDSP-2000 family has been designed to provide a high resolution information display subsystem. Each character of the 4 character package consists of a 5x7 array of LEDs which can display a full range of alphabetic and numeric characters plus punctuation, mathematical and other special symbols. The HDSP-2000 family is available in four colors: red, high efficiency red, yellow, and high performance green.

The character height, character spacing, color and part number of each member of the HDSP-2000 family of displays is shown in Table 1. The overall package size is designed to allow end stacking of multiple clusters to form character strings of any desired length.

ELECTRICAL DESCRIPTION

The on-board electronics of the HDSP-2000 display family eliminates some of the classical difficulties associated with the use of alphanumeric displays. Traditionally, single digit LED dot matrix displays have been organized in an x-y addressable array requiring 12 interconnect pins per digit plus extensive row and column drive support electronics. All members of the HDSP-2000 display family provide on-board storage of decoded row data plus constant current sinking row drivers for each of the 28 rows in the 4 character display. This approach allows the user to address each display package through just 11 active interconnections vs. the 176 interconnections and 36 components required to effect a similar function using conventional LED matrices.

Figure 1 is a block diagram of the internal circuitry of the HDSP-2000 display. The device consists of four LED matrices and two 14-bit serial-in-parallel-out shift registers. The LED matrix for each character is a 5x7 diode array organized with the anodes of each column tied in common and the cathodes of each row tied in common. The 7 row cathode commons of each character are tied to the constant current sinking outputs of 7 successive stages of the shift register. The like columns of the 4 characters are tied together and brought to a single address pin (i.e., column 1 of all 4 characters is tied to pin 1, etc.). In this way, any diode in the four 5x7 matrices may be addressed by shifting data to the appropriate shift register location and applying a voltage to the appropriate column.

The serial-in-parallel-out (SIPO) shift register has a constant current sinking output associated with each shift register stage. This constant current output drives each LED at a nominal peak current of 12 to 14 mA peak. The output stage is a current mirror design with a nominal current gain of 10. A logical 1 loaded into each shift register bit will turn "ON" the corresponding current source provided that a logical 1 is applied to the Blanking Input, V_B. If V_{COL} is applied to the appropriate Column Input, the corresponding LED diode will be turned "ON". Since the row drivers have a constant current output, the LED current will remain constant as long as the Column Input voltage exceeds 2.4V for red and 2.75V for high efficiency red, yellow, and high performance green devices.

Table 1. The HDSP-2000 Alphanumeric Display Family

Device	Color	Character Height	Character Spacing	Operating Temperature
HDSP-2000	Red	3.8 mm (0.15 in.)	4.5 mm (0.175 in.)	-20°C to +85°C
HDSP-2001	Yellow	3.8 mm (0.15 in.)	4.5 mm (0.175 in.)	-20°C to +85°C
HDSP-2002	High Efficiency Red	3.8 mm (0.15 in.)	4.5 mm (0.175 in.)	-20°C to +85°C
HDSP-2003	High Performance Green	3.8 mm (0.15 in.)	4.5 mm (0.175 in.)	-20°C to +85°C
HDSP-2300	Red	4.9 mm (0.192 in.)	5.0 mm (0.197 in.)	-20°C to +85°C
HDSP-2301	Yellow	4.9 mm (0.192 in.)	5.0 mm (0.197 in.)	-20°C to +85°C
HDSP-2302	High Efficiency Red	4.9 mm (0.192 in.)	5.0 mm (0.197 in.)	-20°C to +85°C
HDSP-2301	High Performance Green	4.9 mm (0.192 in.)	5.0 mm (0.197 in.)	-20°C to +85°C
HDSP-2490	Red	6.9 mm (0.27 in.)	8.9 mm (0.35 in.)	-20°C to +85°C
HDSP-2491	Yellow	6.9 mm (0.27 in.)	8.9 mm (0.35 in.)	-20°C to +85°C
HDSP-2492	High Efficiency Red	6.9 mm (0.27 in.)	8.9 mm (0.35 in.)	-20°C to +85°C
HDSP-2493	High Performance Green	6.9 mm (0.27 in.)	8.9 mm (0.35 in.)	-20°C to +85°C
HDSP-2010	Red	3.8 mm (0.15 in.)	4.5 mm (0.175 in.)	-40°C to +85°C
HDSP-2310	Red	4.9 mm (0.192 in.)	5.0 mm (0.197 in.)	-55°C to +85°C
HDSP-2311	Yellow	4.9 mm (0.192 in.)	5.0 mm (0.197 in.)	-55°C to +85°C
HDSP-2312	High Efficiency Red	4.9 mm (0.192 in.)	5.0 mm (0.197 in.)	-55°C to +85°C
HDSP-2450	Red	6.9 mm (0.27 in.)	8.9 mm (0.35 in.)	-55°C to +85°C
HDSP-2451	Yellow	6.9 mm (0.27 in.)	8.9 mm (0.35 in.)	-55°C to +85°C
HDSP-2452	High Efficiency Red	6.9 mm (0.27 in.)	8.9 mm (0.35 in.)	-55°C to +85°C

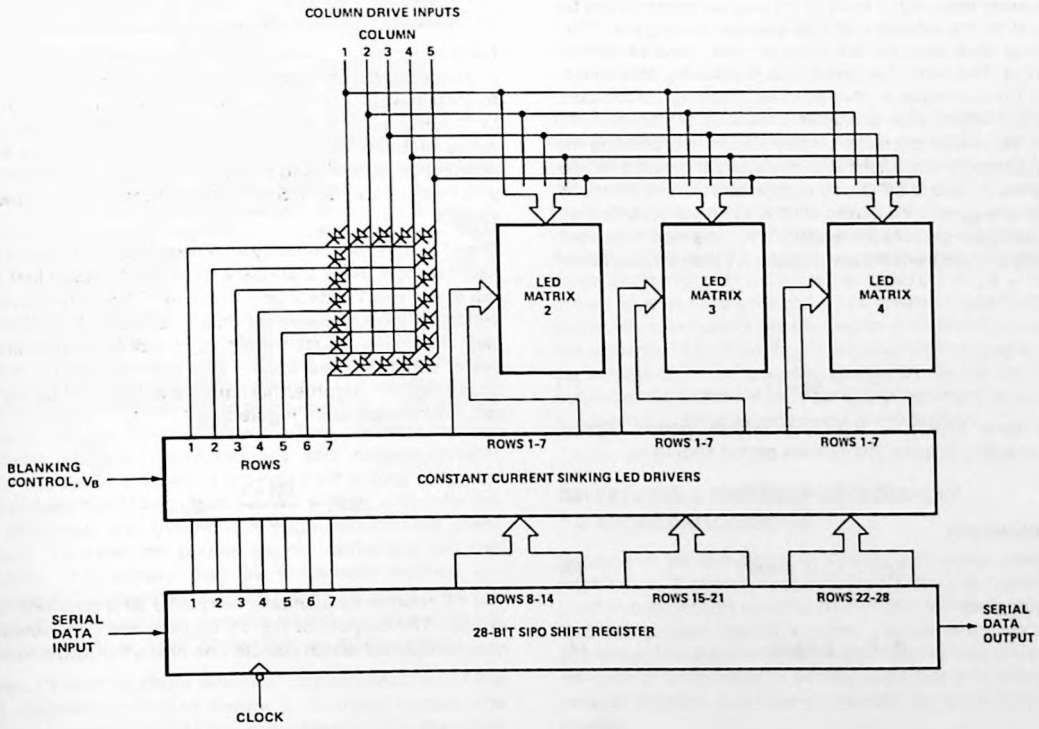


Figure 1. Block Diagram

APPLICATIONS

Data is loaded serially into the shift register on the high to low transition of the Clock Input. During the time that data is being loaded into the display, the column current must be disabled to minimize the generation of "current spikes" between V_{CC}, the columns, and ground. The resulting power supply noise could induce noise on the Clock and Data Inputs. The column current can be disabled either by switching off the column drivers or by applying a logical 0 to the Blanking Input.

The Data Output terminal is a TTL buffer interface to the 28th bit of the shift register (i.e., the 7th row of character 4 in each package). The Data Output is arranged to directly interconnect to the Data Input on a succeeding 4 digit HDSP-2000 display package. The Data, Clock and V_B inputs are all buffered to allow direct interface to any TTL logic family.

THEORY OF OPERATION

Dot matrix alphanumeric display systems generally have a logical organization which prescribes that any character be generated as a combination of several subsets of data. In a 5x7 matrix, this could be either 5 subsets of 7 bits each or 7 subsets of 5 bits each. This technique is utilized to reduce from 35 to 5 or 7 the number of outputs required from the character generator. In order to display a complete character, these subsets of data are then presented sequentially to the appropriate locations of the display matrix. If this process is repeated at a rate which insures that each of the appropriate matrix locations is re-energized a minimum of 100 times per second, the eye will perceive a continuous image of the entire character. The apparent intensity of each of the display elements will be equal to the intensity of that element during the "ON" period multiplied by the ratio of "ON" time to refresh period. This ratio is referred to as the display duty factor, and the technique is referred to as "strobing". In the case of HDSP-2000, each character is made up of 5 subsets of 7 bits. For a four character display, 28 bits representing the first subset of each of the four characters are loaded serially into the on-board SIPO shift register and the first column is then energized for a period of time, T. This process is then repeated for columns 2 through 5. If the time required to load the 28 bits into the SIPO shift register is t, then the duty factor is:

$$D.F. = \frac{T}{5(t+T)} \; ; \qquad (1)$$

the term 5(t+T) is then the refresh period. For a satisfactory display, the refresh period should be:

$$1/[5(t+T)] \geq 100 \text{ Hz} \qquad (2)$$

or conversely

$$5(t+T) \leq 10 \text{ msec}, \qquad (3)$$

which gives

$$(t+T) \leq 2 \text{ msec}. \qquad (4)$$

The time averaged luminous intensity of the display can be varied continuously over a range greater than 1000 to 1 by turning off or blanking the display before loading new data into the SIPO shift register. If the time that the display is blanked is T_B, then the duty factor of the display becomes:

$$D.F. = \frac{T}{5(t+T+T_B)} \qquad (5)$$

where

$$(t + T + T_B) \leq 2 \text{ msec}.$$

DRIVE CIRCUIT CONCEPTS

A practical display system utilizing the HDSP-2000 family of displays requires interfacing with a character generator, refresh memory and some timing circuitry. A block diagram of such a display system is depicted in Figure 2. This circuit provides for ASCII data storage and decoding and properly refreshes the display at a 100 Hz refresh rate. In this figure, the display length is shown as N characters with the leftmost display character labeled as character 1 and the right most character of the display labeled as character N. The refreshing of the display is accomplished by a series of counters.

The ÷N counter sequentially accesses N coded information symbols from the Nx7 RAM. Note that for the normal configuration of the HDSP-2000 displays, character 1 is the leftmost character, character 4 is the rightmost character and shift register cascades from left to right. Thus, the symbol corresponding to character N is decoded first, then the symbol corresponding to character (N-1), and the symbol corresponding to character 1 is decoded last.

Each coded information symbol is read from the Nx7 RAM and decoded by a 5x7 decoder. The decoder can be selected to decode ASCII, EBDIC, or any customized character font. In this example, the ASCII decoder is organized as 128x7 words of 5 bits each. The ASCII symbol and row select information is applied to the decoder and the decoder outputs information for all 5 columns for the selected row and symbol.

The ÷7 counter sequentially accesses all seven rows of each ASCII symbol. Note that row 7 must be decoded first, then row 6, and row 1 is decoded last. The ÷M counter is used to periodically load new serial data into the HDSP-2000 display. During one count, the display clock is enabled and 7N bits of serial data are loaded into the display. During the remaining (M-1) counts, this data is displayed. Thus the duty factor for the circuit in Figure 2 is:

$$D.F. = \frac{(M-1)}{5M} = .20\,(1 - M^{-1}) \qquad (6)$$

The ÷5 counter sequentially refreshes all 5 columns of the display. The outputs of the ÷5 counter are connected to a data multiplexer which selects one of the 5 outputs from the

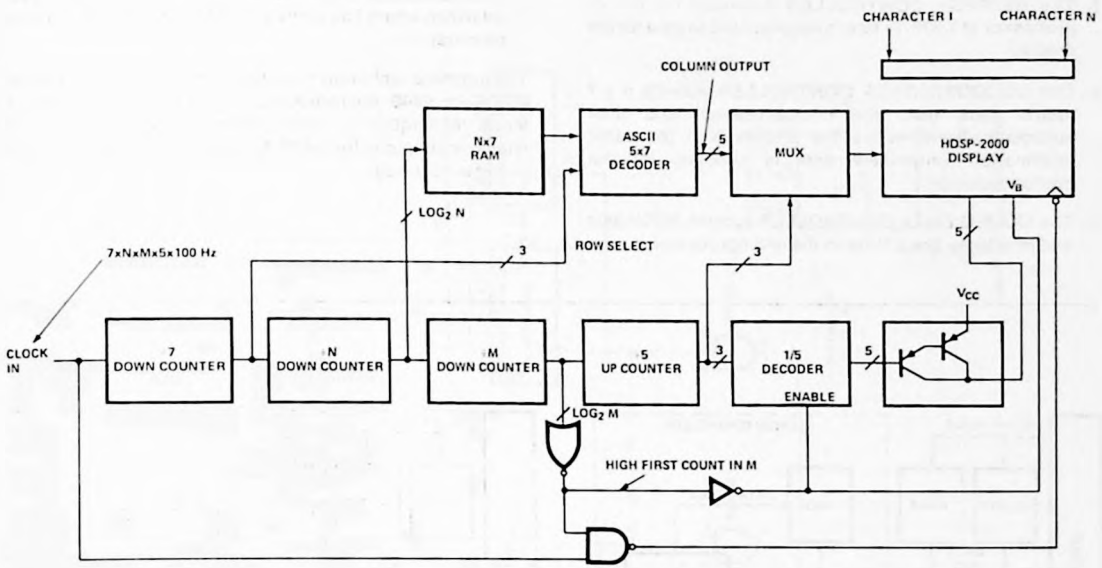


Figure 2. CKT Block Diagram

ASCII decoder and loads it into the Data Input of the HDSP-2000 display string. The ÷5 counter also enables one of the 5 column driver transistors. Note that the display is blanked via the V_B input and also that the column driver transistors are turned off during the time that new data is being loaded into the HDSP-2000 display string. This will eliminate any high current transients between the column inputs and ground during the data shifting operation.

Since data is loaded for all of the like columns in the display string and these columns are then enabled simultaneously, only five column switch transistors are required regardless of the number of characters in the string. The column switch transistors should be selected to handle 105 to 130 mA per character in the display string. The collector emitter saturation voltage characteristics and column voltage supply should be chosen to provide $2.4V \leq V_{COL} \leq V_{CC}$ for the standard red displays and $2.75V \leq V_{COL} \leq V_{CC}$ for the high efficiency red, yellow, and high performance green displays. To save on power supply costs and improve efficiency, this supply may be a fullwave rectified unregulated DC voltage as long as the PEAK value does not exceed the value of V_{CC} and the minimum value does not drop below 2.4V or 2.75V depending on display color.

Figures 13 and 16 show practical implementations of the block diagram shown in Figure 2. In those circuits, the display is mounted upside down, so that pin 1 is in the upper right hand corner. With this technique, data is loaded into display character N and data shifts from right to left as new data is loaded. The first bit loaded into the display would be row 1, character 1, then row 2, etc., and the last bit loaded would be row 7 of character N. This allows the ÷7, ÷N and ÷M counters to be implemented as up counters instead of down counters. Since the display is upside down, column 5 of the display appears to be column 1 and column 4 of the display appears to be column 2. Thus, column 1 data for the display must be loaded into the display and column 5 must subsequently be enabled. This is accomplished by reversing the outputs of the 5x7 decoder. The D_0, D_1, D_2, D_3, and D_4 outputs of the MCM6674 decoder output column 5, column 4, column 3, column 2, and column 1 information.

INTERFACING THE HDSP-2000 DISPLAY TO MICROPROCESSORS

Because of the complexity of dealing with alphanumeric information, a microprocessor based system is typically used in conjunction with the HDSP-2000 family displays. Depending upon overall systems configuration, microprocessor time available to dedicate to display support, and the type of information to be displayed, one may choose several different partitioning schemes to drive such a display.

Figure 3 shows four different techniques to interface the HDSP-200 family displays to microprocessor systems:

1. The REFRESH CONTROLLER interrupts the microprocessor at a 500 Hz rate to request refresh data for the display.
2. The DECODED DATA CONTROLLER accepts 5 x 7 matrix data from the microprocessor and then automatically refreshes the display with the same information until new data is supplied by the microprocessor.
3. The CODED DATA CONTROLLER accepts ASCII data and interfaces like a RAM to the microprocessor.
4. The DISPLAY PROCESSOR CONTROLLER (HDSP-247X series) employs a dedicated single chip microprocessor as a data display/control/keyboard interface which has many of the features of a complete terminal.

The interface techniques depicted are specifically for the 8080A or 6800 microprocessor families. Extension of these techniques to other processors should be a relatively simple software chore with little or no hardware changes required.

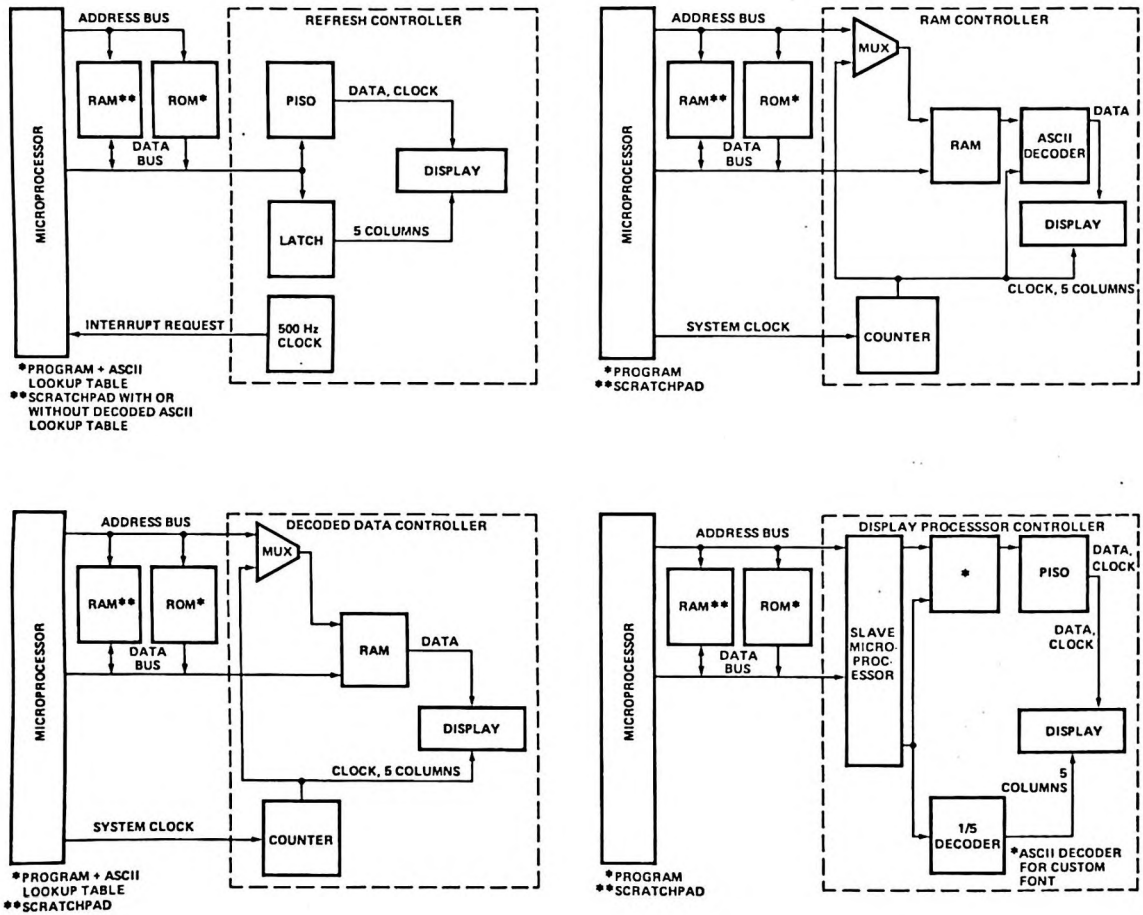


Figure 3. Four Different Techniques to Interface the HDSP-2000 Alphanumeric Display to a Microprocessor System

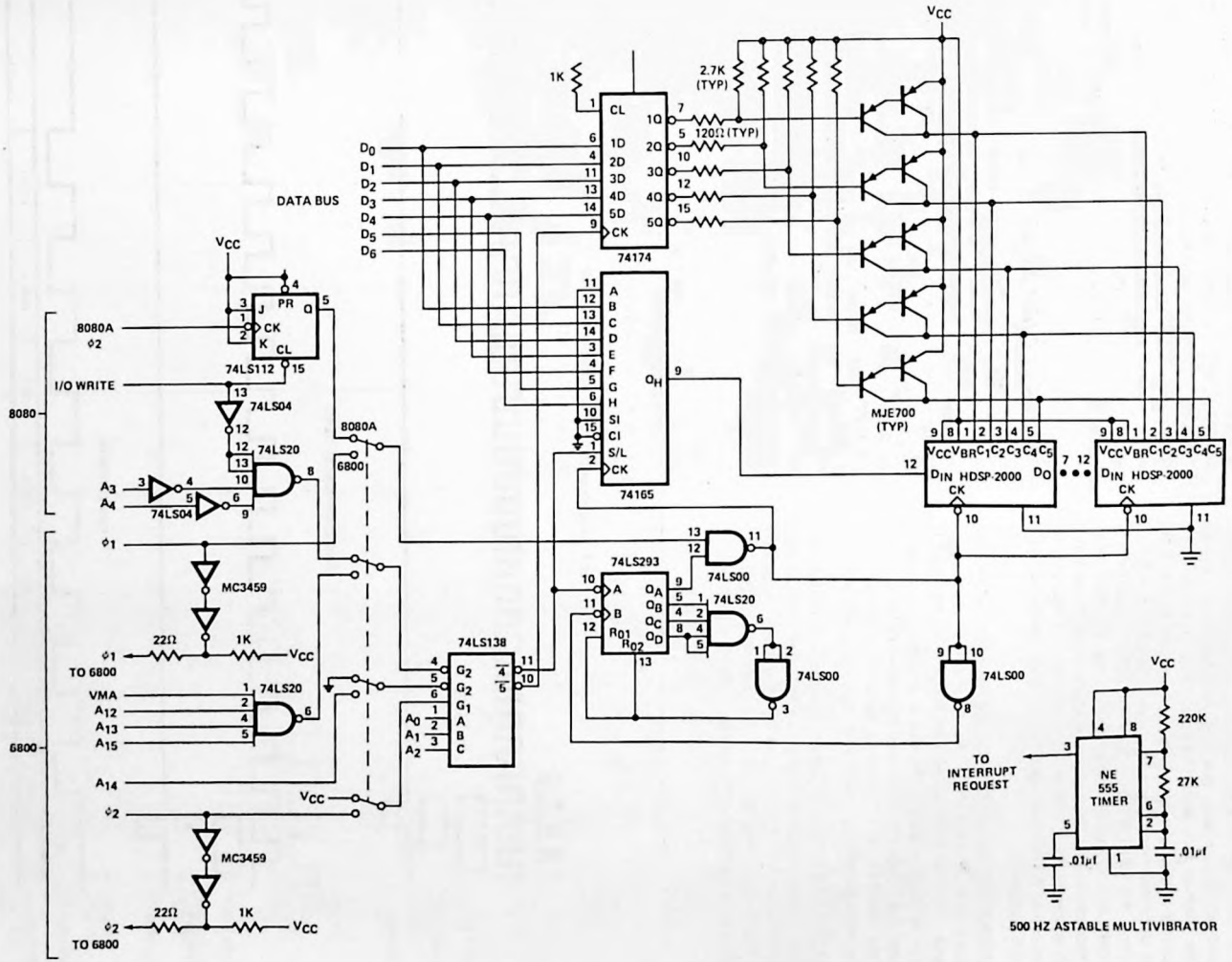


Figure 4. 6800 or 8080A Microprocessor Interface to the HDSP-2000 REFRESH CONTROLLER

The choice of a particular interface is an important consideration because it affects the design of the entire microprocessor system. The REFRESH CONTROLLER provides the lowest cost interface because it uses the microprocessor to provide ASCII decoding and display strobing. Because the ASCII decoder is located within the microprocessor system, the designer has total control over the display font within the program. This feature is particularly important when the system will be used to display different languages and special graphic symbols. However, the REFRESH CONTROLLER requires a significant amount of microprocessor time. Furthermore, while the interrupt allows the refresh program to operate asynchronously from the main program, this technique limits some of the software techniques that can be used in the main program.

The DECODED DATA CONTROLLER requires microprocessor interaction only when the display message is changed. Like the REFRESH CONTROLLER, the ASCII decoder is located within the microprocessor program. However, the time required to decode the ASCII string and store the resulting 5 x 7 display data into the interface requires several milliseconds of microprocessor time.

The CODED DATA CONTROLLER also requires interaction from the microprocessor system only when the display message is changed. Because the ASCII decoder is located within the display interface, the microprocessor requires much less time to load a new message into the display.

The DISPLAY PROCESSOR CONTROLLER, the HDSP-247X series, is the most powerful interface. The software within the DISPLAY PROCESSOR CONTROLLER further reduces the host microprocessor interaction by providing more powerful left and right data entry modes compared to the RAM entry mode of the DECODED DATA and CODED DATA CONTROLLERS. The DISPLAY PROCESSOR CONTROLLER can also provide features such as a Blinking Cursor, Editing Commands, and a Data Out function. One version of the DISPLAY PROCESSOR CONTROLLER allows the user to provide a custom ASCII decoder for applications needing a special character font.

REFRESH CONTROLLER

The REFRESH CONTROLLER circuit depicted in Figure 4 operates by interrupting the microprocessor every two milliseconds to request a new block of display data and column select data. Display data is loaded from the data bus into the serial input of the HDSP-2000 via a 74165 parallel in, serial out shift register. The 74LS293 counter and associated gates insure that only seven clock pulses are delivered to the shift register and the HDSP-2000 for each word loaded. Column Select data is loaded into a 74174 latch which, in turn, drives the column switch transistors. The circuit timing relative to the microprocessor clock and I/O is depicted in Figure 5.

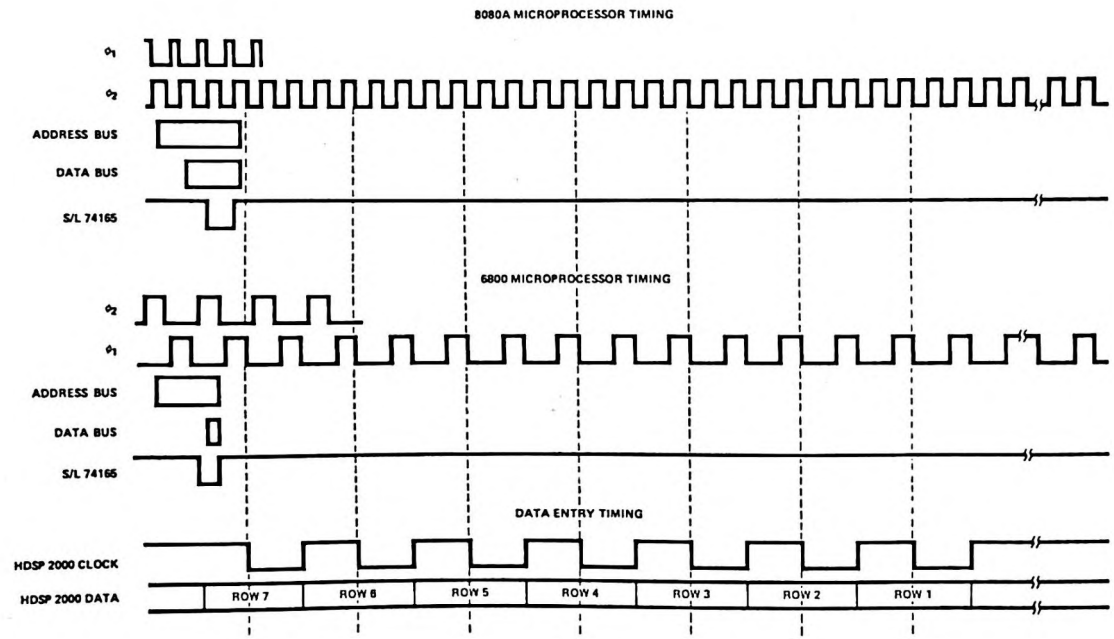


Figure 5. REFRESH CONTROLLER Timing

The 6800 software necessary to support this interface is divided into two separate subroutines, "RFRSH" and "LOAD" (Figure 6). This approach is desirable to minimize microprocessor involvement during display refresh. The subroutine "RFRSH" loads a new set of decoded display data from the microprocessor scratchpad memory into the interface at each interrupt request. The subroutine "LOAD" is utilized to decode a string of 32 ASCII characters into 5 x 7 formatted display data and store this data in the scratchpad memory used by "RFRSH".

Figures 7 and 8 depict two different software routines for interfacing the REFRESH CONTROLLER to an 8080A microprocessor. The two subroutines shown in Figure 7 are functional replacements for the 6800 program shown in Figure 6. The programs shown in Figures 6 and 7 require a 5N byte scratchpad memory where N is the display length. The routine in Figure 8 eliminates this scratchpad memory by decoding and loading data each time a new interrupt request is received.

Because the microprocessor system is interrupted every 2ms, proper software design is especially important for the REFRESH CONTROLLER. The use of the scratchpad memory significantly reduces the time required to refresh the display. The fastest program, shown in Figure 6, uses in-line code to access data from the buffer and output it to the display. This program requires 3.7% + .50N% of the available microprocessor time for a 1MHz clock. The program shown in Figure 7 is similar to the one shown in Figure 6, except that it uses a program loop instead of the in-line code. This program uses 5.4% + .93N% of the microprocessor time for a 2MHz clock. These programs utilize a subroutine "LOAD" which is called whenever the display message is changed. This subroutine executes in 10.2ms and 7.5ms respectively for Figure 6 and Figure 7. The program in Figure 8 uses 7.6% + 1.35N% of the microprocessor time for a 2MHz clock. A 50% reduction in the previously described microprocessor times can be achieved by using faster versions of the 6800 and 8080A microprocessors.

```
      OBJECT
LOC   CODE     SOURCE STATEMENTS
                       .
                       .
       BF 05   CDVR    EQU    $BF05
       BF 04   RDVR    EQU    $BF04
       06 00   DECDR   EQU    $0600
0000           POINT   RMB    2
0002           COLMN   RMB    1
0003           COUNT   RMB    2

0005 00 AD     ASCII   FDB    DATA
0007           DISPNT  RMB    2
0009           DCRPNT  RMB    2
000B           COLCNT  RMB    1
000C           DIGCNT  RMB    1

000D           BUFFR   RMB    160
00AD           DATA    RMB    32

0400                   ORG    $0400
0400 86 FF     RFRSH   LDA A  I, $FF
0402 B7 BF 05          STA A  E, CDVR
0405 DE 00             LDX    D, POINT
0407 A6 00     LOOPHH  LDA A  X, 0
0409 B7 BF 04          STA A  E, RDVR
040C A6 01             LDA A  X, 1
040E B7 BF 04          STA A  E, RDVR
                       .
                       .
                       .
04A2 A6 1F             LDA A  X, 31
04A4 B7 BF 04          STA A  E, RDVR
04A7 96 02             LDA A  D, COLMN
04A9 B7 BF 05          STA A  E, CDVR
04AC 81 EF             CMP A  I, $EF
04AE 27 10             BEQ    LOOPB
04B0 D6 00             LDA B  D, POINT +1
04B2 CB 20             ADD B  I, 32
04B4 D7 00             STA B  D, POINT +1
04B6 24 03             BCC    LOOPA
04B8 7C 00 00          INC    E, POINT
04BB 0D        LOOPA   SEC
04BC 79 00 02          ROL    E, COLMN
04BF 3B                RTI
04C0 CE 00 0D  LOOPB   LDX    I, BUFFR
04C3 DF 00             STX    D, POINT
04C5 DE 03             LDX    D, COUNT
04C7 09                DEX
04C8 DF 03             STX    D, COUNT
04CA 86 FE             LDA A  I, $FE
04CC 97 02             STA A  D, COLMN
04CE 3B                RTI

04CF 5F        LOAD    CLR B
04D0 CE 00 0D          LDX    I, BUFFR
04D3 DF 07             STX    D, DISPNT
04D5 86 06             LDA A  I, <DECDR
04D7 97 09             STA A  D, DCRPNT
04D9 86 05             LDA A  I, 5
04DB 97 0B             STA A  D, COLCNT
04DD 86 20     LOOP1   LDA A  I, 32
04DF 97 0C             STA A  D, DIGCNT
04E1 9B 06             ADD A  D, ASCII+1
04E3 24 03             BCC    LOOP2
04E5 7C 00 05          INC    E, ASCII
04E8 97 06     LOOP2   STA A  D, ASCII+1
04EA DE 05     LOOP3   LDX    D, ASCII
04EC 09                DEX
04ED A6 00             LDA A  X, 0
04EF DF 05             STX    D, ASCII
04F1 1B                ABA
04F2 97 0A             STA A  D, DCRPNT+1
04F4 DE 09             LDX    D, DCRPNT
04F6 A6 00             LDA A  X, 0
04F8 DE 07             LDX    D, DISPNT
04FA A7 00             STA A  X, 0
04FC 08                INX
04FD DF 07             STX    D, DISPNT
04FF 7A 00 0C          DEC    E, DIGCNT
0502 26 E6             BNE    LOOP3
0504 CB 80             ADD B  I, $80
0506 24 03             BCC    LOOP4
0508 7C 00 09          INC    E, DCRPNT
050B 7A 00 0B  LOOP4   DEC    E, COLCNT
050E 26 CD             BNE    LOOP1
0510 39                RTS
```

Figure 6. 6800 Microprocessor Program Utilizing a 160 Byte RAM Buffer that Interfaces to the REFRESH CONTROLLER

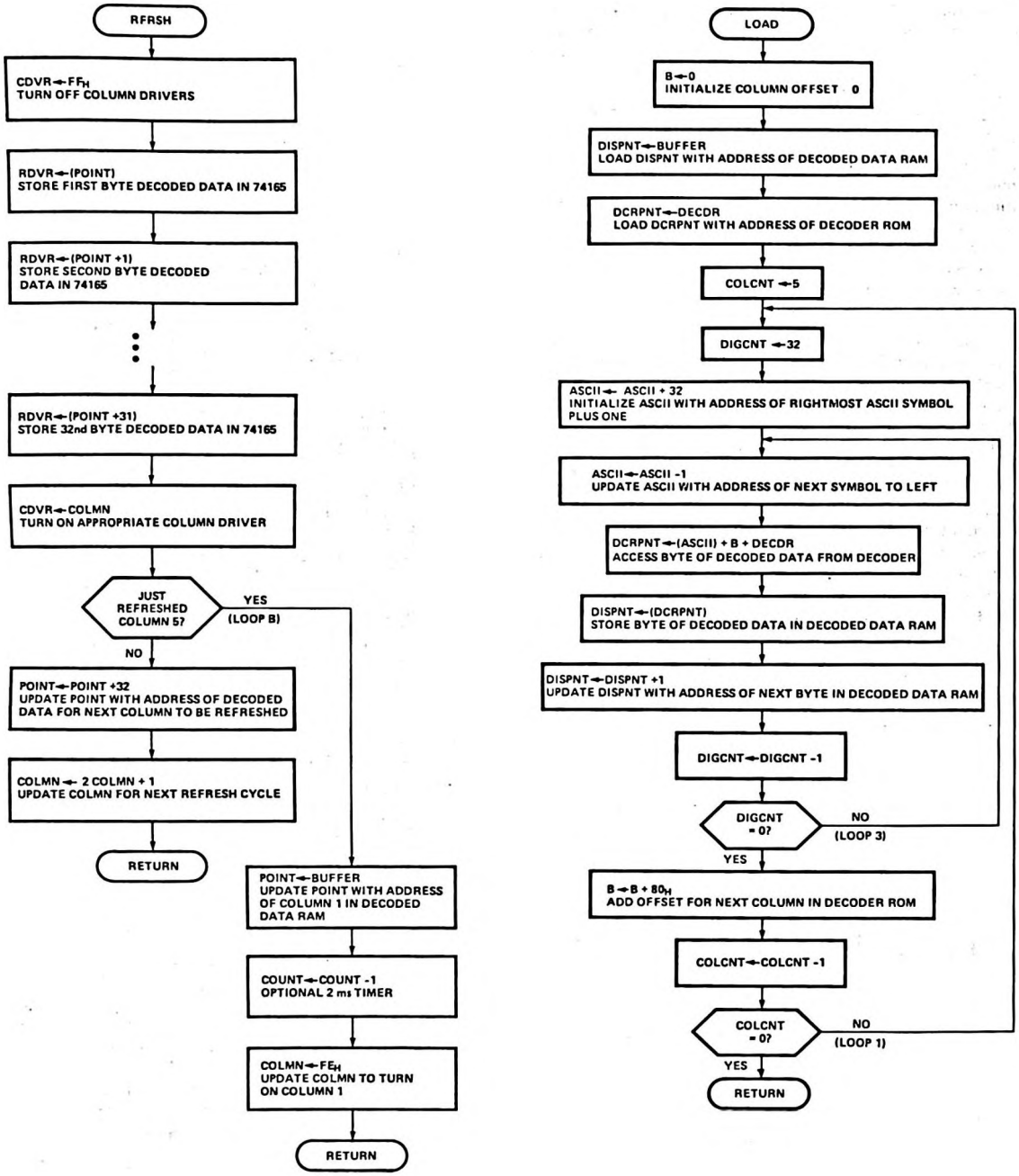


Figure 6. 6800 Microprocessor Program Utilizing a 160 Byte RAM Buffer that Interfaces to the REFRESH CONTROLLER (cont.)

The ASCII to 5 x 7 dot matrix decoder used by the programs in Figures 6, 7, and 8 is located within the microprocessor program. This decoder requires 640 bytes of storage to decode the 128 character ASCII set. The decoder used by these controllers is formatted so that the first 128 bytes contain column 1 information; the next 128 bytes contain column 2 information, etc. Each byte of this decoder is formatted such that D_6 through D_0 contain Row 7 through Row 1 display data respectively. The data is coded so that a HIGH bit will turn the corresponding 5 x 7 display dot ON. This decoder table is shown in Figure 9. The resulting 5 x 7 dot matrix display font is shown in the HDSP-2471 data sheet.

DECODED DATA CONTROLLER

The DECODED DATA CONTROLLER circuit schematic for a 32 character display is depicted in Figure 10. The circuit is specifically designed for interface to an 8080A microprocessor. This circuit is designed to accept and store in local memory all of the display data for a 32 character HDSP-2000 display (1120 bits). The microprocessor loads 160 bytes of display data into the two 1K x 1 RAM's via the 74165 parallel in, serial out shift register. Each byte of data represents one column of display data. The counter string automatically generates the proper address location for each serial bit of data after initialization by $\overline{\text{MEM W}}$, the character address, and the desired column. Once the loading is complete, the counter sequentially loads and displays each column (224 bits) of data at a 90Hz rate (2MHz input clock rate). The timing for this circuit is shown in Figure 11. The software required to decode a 32 character ASCII string is shown in Figure 12. This program decodes the 32 ASCII characters into 160 bytes of display data which are then stored in the controller. The program requires about 6.6ms, for a 2MHz clock, to decode and load the message into the DECODED DATA CONTROLLER. This program also uses the same decoder table as shown in Figure 9.

```
LOC   OBJECT CODE     SOURCE STATEMENTS

0004                  RDVR    EQU     0004H
0005                  CDVR    EQU     0005H
E500                  DECDR   EQU     0E500H

                      ORG     0E000H
E000  05 E0           POINT   DW      BUFFR
E002  FE              COLMN   DB      0FEH
E003  FF FF           COUNT   DW      0FFFFH
E005  00              BUFFR   DS      160

                      ORG     0E0A5H
E0A5  A7 E0           ASCII   DW      DATA
E0A7  00              DATA    DS      32

                      ORG     0E400H
E400  F5              RFRSH   PUSH    PSW
E401  C5                      PUSH    B
E402  E5                      PUSH    H
E403  2A 00 E0                LHLD    POINT
E406  06 20                   MVI     B, 32
E408  3E FF                   MVI     A, 0FFH
E40A  D3 05                   OUT     CDVR
F40C  7E              LOOP    MOV     A, M
E40D  D3 04                   OUT     RDVR
E40F  23                      INX     H
E410  05                      DCR     B
E411  C2 0C E4                JNZ     LOOP
E414  3A 02 E0                LDA     COLMN
E417  D3 05                   OUT     CDVR
E419  FE EF                   CPI     0EFH
E41B  CA 28 E4                JZ      FIRST
E41E  22 00 E0                SHLD    POINT
E421  07                      RLC
E422  32 02 E0                STA     COLMN
E425  C3 3A E4                JMP     END
E428  21 05 E0 FIRST          LXI     H, BUFFR
E42B  22 00 E0                SHLD    POINT
E42E  3E FE                   MVI     A, 0FEH
E430  32 02 E0                STA     COLMN
E433  2A 03 E0                LHLD    COUNT
E436  2B                      DCX     H
E437  22 03 E0                SHLD    COUNT
E43A  E1              END     POP     H
E43B  C1                      POP     B
E43C  F1                      POP     PSW
E43D  C9                      RET

E43E  11 24 E0 LOAD           LXI     D, BUFFR+31
E441  0E 20                   MVI     C, 32
E443  2A A5 E0 LOOP1          LHLD    ASCII
E446  7E                      MOV     A, M
E447  23                      INX     H
E448  22 A5 E0                SHLD    ASCII
E44B  26 E5                   MVI     H, DECDR/256
E44D  6F                      MOV     L, A
E44E  06 05                   MVI     B, 5
E450  7E              LOOP2   MOV     A, M
E451  12                      STAX    D
E452  7D                      MOV     A, L
E453  C6 80                   ADI     80H
E455  6F                      MOV     L, A
E456  D2 5A E4                JNC     LOOP3
E459  24                      INR     H
E45A  7B              LOOP3   MOV     A, E
E45B  C6 20                   ADI     32
E45D  5F                      MOV     E, A
E45E  05                      DCR     B
E45F  C2 50 E4                JNZ     LOOP2
E462  7B                      MOV     A, E
E463  C6 5F                   ADI     5FH
E465  5F                      MOV     E, A
E466  0D                      DCR     C
E467  C2 43 E4                JNZ     LOOP1
E46A  C9                      RET
```

Figure 7. 8080A Microprocessor Program Utilizing a 160 Byte RAM Buffer that Interfaces to the REFRESH CONTROLLER

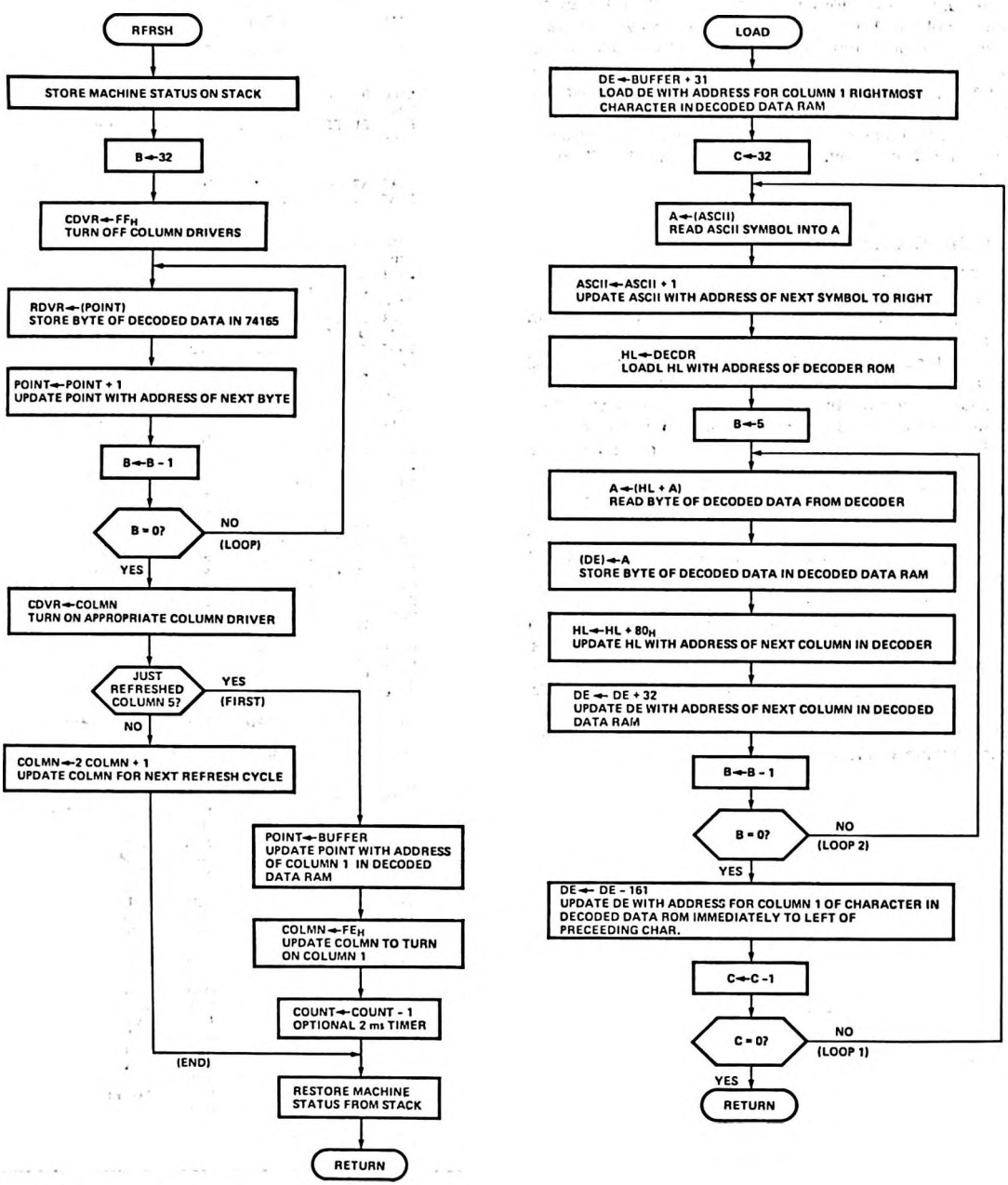


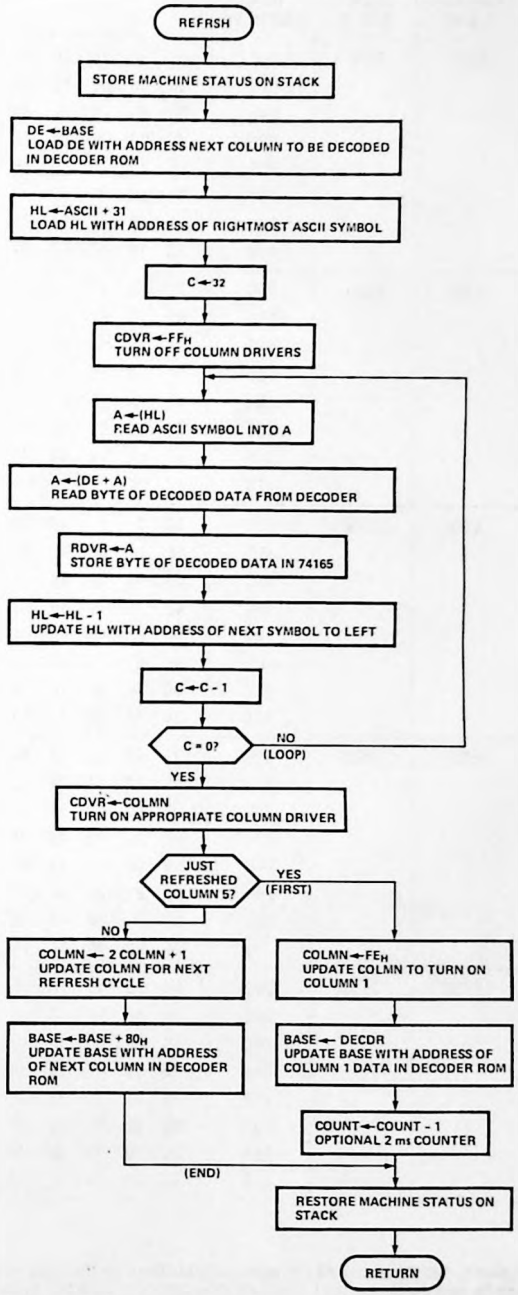
Figure 7. 8080A Microprocessor Program Utilizing a 160 Byte RAM Buffer that Interfaces to the REFRESH CONTROLLER (cont.)

```
LOC   OBJECT CODE    SOURCE STATEMENTS

0004                 RDVR    EQU     0004H
0005                 CDVR    EQU     0005H
E500                 DECDR   EQU     0E500H

                     ORG     0E000H
E000  07  E0         ASCII   DW      DATA
E002  FE             COLMN   DB      0FEH
E003  FF  FF         COUNT   DW      0FFFFH
E005  00  E5         BASE    DW      DECDR
E007  00             DATA    DS      32

                     ORG             0E400H
E400  F5             RFRSH   PUSH    PSW
E401  C5                     PUSH    B
E402  D5                     PUSH    D
E403  E5                     PUSH    H
E404  2A  05  E0             LHLD    BASE
E407  EB                     XCHG
E408  2A  00  E0             LHLD    ASCII
E40B  01  1F  00             LXI     B, 31
E40E  09                     DAD     B
E40F  43                     MOV     B, E
E410  0E  20                 MVI     C, 32
E412  3E  FF                 MVI     A, 0FFH
E414  D3  05                 OUT     CDVR
E416  78             LOOP    MOV     A, B
E417  86                     ADD     M
E418  5F                     MOV     E, A
E419  1A                     LDAX    D
E41A  D3  04                 OUT     RDVR
E41C  2B                     DCX     H
E41D  0D                     DCR     C
E41E  C2  16  E4             JNZ     LOOP
E421  EB                     XCHG
E422  3A  02  E0             LDA     COLMN
E425  D3  05                 OUT     CDVR
E427  FE  EF                 CPI     0EFH
E429  CA  3B  E4             JZ      FIRST
E42C  07                     RLC
E42D  32  02  E0             STA     COLMN
E430  68                     MOV     L, B
E431  01  80  00             LXI     B, 0080H
E434  09                     DAD     B
E435  22  05  E0             SHLD    BASE
E438  C3  4D  E4             JMP     END
E43B  3E  FE         FIRST   MVI     A, 0FEH
E43D  32  02  E0             STA     COLMN
E440  21  00  E5             LXI     H, DECDR
E443  22  05  E0             SHLD    BASE
E446  2A  03  E0             LHLD    COUNT
E449  2B                     DCX     H
E44A  22  03  E0             SHLD    COUNT
E44D  E1             END     POP     H
E44E  D1                     POP     D
E44F  C1                     POP     B
E450  F1                     POP     PSW
E451  C9                     RET
```



APPLICATIONS

Figure 8. 8080A Microprocessor Program that Decodes a 32 Character ASCII String Prior to Loading into the REFRESH CONTROLLER

DECODER ADDRESS FOR FIG. 7, 8, 12	DECODER ADDRESS FOR FIG. 6	HDSP-2471 ROM ADDRESS	HEXIDECIMAL DATA																
E500	0600	080	08	30	45	7D	7D	38	7E	30	60	1E	3E	62	40	08	38	41	$COLUMN_1$
		090	10	18	5E	78	38	78	38	3C	38	3C	38	08	20	12	48	01	
		0A0	00	00	00	14	24	23	36	00	00	00	08	08	00	08	00	20	
		0B0	3E	00	62	22	18	27	3C	01	36	06	00	00	00	14	41	06	
		0C0	3E	7E	7F	3E	7F	7F	7F	3E	7F	00	20	7F	7F	7F	7F	3E	
		0D0	7F	3E	7F	26	01	3F	07	7F	63	03	61	00	02	41	04	40	
		0E0	00	38	7F	38	38	38	08	08	7F	00	20	00	00	78	7C	38	
		0F0	7C	18	00	48	04	3C	1C	3C	44	04	44	00	00	00	08	2A	
E580	0680	100	1C	48	29	09	09	44	01	4A	50	04	49	14	3C	7C	44	63	$COLUMN_2$
		110	08	24	61	14	44	15	45	43	45	41	42	08	7E	19	7E	12	
		120	00	5F	03	7F	2A	13	49	0B	00	41	2A	08	58	08	30	10	
		130	51	42	51	41	14	45	4A	71	49	49	36	5B	08	14	22	01	
		140	41	09	49	41	41	49	09	41	08	41	40	08	40	02	04	41	
		150	09	41	09	49	01	40	18	20	14	04	51	00	04	41	02	40	
		160	07	44	48	44	44	54	7E	14	08	44	40	7F	41	04	08	44	
		170	14	24	7C	54	3E	40	20	40	28	48	64	08	00	41	04	55	
E600	0700	180	3E	45	11	11	05	44	29	4D	48	04	49	08	20	04	44	55	$COLUMN_3$
		190	78	7E	01	15	45	14	44	42	44	40	40	2A	02	15	49	7C	
		1A0	00	00	00	14	7F	08	56	07	3E	3E	1C	3E	38	08	30	08	
		1B0	49	7F	49	49	12	45	49	09	49	49	36	3B	14	14	14	51	
		1C0	5D	09	49	41	41	49	09	41	08	7F	40	14	40	0C	08	41	
		1D0	09	51	19	49	7F	40	60	18	08	78	49	7F	08	7F	7F	40	
		1E0	0B	44	44	44	44	54	09	54	04	7D	44	10	7F	18	04	44	
		1F0	24	14	08	54	44	40	40	30	10	30	54	36	77	36	08	2A	
E680	0780	200	7F	40	29	21	05	38	2E	49	50	38	49	10	20	7C	3C	49	$COLUMN_4$
		210	08	24	61	14	3C	15	3D	43	45	41	42	1C	02	12	41	12	
		220	00	00	03	7F	2A	64	20	00	41	00	2A	08	00	08	00	04	
		230	45	40	49	49	7F	45	49	05	49	29	00	00	22	14	08	09	
		240	55	09	49	41	41	49	09	51	08	41	40	22	40	02	10	41	
		250	09	21	29	49	01	40	18	20	14	04	45	41	10	00	02	40	
		260	00	3C	44	44	48	54	02	54	04	40	3D	28	40	04	04	44	
		270	24	7C	04	54	20	20	20	40	28	08	4C	41	00	08	10	55	
E700	0800	280	00	30	45	7D	79	44	10	30	60	40	3E	60	1C	02	04	41	$COLUMN_5$
		290	04	18	5E	78	40	78	40	3C	38	3C	38	08	02	00	42	01	
		2A0	00	00	00	14	12	62	50	00	00	00	08	08	00	08	00	02	
		2B0	3E	00	46	36	10	39	30	03	36	1E	00	00	41	14	00	06	
		2C0	1E	7E	36	22	3E	41	01	72	7F	00	3F	41	40	7F	7F	3E	
		2D0	06	5E	46	32	01	3F	07	7F	63	03	43	41	20	00	04	40	
		2E0	00	40	38	20	7F	08	00	3C	78	00	00	44	00	78	78	38	
		2F0	18	40	04	20	00	7C	1C	3C	44	04	44	00	00	00	08	2A	

Figure 9. 128 Character ASCII Decoder Table Used by the 6800 Refresh Program in Figure 6. 8080A Refresh Programs in Figures 7, 8, and 12, and the HDSP-2471 DISPLAY PROCESSOR CONTROLLER. Decoded 5x7 Display Font is shown in the HDSP-247X Data Sheet

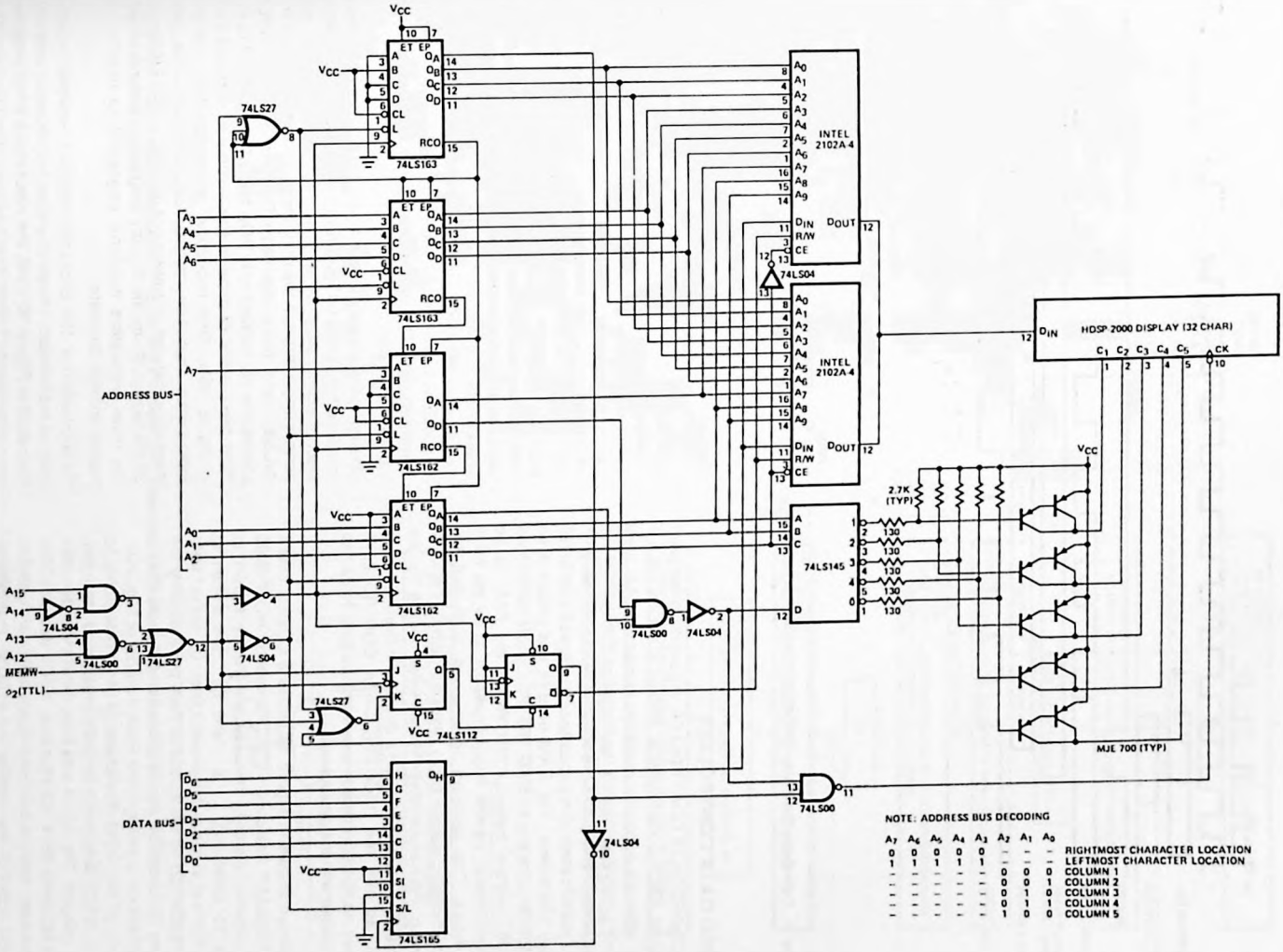


Figure 10. 8080A Microprocessor Interface to the HDSP-2000 DECODED DATA CONTROLLER

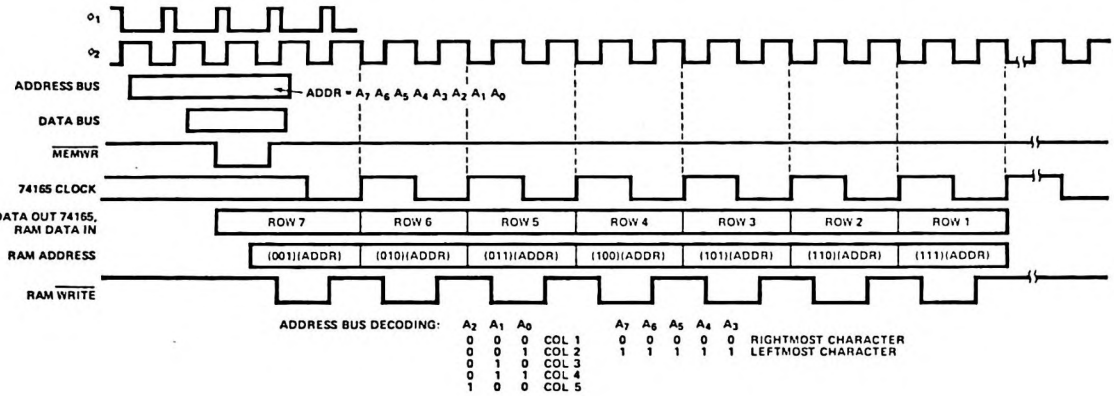


Figure 11. Data Entry Timing for DECODED DATA CONTROLLER

CODED DATA CONTROLLER

The CODED DATA CONTROLLER (Figure 13) is designed to accept ASCII coded data for storage in a local 128 x 8 RAM. After the microprocessor has loaded the RAM, local scanning circuitry controls the decoding of the ASCII, the display data loading, and the column select function. With minor modification, the circuit can be utilized for up to 128 display characters. The RAM used in this circuit is an MCM6810P with the Address and Data inputs isolated via 74LS367 tristate buffers. This allows the RAM to be accessed either by the microprocessor or by the local electronics. The protocol is arranged such that the microprocessor always takes precedence over the local scanning electronics. The "Write" cycle timing for the CODED DATA CONTROLLER is depicted in Figure 14. This circuit, as with the DECODED DATA CONTROLLER, requires no microprocessor time once the local RAM has been loaded with the desired data.

The circuit shown in Figure 13 shows a CODED DATA CONTROLLER designed for a 32 character HDSP-2000 alphanumeric display. The key waveforms shown in Figure 15, labeled ① , ② , and ③ , are shown to simplify the analysis of this circuit. Label ① is the 1 MHz clock. Label ② is the output of 7404 pin 2 which is the inverted Q_D output of the 74197. Label ③ is the output of the 7404 pin 6 which is the ANDed output of $2Q_B$, $2Q_C$, and $2Q_D$ of the 74393. The Motorola 6810 RAM stores 32 bytes of ASCII data which is continuously read, decoded, and displayed. The ASCII data from the RAM is decoded by the Motorola 6674 128 character ASCII decoder. The 6674 decoder has five column outputs which are gated to the Data Input of the display via a 74151 multiplexer. Strobing of the display is accomplished via the 74197, 74393, and 7490 counter string. The 74197 is connected as a divide by 8 counter that sequentially selects the seven rows within the 6674. As shown by waveform ② , the 74197 also enables seven clock cycles to be gated to the clock input of the display. The 74393 is a divide by 256 counter connected so that the five lowest order outputs select each of the 32 ASCII characters within the RAM. The three highest order outputs determine the relationship between load time and column on time. When $2Q_B = 2Q_C = 2Q_D = 1$ of the 74393, waveform ③ goes to a logical 1. The circuit then scans 32 characters from the RAM and serializes the column data by counting through each of the seven rows of the 6674 and gating the appropriate column of the display. During the seven counts when $2Q_B$, $2Q_C$, and $2Q_D$ of the 74393 are not equal to a logical 1, the column data is displayed, as shown in waveform ④ . The duty factor of the display shown in Figure 13 is 17.5%.

Changing the display length to 64 characters is a simple modification. This configuration can be easily realized by disconnecting $2Q_B$ of the 74393 from the 7410 and connecting it through the remaining tri-state buffer on the 74LS367 and using the 6810 RAM to store 64 ASCII characters. By leaving only $2Q_C$ and $2Q_D$ attached to the 7410, the column on time of the display is reduced from 17.5% to 15%. This reduction is caused because the relationship between actual column on time and theoretical column on time is 3/4 as opposed to 7/8 for the 32 characters. Since the display length has been doubled, the drive transistors must be upgraded to handle the higher column currents.

To implement a 128 character display, several modifications are needed. These changes are incorporated into the circuit in Figure 16. First, the input clock frequency has been increased to 2 MHz. This has been done to maintain a refresh rate of approximately 100 Hz for each digit, thus providing a flicker-free display. This higher speed of operation causes propagation delay problems within the

```
LOC   OBJECT CODE     SOURCE STATEMENTS

B000                  DISPL   EQU     0B000H
E500                  DECDR   EQU     0E500H

                      ORG     0E000H
E000  02  E0          ASCII   DW      DATA
E002  00              DATA    DS      32

                      ORG     0E400H
E400  11  F8  B0      LOAD    LXI     D, DISPL+00F8H
E403  0E  20                  MVI     C, 32
E405  2A  00  E0      LOOP1   LHLD    ASCII
E408  7E                      MOV     A, M
E409  23                      INX     H
E40A  22  00  E0              SHLD    ASCII
E40D  26  E5                  MVI     H, DECDR/256
E40F  6F                      MOV     L, A
E410  06  05                  MVI     B, 5
E412  7E              LOOP2   MOV     A, M
E413  12                      STAX    D
E414  13                      INX     D
E415  7D                      MOV     A, L
E416  C6  80                  ADI     80H
E418  6F                      MOV     L, A
E419  D2  1D  E4              JNC     LOOP3
E41C  24                      INR     H
E41D  05              LOOP3   DCR     B
E41E  C2  12  E4              JNZ     LOOP2
E421  7B                      MOV     A, E
E422  D6  0D                  SUI     13
E424  5F                      MOV     E, A
E425  0D                      DCR     C
E426  C2  05  E4              JNZ     LOOP1
E429  C9                      RET
```

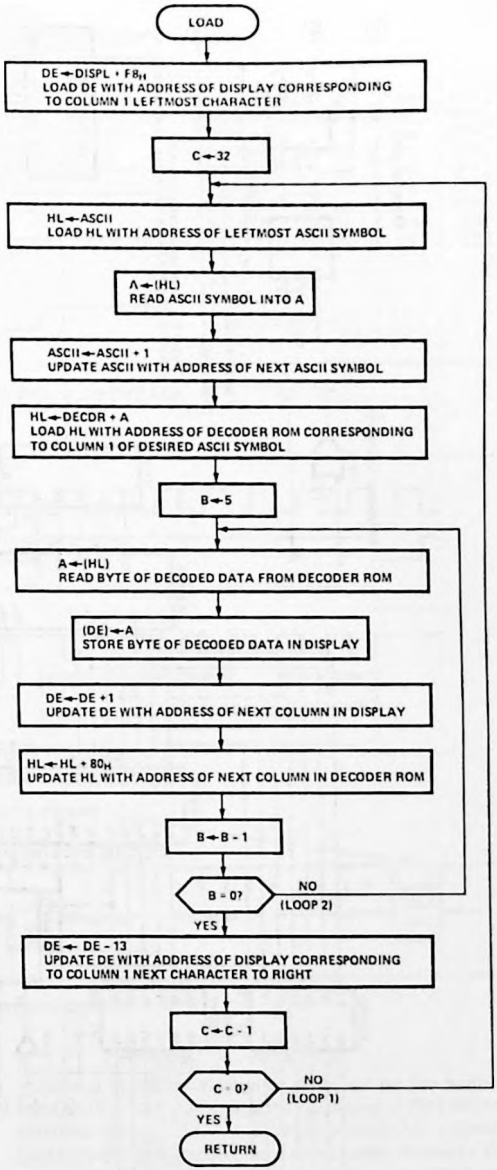


Figure 12. 8080A Microprocessor Program that Decodes a 32 Character ASCII String Prior to Loading into the DECODED DATA CONTROLLER

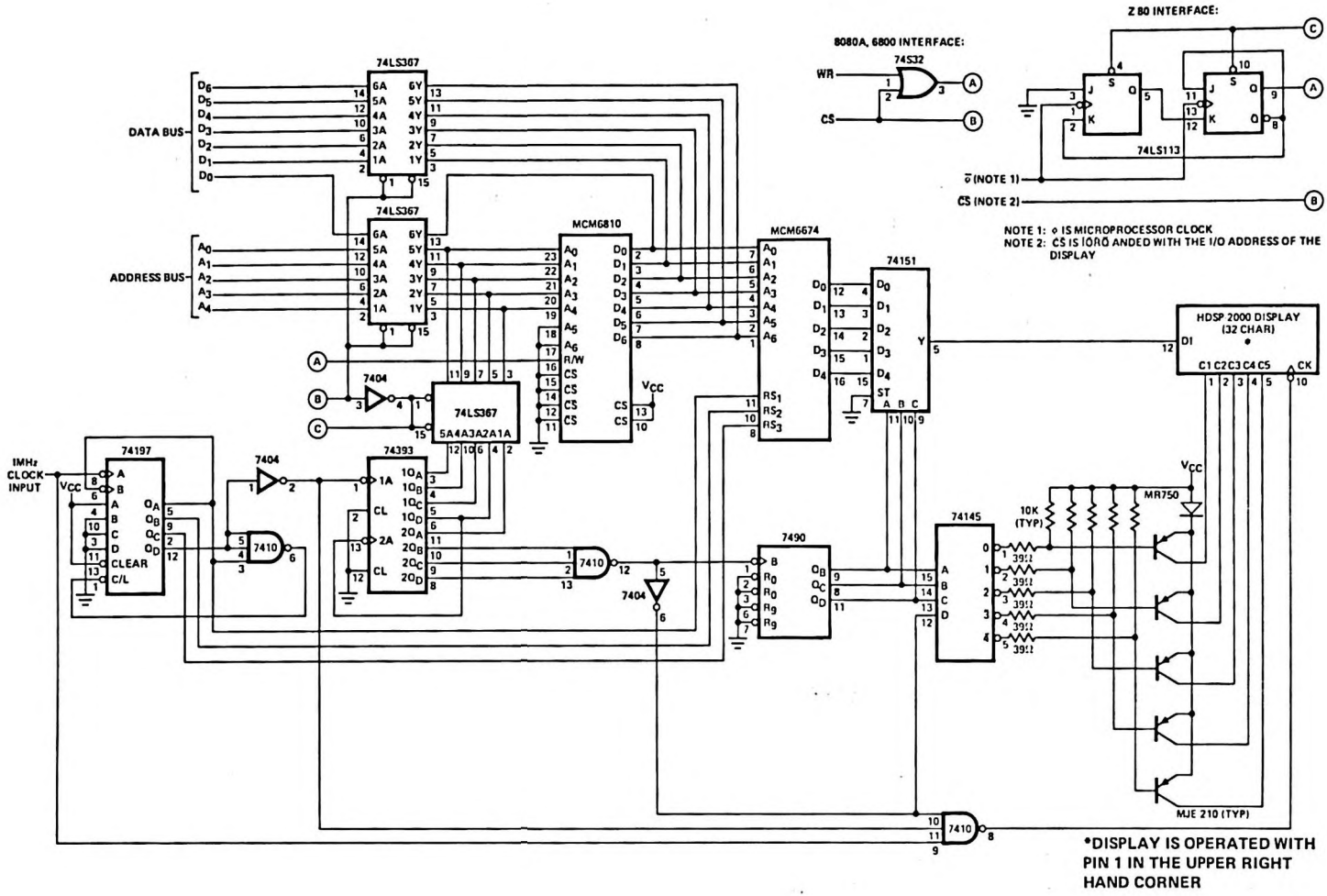
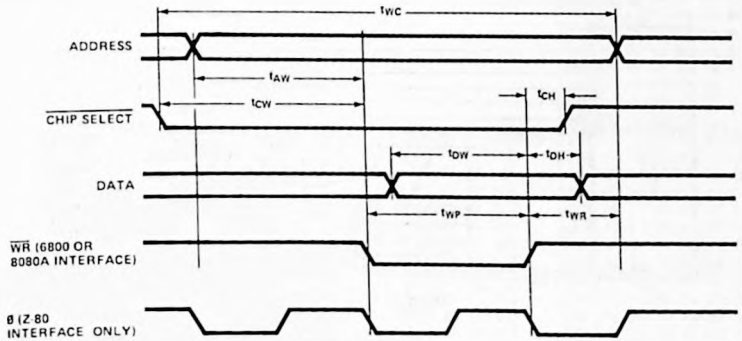


Figure 13. 8080A Microprocessor Interface to the 32 Character HDSP-2000 CODED DATA CONTROLLER



PARAMETER	SYMBOL	MIN.
WRITE CYCLE	t_{WC}	390ns
WRITE DELAY	t_{AW}	65ns
CHIP ENABLE TO WRITE	t_{CW}	65ns
DATA SETUP	t_{DW}	220ns
DATA HOLD	t_{DH}	20ns
WRITE PULSE	t_{WP}	310ns
WRITE RECOVERY	t_{WR}	10ns
CHIP ENABLE HOLD	t_{CH}	20ns

Figure 14. Memory Write Timing for the 32 Character HDSP-2000 CODED DATA CONTROLLER

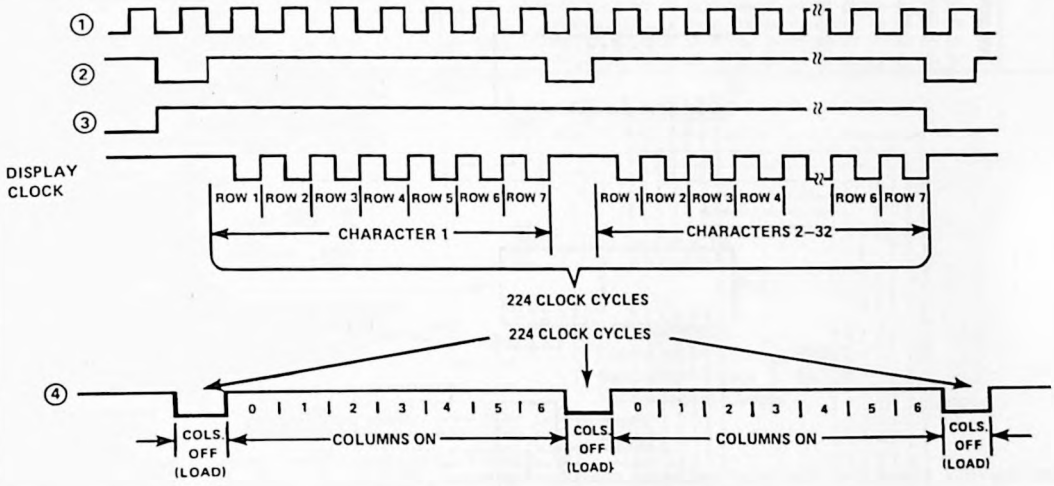


Figure 15. Timing Information for the 32 Character HDSP-2000 CODED DATA CONTROLLER

MCM6674 (NMOS) whose maximum access time is 350ns. For this reason, the MCM6674 must be replaced by a faster Bipolar PROM. If this PROM is programmed with the code listed in Figure 17, it will decode a character font identical to the MCM6674. This same propagation delay problem is present with the MCM6810 RAM. Following worst case design procedures, the MCM68A10 1.5 MHz RAM should be used. To accommodate the additional address line made necessary by the display length expansion, the two 74LS367 tri-state buffers have been replaced with the 74LS244 octal version. Strobing of the display is accomplished using the 74197, 74393, and 7490 counter string. The 74197 is connected as a divide by 8 counter that sequentially selects the seven rows within the 82S2708. The 74393 is a divide by 256 counter connected so that the seven lowest outputs select each of the 128 ASCII characters within the RAM. The previously unused input A/output Q_A of the 7490 has been used as an additional divide by 2 counter. Thus, when the highest output of the 74393, $2Q_D$, and the Q_A output of the 7490 are NANDed through 7437, the basic relationship between load time and column on time is established. However, the external gating that has been added does affect the duty factor slightly. Although these additional gates increase the total package count by one, they perform the necessary function of ensuring that the column drivers are turned off before the clock is gated to the display. This prevents noise from being generated on the clock of the display and eliminates erroneous display data. The resultant duty factor is (23/32) (1/5) or 14.4%. Since the HDSP-2000 is rated at $I_{col(max)} = 410$ mA and there are 32 modules of four digits each, the transistors must source up to 32 times 410 mA or approximately 13A. Darlington PNP power transistors (2N6285) with the proper resistors have been used to accomplish this task.

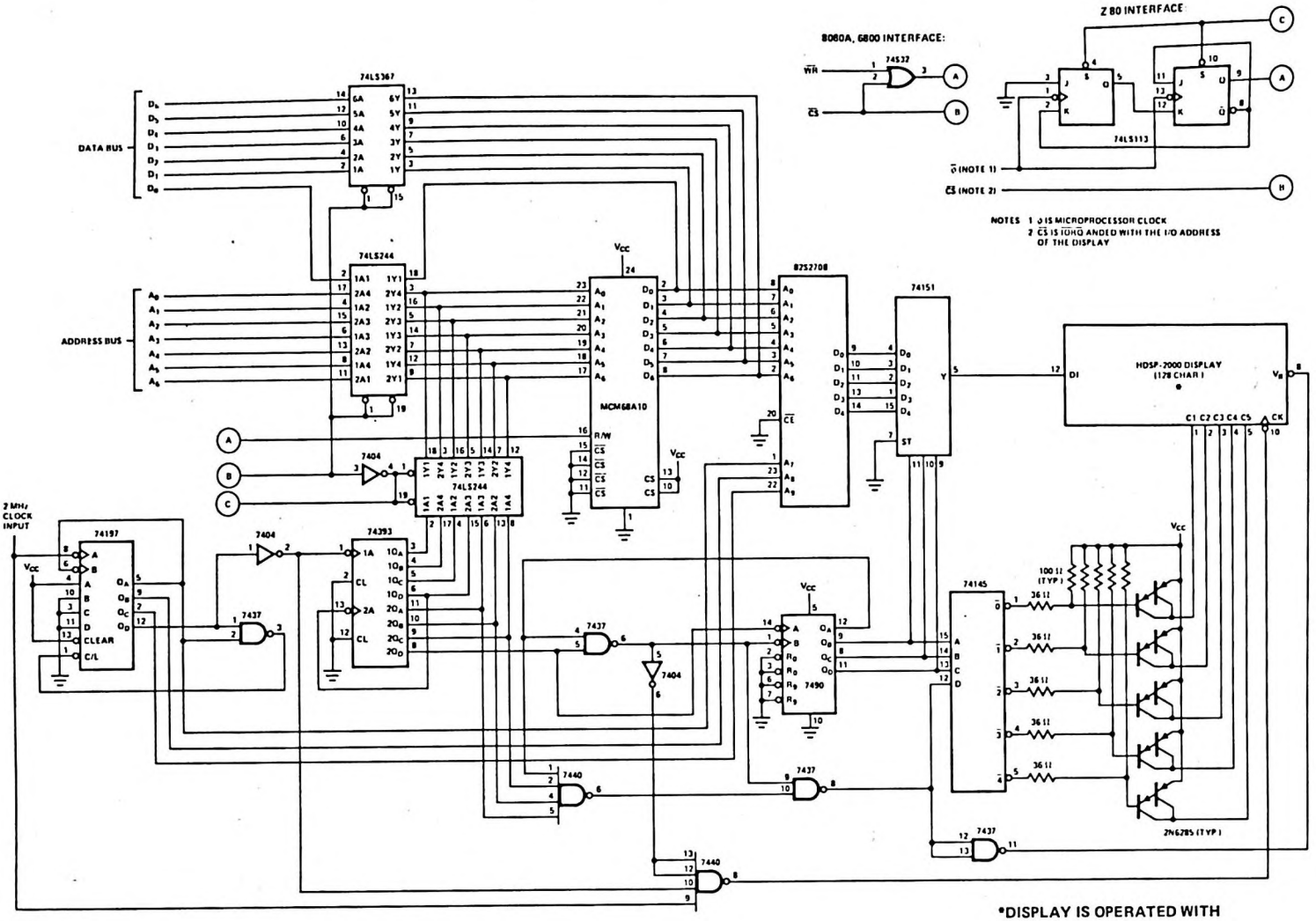


Figure 16. 6800, 8080A, and Z-80 Interface to the 128 Character HDSP-2000 CODED DATA CONTROLLER

PROM ADDRESS	HEXIDECIMAL DATA																
080	FF	FF	E4	E1	E8	FF	E0	EE	E4	E0	FF	E0	E4	E0	EE	EE	ROW 1
090	FF	EE	EE	EE	EE	E0	EE	E1	FF	E4	EE	EE	FF	FF	FF	FF	
0A0	E0	E4	EA	EA	E4	F8	E8	EC	E2	E8	E4	E0	E0	E0	E0	E0	
0B0	EE	E4	EE	EE	E2	FF	E6	FF	EE	EE	E0	EC	E2	E0	E8	EE	
0C0	EE	E4	FE	EE	FE	FF	FF	EF	F1	EE	E1	F1	F0	F1	F1	EE	
0D0	FE	EE	FE	EE	FF	F1	F1	F1	F1	F1	FF	EE	E0	EE	E4	E0	
0E0	E6	E0	F0	E0	E1	E0	E2	ED	F0	E4	E1	F0	EC	E0	E0	E0	
0F0	F6	ED	E0	E0	E4	E0	E0	E0	E0	F1	E0	E2	E4	E8	E8	EA	
100	F1	F0	E4	E1	E4	F1	E1	F1	E8	E4	E0	E4	F5	E4	F1	F1	ROW 2
110	F1	F5	F1	F1	F5	E5	EA	E1	F1	E4	F1	F1	F5	F1	F1	F5	
120	E0	E4	EA	EA	EF	F9	F4	EC	E4	E4	F5	E4	E0	E0	E0	E1	
130	F1	EC	F1	F1	E6	F0	E8	E1	F1	F1	EC	EC	E4	E0	E4	F1	
140	F1	EA	E9	F1	E9	F0	F0	F0	F1	E4	E1	F2	F0	FB	F9	F1	
150	F1	F1	F1	F1	E4	F1	F1	F1	F1	F1	E1	E8	F0	E2	EA	E0	
160	E6	E0	F0	E0	E1	E0	E5	F3	F0	E0	E0	F0	E4	E0	E0	E0	
170	F9	F3	E0	E0	E4	E0	E0	E0	E0	F1	E0	E4	E4	E4	F5	F5	
180	F1	F0	E4	E1	E2	FB	E2	F1	FE	E2	E0	E4	EE	E8	FB	F1	ROW 3
190	F1	F5	F1	F1	F5	E2	EA	E1	EA	EE	F0	F1	F5	F1	F1	F5	
1A0	E0	E4	EA	FF	F4	E2	F4	E8	E8	E2	EE	E4	E0	E0	E0	E2	
1B0	F3	E4	E1	E1	EA	FE	F0	E2	F1	F1	EC	E0	E8	FF	E2	E1	
1C0	E1	F1	E9	F0	E9	F0	F0	F0	F1	E4	E1	F4	F0	F5	F5	F1	
1D0	F1	F1	F1	F0	E4	F1	F1	F1	EA	EA	E2	E8	E8	E2	F1	E0	
1E0	E4	EE	F6	EE	ED	EE	E4	F3	F6	EC	E1	F2	E4	FA	F6	EE	
1F0	F1	F1	F6	EF	FF	F1	F1	F1	F1	F1	FF	E4	E4	E4	E2	EA	
200	F1	F0	E4	E1	EF	F5	F4	FF	E9	FF	FF	F5	E4	FF	F5	F5	ROW 4
210	FF	F7	F7	FD	FD	F5	EA	FF	E4	EE	E8	FF	FD	FD	F7	F7	
220	E0	E4	E0	EA	EE	E4	E8	F0	E8	E2	FF	FF	EC	FF	E0	E4	
230	F5	E4	EE	E6	F2	E1	FE	E4	EE	EF	E0	EC	F0	E0	E1	E2	
240	ED	F1	EE	F0	E9	FC	FC	F3	FF	E4	E1	F8	F0	F5	F3	F1	
250	FE	F1	FE	EE	E4	F1	EA	F1	E4	E4	E4	E8	E4	E2	E0	E0	
260	E2	E1	F9	F1	F3	F1	EE	ED	F9	E4	E1	F4	E4	F5	F9	F1	
270	F9	F3	F9	F0	E4	F1	F1	F1	EA	EF	E2	E8	E0	E2	E0	F5	
280	F1	F0	E4	E1	E4	FB	F8	EA	E5	E2	E0	EE	F5	E8	FB	F1	ROW 5
290	F1	F1	F5	F5	F1	F8	EA	E1	EA	E4	E4	F1	F1	F5	F5	F1	
2A0	E0	E4	E0	FF	E5	E8	F5	E0	E8	E2	EE	E4	EC	E0	E0	E8	
2B0	F9	E4	F0	E1	FF	E1	F1	E8	F1	E1	EC	EC	E8	FF	E2	E4	
2C0	F5	FF	E9	F0	E9	F0	F0	F1	F1	E4	E1	F4	F0	F1	F1	F1	
2D0	F0	F5	F4	E1	E4	F1	EA	F5	EA	E4	E8	E8	E2	E2	E0	E0	
2E0	E0	EF	F1	F0	F1	FF	E4	E1	F1	E4	E1	F8	E4	F5	F1	F1	
2F0	F6	ED	F0	EE	E4	F1	F1	F5	E4	E1	E4	E4	E4	E4	E0	EA	
300	F1	F0	E4	E1	E2	F1	F0	EA	E1	E4	E0	E4	EE	E4	F1	F1	ROW 6
310	F1	F1	F5	F5	F1	F0	EA	E1	F1	E4	E0	F1	F1	F5	F5	F1	
320	E0	E0	E0	EA	FE	F3	F2	E0	E4	E4	F5	E4	E8	E0	EC	F0	
330	F1	E4	F0	F1	E2	F1	F1	F0	F1	E2	EC	E8	E4	E0	E4	E0	
340	F5	F1	E9	F1	E9	F0	F0	F1	F1	E4	F1	F2	F0	F1	F1	F1	
350	F0	F2	F2	F1	E4	F1	E4	FB	F1	E4	F0	E8	E1	E2	E0	E0	
360	E0	F1	F9	F1	F3	F0	E4	F1	F1	E4	F1	F4	E4	F5	F1	F1	
370	F0	E1	F0	E1	E5	F3	EA	F5	EA	F1	E8	E4	E4	E4	E0	F5	
380	FF	F0	FF	FF	E1	FF	E0	FB	E1	E0	FF	E0	E4	E0	EE	EE	ROW 7
390	FF	EE	EE	EE	EE	E0	FB	E1	FF	E4	E4	EE	FF	FF	FF	FF	
3A0	E0	E4	E0	EA	E4	E3	ED	E0	E2	E8	E4	E0	F0	E0	EC	E0	
3B0	EE	EE	FF	EE	E2	EE	EE	F0	EE	EC	E0	F0	E2	E0	E8	E4	
3C0	EE	F1	FE	EE	FE	FF	F0	EF	F1	EE	EE	F1	FF	F1	F1	EE	
3D0	F0	ED	F1	EE	E4	EE	E4	F1	F1	E4	FF	EE	E0	EE	E0	FF	
3E0	E0	EF	F6	EE	ED	EE	E4	EE	F1	EE	EE	F2	EE	F5	F1	EE	
3F0	F0	E1	F0	FE	E2	ED	E4	EA	F1	EE	FF	E2	E4	E8	E0	EA	

Figure 17. 82S2708 PROM Listing

DISPLAY PROCESSOR CONTROLLER

The previously mentioned interface techniques provide only for the display of ASCII coded data. Such important features as a blinking cursor, editing routines, and character addressing must be provided by other subroutines in the microprocessor software. The DISPLAY PROCESSOR CONTROLLER is a system which utilizes a dedicated 8048 single chip microprocessor to provide these important features. This controller, as depicted in Figure 18, is a series of printed circuit board subsystems available from Hewlett-Packard under the following part numbers:

HDSP-2470 — Controller with 64 character ASCII to 5 x 7 decoder

HDSP-2471 — Controller with 128 character universal ASCII to 5 x 7 decoder

HDSP-2472 — Controller with socket for user supplied custom coded ROM/PROM/EPROM.

All of the controllers have the following features:

- Choice of character string length:
  4 to 48 characters in increments of four characters
- Four modes of data entry
  Left Entry
  Right Entry
  RAM Entry (≤ 32 characters only)
  Block Entry
- Flashing Cursor — Left Entry Only
- Data Out (≤ 32 characters only)
- Edit Functions
  Clear Display, Backspace Cursor → RIGHT ENTRY
  Forwardspace Cursor, Insert, Delete → LEFT ENTRY

These controllers have been designed to eliminate the burden of data handling between keyboard, display, and microprocessor. The product data sheet describes the technical function of the controllers in detail.

Interfacing the controller to microprocessor systems depends on the needs of the particular application. Figure 19 depicts a latched interface from a master microprocessor to the HDSP-247X series of controllers. These interfaces are utilized to avoid having the master processor wait for the controller to accept data.

In sophisticated systems, it may be desirable to have the HDSP-247X controller handle all of the keyboard/display interface while the microprocessor reads edited messages from the controller DATA OUT port. This function can be achieved through the use of peripheral interface adapters (PIA) available from the microprocessor manufacturers. Figure 20 depicts a 6800 based system in which data may enter the display from either a keyboard or a microprocessor. This interface uses a 6821 PIA configured so that PB_7 controls whether the microprocessor or keyboard enters data into the controller. The 6800 program is shown in Figure 21. Subroutine "LOAD" uses CA_1 and CA_2 to provide a data entry handshake that

APPLICATIONS

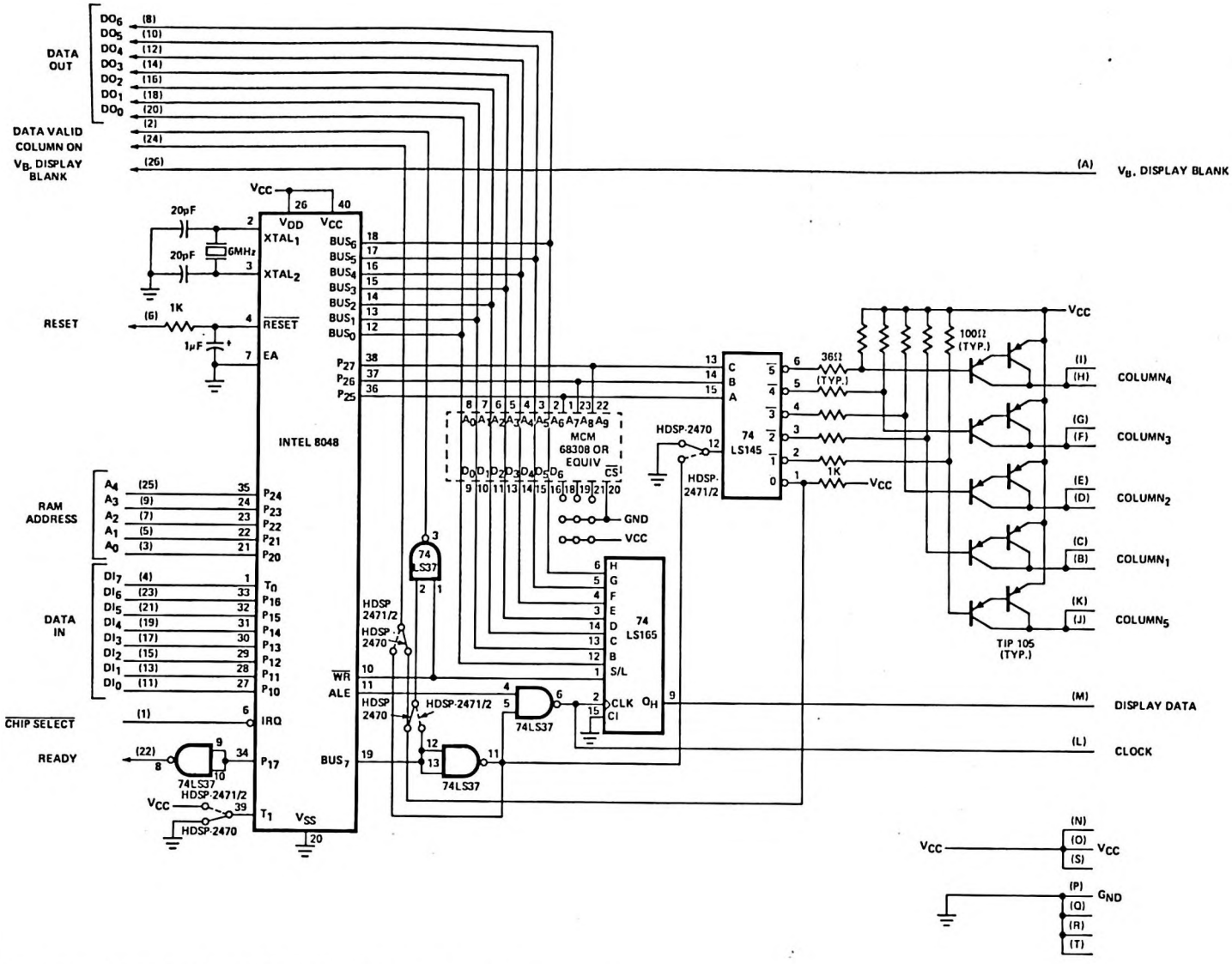


Figure 18. HDSP-2470/-2471/-2472 DISPLAY PROCESSOR CONTROLLER

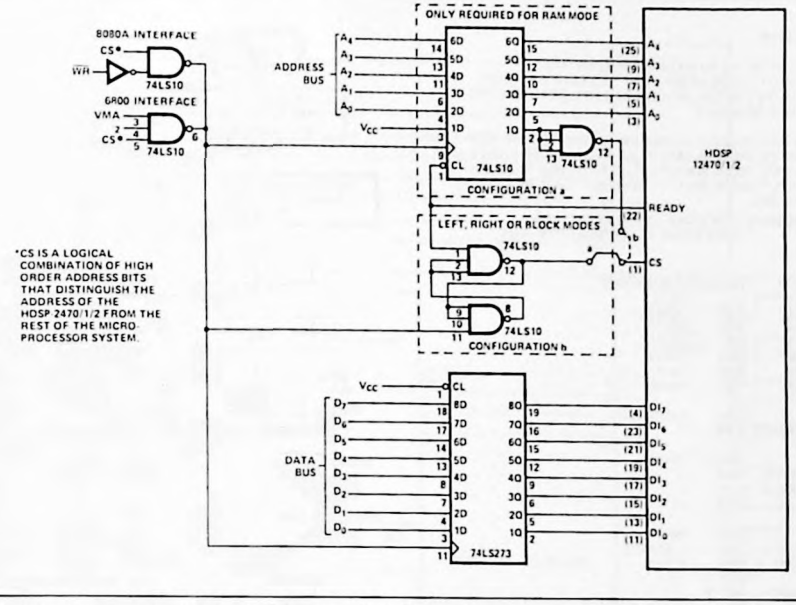


Figure 19. Latched Interface to the HDSP-2470/-2471/-2472 DISPLAY PROCESSOR CONTROLLER

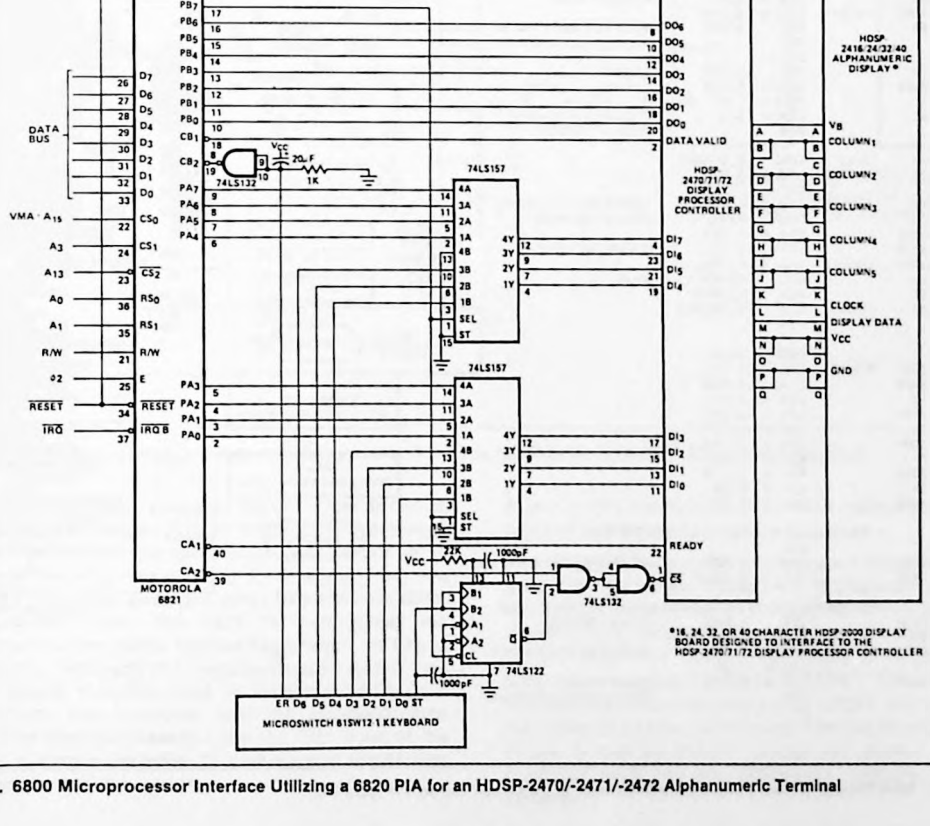


Figure 20. 6800 Microprocessor Interface Utilizing a 6820 PIA for an HDSP-2470/-2471/-2472 Alphanumeric Terminal

APPLICATIONS

```
* PORT CONFIGURATION:
* 1.  PORT A:
*           PA0-PA7 OUTPUTS TO DATA IN OF HDSP-247X
*           CA1  (INPUT) MODE 00 SET FLAG NEG EDGE OF READY
*           CA2  (OUTPUT) MODE 100 CLEARED MPU READ PRA. SET
*           NEG  EDGE OF READY
* 1.  PORT B:
*           PB0-PB6 INPUTS DATA TO 6800 FROM DATA OUT OF HDSP-247X
*           CB1  (INPUT) MODE 00 SETS FLAG NEG EDGE OF DATA VALID
*           CB2  (INPUT) MODE 000 SETS FLAG NEG EDGE OF ER KEY
*           CB2  (INPUT) MODE 001 SETS FLAG NEG EDGE OF ER KEY
*           CAUSING IRQ
*           PB7  (OUTPUT) LOW ENABLES PA0-PA7 TO MUX
*                         HIGH ENABLES  KEYBOARD TO MUX
*

LOC   OBJECT    CODE      SOURCE STATEMENT

      8008      PRA       EQU     $8008
      8008      DRA       EQU     $8008
      8009      CRA       EQU     $8009
      800A      PRB       EQU     $800A
      800A      DRB       EQU     $800A
      800B      CRB       EQU     $800B

                          ORG     $0000
0000            MESSAGE   RMB     2

                          ORG     $0100
0100            STATUS    RMB     1
0101            CURSOR    RMB     1
0102            DATA      RMB     32

                          ORG     $0400
0400  CE 0100  READ      LDX     I, STATUS
0403  B6 800A  LOOP1     LDA A   E, PRB          CLEAR CB1 AND CB2
0406  5F                CLR B
0407  5C        LOOP2     INC B
0408  B6 800B            LDA A   E, CRB
040B  2A FA               BPL     LOOP2         WAIT FOR DATA VALID
040D  C1 0A               CMP B   I, 10
040F  23 F2               BLS     LOOP1
0411  C6 21               LDA B   I, 33
0413  B6 800A  LOOP3     LDA A   E, PRB          READ AND CLEAR CB1
0416  84 7F               AND A   I, $7F
0418  A7 00               STA A   X, 0          STORE IN RAM
041A  B6 800B  LOOP4     LDA A   E, CRB
041D  2A FB               BPL     LOOP4         WAIT FOR DATA VALID
041F  08                  INX
0420  5A                  DEC B
0421  26 F0               BNE     LOOP3         READ DATA
0423  B6 800A            LDA A   E, PRB
0426  84 7F               AND A   I, $7F
0428  A7 00               STA A   X, 0
042A  39                  RTS

042B  DE 00     LOAD      LDX     D, MESSGE
042D  A6 00     LOOP10    LDA A   X, 0
042F  08                  INX
0430  81 FF               CMP A   I, $FF        LAST WORD IN STRING
0432  27 0D               BEQ     ENDL          JUMP WHEN DONE
0434  B7 8008             STA A   E, PRA
0437  7D 8008             TST     E, PRA        CLEAR CA1 AND CA2
043A  B6 8009   LOOP11    LDA A   E, CRA
043D  2A FB               BPL     LOOP11        WAIT
043F  20 EC               BRA     LOOP10
0441  DF 00     ENDL      STX     D, MESSGE
0443  39                  RTS

                          ORG     $0500
0500  7F 8009   START     CLR     E, CRA
0503  7F 800B             CLR     E, CRB
0506  86 FF               LDA A   I, $FF
0508  B7 8008             STA A   E, DRA
050B  86 24               LDA A   I, $24
050D  B7 8009             STA A   E, CRA
0510  86 80               LDA A   I, $80
0512  B7 800A             STA A   E, DRB
0515  86 04               LDA A   I, $04
0517  B7 800B             STA A   E, CRB

                * PROCEDURE TO LOAD HDSP-247X SYSTEM
051A  0E                  CLI
051B  7F 800A             CLR     E, PRB        DISABLE KEYBD FROM MUX
051E  BD 042B             JSR     E, LOAD

                * PROCEDURE TO READ DATA OUT OF HDSP-247X SYSTEM
0521  7D 800A             TST     E, PRB        CLEAR CB1, CB2
0524  86 80               LDA A   I, $80
0526  B7 800A             STA A   E, PRB        ENABLE KEYBD TO MUX
0529  86 0C               LDA A   I, $0C
042B  B7 800B             STA A   E, CRB        ENABLE IRQ,
052E  0F                  SEI                   IRQ CAUSE JSR TO READ
```

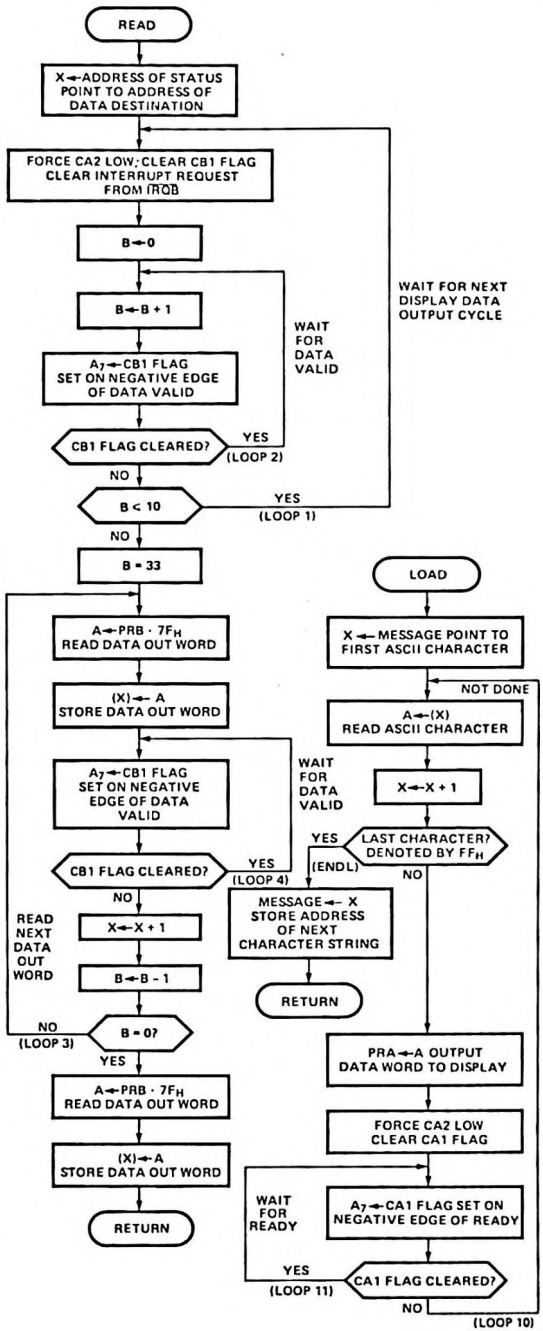


Figure 21. 6800 Microprocessor program that interfaces to the circuit shown in Figure 14.

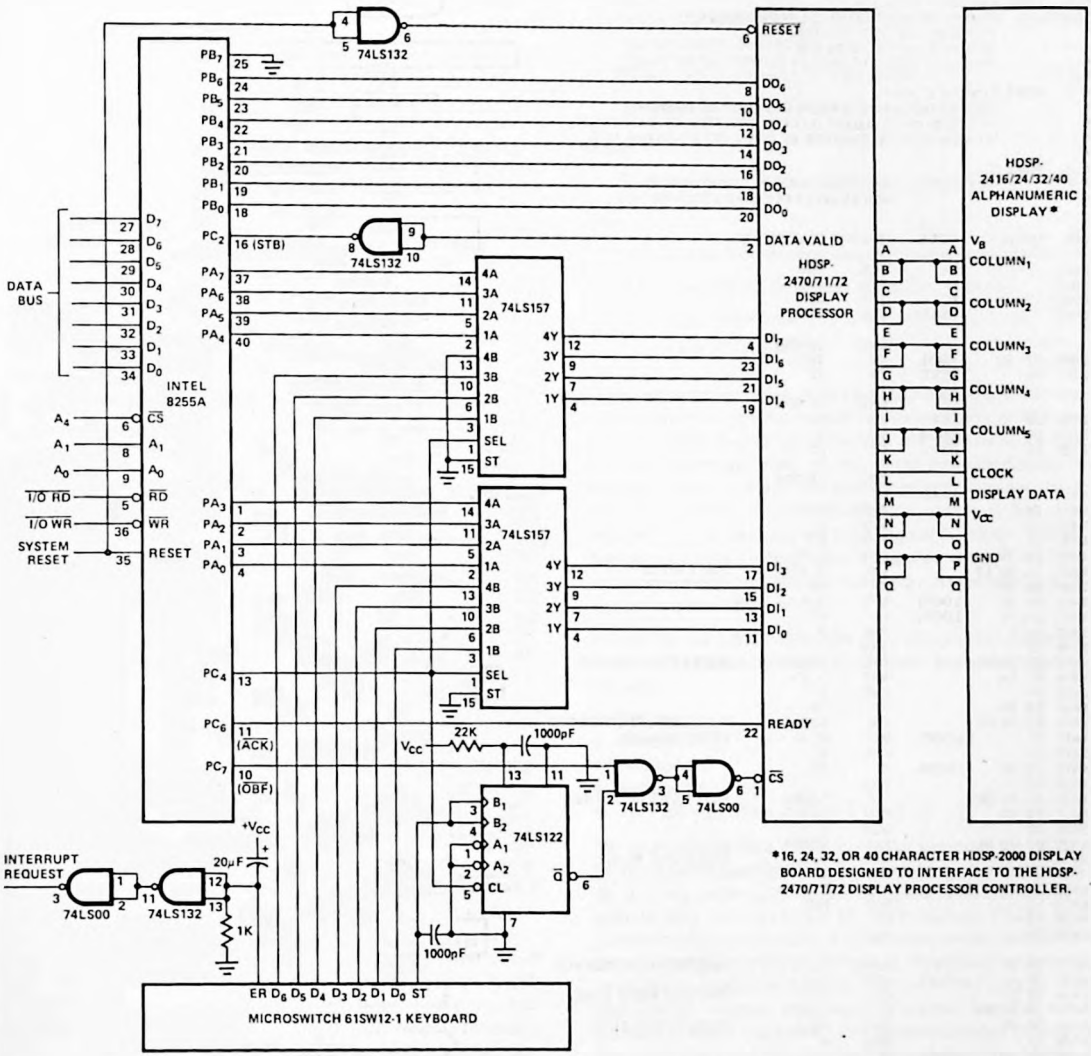


Figure 22. 8080A Microprocessor Interface Utilizing an 8255 PIA for an HDSP-2470/-2471/-2472 Alphanumeric Terminal

allows the 6800 to load data into the controller as fast as the controller can accept it. After the prompting message has been loaded, the microprocessor turns the control of data entry over to the keyboard. A signal from the keyboard ("ER" in the example) sets a flag within the 6821. Depending on how the 6821 is configured, the microprocessor can either test the flag or allow the flag to automatically interrupt the microprocessor. Subroutine "READ" would then be used to read the DATA OUT outputs from the controller into the microprocessor system. The microprocessor uses the CB_1 input of the 6821 PIA to determine when to read each of the 34 data output words into the system.

A similar PIA interface for the 8080A microprocessor is depicted in Figures 22 and 23.

The HDSP-247X series of controllers are programmed to default to "Left Entry" mode for a 32 character string of displays. If some other entry mode or string length is desired, it is necessary to either load the appropriate control word from the microprocessor or to provide a control word during POWER ON RESET. The controller will read the DATA IN lines during RESET and interpret the contents as the control word. The circuit depicted in Figure 24 can be utilized to load any desired preprogrammed word into the HDSP-247X controller, during power on.

```
• PORT CONFIGURATION:
• 1. PORT A (MODE 1 OUTPUT):
•          PA0-PA7 OUTPUTS TO DATA IN OF HDSP-247X
•          PC7 (OBF) OUTPUT; TO CHIP SELECT
•          PC6 (ACK) INPUT; TO READY
•          FLAG PC7 (OBF) CLEARED BY OUTPUT; SET BY READY
•
• 2. PORT B (MODE 1 INPUT):
•          PB0-PB6 INPUTS DATA FROM DATA OUT OF HDSP-247X
•          PC2 (STB) INPUT; LOADS DATA ON NEG EDGE OF DATA VALID
•          FLAG PC0 (INTR) CLEARED BY INPUT, SET BY DATA VALID
•
• 3. PORT C:
•          PC4 OUTPUT; LOW ENABLES PA0-PA7 TO HDSP-247X
•                      HIGH ENABLES KEYBOARD TO HDSP-247X

LOC  OBJECT    CODE     SOURCE STATEMENTS

000C           PA       EQU    0CH
000D           PB       EQU    0DH
000E           PC       EQU    0EH
000F           CNTRL    EQU    0FH

                        ORG    0E000H
E000 02 E0     ASCII    DW     TEXT
E002 00        TEXT     DS     32

                        ORG    0E100H
E100 00        STAT     DB     0
E101 00        ADDR     DB     0
E102 00        DATA     DS     32

                        ORG    0E400H
E400 F3        READ     DI
E401 F5                 PUSH   PSW
E402 E5                 PUSH   H
E403 C5                 PUSH   B
E404 0E 20              MVI    C, 32
E406 21 00 E1           LXI    H, STAT      FIRST WORD
E409 DB 0D              IN     PB           CLEAR INTR
E40B 06 00     LOOP1    MVI    B, 0
E40D DB 0E     LOOP2    IN     PC
E40F 04                 INR    B
E410 1F                 RAR
E411 D2 0D E4           JNC    LOOP2        WAIT UNTIL INTR IS SET
E414 3E 0A              MVI    A, 10
E416 B8                 CMP    B
E417 DB 0D              IN     PB
E419 D2 0B E4           JNC    LOOP1        WAIT UNTIL STATUS WORD
E41C 77        LOOP3    MOV    M, A         STORE IN RAM
E41D 23                 INX    H
E41E DB 0E     LOOP4    IN     PC
E420 1F                 RAR
E421 D2 1E E4           JNC    LOOP4        WAIT UNTIL INTR IS SET
E424 DB 0D              IN     PB
E426 0D                 DCR    C
E427 C2 1C E4           JNZ    LOOP3
E42A 77                 MOV    M, A         STORE LAST WORD
E42B C1                 POP    B
E42C E1                 POP    H
E42D F1                 POP    PSW
E42E FB                 EI
E42F C9                 RET

E430 2A 00 E0  LOAD     LHLD   ASCII        FIRST WORD OF MESSAGE
E433 7E        LOOP5    MOV    A, M
E434 FE FF              CPI    0FFH         CHECK TO SEE IF DONE
E436 CA 45 E4           JZ     ENDL
E439 D3 0C              OUT    PA           OUTPUT TO DISPLAY
E43B 23                 INX    H
E43C DB 0E     LOOP6    IN     PC
E43E 17                 RAL
E43F D2 3C E4           JNC    LOOP6        WAIT
E442 C3 33 E4           JMP    LOOP5        NEXT WORD
E445 23        ENDL     INX    H
E446 22 00 E0           SHLD   ASCII
E449 C9                 RET

E44A 3E A7     START    MVI    A, 0A7H      PA OUTPUT, PB INPUT
E44C D3 0F              OUT    CNTRL
E44E 3E 0C              MVI    A, 0CH       CLEAR INTE A
E450 D3 0F              OUT    CNTRL
E452 3E 05              MVI    A, 05H
E454 D3 0F              OUT    CNTRL        SET INTE B

                • PROCEDURE TO LOAD HDSP-247X SYSTEM
E456 3E 08              MVI    A, 08H
E458 D3 0F              OUT    CNTRL        ENABLE A SIDE OF MUX
E45A CD 30 E4           CALL   LOAD

                • PROCEDURE TO READ DATA OUT OF HDSP-247X SYSTEM
E45D 3E 09              MVI    A, 09H
E45F D3 0F              OUT    CNTRL        ENABLE B SIDE OF MUX
E461 FB                 EI                  INT MUST CALL READ
```

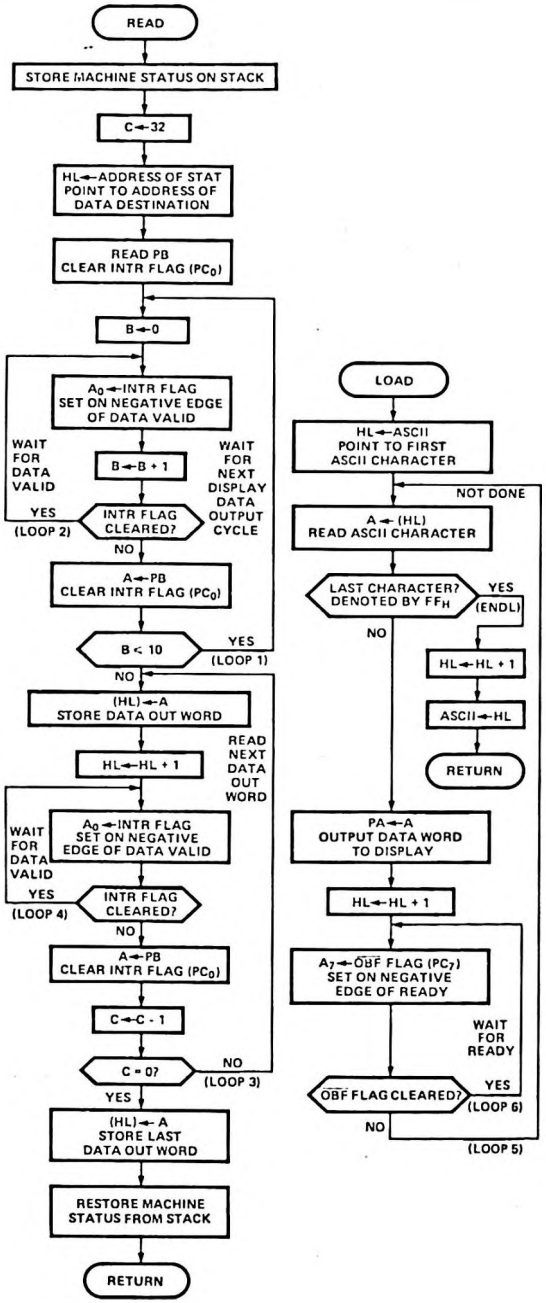


Figure 23. 8080A Microprocessor Program that Interfaces to the Circuit shown in Figure 17.

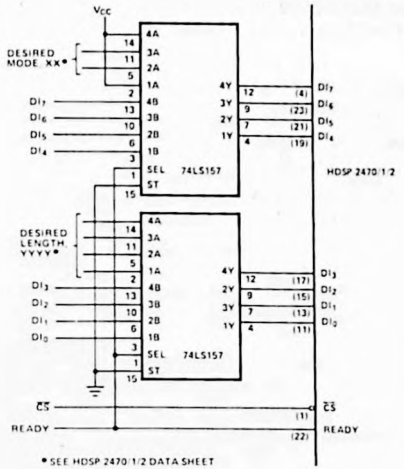


Figure 24. External Circuitry to Load a Control Word into the HDSP-2470/-2471/-2472 Alphanumeric System upon Reset

DISPLAY POWER DISSIPATION

The HDSP-2000 combines a significant amount of logic and display capability in a very small package. As such, on-board power dissipation is relatively high and thermal design of the display mounting becomes an important consideration. The HDSP-2000 is designed to permit operation over a wide range of temperature and supply voltages. The design of a heatsink to maintain a junction temperature of less than 125°C for a multiple package system where every electrical input operates at maximum voltage and current would be difficult at best. However, in virtually all applications, the actual power dissipation is only a small fraction of the maximum power dissipation, since V_{COL} is less than 5.25V, only a fraction of the 35 LEDs are on at any time, and the duty factor is never 20%. The calculation of power dissipation is important since the result is largely a function of external circuit parameters. The minimization of power dissipation will reduce the amount of heatsinking required for the displays. Furthermore, by the Arrhenius model, the display reliability is increased by 40% for a 10°C reduction in junction temperature. Thus, reduced power dissipation or better heatsinking can also increase the reliability of the display system.

Calculation of power dissipation in the HDSP-2000 display family can be made using the following formulas:

$$P_D = P(I_{CC}) + P(I_{REF}) + P(I_{COL}) \quad (7)$$

where

$$P(I_{CC}) = I_{CC1}\, V_{CC} \quad (8)$$

when V_{CC} is applied continuously to the display

$$P(I_{CC}) = I_{CC1}\, V_{CC}\, (t + T) / (t + T + T_B) \quad (9)$$

when V_{CC} is turned off during the time T_B

where

$$P(I_{REF}) = (I_{CC2} - I_{CC1})\, V_{CC}\, (n/35) \quad (10)$$

when V_B is connected to V_{CC} and V_{CC} is applied continuously to display

$$P(I_{REF}) = 5\, (I_{CC2} - I_{CC1})\, V_{CC}\, (n/35)\, D.F. \quad (11)$$

when V_B is logical 0 during times t and T_B

where

$$P(I_{COL}) = 5\, I_{COL}\, V_{COL}\, (n/35)\, D.F. \quad (12)$$

where

n = average number of diodes illuminated per character

D.F. = column on time from equation (1) or (5)

$I_{CC1} = I_{CC}\ (V_B = 0.4V)$

$I_{CC2} = I_{CC}\ (V_B = 2.4V)$

$P(I_{CC})$ is the power which is dissipated in the logic within the shift register. $P(I_{CC})$ is constant regardless of n, or D.F. as long as voltage is applied to the V_{CC} pin. However, for low D.F., I_{CC} can be switched off during the time the display is blanked. $P(I_{REF})$ is the power dissipated in the logic to drive the current mirror output. Thus, if the output of the shift register and the V_B input are both logical 1, $P(I_{REF})$ will be dissipated. $P(I_{COL})$ is the power dissipated within the LEDs and the constant current outputs during the time that V_{COL} is applied and the LEDs are on.

As can be seen from formulas (7) through (12) there are several techniques by which total power dissipation can be reduced:

- Reduce n
- Reduce V_{COL}
- Reduce D.F.
- Reduce V_{CC}
- Turn off V_{CC} when display is blanked

For most applications, $n \leq 20$ dots. For example, the HDSP-2470 character generator has 3 characters with 20 dots on (#, @, B), 1 character with 19 dots on (zero), and 6 characters with 18 dots on (A,D,E,M,R,W). With custom PROM programming these 4 symbols (#, @, B, zero) can be modified to reduce the total number of dots on to 18 or less. The average of all 36 alphabetic and numeric symbols is 14.7 dots on. The calculations assume that every character has the same number of illuminated dots. This assumption can overstate the maximum power dissipation if the application includes a fixed number of spaces in the display.

Above 2.4V V_{COL} for standard red devices and 2.75V V_{COL} for GaP devices, I_{COL} is nearly constant. While it is possible to operate the columns of the HDSP-2000 display using fullwave rectified unregulated DC, lower power dissipation can be achieved by using the regulated V_{CC} supply. Then, V_{COL} is equal to V_{CC} minus the collector to emitter saturation voltage across the column switching transistors. Since the minimum recommended V_{COL} is 2.4V or 2.75V, PNP Darlington transistors with a silicon diode in series with the emitter can be used to lower the power dissipation within the display.

The time averaged luminous intensity for the display is equal to the peak luminous intensity on the data sheet times D.F. Thus, reduction in D.F. will also reduce the time averaged luminous intensity as well as power dissipation. For most indoor applications, a D.F. of 10% for standard red and 5% for GaP displays will provide satisfactory luminous intensity. For example, the 40 character HDSP-2470 system has a D.F. of 11.6%. However, a D.F. of 17% or higher is recommended for sunlight viewable applications for the GaP displays.

The HDSP-2000 family of alphanumeric displays are specified for operation with a 5% tolerance 5 volt supply. A tighter tolerance supply will also reduce the power dissipation in the display.

I_{CC} can be switched off during the time the display is blanked. Thus, power would be applied to the display; the shift register would be loaded with information; the columns would be turned on; and then the column current, V_B, and V_{CC} would be switched off until the next column refresh cycle. For low D.F., this can significantly reduce the power dissipation within the display. As D.F. increases, the display is blanked for a smaller portion of the refresh cycle and the power reduction is reduced. When the blanking time goes to zero, the power reduction also goes to zero.

For example, the maximum power dissipation for a four character HDSP-2000 display ($n = 20$, $V_{COL} = 3.5V$, $V_B = 2.4V$, D.F. = 17.5%, $V_{CC} = 5.25V$) can be calculated as shown below:

$$P(I_{CC}) = (60\ mA)(5.25V) = 315\ mW \quad (13)$$

$$P(I_{REF}) = 5(95\ mA - 60\ mA)(5.25V)(20/35)(0.175) = 92\ mW \quad (14)$$

$$P(I_{COL}) = 5(410\ mA)(3.5V)(20/35)(0.175) = 718\ mW \quad (15)$$

$$P_D = P(I_{CC}) + P(I_{REF}) + P(I_{COL}) = 1125\ mW \quad (16)$$

Assumptions Used in	Maximum Power Dissipation Operating Conditions (Unless otherwise specified)	Power Dissipation	Typical Power Dissipation Operating Conditions (Unless otherwise specified)	Power Dissipation
	$V_{CC} = 5.25V$ $V_{COL} = 3.5V$ $n = 20$ D.F. = .175 V_B = logical 0 during t (and T_B) $T_B = 0$	1.12W	$V_{CC} = 5.00V$ $V_{COL} = 3.0V$ $n = 15$ D.F. = .175 V_B = logical 0 during t (and T_B) $T_B = 0$	.65W
1. Reduce n	$n = 18$	1.04W		
2. Reduce n and V_{COL}	$n = 18$ $V_{COL} = 3.0V$	.95W		
3. Reduce V_{COL}	$V_{COL} = 3.0V$	1.02W	$V_{COL} = 2.4V$	.58W
			$V_{COL} = 2.75V$	.62W
4. Reduce D.F.	D.F. = .10	.78W	D.F. = .10	.47W
	D.F. = .05	.55W	D.F. = .05	.35W
5. Reduce V_{COL} and D.F.	$V_{COL} = 3.0V$ D.F. = .10	.72W	$V_{COL} = 2.4V$ D.F. = .10	.43W
	$V_{COL} = 3.0V$ D.F. = .05	.52W	$V_{COL} = 2.75V$ D.F. = .05	.34W
6. Reduce D.F. Turn-off V_{CC} during T_B	D.F. = .10 X = .625	.66W	D.F. = .10 X = .625	.39W
	D.F. = .05 X = .375	.45W	D.F. = .05 X = .375	.21W
7. Reduce V_{COL}, Reduce D.F., Turn-off V_{CC} during T_B	$V_{COL} = 3.0V$ D.F. = .10 X = .625	.60W	$V_{COL} = 2.4V$ D.F. = .10 X = .625	.34W
	$V_{COL} = 3.0V$ D.F. = .05 X = .375	.32W	$V_{COL} = 2.75V$ D.F. = .05 X = .375	.20W

where $x = \left(\frac{t+T}{t+T+T_B}\right)$

Figure 25. Maximum and Typical Power Dissipation for the HDSP-2000/1/2/3 and HDSP-2300 Alphanumeric Displays

Similarly, a typical power dissipation for a four character HDSP-2000 display (n = 15, V_{COL} = 3.0V, D.F. = 17.5%, V_{CC} = 5.00V) can be calculated as:

$$P(I_{CC}) = (45\ mA)(5.00V) = 225\ mW \quad (17)$$

$$P(I_{REF}) = 5(73\ mA - 45\ mA)(5.00V)(15/35)(0.175) = 52\ mW \quad (18)$$

$$P(I_{COL}) = 5(335\ mA)(3.0V)(15/35)(0.175) = 377\ mW \quad (19)$$

$$P_D = P(I_{CC}) + P(I_{REF}) + P(I_{COL}) = 654\ mW \quad (20)$$

Some typical power dissipations for other values of n, V_{COL}, D.F., V_{CC}, are shown in Figure 25. Note that at a D.F. of 17.5%, which would be appropriate for a sunlight viewable application, the maximum power dissipation can be reduced to under 1.0W, while the typical power dissipation can be reduced to 0.60W. In most indoor ambients, the D.F. can be reduced to 10% for standard red and 5% for GaP displays. Under these conditions the maximum power dissipation is 0.72W or 0.52W and the typical power dissipation is 0.43W or 0.34W. Thus, in power sensitive applications, GaP displays can be used to conserve power. Turning off V_{CC} during the time the display is blanked can further reduce the power dissipation. In this manner the maximum power dissipation can be reduced .32W and the typical power dissipation can be reduced to 0.20W for the GaP displays.

HEAT SINKING CONSIDERATIONS

For operation at the maximum temperature of 85°C, it is important that the following criteria be met:

a. $T_{PIN} \leq 100°C$

where T_{PIN} = temperature of hottest pin

b. $T_J \leq 125°C$

The thermal resistance IC junction to case, Θ_{JC}, or IC junction to pin, Θ_{J-PIN}, is shown in Table 2. Using these factors, it is possible to determine the required heat sink power dissipation capability and associated power derating through the following equations:

$$T_* = \Theta_{*A} P_D + T_A \quad (21)$$

$$T_J = T_* + \Theta_{J*} P_D \quad (22)$$

where

* = Pin or Case

Table 2. Device Thermal Resistance

Device	Θ_{JC}	Θ_{J-PIN}
HDSP-2000 Series	20°C/W	25°C/W
HDSP-2300 Series	7.5°C/W	10°C/W
HDSP-2490 Series	7.5°C/W	13°C/W

For example, given Θ_{PIN-A} of 35°C/W an ambient temperature of 60°C, and the operating conditions shown in equations (13), (14), and (16) the T_{PIN} and T_J for the HDSP-2000 family can be calculated as shown below:

$$T_{PIN} = (35°C/W)(1.12W) + 60°C = 99°C \quad (23)$$

$$T_J = 99°C + (25°C/W)(1.12W) = 99°C + 28°C = 127°C \quad (24)$$

Heat sink design for the HDSP-2000 family of displays can be accomplished in a variety of ways. For single line applications, a maximum metalized printed circuit board such as shown in Figure 26 can be used. For example, the HDSP-2416/-2424/-2432/-2440 display boards consist of 16, 24, 32 or 40 characters of HDSP-2000 displays mounted on a maximum metalized printed circuit board. The HDSP-2432 printed circuit board is 2.3" x 6.4" and has a Θ_{PIN-A} of about 45°C/W per package for a 1/2 ounce copper clad printed circuit. These display boards are designed for free air operation of 55°C and operation to 70°C with forced air cooling of 150 fpm normal to the rear side of the board, for displays operating at a P_D of 1.00 watt or less.

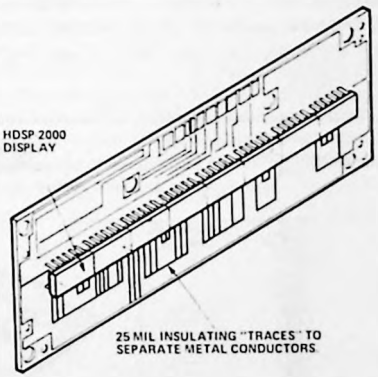


Figure 26. Maximum Metalized Printed Circuit for the HP HDSP-2000

HEAT SINK DESIGN FOR OPERATION ABOVE 70°C

A free air operating temperature of 85° C can be achieved by heat sinking the display. Figure 27 depicts a two part heat sink which can be assembled using two different extruded parts. In this design, the vertical fins promote heat transfer due to naturally induced convection. Care should be taken to insure a good thermal path between the two portions of the heat sink. To optimize power handling capability, the heat transfer contact area between the printed circuit board metallization and the heat sink should be maximized. A thermally conductive silicon rubber sheet can be used to insulate the printed circuit board. Heatsink assemblies similar to the one shown in Figure 27 typically exhibit a thermal resistance, Θ_{PIN-A}, of 14° C/W per package for a 32 character display.

Copper or aluminum bars mounted underneath the displays can also be used to heatsink the display assembly. Heat generated within the displays is conducted through the ceramic substrate into the bar. The ends of the bar are mounted to a heatsink or to a metal front panel. The bar can be insulated from the pins of the display and the printed circuit board with a thermally conductive silicon rubber sheet. Figure 28 shows a metal plate with slots milled in the plate for each row of displays such that each horizontal row of displays straddles a bar.

A thermal resistance model for this heatsinking technique is shown in Figure 29. This model assumes that all heat generated in the display is generated in the center of each display package and that the ends of the bar are connected to an ideal heatsink. Then the temperature rise of the centermost display in the bar can be calculated as shown below:

$$T_C = 4(\Theta/2)P_D + 3\Theta P_D + 2\Theta P_D + \Theta P_D + T_A$$
$$= 8\Theta P_D + T_A \qquad (25)$$

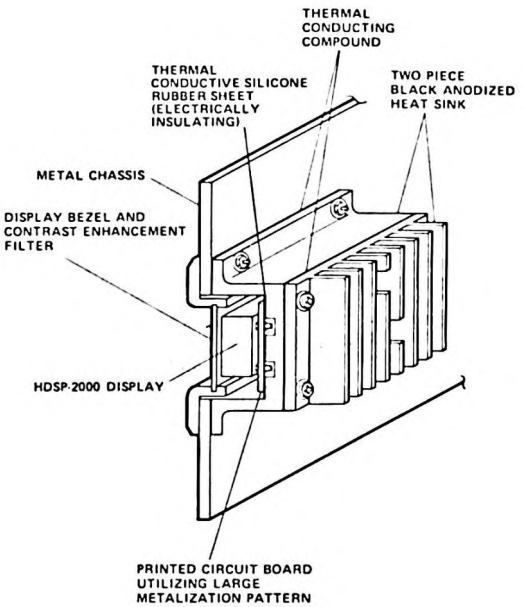


Figure 27. Two-Part Heat Sink for the HDSP-2000

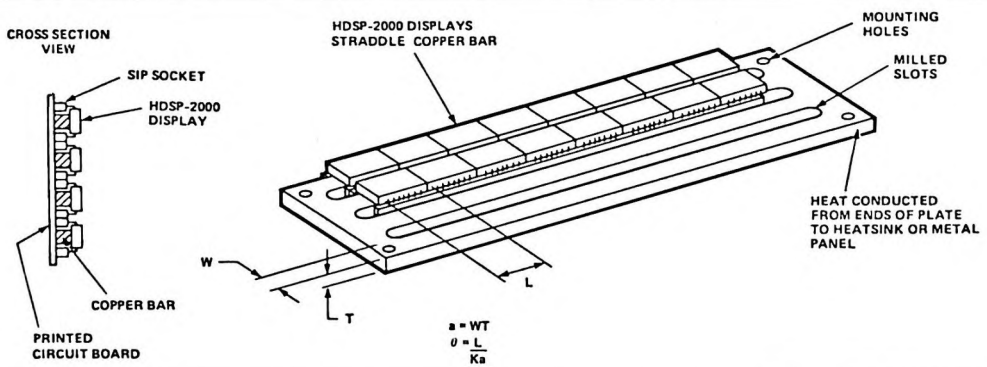


Figure 28. Multiline HDSP-2000 Heat Sink

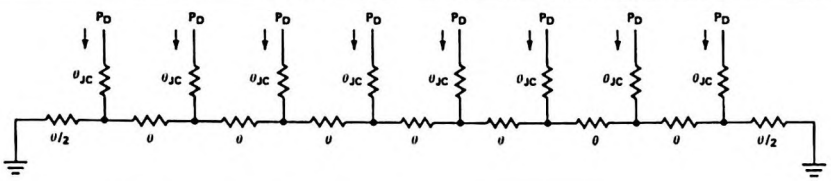


Figure 29. Thermal Resistance Model for Multiline HDSP-2000 Heat Sink

For display strings of an even number of n displays, the case temperature of the center-most displays can be calculated as

$$T_C = (n^2/8)\,\Theta P_D + T_A \quad (26)$$

The effectiveness of this type of heatsink can be determined by calculating the thermal resistance of each section of bar under each display

$$\Theta = \frac{L}{Ka} \quad (27)$$

where

L = length of bar under each display, mm
K = thermal conductivity of bar, W/mm°C (0.3937 W/mm°C for copper)
a = cross sectional area of bar, mm²

If the displays are mounted in a strip socket such as the Robinson Nugent SB-25-100-G socket, then the bar cross sectional area could be 6.35 mm (0.25") thick times the row-to-row pin spacing of the display minus 2.54 mm (.10"). Thus, Θ can be calculated as shown below:

HDSP-2000 Family

$$\Theta = \frac{17.8\text{ mm}}{(0.3937\text{ W/mm°C})(6.35\text{ mm})(5.08\text{ mm})} = 1.40\text{°C/W} \quad (28)$$

HDSP-2300 Family

$$\Theta = \frac{20.3\text{ mm}}{(0.3937\text{ W/mm°C})(6.35\text{ mm})(3.81\text{ mm})} = 2.13\text{°C/W} \quad (29)$$

HDSP-2490 Family

$$\Theta = \frac{35.6\text{ mm}}{(0.3937\text{ W/mm°C})(6.35\text{ mm})(12.7\text{ mm})} = 1.12\text{°C/W} \quad (30)$$

The T_C and T_J can be calculated for a 32 character HDSP-2000 display with a copper bar mounted under the row of displays for an ambient temperature of 85°C and the operating conditions shown in equations (13), (14), (15), and (16):

$$T_C = 8\,(1.40\text{°C/W})\,(1.12\text{W}) + 85\text{°C} = 98\text{°C} \quad (31)$$

Adding in the junction-to-case temperature rise as shown in equation (22), the T_J can be calculated as:

$$T_J = 98\text{°C} + (20\text{°C/W})\,(1.12\text{W}) = 98\text{°C} + 22\text{°C} = 120\text{°C} \quad (32)$$

INTENSITY CONTROL

An important consideration regarding display intensity is the control of the intensity with respect to the ambient lighting level. In dim ambients, a very bright display will produce very rapid viewer fatigue. Conversely, in bright ambient situations, a dim display will be difficult if not impossible to read and will also produce viewer fatigue and high error rates. For this reason, control of display intensity with respect to the environment ambient intensity is an important consideration. The HDSP-2000 family of displays is ideally suited for wide ranges of ambient lighting since the intensity of these displays can be varied over a very wide dynamic range. The propagation delay between the V_B input and the time that the LEDs turn on or off is under a microsecond, allowing dynamic variations of over 2000 to 1 in display luminous intensity at a 100 Hz refresh rate.

Figure 30 depicts a scheme which will automatically control display intensity over a range of 10 to 1 as a function of ambient intensity. This circuit utilizes a resettable monostable multivibrator which is triggered by the column enable pulse. The duration of the multivibrator output is controlled by a photoconductor. At the end of a column enable pulse, the multivibrator is reset to insure that column current is off prior to the initiation of a new display shift register loading sequence. The output of this circuit is used to modulate either the V_B inputs of the HDSP-2000 displays or the column enable input circuitry. For maximum reduction in display power, both inputs should be modulated.

In the circuit shown in Figure 30, the photocell may be replaced by a 50K Ω potentiometer to allow manual control of display intensity.

Figure 31 shows a manually adjustable dimming circuit that provides a very wide range of display intensity. With a 100 Hz display refresh rate, a 4000 to 1 dynamic range of display intensity can be achieved. The Intersil ICM7555 timer is used as a retriggerable monostable multivibrator. The output of the timer is used to simultaneously pulse width modulate V_B, the display column current, and the display supply current. Initially the 100 pF capacitor is held discharged by the timer. At the negative transition of the trigger input the timer would normally allow the capacitor to charge, however the 2N3906 transistor keeps the capacitor discharged until the trigger input goes high. As soon as the trigger input goes high, the capacitor is charged by a constant current source formed by the RCA CA3084 transistor array. As soon as the voltage across the capacitor reaches 2/3 V_{CC} the output of the timer goes low, and the timer discharges the capacitor. The 2N3906 transistor always discharges the capacitor when the trigger is low, therefore the output of the timer stays high if the voltage across the capacitor never reaches 2/3 V_{CC}. For the values shown, t can be varied exponentially from .5 μs to about 1900 μs. Since Q1 and Q2 are monolithic transistors, t is relatively independent of temperature.

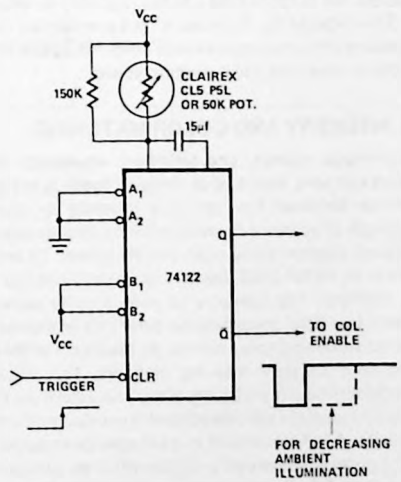


Figure 30. Intensity Modulation Control Using a One Shot Multivibrator

APPLICATIONS

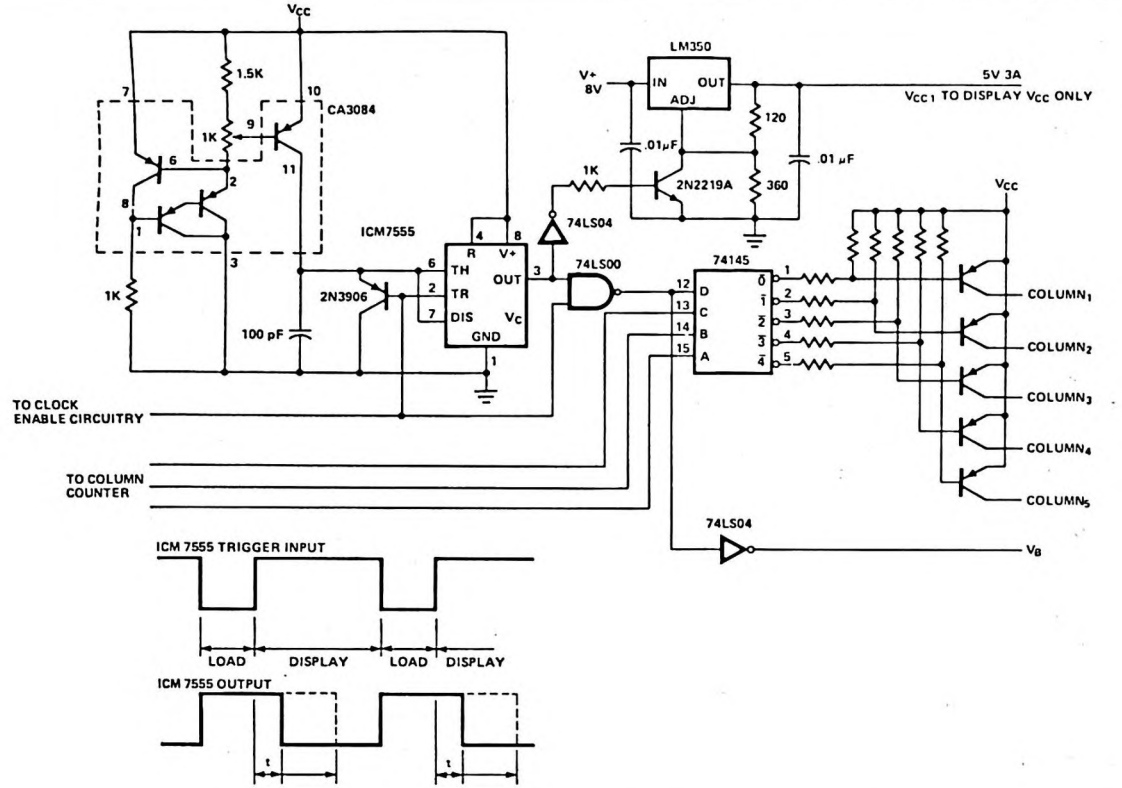


Figure 31. Wide Range Intensity Modulation Control and Power Switching of Display I_{CC} to Conserve Power

Figure 31 also shows a circuit to switch V_{CC} of the displays off during the time that the display is blanked. When the 2N2219A transistor is off, the LM350 provides a regulated 3A 5V output. However, when the 2N2219A transistor is turned on, the output of the LM350 regulator is reduced to 1.2V. This reduces I_{CC} to under 10 mA per display. Capacitive loading of the regulator should be minimized as much as possible to maximize the switching speed.

THE INTENSITY AND COLOR MATCHING

The luminous intensity and dominant wavelength of LED displays can vary over a wide range. If there is too great a difference between the luminous intensity or dominant wavelength of adjacent characters in the display string, the display will appear objectionable to the viewer. To solve the problem, all HDSP-2000 displays are categorized for luminous intensity. The category of each display package is indicated by a letter preceding the date code on the package. When assembling display strings, all packages in the string should have the same intensity category. This will insure satisfactory intensity matching of the characters. All HDSP-2000 family displays are categorized in overlapping intensity categories. All characters of all packages designated to be within a given letter category will fall within an intensity ratio of less than 2:1. For dot matrix displays, a character-to-character intensity ratio of 2:1 is not generally discernable to the human eye.

Since the human eye is very sensitive to variations in dominant wavelength in the yellow and green region, all yellow and green HDSP-2000 family displays are also categorized for dominant wavelength. The dominant wavelength bin for each display package is indicated by a number code following the category letter code on the back of the package. The dominant wavelength bins are 3.5 nm wide for yellow and 4.0 nm wide for green. These dominant wavelength variations are generally not discernable by the human eye.

CONTRAST ENHANCEMENT

Another important consideration for optimum display appearance and readability is the contrast between the display "ON" elements and the background. High contrast can be achieved by placing a filter over the display. The filter, if properly chosen, will transmit the luminance of the light emitting elements while attenuating the luminance of the background.

Filter choice is dependent upon the LED display package, ambient lighting conditions and the desired front panel appearance. For alphanumeric displays in indoor lighting ambients a plastic or glass wavelength filter can be used. In sunlight ambients a neutral density circular polarizer sandwiched between two pieces of optically coated glass is recommended. Figure 32 lists the filter materials recommended for each particular display color. For further information please see Application Note 1015 on Contrast Enhancement for LED Displays.

Display Color	Ambient Lighting		
	Dim	Moderate	Bright
HDSP-2XX0 Standard Red	Homalite H100-1650 3M Panel Film R6510 Panelgraphic Dark Red 63 Ruby Red 60 Chequers Red 118 Rohm & Haas 2423	Homalite H100-1266 Gray H100-1250 Gray H100-1230 Bronze Rohm & Haas 2074 Gray 2370 Bronze	
HDSP-2XX1 (Yellow)	Homalite H100-1726 H100-1720 3M Panel Film A5910 Panelgraphic Yellow 27 Amber 23 Chequers Amber 107	Polaroid HNCP37 3M Light Control Film N00220 Panelgraphic Gray 15 Gray 10 Chequers Gray 105	
HDSP-2XX2 (HER)	Homalite H100-1670 3M Panel Film R6310 Panelgraphic Scarlet Red 65 Chequers Red 112		Polaroid HNCP10
HDSP-2XX3 (HP Green)	Homalite H100-1440 H100-1425 Panelgraphic Green 48 Chequers Green 107		

Figure 32. Contrast Enhancement Filters

HEWLETT PACKARD

APPLICATION NOTE 1017

LED Solid State Reliability

INTRODUCTION

The light emitting diode display technology offers many attractive features. Among them are ability to display information in red, yellow, green, or any combination of these colors; high performance devices readable in direct sunlight; and continuously variable intensity adjustment. One of the most common reasons that LED displays are designed into an application, however, is the high level of reliability of the LED display. Hewlett-Packard has taken a leadership role in setting reliability standards for LED displays and documenting reliability performance.

Reliability data is instrumental in choosing a device package and optimizing the performance of that device. This application note explains how to use the reliabilty data sheets published for Hewlett-Packard LED indicators and displays.

The note begins with a description of LED indicator and display packages. Device failures are defined and explained. The parameters affecting useful life failure rate and mechanical test performance are discussed. As an example, the reliability of an LED display system is calculated.

HP Indicator and Display Packages

Hewlett-Packard has a wide variety of indicator and display components. Indicator products include solid state lamps, light bar annunciators, and bar graph arrays. Display products include numeric and alphanumeric devices.

Many LED devices have similar packaging and construction. T-1 3/4, T-1, rectangular, and subminiature LED lamps are epoxy encapsulated packages. Construction features of the T-1 3/4 lamp are illustrated in Figure 1. Hermetic LED lamps are air-gap devices, assembled in a TO-46 package.

Large seven segment numeric displays, light bars, and bar graph arrays are called stretched-segment packages. These devices are manufactured using the concept of stretching the light from an LED by diffusion and reflection. The LED chips are mechanically supported and electrically connected by a lead frame. The plastic housing, called a "scrambler", contains reflective cavities which act as light pipes. These cavities are filled with a diffusant loaded epoxy to provide uniform illumination at the emitting surface. Figure 2 illustrates the construction of a bar graph array.

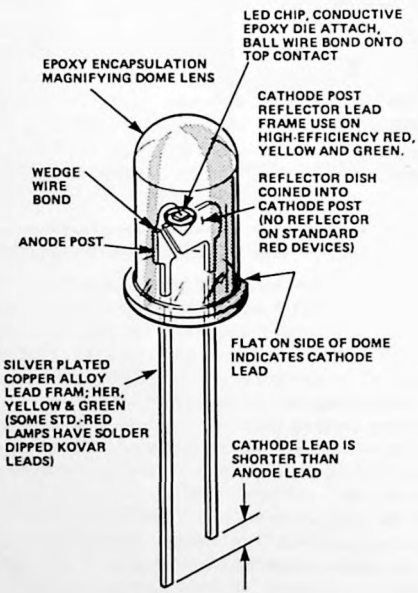


Figure 1. Construction Features of T-1 3/4 Plastic LED Lamp

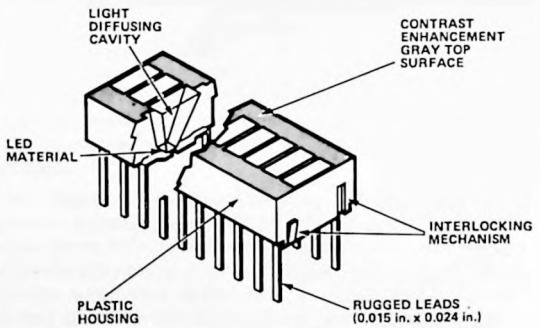


Figure 2. 10 Element Bar Graph (Cutaway)

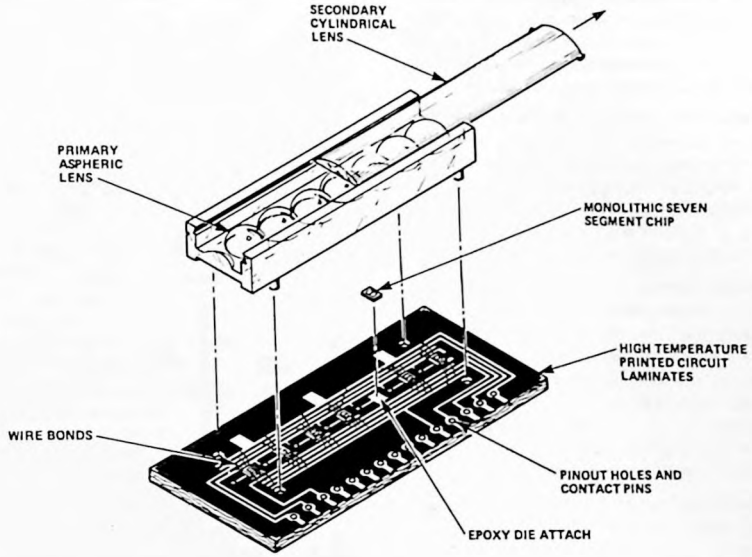


Figure 3. Mechanical Construction of a Monolithic Display Constructed on a PC Board with a Non-Immersion Lens

Monolithic displays include bargraph, numeric, and alphanumeric devices. Individual light emitting segments are formed by diffusing separate LED junctions into a single chip. In most cases, the monolithic display is magnified by an external lens. Monolithic displays can be classified into two basic categories according to whether the lens is of the immersion or non-immersion type. Immersion lenses are formed by molding an epoxy lens directly over the LED chip. Non-immersion lenses have a layer of air between the LED chip and the separately cast epoxy lens. Construction features of a monolithic display with non-immersion lens is shown in Figure 3.

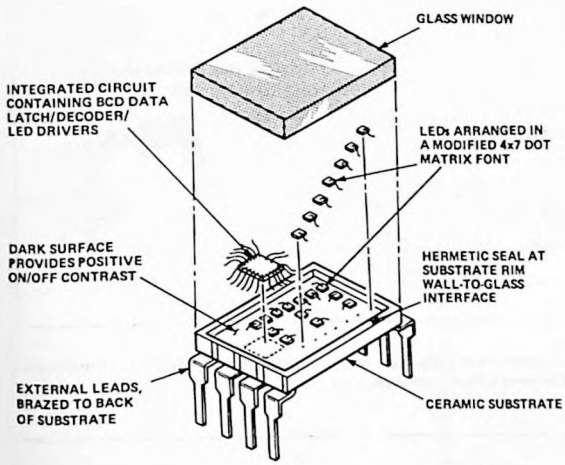


Figure 4. Construction Features of a Hermetic OBIC LED Display

Hewlett-Packard's dot matrix numeric displays have a modified 4x7 dot matrix font. This font allows both decimal numeric and hexadecimal devices. These devices feature an on-board integrated circuit (OBIC) which functions as a latch/decoder/driver. Construction features of the hermetic dot matrix numeric device are shown in Figure 4. In addition to the hermetic package, epoxy sealed and epoxy encapsulated packages are available for the dot matrix numeric displays.

The dot matrix alphanumeric display was designed by Hewlett-Packard to provide a high resolution information display subsystem. Each character of the four character package consists of a 5x7 array of LEDs which can display a full range of alphanumeric characters and other symbols (see Figure 5). Hewlett-Packard dot matrix alphanumeric displays provide on-board storage of decoded data plus constant current sinking drivers for each of the 28 rows in the four character display. These hermetic and epoxy sealed displays have construction features similar to the dot matrix numeric devices.

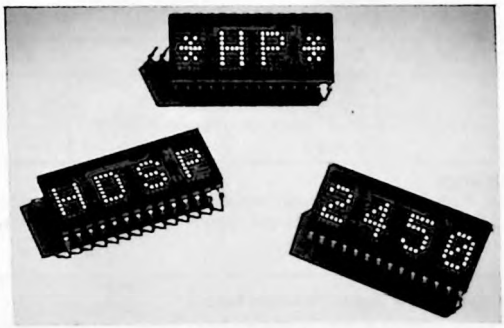


Figure 5. HDSP-2450 Series of Hermetic, Extended Temperature Range 5x7 Alphanumeric Displays

APPLICATIONS

LED FAILURE RATE CHARACTERISTICS

Failure is defined as termination of the capability to perform intended functions. An understanding of how LED displays fail is essential to improving the reliability of the displays as well as that of the systems in which they are used.

LED devices can experience either parametric or catastrophic failure modes. A parametric failure occurs when the device fails to meet data sheet electrical or optical specifications. A parametric failure will not generally cause display system failure with typical drive circuits. Intensity degradation is an example of a parametric failure mode and is discussed later in this application note.

Catastrophic failures are defined as parameters exceeding data sheet limits to a degree which would cause display system failure. Catastrophic failures in lamps, stretched segment, and monolithic displays result in dim or unlit LEDs. The cause or failure mechanism for dim or unlit LEDs can be defective wire bonds, lifted LED die, cracked, or chipped LEDs. Failure mechanisms in dot matrix displays also include IC failures which result in incorrect font or input/output lines which do not meet electrical specifications.

Failure rate can be defined as the percent device failures per unit time of operation. Mean time between failure, MTBF, is simply the reciprocal of failure rate and is expressed in hours. Operating life of an LED display can be divided into three time periods each with a characteristic failure rate. Figure 6 shows the burn-in period, useful life period, and wearout period of operating life. During the burn-in or infant mortality period, failure rate decreases as weak components fall out.

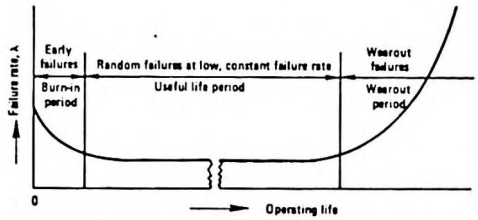


Figure 6. Typical Failure Rate Curve

During the useful life period which follows, failures occur at a low, constant rate. The failures that do occur are truly random and cannot be prevented by additional testing or burn-in of the components. Figure 7 presents useful life failure rates representative of LED lamps, stretched segment, monolithic, dot matrix numeric, and dot matrix alphanumeric displays. The format of Figure 7 is identical to the "Life Test" section of Hewlett-Packard's Reliability Data Sheets. The test conditions represent maximum allowable stress in order to generate worst-case failure rates. Total hours tested is the product of units tested times test hours/unit. The point failure rate is simply the number of failures divided by the total device hours. Units for failure rate are percent failures per 1000 hours of operation. If no failures occur during testing, the point failure rate is calculated assuming one failure.

Device	Description	Test Conditions[1]	Units Tested	Total Hours	Failed	Point Failure Rate % per 1K Hrs.[2]	90% Confidence Failure Rate % per 1K Hrs.[2]
HLMP-3750	Lamp	$T_A = 55°C$ I_F = Max.	16,270	17,275,630	1	0.006	0.023
HDSP-4830	10 Element Bar graph	$T_A = 55°C$ I_F = Max. All Seg. On	410	2,080,856	0	0.048	0.111
HDSP-6508	Monolithic Alphanumeric 8 Character Display	$T_A = 55°C$ I_F = Max. $P_{avg} = \frac{123\ mW}{Char}$	223	884,000	0	0.113	0.260
4N51	Dot-Matrix Numeric	$T_A = 100°C$ Numeric Cycle $V_{CC} = 5.0V$	576	806,000	0	0.124	0.285
HDSP-2000	Dot-Matrix Alphanumeric Four Character Display	$T_A = 70°C$ $V_{CC} = V_b = 5.25V$ $V_{col} = 3.5V$ $P_{avg} = \frac{210\ mW}{Char}$	360	870,000	3	0.345	0.768

NOTES:
1. T_A is ambient temperature during testing. I_F is the average forward current per LED. V_{CC} is the supply voltage. 5.25V is maximum recommended blanking input voltage, V_b. 3.5V is maximum recommended column voltage, V_{col}.
2. Failure rate per package.

Figure 7. LED Useful Life Failure Rates

Reliability data sheets specify 90% confidence level failure rate in addition to point failure rate. LED displays like other semiconductor devices have extremely low failure rates during useful life. As a result, very few device failures are experienced during reliability testing. Statistics tell us that the more device failures that can be generated during reliability testing, the closer the experimental failure rate is to the true device population average failure rate. For instance, if no device failures are generated during reliability testing, the true device failure rate may be very different than the point failure rate. The 90% confidence level failure rate means there is a 90% probability that the actual failure rate of a device will be better than the stated value. Hence, the 90% confidence level failure rate gives more confidence in reliability calculations than the point failure rate. The 90% confidence level failure rate is based on the statistics of the distribution of failures. The assumed distribution of failures is exponential versus time. This particular distribution is commonly used in describing useful life failures in LED devices and other semiconductor components.

Figure 7 illustrates that failure rate is related to package design and package complexity. Of the epoxy encapsulated devices, the 10 element bargraphs have a point failure rate that is about an order of magnitude larger than LED lamps. However, the HDSP-4830 10 element bar graph array has 10 times as many LED die as the HLMP-3750 lamp. The 8 character HDSP-6508 air-gap package has a comparable failure rate to the epoxy encapsulated HDSP-4830 though the HDSP-6508 has 144 wire bonds and the HDSP-4830 has 10 wire bonds. The construction of the 4N51 and HDSP-2000 displays yields an impressive useful life failure rate with a comparatively large number of LED die per character. Note that the 4N51 is a single character device while the HDSP-2000 is a four character package.

FAILURE RATE PREDICTION

To obtain useful life failure rates in a reasonable amount of time, a higher-than-normal stress is applied to a sample quantity of devices known to represent the device population. This is known as accelerated life testing. The most common stress factor used is temperature. Failure rate prediction is the estimation of normal operating temperature failure rates based on maximum operating temperature failure rate.

The Arrhenius Model is an experimentally proven mathematical expression for failure rate prediction. The model includes the effect of temperature and the activation energy of a failure mechanism, permitting it to be used to predict failure rates at normal operating temperatures based on tests performed at above-normal device junction temperatures:

$$\lambda_1 = \lambda_2 e^{-\frac{E}{K}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)}$$

where λ_1 = failure rate at junction temperature T_1
λ_2 = failure rate at junction temperature T_2
T = junction temperature in °K
E = thermal activation energy in electron volts (eV)
K = Boltzman's constant (8.617×10^{-5} eV/°K)

Recall that °K = °C + 273

Application of the Arrhenius Model requires calculation of device junction temperature both for the reliability test and for the actual field operating conditions. LED junction temperature is a function of ambient temperature, power dissipated in the junction, and thermal resistance:

$$T = T_A + P_D (R\theta_{J\text{-}A})$$

where T = LED junction temperature in °C
T_A = ambient temperature in °C
P_D = power dissipated in LED junction in watts
$R\theta_{J\text{-}A}$ = thermal resistance junction-to-ambient in °C/W.

Activation energy is a constant which defines the dependence of failure rate on junction temperature for a failure mechanism. Several failure mechanisms exist for LED indicators and displays. Failure rate predictions or Hewlett-Packard's reliability data sheets are conservatively based on a failure mechanism with small activation energy. Using the smallest activation energy for failure rate prediction brings about the largest failure rates at any junction temperature below the tested condition. Interconnection failure mechanisms, such as defective wire bonds, have the smallest activation energy of typical LED device failure mechanisms. MIL-HDBK-217C specifies an activation energy of 0.43eV for interconnection failure mechanisms in hybrid microelectronics. A 0.43eV activation energy is used for failure rate prediction in Hewlett-Packard's reliability data sheets for indicators and displays.

Figure 8 shows the predicted improvement in failure rate and MTBF that can be realized by reducing the junction temperature of the 4N51 series of displays. The failure rate and the MTBF improve by over an order of magnitude as ambient temperature is reduced from 100° C to 30° C.

Ambient Temperature - °C	Junction Temperature - °C	Point	
		MTBF - Hours	Failure Rate/ 1K Hours Operation
100	130	806,000	0.124%
90	120	1,108,000	0.090%
80	110	1,549,000	0.065%
70	100	2,205,000	0.045%
60	90	3,200,000	0.031%
50	80	4,745,000	0.021%
40	70	7,199,000	0.014%
30	60	11,201,000	0.009%

Figure 8. Failure Rate Prediction for LED Dot Matrix Numeric Displays

Reducing the product of power dissipated and thermal resistance can have effects on reliability similar to reducing ambient temperature. Blanking the display wherever possible can reduce junction temperature significantly. Junction-to-ambient thermal resistance is the sum of junction-to-case plus case-to-ambient thermal resistance. Junction-to-case thermal resistance is defined by the display package design and is specified on the device data sheet. The display system designer, however, has control over case-to-ambient thermal resistance. For devices such as lamps, stretched-segment, and monolithic devices, the primary thermal path from the LED junction is through the device cathode leads. Providing a maximum printed circuit board trace width to the cathode lead is one way to reduce thermal resistance in these devices. Heat-sinking the substrate of dot matrix devices is a technique that will improve their reliability.

DISPLAY SYSTEM RELIABILITY

Reliability is defined as the probability that a device will perform its intended function for a specified period of time under stated conditions. When failure rate remains constant, as in the useful life period, display system reliability may be predicted by the exponential distribution:

$$R = e^{-t(\lambda 1 + \lambda 2 + \lambda 3 + \ldots)}$$

where R = reliability or probability of survival
t = mission time or actual utilization time[1]
λ_i = component (i) useful life failure rate

As an example, the useful life reliability of the LED display system in Figure 9 will be calculated. This eight digit numeric display uses Hewlett-Packard's 4N51 series of dot matrix displays. The on-board-integrated-circuitry on these devices minimizes display system component count. On-board circuitry includes a latch, a BCD to dot matrix decoder, and LED drivers.

For this example let us assume that the display system in Figure 9 will be operational 8 hours/day and 5 days/week for 5 years. Mission time can then be calculated:

$$t = \left(\frac{8 \text{ hrs.}}{\text{day}}\right)\left(\frac{5 \text{ days}}{\text{week}}\right)\left(\frac{52 \text{ weeks}}{\text{year}}\right)(5 \text{ years})$$

$$t = 10.40\text{K hrs.}$$

Let us also assume that the display system will be used in ambient temperature of 55° C. The next step is to calculate the sum of the individual component failure rates. From Figure 8 the point failure rate for each of the 4N51 series displays is 0.026% per 1000 hours of operation at 55° C ambient. Point failure rate for each of the LSTTL components is .007% per 1000 hours of operation.[2] Point failure rate for the microcomputer is .043% per 1000 hours of operation.[3] The sum of individual component failure rates, λ_{total} is then:

$$\lambda_{total} = (.043\%/1\text{K hrs.}) + 2(.007\%/1\text{K hrs.}) + 8(.026\%/1\text{K hrs})$$

$$\lambda_{total} = .265\%/1\text{K hrs.}$$

The probability of survival of the 8 digit LED display system is then:

$$R = e^{-t(\lambda_{total})} = 97\%$$

[1]Mission time cannot exceed the useful life of any component when calculating system reliabilty.
[2]1981 cumulative data for LSTTL components from Texas Instruments. A .43 eV activation energy is assumed.
[3]Data taken from Intel reliability report RR-25, December, 1979. A .3 eV activation energy is assumed.

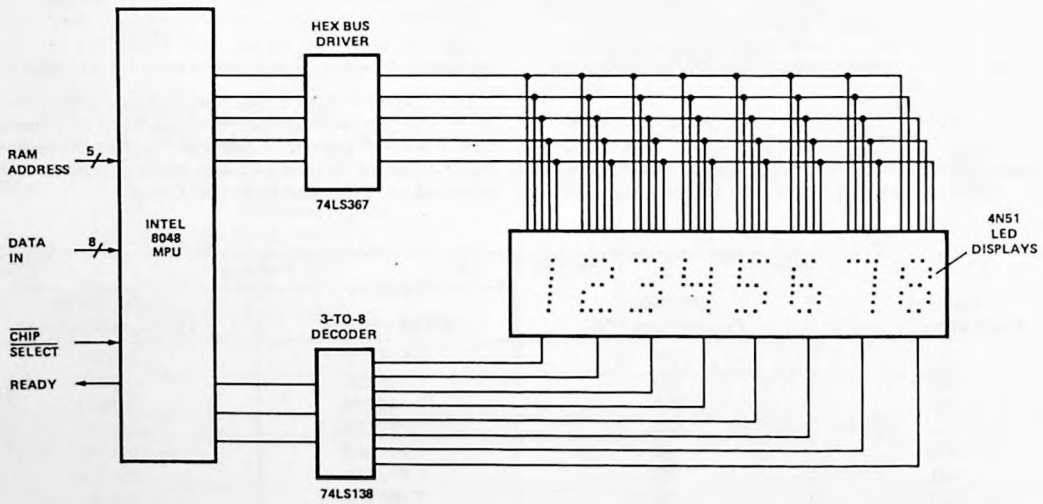


Figure 9. 4N51 Display System

INTENSITY DEGRADATION

Intensity degradation is a long term wearout mechanism in LED displays. Hewlett-Packard defines a 50% reduction in intensity as a parametric failure mode. A 50% change in intensity is one that the human eye can easily recognize. Figure 10 presents normalized luminous intensity vs. stress time for red LED displays. Figure 10 represents averaged data because the rate of intensity degradation is not identical for all LEDs. The logarithmic stress time axis implies that the rate of intensity degradation decreases as time increases. Even curve D, which represents operation at 200% of maximum ratings, does not bring about noticeable degradation after 10,000 hours stress time. Curves A and B indicate that increased current density results in more rapid degradation. Curves B and C indicate that junction temperature has little effect on rate of degradation. Curve C represents degradation at absolute maximum drive levels. Curves A through D are for direct drive of LEDs. Strobed operation brings about approximately equal rates of degradation for equal average currents. When Hewlett-Packard displays are driven at maximum rated current, the rate of high efficiency red and green degradation is about the same as the rate of red. Yellow degradation is about two times the rate of red.

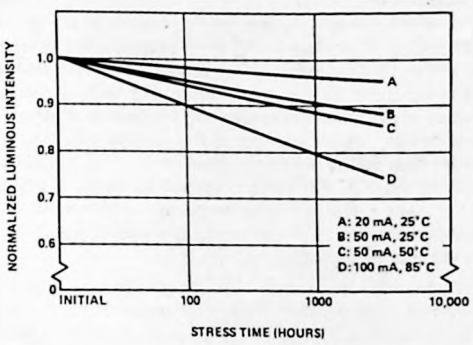


Figure 10. Intensity Degradation vs. Stress Time

MECHANICAL AND ENVIRONMENTAL TESTS

Reliability data sheets for Hewlett-Packard's standard products include life test data, failure rate prediction, mechanical, and environmental test performance. Tests are performed in accordance with the latest revisions of MIL-STD-750 and MIL-STD-883. Mechanical and environmental test data for the Hewlett-Packard 5082-7350 dot matrix numeric display is given in Figure 11. The 5082-7350 is an epoxy sealed, air-gap package.

Mechanical tests are performed to insure package integrity. Solderability determines the ability of the device to be soldered via conventional techniques. With no preparatory cleaning the device leads are immersed in flux for 5 to 10 seconds, then into molten solder which has been stabilized to 260° C. After immersion in a solder bath for the specified time and cooling for 5 minutes, devices are examined using 10X magnification. Pinholes and voids must not be concentrated in one area and must not exceed 10% of the total area

Test	MIL-STD-883 Reference	Test Conditions	Units Tested	Total Failed
Solderability	2003	Sn 60, Pb 40 Solder at 260° C for 5 sec.	25	0
Temperature Cycling	1010	500 cyc., -55 to 100° C electrical & leak failures	45	0
Thermal Shock	1011	50 cycles, 0 to 100° C, 3 sec transfer	25	0
Moisture Resistance	1004	10 days, 90-98% RH, -10 to 65° C, non-op	25	0
Shock	2002	5 blows each X1, Y1, Z1 axis 1500g .5 msec.	25	0
Vibration, Variable Frequency	2007	3, 4 min cycles each X, Y, Z axis at 20g min 20 to 2000 Hz	25	0
Constant Acceleration	2001	20,000 g's, Y1 axis, 1 minute	25	0
Terminal Strength	2004	Condition B2, 3 bends > 15°	25	0
Salt Atmosphere	1009	35° C fog for 24 hours	25	0
Electrostatic Discharge	3015	5 discharges each pin 1000V, 500Ω, 300 pF	5	0

Figure 11. Mechanical Tests 5082-7350 Series Displays

Temperature cycling tests are performed to define a thermomechanical life. Various parts of the optoelectronic device are in contact such as the substrate, LED die, and bond wires. If coefficients of thermal expansion are not well matched, temperature changes are accompanied by physical strain. The magnitude of the physical strain increases as the magnitude of the temperature excursion increases. Probability of failure increases with the number of temperature cycles. Seven segment displays have less than 1% failure after 500 cycles from -40 to +85° C. Air-gap packages such as the 5082-7350 offer improved temperature cycling performance over epoxy encapsulated displays. With no encapsulant epoxy, there is less physical strain on wire bonds and die attachments.

The thermal shock test exposes devices to alternate extremes in temperature. Parts are transfered from liquid at 0° C to liquid at 100° C. Airgap packages can withstand a larger number of thermal shocks than epoxy encapsulated devices.

If the device package material is not impervious to the diffusion of water vapor, long term exposure to high humidity will eventually subject the active elements to high humidity. Humidity can lead to failure from corrosion of the active elements or from increased surface leakage currents. The moisture resistance test achieves accelerated effectiveness through temperature cycling. Temperature cycling provides alternate periods of condensation and drying which accelerate the development of corrosive processes.

Hermetic LED displays are packaged using a glass to metal or glass to ceramic seal. These products are impervious to moisture and meet hermeticity testing to prescribed levels. In addition, Hewlett-Packard makes displays which have an epoxy seal such as the 5082-7350 and the dot matrix alphanumeric displays. These displays are also capable of passing fine and gross leak hermeticity tests.

The shock test determines the ability of LED components to withstand shock of the same severity as that produced by collision impacts, near-miss gunfire, or underwater explosions. A 1500 G shock would be approximately equal to the shock that a device would experience if it were mounted to a rigid, 40 pound enclosure and dropped from three feet onto a concrete floor.

Vibration and acceleration tests expose parts to the predominant frequency ranges and magnitudes that may be encountered during field service.

In addition to standard LED display products, Hewlett-Packard offers a high-reliability product line. Special electrical and mechanical testing is performed on standard Hewlett-Packard displays to comply with the requirements of the U.S. Military qualified parts list, Hewlett-Packard defined specifications, or customer defined specifications. The special testing can be performed on a lot qualification basis, 100% screen, or a combination of lot qualification and 100% screen. Based on estimates in MIL-HBDK-217C, lot qualification testing can improve useful life failure rates by as much as five-fold. One hundred percent screening is designed to eliminate infant failures.

Display components can have significant impact on the reliability of an electronic system. System reliability is a function of the sum of individual component failure rates. It takes a combination of good design, quality pieceparts, and tightly controlled production processes to yield reliable display components. Components which appear to have the same design may have very different mechanical and operating life performance characteristics. Hewlett-Packard has reliability data sheets available for indicator and display products from your local field sales office.

HEWLETT PACKARD

APPLICATION NOTE 1018

Designing with the HCPL-4100 and HCPL-4200 Current Loop Optocouplers

PREFACE

Hewlett-Packard produces a comprehensive line of optocouplers which address different speed and current gain requirements for isolation interface circuits. New Hewlett-Packard optocoupler products build on the established base of optocoupler technology and expand with additional features that make optocouplers easier to use in special applications. The HCPL-4100 (transmitter) and the HCPL-4200 (receiver) optocouplers include specialized circuits for 20 mA digital current loop applications. These optocouplers are designed to easily interface TTL, LSTTL, and CMOS logic systems to current loop systems. An external current source is needed to complete the current loop system.

This application note will assist the circuit design engineer to achieve maximum performance from Hewlett-Packard HCPL-4100 and HCPL-4200 current loop optocouplers. Practical applications for interfacing to and from a current loop will be shown. In addition, overall current loop system aspects and current source designs will be discussed. Potential applications of current loops, configurations, types of current sources, and inherent tradeoffs between data rate and length of wire line are covered.

INTRODUCTION

Data transmission between electronic equipment, which are physically separated by distances of more than a few feet, can be accomplished in many ways. Wire links, microwave links, and fiber optic links are among the most common means. Each technology has inherent trade-offs in data rate, error rate, simplicity of use, reliability and cost. Of the wire techniques, a signal can be transmitted as a voltage signal or a current signal. Many popular industry standards exist for voltage signal transmission, such as RS-232-C, RS-422, RS-423 (serial data transmission), or IEEE-488 (parallel data transmission), etc. When compared to these voltage signal techniques, a current signal or current loop can provide an excellent alternative.

First, some basic definitions are in order. A current loop is a loop which carries a current, generally 20 mA or 60 mA, between electronic equipment via a twisted pair of wires. The loop can be opened and closed by a transmitter within equipment connected to the loop. These interruptions of current are sensed by other equipment connected to the current loop (receiver). The convention used in this application note for a MARK, or logic 1, corresponds to a presence of loop current, e.g., 20 mA. A SPACE, or logic 0, corresponds to an absence of loop current, e.g., 0 mA. A current loop transmitter or receiver can be either of two types: active (source) or passive (sink). An active transmitter supplies current to the loop. Any receivers or other transmitters within that loop must then be passive units which accept the supplied loop current. Alternatively, an active receiver supplies current to passive transmitters or other passive receivers in the current loop.

Current sources used within a current loop vary in complexity. The simplest current source is a resistor and voltage source. More complex current sources will contain active elements or special integrated circuits to provide constant current under various power supply and load conditions. The compliance voltage of a current source is a term which is used to indicate at what level the current decreases to zero.

There are no widely accepted industry standards for current loops, only accepted conventions. Common digital current loops are 0-20 mA and 0-60 mA, while the analog current loop is 4-20 mA. These levels were originally associated with digital teleprinter equipment and analog industrial sensors such as thermocouples, strain gauges, etc. The HCPL-4100 and HCPL-4200 optocouplers address only the 20 mA digital current loop applications.

Basic Advantages of Current Loops

In voltage based transmission lines, a voltage signal attenuates over distance. A current loop design ensures constant current through the loop resulting in no signal attenuation. Noise immunity is higher with current loop systems. A constant current maintains a high signal-to-coupled noise ratio. The voltage signal attenuation reduces this ratio.

Even with expensive, low capacitance cable, RS-232-C wire communication over distances greater than 60 m (200 ft.) at 20 kBd is impractical. RS-232-C wire distances are severely limited when compared to current loop distances

APPLICATIONS

at the same operating data rate. Current loop systems employ inexpensive twisted pair wire cable. Serial data transmission is accomplished by a simple two-wire arrangement. Multiple stations can be connected in series provided sufficient compliance voltage is available. Unlike voltage techniques, if a fault should open the loop, permanent loop current disruption could be sensed.

Optocouplers can be used in current loops to provide optical isolation of the logic circuits from the current loop circuit. This optical isolation prevents ground potential differences or common mode influences from affecting the current loop performance. Optocoupler construction and sophisticated integrated circuit processing achieve excellent common mode rejection (10 kV/μs). Electrical independence between input and output circuits of an optocoupler permit different reference grounds on either side of the interface.

The maximum data rate of a 20 mA current loop system is determined by the characteristics of the transmitter and receiver and the length and characteristics of the transmission line. For short transmission lines, less than 40 m (131 ft.), the maximum data rate is approximately 120 kBd for the HCPL-4100 and approximately 4.5 MBd for the HCPL-4200.

The small eight pin dual-in-line plastic package results in a savings of printed circuit board space. Standard automatic insertion equipment can be used.

The easy design and implementation of a 20 mA current loop using the HCPL-4100 and HCPL-4200 permits rapid design, fabrication, and testing.

CURRENT LOOP APPLICATIONS

Current loops are used because they offer communications link lengths up to 10 km, have high immunity to errors caused by noise, and are low cost. Previous 20 mA current loop designs were often limited to 5 or 10 kBd speeds even for short line lengths. Hewlett-Packard 20 mA current loop transmitters and receivers are capable of 20 kBd at 400 metres.

In the industrial control industry, current loops are used when there is a need to communicate digital information. Because of the proliferation of the microprocessor and advances in digital circuitry and software, digital control of industrial processes is becoming widely accepted. Micro, mini, and mainframe computers are distributed throughout the factory and need to exchange information. The same considerations apply where distributed data processing equipment is used in a factory environment for inventory control or workflow monitoring. Hewlett-Packard 20 mA current loops are a natural choice for noisy environments.

For these applications, 20 mA current loops are desirable because they are resistant to errors caused by noise, they eliminate ground loops, can be used in communications links up to 10 km long, are low cost, and can be easily installed. No other common communications system can equal these features.

HEWLETT-PACKARD CURRENT LOOP OPTOCOUPLERS

General Design Considerations with Optocouplers

When ordinary optocouplers are used as the interface between logic systems and a current loop, and vice versa, careful design must be followed. The light emitting diode (LED) in a current loop receiver must be protected from current overstress. A threshold needs to be established with hysteresis in order to define the MARK and SPACE conditions and to avoid possible noise effects. The threshold circuit should be located prior to the optical isolation to prevent the current transfer ratio (CTR) changes within an optocoupler over time from influencing established threshold levels. This input protection/threshold circuit should be powered solely by the current loop to maintain isolation and reduce power supply requirements. The receiver output circuit should be simple to interface to TTL or CMOS systems. The total current loop receiver circuit needs to occupy minimal board space within loop station equipment. Of course, the design must have good speed performance in order to meet ever increasing speed requirements.

Similar considerations exist for current loop transmitter design. The transmitter will operate from either a TTL or CMOS input data signal. The output of the transmitter should be protected and buffered to handle the loop current and compliance voltage level of the current source. Output protection needs to be provided to ensure against miswired connection of the current loop to the transmitter terminals. The output circuit must be powered by the current loop source. If power failure occurs to the transmitter, the transmitter must remain ON in order to prevent obstruction of data on the current loop. Other subtle effects such as the type of current source and termination used will also influence speed performance of the loop.

These design considerations have been incorporated into the HCPL-4100 and HCPL-4200 to simplify the circuit designer's task.

Features Common to the HCPL-4100 (Transmitter) and the HCPL-4200 (Receiver)

The Hewlett-Packard current loop optocoupler product family consists of two devices: a current loop transmitter (HCPL-4100) and a current loop receiver (HCPL-4200). Their unique characteristics will be explained by first discussing the features which are common to both devices; then particular characteristics of each device will be addressed.

Optical isolation is provided within each device to permit electrical independence of the logic systems from the current loop system. Electrical independence specifically means two concepts: 1. signal isolation capability between the two sytems, 2. insulation capability between the two systems. Signal isolation is the ability of the device to reject common mode signal interference. The common mode rejection capability of both the HCPL-4100 and the HCPL-4200 is typically 10 kV/μs with a specified minimum of 1000 V/μs. The device insulation capability is the ability to withstand a transient potential difference stress between the two systems. The Withstand Test Voltage is 3 kV DC for five seconds.

Speed performance of each device has a typical propagation delay of 0.2 μs — 0.3 μs with a specified maximum of 1.6 μs over 0°C to 70°C, excluding transmission line delay. Depending upon the location of the current source within a loop, data rates of 1.5 MBd for 250 metres loop length is achieved with the HCPL-4200 receiver. Up to 75 kBd for 100 metres of loop length with the HCPL-4100 transmitter is also achieved.

The transmitter input and receiver output are compatible with TTL, LSTTL and CMOS logic levels. Passive current

loop switching or monitoring is performed by integrated circuits (ICs) within each device which are powered from an external 20 mA current source. No additional design for power supplies or buffer circuitry is needed for either unit. Current protection of up to ±30 mA is provided in each optocoupler. Specific, simple current sources which can be used are explained in a subsequent section.

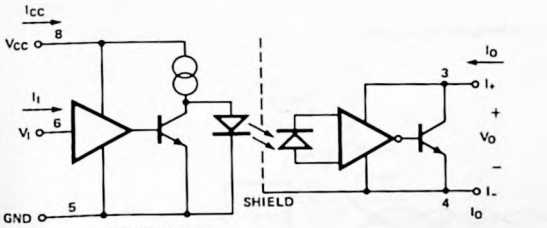
The HCPL-4100 20 mA current loop transmitter and HCPL-4200 20 mA current loop receiver incorporate these features in eight pin dual-in-line plastic packages. The eight pin dual-in-line package allows for automatic insertion capability and conserves printed circuit board space.

Features of the HCPL-4100 Transmitter

The output integrated circuit of the HCPL-4100 transmitter directly controls a recommended 20 mA loop current. The minimum breakdown voltage of this IC, which determines the upper compliance voltage limit of the current source, is 27 V DC. At a recommended loop current of 20 mA, the MARK state voltage drop across the output terminals is typically 2.35 V DC. The SPACE state current level is typically 1.1 mA (maximum 2 mA) which powers the output integrated circuit. Should power fail to the input IC of the HCPL-4100 transmitter, the output IC will remain in the MARK state. This important feature is needed in multidrop current loop applications. A minimum capacitive loading of 1000 pF is required for the output IC (loop side) of the transmitter. This guarantees stability of the IC under all possible load conditions. In general, an external 1000 pF capacitor can be omitted for twisted wire cable lengths greater than 30 metres (100 ft.). If there is any possibility of using a wire loop length less than 30 metres (100 ft.), the 1000 pF capacitor must be connected. Good engineering practice is to use a bypassing capacitor (0.1 μF) from V_{CC} to ground for the input IC of the transmitter. Data from directly connected TTL, LSTTL or CMOS units to the input of the HCPL-4100 transmitter will properly operate this device. A block diagram of the HCPL-4100 is given in Figure 1 and transfer characteristic is illustrated in Figure 2.

Features of the HCPL-4200 Receiver

The HCPL-4200 receiver input IC directly monitors the 20 mA loop current. Power for this IC is supplied by the current loop from the external current source. Loop current level detection is performed prior to the optical isolation.



TRUTH TABLE (POSITIVE LOGIC)*

V_I	V_{CC}	I_O
H	ON	H
L	ON	L
H	OFF	H
L	OFF	H

*CURRENT LOOP CONVENTION – H = MARK: I_O > 12 mA, L = SPACE: I_O < 2 mA.

Figure 1. Block Diagram and Truth Table for HCPL-4100 Optocoupler

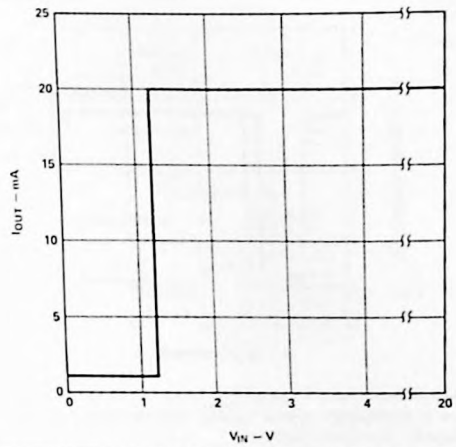
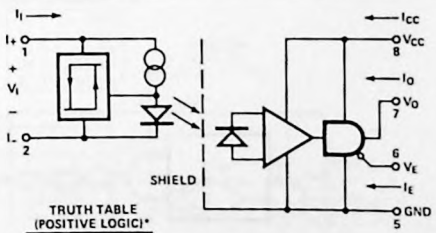


Figure 2. HCPL-4100 Typical Transfer Characteristic. Output Loop Current vs. Input Voltage. MARK State Loop Current Is Provided by External Current Source.

Specified current thresholds are a minimum of 12 mA for MARK state and a maximum of 3 mA for SPACE state. The typical threshold for MARK state is 6.8 mA with 0.8 mA hysteresis. A guaranteed switching threshold level for loop current provides additional common mode and differential mode noise immunity, and prevents possible current transfer ratio (CTR) changes from affecting loop current threshold levels. At the recommended loop current of 20 mA, the MARK state voltage drop across the input terminals is typically 2.52 V DC.

The output integrated circuit of the HCPL-4200 receiver can have a voltage output (V_O) greater than the power supply voltage (V_{CC}). The absolute maximum voltage level for V_O and V_{CC} is 20 V DC. A third state (high impedance) output enable feature is available for use with buss interface applications or special inhibit functions. The output will remain at a high impedance level (third state) if V_{CC} is zero volts. A block diagram of the HCPL-4200 is given in Figure 3 and the transfer characteristic is illustrated in Figure 4. Conventional TTL and LSTTL logic devices can be directly connected to the output of the HCPL-4200 unit. A standard CMOS interface for the HCPL-4200 receiver is given in Figure 5.



TRUTH TABLE (POSITIVE LOGIC)*

I_I	V_E	V_O
H	H	Z
L	H	Z
H	L	H
L	L	L

*CURRENT LOOP CONVENTION – H = MARK: I_I = 12 mA, L = SPACE: I_I = 3 mA, Z = OFF (HIGH IMPEDANCE) STATE.

Figure 3. Block Diagram and Truth Table for HCPL-4200 Optocoupler

APPLICATIONS

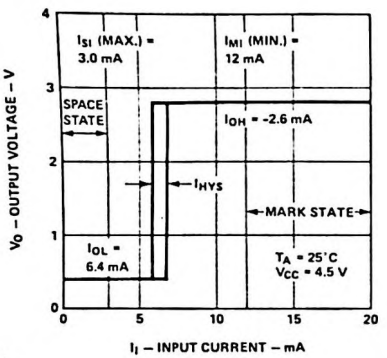


Figure 4. HCPL-4200 Typical Transfer Characteristic. Output Voltage vs. Input Loop Current

CURRENT LOOP CONFIGURATIONS

Current loop configurations can be arranged in three basic ways: simplex, half duplex and full duplex. Two variations within each configuration can exist, i.e., point-to-point or multidrop connections. Definitions for these terms, recommended interface circuits, performance tradeoffs and measured performance data will be discussed and illustrated within this section.

Simplex

The most fundamental loop configuration is simplex point-to-point. The data flows in only one direction from the transmitter over the current loop to the remote receiver. This configuration is shown in Figures 6a and 6b. Figure 6a illustrates a non-isolated, active current loop transmitter used with an isolated HCPL-4200 receiver. Figure 6b shows an isolated HCPL-4100 current loop transmitter used with a non-isolated, active receiver. A possible point-to-point application is to use a 20 mA current loop for communication between a computer and remote printer. The simplex topology can be expanded from point-to-

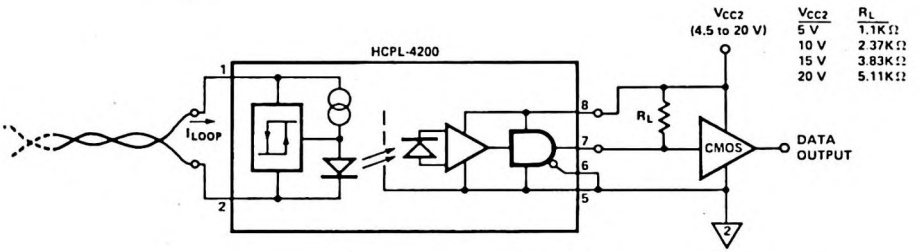
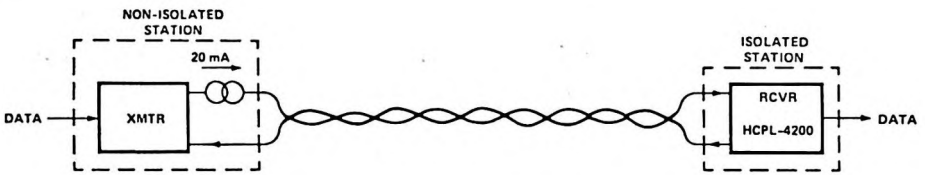
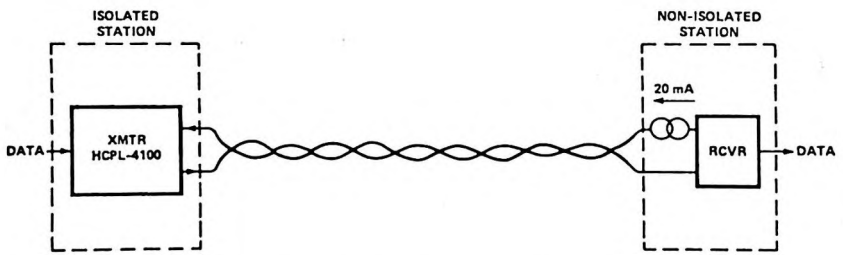


Figure 5. Recommended Interface from HCPL-4200 Receiver to CMOS Circuit

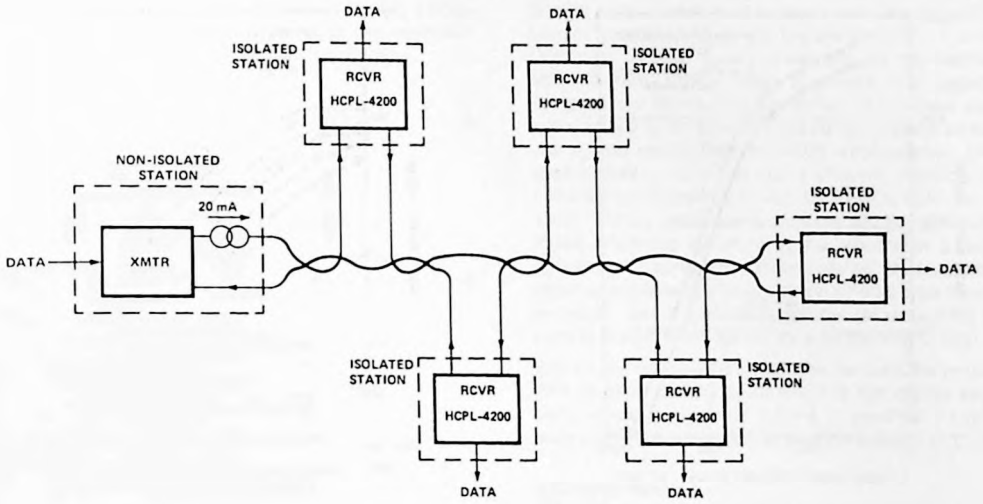


a. Simplex, Point-to-Point with Isolated Receiver



b. Simplex, Point-to-Point with Isolated Transmitter

Figure 6. Simplex Current Loop Configurations: Point-to-Point with Current Source Located at: a. Transmitter, b. Receiver; c. Multidrop



c. Simplex, Multidrop with Isolated Receivers

Figure 6. Simplex Current Loop Configurations: Point-to-Point with Current Source Located at: a. Transmitter, b. Receiver; c. Multidrop

point to multidrop. In a multidrop system, a number of receivers are in series on the loop which contains only one transmitter as illustrated in Figure 6c. A configuration with multiple transmitters and one receiver is possible as well. However, the priority of the operating transmitter must be established in that case.

Undesired ground loops are eliminated and common mode rejection is increased by providing electrical isolation of the current loop. This isolation can be provided at either the receiver or transmitter end of the loop as illustrated in Figures 6a and 6b respectively. The opposite end need not be isolated. The non-isolated unit will supply the current (active) for this simplex configuration. A circuit diagram of a non-isolated, active transmitter connected to the HCPL-4200 receiver (Figure 6a) is given in Figure 7. The data rate performance versus the length of the current loop for this circuit is given in Figure 8.

The circuit for the alternate simplex arrangement of a non-isolated, active receiver connected to the HCPL-4100 transmitter is given in Figure 9. The trade-off of data rate versus loop length and compliance voltage is illustrated in Figure 10.

Comparing the data rate performance for each circuit shows that the active, non-isolated transmitter configuration is faster by a factor of 11 at 1000 metres (3281 ft.) of loop distance.

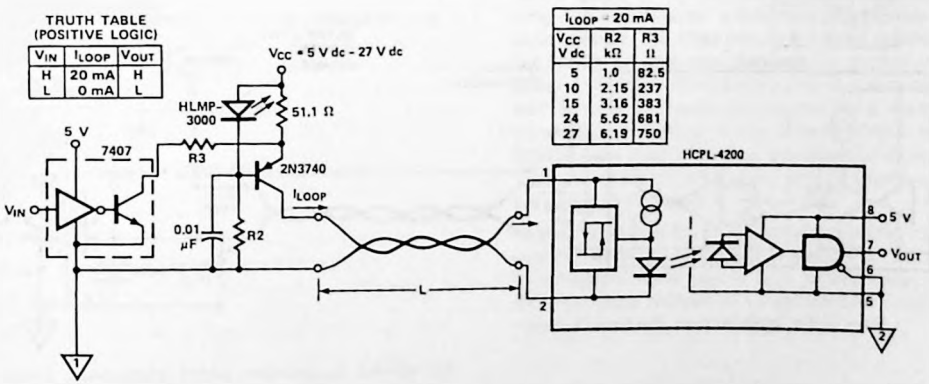


Figure 7. Recommended Non-Isolated Active Transmitter with HCPL-4200 Isolated Receiver for Simplex Point-to-Point 20 mA Current Loop

APPLICATIONS

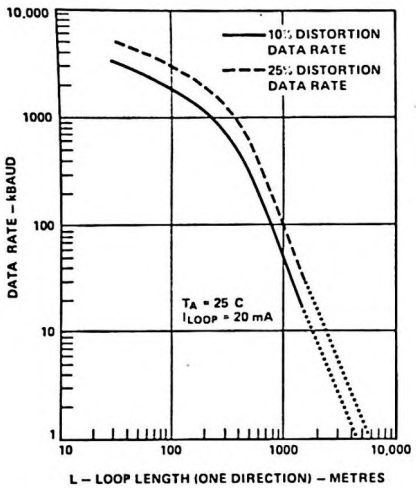


Figure 8. Typical Data Rate vs. Distance for Circuit of Figure 7

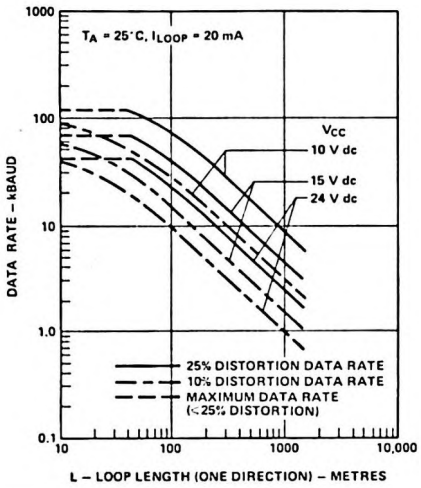


Figure 10. Typical Data Rate vs. Distance and Supply Voltage for Circuit of Figure 9

The design and location of the current source determine loop length and data rate performance. In both simplex configurations, the current source compliance voltage can be much lower than the HCPL-4100 device maximum of 27 V. However, limitation on the length of the loop (DC resistance) and data rate capability would dictate a minimum V_{CC} which can be used for the current source. With a 24 V ±10% power supply, multidrop applications for very long loop lengths (>3 km) can be done. Device performance as a function of current source design is covered in a later section.

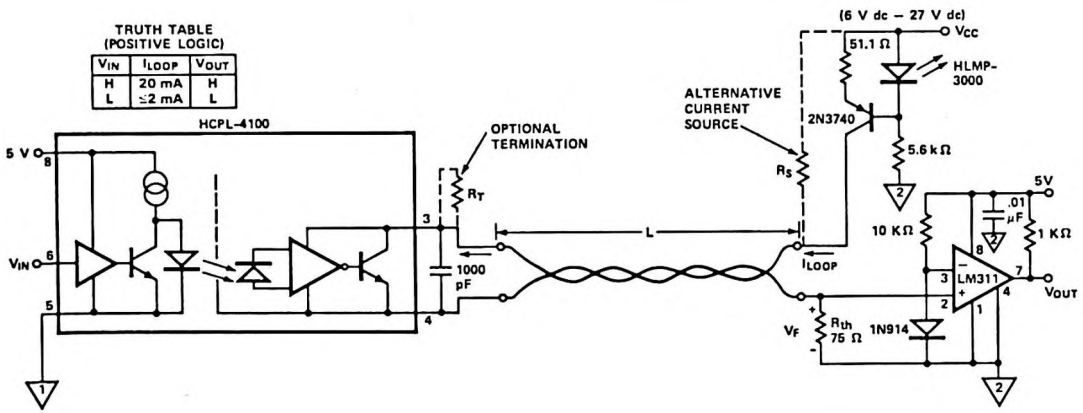


Figure 9. Recommended Non-Isolated Active Receiver with HCPL-4100 Isolated Transmitter for Simplex Point-to-Point 20 mA Current Loop

DC Performance

By summing the MARK state voltage drops around the current loop, a basic equation is derived for DC performance for the loop. This is expressed as the maximum distance over which a current loop can be operated.

$$L = \frac{V_{COMP} - \Sigma V_{RCVR}{}_{MARK} - \Sigma V_{XMTR}{}_{MARK}}{2\, I_{LOOP} R_{LINE}} \quad (1)$$

Where

L = Length of wire in one direction

V_{COMP} = Compliance voltage of current source = $(V_{CC} - V_{SAT})$[1] (2)

V_{CC} = Supply voltage for current source;

V_{SAT} = Saturation voltage of current source

I_{LOOP} = Operating loop current

R_{LINE} = DC resistance of wire per length

$\Sigma V_{XMTR}{}_{MARK}$ = Summation of voltage drops across each non-isolated and isolated transmitter current loop terminals when MARK state current flows.[2]

$\Sigma V_{RCVR}{}_{MARK}$ = Summation of voltage drops across each non-isolated and isolated receiver current loop terminals when MARK state current flows.[2]

Notes:

1. V_{COMP} must be less than the breakdown voltage rating of the transmitter unit in SPACE state.
2. The non-isolated unit will supply loop current. If two or more non-isolated units are used, then only one of these units needs to supply loop current.

This equation can be solved for any particular parameter of interest if the other remaining parameters are known. For example, Equations (1) and (2) can be solved for minimum power supply voltage, V_{CC}, which can be used for current source of Figure 7 for the following conditions.

$$V_{COMP} = \Sigma V_{RCVR}{}_{MARK} + \Sigma V_{XMTR}{}_{MARK} + 2\, L I_{LOOP}\, R_{LINE} \quad (3)$$

Where,

$\Sigma V_{RCVR}{}_{MARK}$ = 2.76 V (One isolated receiver)

$\Sigma V_{XMTR}{}_{MARK}$ = 0 V (Non-isolated transmitter voltage drop is incorporated in V_{COMP})

I_{LOOP} = 22 mA (20 mA + 10%),

R_{LINE} = 0.053 Ω/m (AWG No. 22),

L = 305 m

V_{COMP} = 2.76 V + 0 V + 2(305 m) (0.022 A) (0.053 Ω/m)

= 3.47 V

and using equation (2)

$V_{CC} = V_{COMP} + V_{SAT}$; where $V_{SAT} = 1.5$ V

$= 3.47$ V + 1.5 V

$V_{CC} = 4.97$ V

For the listed conditions, these calculations are for the worst case temperature and unit to unit variations.

To address device voltage breakdown concerns, the current source compliance level for the current loop and the SPACE state current need to be known. The SPACE state current is determined by the transmitter when it is in the OFF state. SPACE state current will not be necessarily equal to zero. Hence, when a current loop receiver is designed, the threshold must be set at a proper level to avoid detecting the SPACE state current as well as to provide a noise margin. With the HCPL-4200 receiver, SPACE state current of 3.0 mA or less is allowed. Should a larger noise current margin be desired for SPACE state, the maximum SPACE state current of the HCPL-4200 can be raised effectively by shunting the input with a resistor. Actual device current threshold does not change; only the loop current level required to reach SPACE state threshold increases. Use of a shunting resistor will reduce the noise current margin in the MARK state for the HCPL-4200.

Should the HCPL-4100 transmitter be used, the maximum SPACE state current is 2.0 mA. For half duplex applications, a noise margin of 1.0 mA is specified for SPACE state with the combination of the HCPL-4100/-4200 units.

AC Performance

AC performance of a current loop is influenced by many factors. Typical data rate capability for the simplex configurations shown in Figures 7 and 9 are shown in Figures 8 and 10 respectively. The 10% (25%) distortion data rate is defined as the rate at which 10% (25%) distortion occurs to the output bit interval with respect to the reference input bit interval. This is expressed by equation (4).

Distortion Data Rate

$$f_D = \frac{1}{t_{BIT}} \quad (4)$$

Where D = % distortion and t_{BIT} is bit time of the input signal when D distortion is present in the output bit interval.

A square wave as well as a 16 bit data stream was used to "exercise" the current loop system. In both simplex point-to-point configurations, the input data rate was adjusted to result in a 10% (25%) distortion to the output signal for either an input square wave or a 16 bit pattern.

The 16 bit pattern was used to provide two propagation delay test conditions for the current loop. One part of the 16 bit waveform tests for data rate distortion affected by a long duration in either a MARK or SPACE state prior to state change. The other part of the 16 bit waveform tests for effects on data rate distortion via short durations in either a MARK or SPACE state prior to a state change. In both simplex configurations, Figures 7 or 9, the transition from either a short or a long duration MARK state to a SPACE state affects the data rate distortion the most. The 16 bit exerciser circuit diagram and bit stream waveform are shown in Appendix A.

In the description of the AC performance that follows, an approximation has been made to simplify the analysis. The transmission line is treated as a lumped capacitance. A more complete analysis of AC performance would require rigorous treatment via transmission line theory.

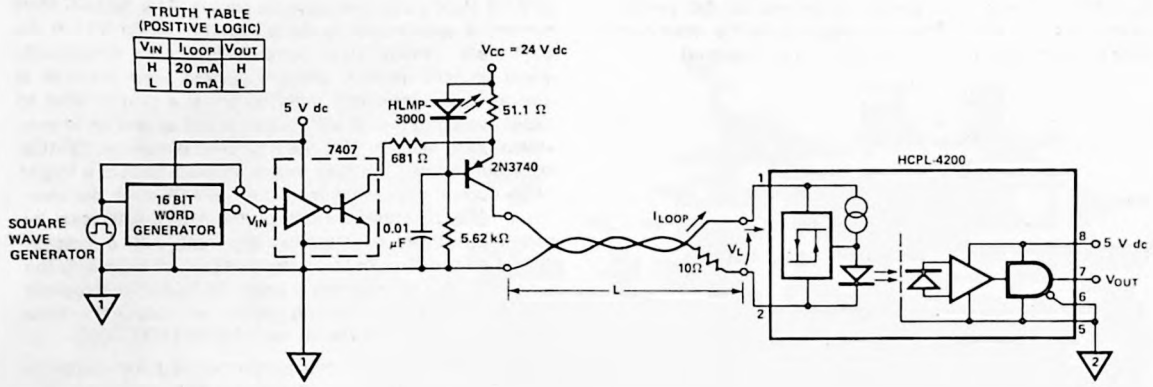


Figure 11. Data Rate Test Circuit for Non-Isolated Active Transmitter to Isolated HCPL-4200 Receiver

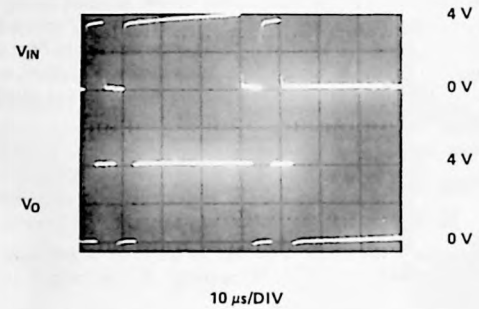


Figure 12. Timing Comparision of Output Signal (V_O) to Input Signal (V_{IN}) using 16-Bit Word at 10% Distortion with 305 m (1000 ft.) Loop Distance. Reference Figure 11.

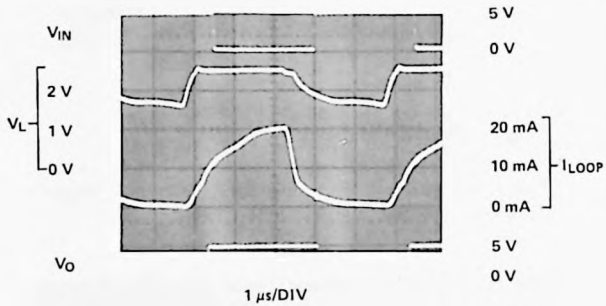


Figure 13. Characteristic Waveform Performance of Circuit in Figure 11 with 305 m (1000 ft.) Loop Distance, Square Wave Input and Output Distortion of 10%. a. Input Voltage (V_{IN}), b. Receiver Load Voltage (V_L), c. Loop Current (I_{LOOP}), d. Output Voltage (V_O)

Non-Isolated Active Transmitter with the HCPL-4200 Receiver

The typical waveforms for the non-isolated active transmitter used with the HCPL-4200 (Figure 11) are shown in Figures 12 and 13. The loop length is 305 metres (1000 ft.). Figure 12 shows 10% distortion when the input signal is a 16 bit pattern. The total propagation delay shown in Figure 12 for a SPACE to MARK transition is 2.4 μs. The propagation delay of the transmitter and receiver is 0.3 μs. Hence, the propagation delay for the transmission line is 2.1 μs. Current and voltage waveforms for the current loop at the receiver end are shown in Figure 13 for a 10% distortion of data to an input square wave. Notice the loop current waveform delay of 2.4 μs before V_O follows V_{IN}. The important parameter to observe is loop current. When the loop current level exceeds the HCPL-4200 current threshold, V_O changes state. Loop voltage at the receiver only follows the current level and changes by approximately one volt. This simplex configuration provides the best speed performance.

Non-Isolated Active Receiver with the HCPL-4100 Transmitter

The typical waveforms for the non-isolated active receiver used with the HCPL-4100 (Figure 14) are shown in Figures 15 and 16. The loop length is 305 metres (1000 ft.). Figure 15 shows 10% distortion when the input signal is a 16 bit pattern. Figure 16 illustrates a 10% distortion for an input square wave. Recall that current level determines the switching point, not the voltage level.

At the input low to high state change, the loop current changes momentarily to the MARK state short circuit output current level, I_{SC}, (typically 85 mA). A current spike appears at the receiver end after the inherent transmission line propagation delay of approximately 2 μs, as expanded in Figure 17. The spike is caused by sudden discharge of cable capacitance. However, the loop current rapidly decreases from the I_{SC} level to a 20 mA level when line discharge is complete. Time duration of I_{SC} can be calculated by referring to the output power dissipation calculations for the HCPL-4100 in Appendix B.

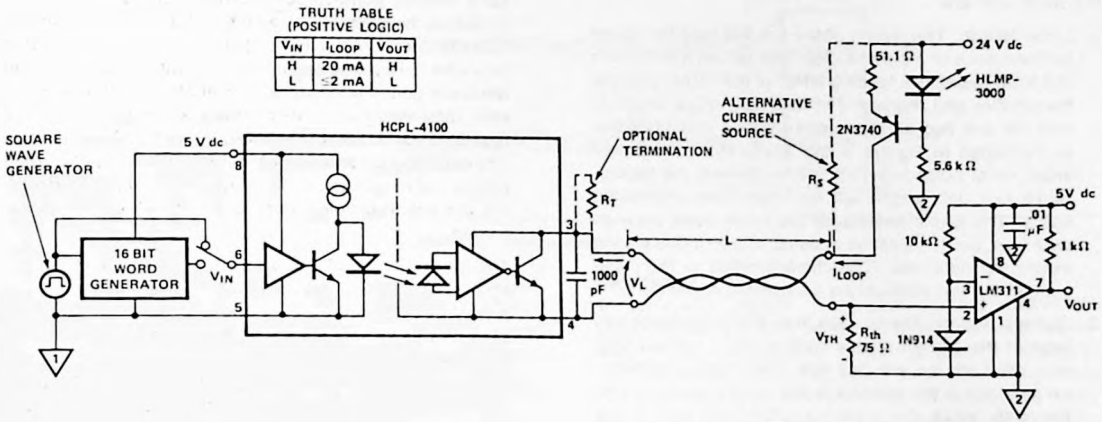


Figure 14. Data Rate Test Circuit for Isolated HCPL-4100 Transmitter to Non-Isolated Active Receiver

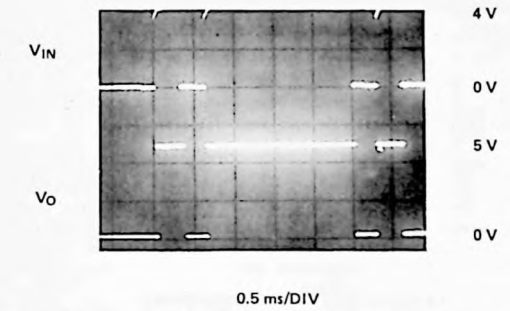


Figure 15. Timing Comparison of Output Signal (V_O) to Input Signal (V_{IN}) Using 16-Bit Word at 10% Distortion with 305 m (1000 ft.) Loop Distance. Reference Figure 14.

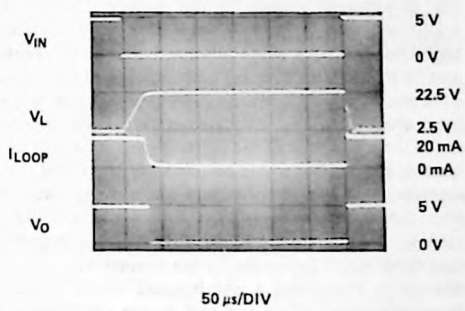


Figure 16. Characteristic Waveform Performance of Circuit in Figure 14 with 305 m (1000 ft.) Loop Distance, Square Wave Input and Output Distortion of 10%. a. Input Voltage (V_{IN}), b. Transmitter Load Voltage (V_L), c. Loop Current (I_{LOOP}), d. Output Voltage (V_O)

The non-isolated receiver switched states when loop current crossed approximately 10 mA level. Yet, the loop voltage took approximately 10 μs to change from a current source voltage compliance level of 22.5 V to a MARK state voltage of 2.4 V at 20 mA. This loop voltage characteristic does not limit the turn on speed performance.

At the input signal high to low transition, the HCPL-4100 transmitter turns off after the device propagation delay. However, the loop current at the receiver does not change from 20 mA until approximately 30 μs later. This is due to the current source charging the line capacitance at a fixed rate of 20 mA from essentially a MARK state voltage level (2.4 V) to the compliance level of the current source. Only after the compliance voltage is reached does the loop current fall below the 10 mA threshold of the receiver. As before, the current level at the receiver determines the switching time. In this example, the compliance voltage of the current source influences the turn off delay of the loop. This dependence is graphically illustrated in Figure 10.

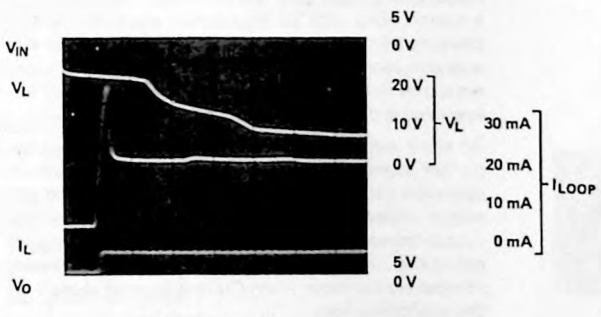


Figure 17. Expanded Waveform Response of Figure 16. Displayed are Details of I_{SC} Magnitude and Duration at Receiver as well as Transmitter Output Voltage (V_L)

General Factors Affecting Data Rate

Three factors which limit data rate and their corresponding trade-offs are:

1. Loop length: The length of the line will limit the speed performance of a current loop. This results mainly from the total capacitive loading effect of the cable upon the transmitter and receiver. The data rate versus length of line for the two simplex point-to-point configurations is illustrated in Figures 8 and 10. Shielded cable provides more noise immunity but, in general, the capacitance per unit length will be larger than unshielded cable. The characteristics of the cable used, such as wire size, twist, insulation material, etc. all influence the maximum data rate. (The characteristics of the cable used in the text applications are listed in Appendix C.)

2. Current Source: The location, type and compliance voltage of the current source used within a current loop can affect the system data rate. The primary limitation on data rate is the location of the current source within the loop. When the current source is located at the transmitter end of the loop rather than at the receiver end, the maximum data rate is much higher for a given loop length. This effect can be seen when comparing data in Figure 8 to Figure 10. The main reason for the lower data rate capability shown in Figure 10 is that the current source must charge the cable capacitance to the compliance voltage of the current source. The speed achieved in Figure 8 results because cable voltage changes by a small amount between the MARK and SPACE states. Practical applications of the HCPL-4100 and HCPL-4200 optocouplers generally will require the current source to be located at the non-isolated end of the loop. For best speed performance, an active non-isolated transmitter would be used with the HCPL-4200 receiver. However, in full duplex applications (two simplex loops), the non-isolated ends should be at a common location. Hence, overall bidirectional system data rates would be limited by the slowest loop, i.e., the one which contained a non-isolated, active receiver. More discussion of full and half duplex applications is found in subsequent sections.

   The type of current source can affect speed performance. A simple resistor, when used with a voltage source at the non-isolated loop end, can set the loop current level. Improper source impedance or termination of the loop causes reflections which distort data resulting in a lower data rate capability. Termination of a current loop with an impedance equivalent to the characteristic impedance of the line can improve the data rate capability by approximately 20%. Termination resistance does reduce part of the voltage available for operating station(s) on the loop.

   An active element current source can be controlled by current steering which allows for a higher speed of operation while providing consistently high on and off output impedance. Less variation in current source output impedance can help to reduce multiple signal reflections from occurring. Active element current sources are described in the Current Sources section of this application note.

   The compliance voltage can influence the speed performance of the non-isolated, active receiver circuit shown in Figure 9. Data rate dependency upon the compliance voltage is shown in Figure 10. Reducing the current source supply voltage from 24 V DC to 10 V DC for a simplex point-to-point current loop configuration increases the data rate by a factor of 3.5 in a 1000 metre (3281 ft.) loop. The reason for the improvement is that less time is required to charge the transmission line to the lower compliance voltage level at a constant charge rate. However, the opposite simplex arrangement of a non-isolated, active transmitter, Figure 7, has no data rate dependency on compliance voltage as illustrated in Figure 8. This is the result of the HCPL-4200 performing current threshold detection, not voltage level detection.

   The maximum usable data rate for a given loop length and configuration is usually determined by the propagation delay differences of the current loop and the amount of skew that is allowed in the user's application. Propagation delay skew is $|t_{PLH} - t_{PHL}|$. Factors which contribute to the system propagation delay skew are the current source compliance voltage level, the current source location, the inherent propagation delay skew of the current source, as well as the optocoupler propagation delay skew. Detailed information on factors which affect distortion of data are discussed in the subsequent Half Duplex section.

3. Device Performance: The propagation delay of the transmitter and the receiver can influence data rates for short loop lengths (<100 metres) in high speed applications (>1 MBd). Generally, current loops are designed to operate over much greater distances than 100 metres. Consequently, the cable capacitance dominates the data rate limitations.

   Another device performance consideration is the power dissipated in the HCPL-4100 transmitter. An example of power dissipation calculation for the HCPL-4100 is given in Appendix B. Derating may be required when operating the unit at large V_{CC} voltage.

Optional Device Protection Considerations

Specific end product applications may require additional device protection. A bridge rectifier can be included in order to remove loop polarity connection concerns. Current buffering can be designed for loop currents greater than 30 mA. Possibility of damage due to electrostatic discharge to the cable or interconnection points can be significantly reduced by the use of energy absorbing devices, such as TransZorbs® or metal oxide varistors (MOV).

Full Duplex

A common and useful extension of the simplex configuration is the full duplex configuration. Full duplex communication is defined as the simultaneous, bidirectional transmission of information between local and remote units. The block diagram in Figure 18 shows this point-to-point configuration.

Essentially, a full duplex arrangement is two point-to-point simplex loops (a four wire system) used simultaneously for back and forth data flow. A common current loop application for full duplex configuration is connecting remote terminals to an I/O interface section of a central computer system.

Implementation of optical isolation within a full duplex current loop system should be done at one common end

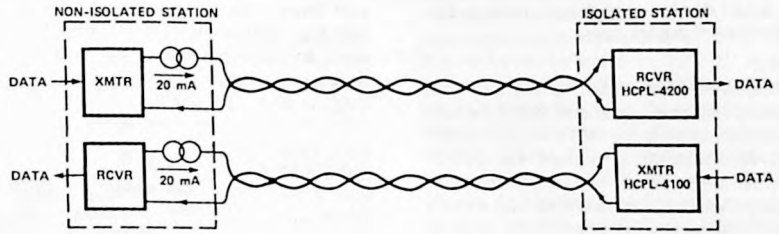


Figure 18. Full Duplex Point-to-Point Current Loop System Configuration

of the loops. Two separate, active, non-isolated units are located at the other end of the loops. Figure 18 illustrates these comments. Providing isolation at one common end will significantly reduce common mode coupling between the two loops. In most cases, the full duplex data rate is limited by the loop containing the HCPL-4100 and the non-isolated active receiver. This limitation can be circumvented by using an isolated current source at the HCPL-4100 end of the loop and a non-isolated passive receiver. The isolated current source increases the cost of the data link, but this increased cost may be justified by the speed improvement obtained. All information which is described in the Simplex section for the performance of a simplex point-to-point current loop configuration will apply to the full duplex applications as well.

Half Duplex

A half duplex current loop provides non-simultaneous, bidirectional data flow between remote and local equipment. This configuration utilizes a simpler two wire interconnection, compared to the four wire arrangement of the full duplex case. The half duplex system can easily be expanded from a point-to-point application to a multidrop application with multiple transmit and receive stations along the loop. The block diagrams of Figure 19 demonstrate the two cases of point-to-point and multidrop for half duplex.

A characteristic of the half duplex configuration is the need to establish priority of transmitters in the current loop whether the loop is point-to-point or multidrop. Protocol in the information being transferred will ensure that

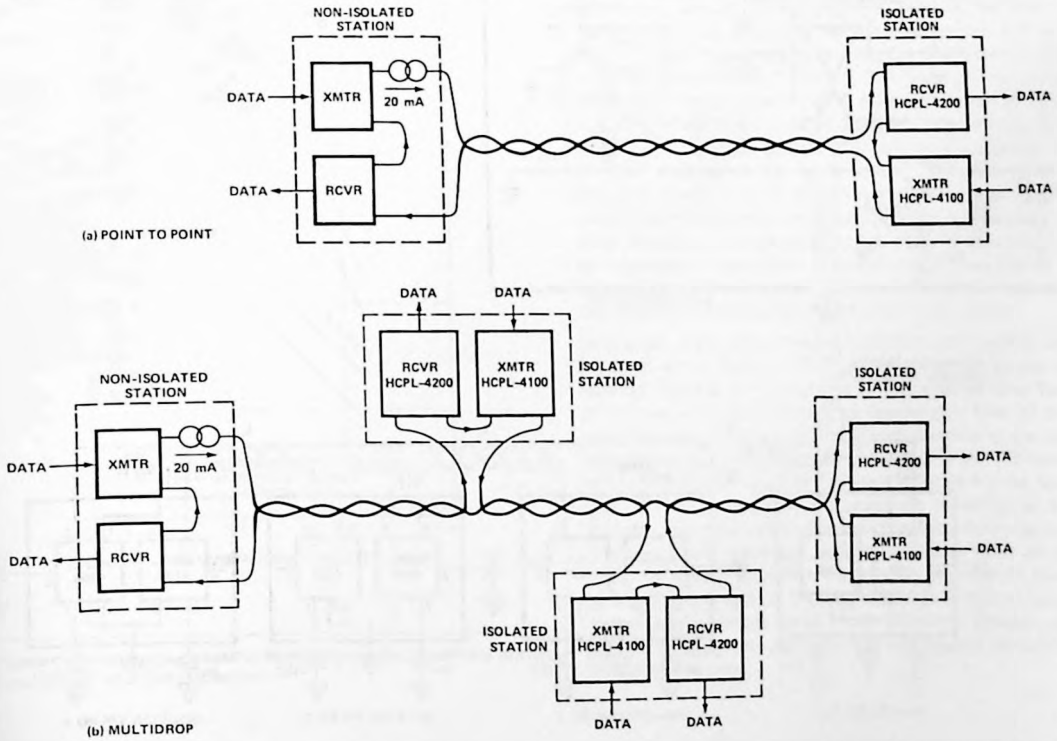


Figure 19. Half Duplex Current Loop System Configurations for: a. Point-to-Point, b. Multidrop

APPLICATIONS

only one transmitter is sending data at any given time. Typical usage of a half duplex current loop parallels similar applications for the full duplex case.

DC Performance

As Figure 19 illustrates, isolation of the current loop from logic systems is easily implemented at one end of the loop by the use of the combination of the HCPL-4100 transmitter and the HCPL-4200 receiver. Significant reduction of common mode influences on the current loop, elimination of ground potential differences and specified loop current noise immunity are achieved by the use of these complementary optocouplers. For this combination of optocouplers, the loop current noise immunity is a minimum of 1 mA in the SPACE state and 8 mA in the MARK state. A non-isolated active transceiver (transmitter and receiver) with one current source operates at the opposite end of the current loop.

The maximum compliance voltage of the current source is limited by the breakdown voltage capability of any transmitter in the half duplex loop. The isolated HCPL-4100 transmitter has a maximum operating voltage of 27 V DC. However, in multidrop applications, each isolated HCPL-4200 receiver will share a portion of the compliance voltage during the SPACE state, worst case 0.9 V DC at a minimum SPACE state current of 0.5 mA. Also, each isolated conducting HCPL-4100 transmitter will share a portion of the compliance voltage during SPACE state as well. Worst case, this is 0.95 V DC at 0.5 mA. For example, with four pairs of HCPL-4100 and HCPL-4200 units being used, an additional worst case 6.5 V DC can be added to increase the maximum compliance voltage value from 27 V DC to 33.5 V DC for the current source. The additional 6.5 V DC is calculated on the basis of one of the HCPL-4100 transmitters interrupting 22 mA loop current at 200 metre station intervals. This increase in the compliance voltage level can allow another isolated station to be used. Minimum V_{CC} required for the current source of Figure 20(b) with five isolated stations in the MARK condition with worst case parameters previously used yields 33.2 V DC. A higher compliance voltage can allow longer loop lengths but data rate will be slower. Precautions must be taken to prevent the removal of any stations from the loop in order to avoid an excessive compliance voltage from overstressing any transmitter remaining in the loop. A design compromise has to be determined for the benefits achieved at different compliance voltages. Equation (1) from the Simplex section can be used to determine any DC parameter in a half duplex application.

A specific active, non-isolated transceiver which can be used in point-to-point and multidrop applications with the HCPL-4100 and HCPL-4200 current loop optocouplers is shown in Figure 20.

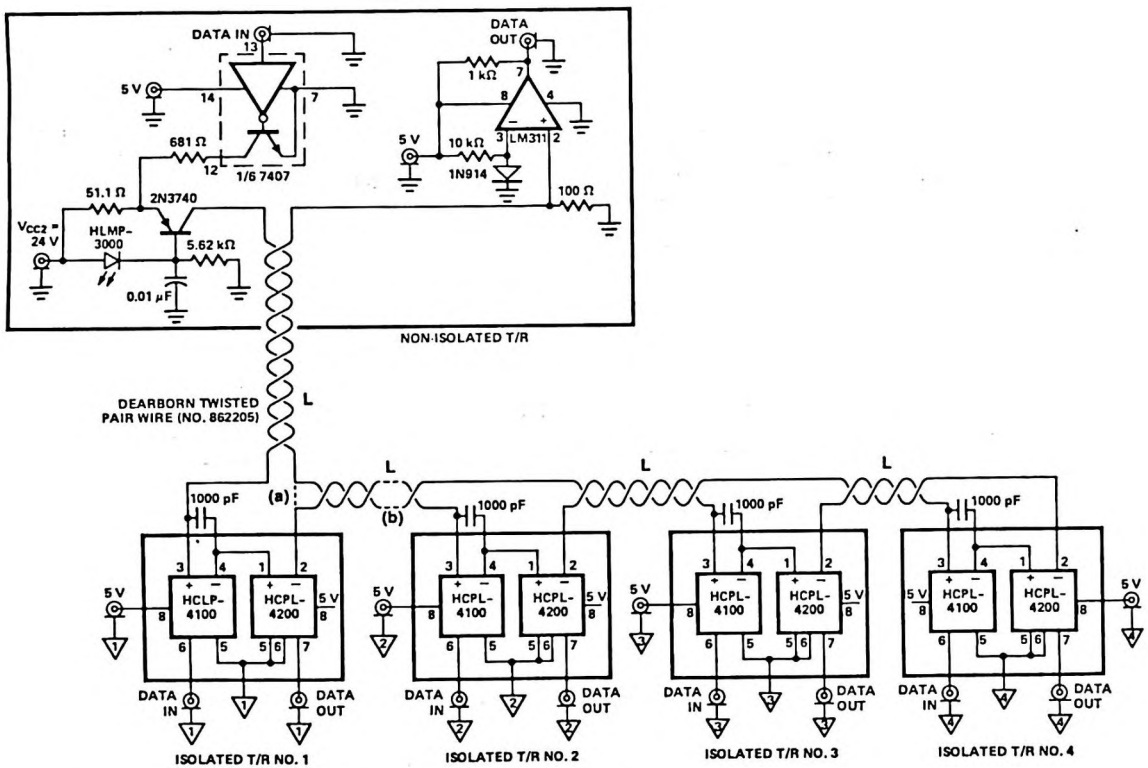


Figure 20. Circuit Schematic of Half Duplex Configurations: a. Point-to-Point, b. Multidrop

AC PERFORMANCE

Point-to-Point

The corresponding data rate performance versus loop distance and direction of data is given in Figure 21 for the half duplex point-to-point application. Definitions for 10% and 25% distortion data rate are given under the Simplex Configuration section.

Transmission of data from an isolated T/R (transmitter and receiver pair) to an active non-isolated T/R limits the half duplex data rate performance. This limitation is due to slower speed of a current loop when using an isolated transmitter. A lower current source compliance voltage will improve the data rate of an isolated T/R to a non-isolated T/R as discussed in the Simplex section.

Multidrop

The data rate performance for half duplex multidrop applications, as illustrated in Figure 20(b), is summarized in Tables 1 and 2. These tables compare data rate versus the loop distance between stations, total length of loop, direction of data, distortion data rate and data format. Table 1 illustrates at fixed distortion (10% or 25%) how data rate can be different at different stations along the loop. Table 2 shows the pulse width distortion that results when the multidrop loop is operated at several fixed data rates.

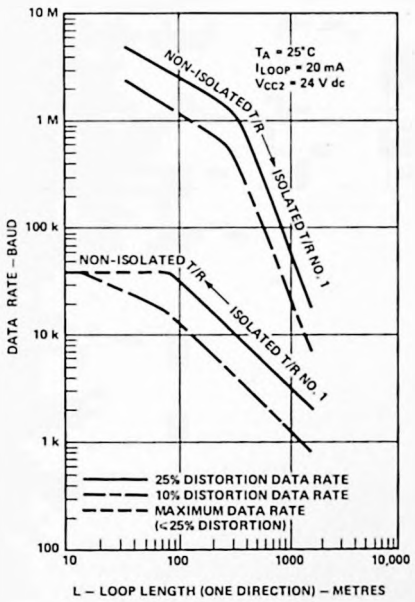


Figure 21. Half Duplex Point-to-Point (Figure 20a) Data Rate vs. Loop Length and Data Direction

Comparision of data rates for point-to-point (half duplex) and multidrop configurations can appear contradictory. Data presented in Figure 21 and Table 1 illustrate this at a 25% distortion on a 915 m (3000 ft.) loop. A comparison shows the influence of multiple stations upon the data rate for a fixed loop length. In the point-to-point case, the data rate is 62.5 kBd from an active, non-isolated T/R to the isolated T/R No. 1. In the multidrop case, non-isolated T/R to the isolated T/R No. 3, data rate in the same direction is 25 kBd. As expected, the data rate in point-to-point is faster because the current source only needs to charge the line to a lower sum (≈ 1/2) of MARK state voltages than in the multiple station case. However, in the opposite direction of isolated T/R No. 1 to active, non-isolated T/R, the point-to-point data rate is 3.33 kBd while the multidrop data rate is 6.25 kBd. In this instance, multidrop is 2X faster than the point-to-point case over the same distance, contrary to "expected" results. The reason for this speed improvement results from the fact that when T/R No. 3 interrupts the loop current, the current source will continue to charge the loop until the compliance voltage is reached causing the current source to shut down. Fortunately, the voltage difference between the sum of all MARK state voltage drops and compliance voltage is small due to the total of four stations in the loop. Hence, a small voltage excursion requires considerably less charging time than if this charging occurred over a larger voltage excursion.

In addition, with the usage of multiple stations at a constant data rate, the data distortion can vary from station to station. This distortion varies with respect to the transmitting station. As an illustration from Table 2, the 915 m (3000 ft.) example with three remote stations (i.e., the isolated T/R No. 3 transmitting at 6.25 kBd to successive 305 m (1000 ft.) stations of T/R No. 2, T/R No. 1 and an active non-isolated transceiver) yields distortion levels of 19%, 31%, 25% respectively. Larger distortion at an interim station than at a station located at an end of a loop is due to different thresholds for each station. Identical current threshold levels at each station will provide progressively increasing distortion levels at each station along the loop. Also, reflection of signals between stations can account for inconsistent distortion levels at various stations on a loop system. The designer will be limited to a data rate that results in acceptable distortion for each station.

In general, data rate limitations in multidrop applications for data which flows from active non-isolated station to isolated stations will be caused by propagation delay time of the line and the charging or discharging time for the total line capacitance. Charging and discharging the line occurs over a voltage level which is equal to the difference between the sum of all MARK state voltages and the sum of all SPACE state voltages which are presented at the active non-isolated loop connection points. Data rate limitations in the opposite direction (isolated units to an active, non-isolated unit) are limited by propagation delay time of the line and by the time to charge total line capacitance over a voltage equal to the difference between the sum of MARK state voltages and compliance voltage of the current source.

Table 1. Constant % Distortion, Variable Data Rate for Half Duplex Multidrop Configuration.

Data In	Data Out	L Length between Data Input and Data Output points		L_T Total Loop Length	Data Rate kBd	% Distortion	Comments
		m	ft.	m (ft.)			
Active Non-Isolated Transceiver	T/R #4 T/R #3 T/R #2 T/R #1	122 92 61 31	400 300 200 100	122 (400)	250 370 370 250	25%	Input Signal: Square Wave Current Source: 20 mA/24 V DC Half Duplex Current Loop Circuit Schematic: Figure 20b.
	T/R #4 T/R #3 T/R #2 T/R #1	122 92 61 31	400 300 200 100		125 167 167 125	10%	
Isolated T/R #4	Non-Iso. T/R T/R #1 T/R #2 T/R #3	122 92 61 31	400 300 200 100		62.5 62.5 82.5 100	25%	
	Non-Iso. T/R T/R #1 T/R #2 T/R #3	122 92 61 31	400 300 200 100		25 25 33.3 40	10%	
Active Non-Isolated Transceiver	T/R #3 T/R #2 T/R #1	915 610 305	3000 2000 1000	915 (3000)	25 33.3 25	25%	
	T/R #3 T/R #2 T/R #1	915 610 305	3000 2000 1000		12.5 16.7 12.5	10%	
Isolated T/R #3	Non-Iso. T/R T/R #1 T/R #2	915 610 305	3000 2000 1000		6.25 5.0 8.25	25%	
	Non-Iso. T/R T/R #1 T/R #2	915 610 305	3000 2000 1000		2.0 2.0 3.33	10%	

Table 2. Constant Data Rate, Variable % Distortion for Half Duplex Multidrop Configuration.

Data In	Data Out	L Length between Data Input and Data Output points		L_T Total Loop Length	Data Rate kBd	% Distortion	Comments
		m	ft.	m (ft.)			
Active Non-Isolated Transceiver	T/R #4	122	400	122 (400)	250	25%	Input Signal: Square Wave Current Source: 20 mA/24 V DC Half Duplex Current Loop Circuit Schematic: Figure 20b.
	T/R #3	92	300		250	30%	
	T/R #2	61	200		250	15%	
	T/R #1	31	100		250	25%	
	T/R #4	122	400		125	10%	
	T/R #3	92	300		125	6%	
	T/R #2	61	200		125	7.5%	
	T/R #1	31	100		125	12%	
Isolated T/R #4	Non-Iso. T/R	122	400		62.5	25%	
	T/R #1	92	300		62.5	25%	
	T/R #2	61	200		62.5	19%	
	T/R #3	31	100		62.5	6%	
	Non-Iso. T/R	122	400		25	10%	
	T/R #1	92	300		25	10%	
	T/R #2	61	200		25	7.5%	
	T/R #3	31	100		25	7.5%	
Active Non-Isolated Transceiver	T/R #3	915	3000	915 (3000)	25	25%	
	T/R #2	610	2000		25	17.5%	
	T/R #1	305	1000		25	25%	
	T/R #3	915	3000		12.5	10%	
	T/R #2	610	2000		12.5	7.5%	
	T/R #1	305	1000		12.5	12%	
Isolated T/R #3	Non-Iso. T/R	915	3000		6.25	25%	
	T/R #1	610	2000		6.25	31%	
	T/R #2	305	1000		6.25	19%	
	Non-Iso. T/R	915	3000		2.0	10%	
	T/R #1	610	2000		2.0	8%	
	T/R #2	305	1000		2.0	12%	

CURRENT SOURCES

Resistor

Current sources used for current loop systems can vary in performance, complexity and cost. The most elementary and inexpensive technique for supplying loop current is to use a series resistor between the non-isolated station power supply and the loop. The resistance value (R_S) to use is a function of the desired loop current (I_{LOOP}), of the type of cable (resistance per length, R_{LINE}), the loop length (L), the number of stations on the loop with their respective MARK state terminal voltages (ΣV_{MARK}) and the power supply voltage (V_{CC}) for the non-isolated station. Equation (5) determines the resistor value. The simplicity of a single resistor yielding a 20 mA loop current is achieved at the expense of requiring that the loop configuration cannot be changed without changing the resistor value.

$$R_S = \frac{V_{CC} - (I_{LOOP})(R_{LINE})2L - \Sigma V_{MARK}}{I_{LOOP}} \qquad (5)$$

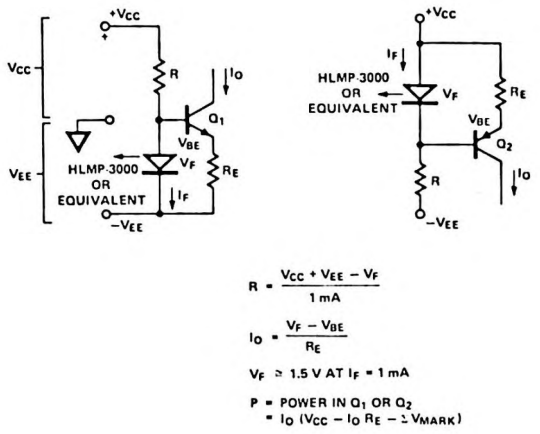
Speed performance of a loop system using a current setting resistor is slower than with an active current source. This difference arises from an exponential current response versus a linear current response associated with an active current source. For a given current threshold level, the linear response will charge a capacitive line quicker than an exponential response. When a current setting resistor is used, termination resistance can be employed at the isolated stations in order to reduce somewhat the signal reflections along a loop. Up to a 20% speed improvement can be obtained with termination resistance equal to characteristic line impedance. However, with the use of termination resistance, allowance must be made for the additional MARK state voltage drop of the terminating resistor with respect to the available compliance range of the current loop.

LED/Transistor

The recommended current source to use is a simple, relatively inexpensive, active constant current source shown in Figure 22. The LED provides a stable voltage reference (V_F) for the transistor base and also helps to compensate the base-emitter junction voltage (V_{BE}) changes with temperature. This current source is fairly independent of the V_{CC} level if the LED bias current (I_F) is set so that the V_F only changes slightly with large variations in I_F (≈ 60 mV/decade of I_F). Regulation of 10% in output current can easily be achieved over a V_{CC} range of 5 V DC - 27 V DC.

When large V_{CC} is used with low MARK state voltage conditions, the use of a transistor with good thermal conduction to the ambient environment will minimize the variation in the source current because of the variation of V_{BE} with temperature. This state is the large power dissipation condition.

This current source can be easily current steered for fast switching. Current steering is illustrated in Figure 7. For applications of this current source at high data rates over short loop distances it is important that the difference in propagation delays from on-to-off and off-to-on be made as small as possible. Status indication is conveniently given by the LED.



$$R = \frac{V_{CC} + V_{EE} - V_F}{1\ mA}$$

$$I_O = \frac{V_F - V_{BE}}{R_E}$$

$V_F \geq 1.5\ V$ AT $I_F = 1\ mA$

P = POWER IN Q_1 OR Q_2
$= I_O (V_{CC} - I_O R_E - \Sigma V_{MARK})$

Figure 22. Recommended Constant Current Source

Specialized Integrated Circuits

More complicated current sources which are usable in current loops can be current mirrors or specialized integrated circuits. A current mirror displayed in Figure 23 requires the use of a matched pair of transistors in order to perform well.

In general, commercially available matched pairs are not designed for output collector currents greater than 10 mA. Additional components which are needed to obtain 20 mA results in greater complexity and higher cost with less reliability. In order to reduce power supply noise influences and improve thermal stability, significant transistor emitter degeneration resistance must be used. This degeneration sacrifices the available voltage range between the total MARK state voltage and the compliance voltage of the current mirror.

In Figure 23(c), the LM234 integrated circuit current source can be used. More components are required for temperature compensation to provide a proper current level and regulation over a wide temperature range as well as to prevent possible oscillations of this active device. In addition, switching characteristics of the LM234 must be considered with regard to the desired loop speed performance. Over all, the current source provides good regulation (±3%) for current loop usage, but the cost of additional components and space in an input-output module may detract from the design convenience of this device.

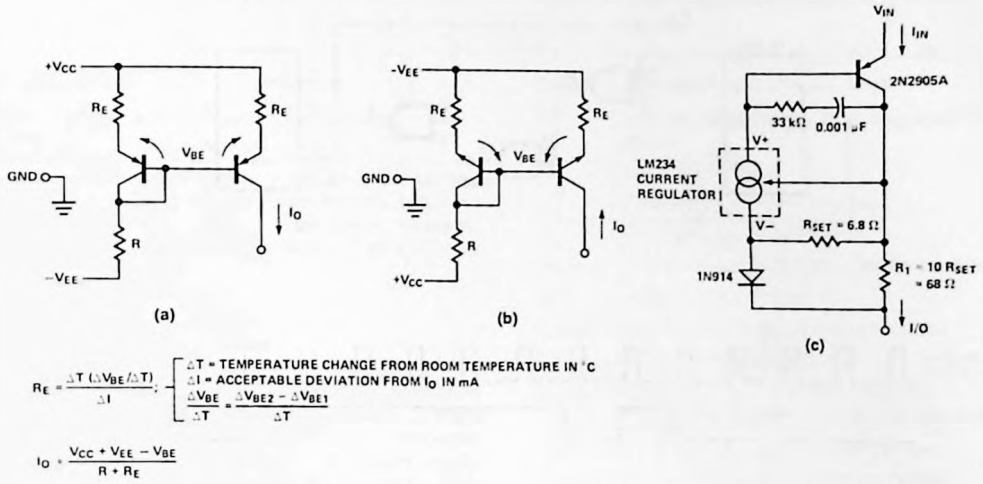


Figure 23. Specialized Integrated Circuit Current Sources. Current Mirrors: a. PNP, b. NPN. Current Regulator: c. LM234 plus Components

APPENDIX A.

16-Bit TTL Data Exerciser Circuit

The purpose of this circuit is to provide long (6 bits) and short (1 bit) durations of the logic one and logic zero states in different time sequences. Figure 24 illustrates the 16-bit TTL output waveform (Q_A).

APPENDIX B.

HCPL-4100 Power Dissipation Calculations

The power dissipation calculation for the HCPL-4100 transmitter is made using the standard method for determining the input power dissipation. Calculation of the output power dissipation must take into account power consumed in three different operating conditions. These conditions are: 1. power dissipated during transition from SPACE to MARK state, 2. power dissipated in MARK state, and 3. power dissipated in SPACE state. The worst case average power dissipated over two bit intervals should be calculated. The average output power dissipation is calculated from the following formula:

$$P_O = \frac{P_{SM}t_{SM} + P_{M}t_{M} + P_{S}t_{S}}{2\,t_{BIT}} \quad (6)$$

where

P_O = Average output power dissipated during a worst case time interval.

P_{SM} = Power dissipated during SPACE to MARK transition

$$= \frac{I_{SC}(V_{COMP} + V_{MO})}{2} \quad (7)$$

I_{SC} = MARK state short circuit output current

V_{COMP} = Compliance voltage of current source

V_{MO} = MARK state output voltage

P_M = Power dissipated during MARK state

$$= V_{MO}I_{LOOP} \quad (8)$$

I_{LOOP} = Loop Current

P_S = Power dissipated during SPACE state

$$= V_{COMP}I_{SO} \quad (9)$$

I_{SO} = SPACE state output current

t_{SM} = Duration time of power dissipated during SPACE to MARK transition

$$= \frac{C_L(V_{COMP} - V_{MO})}{I_{SC}} \quad (10)$$

C_L = Total load capacitance

t_M = Duration time of MARK state

t_S = Duration time of SPACE state

t_{BIT} = Time of bit interval

These formulas are based upon an assumption of a linear discharge of a capacitive load.

APPLICATIONS

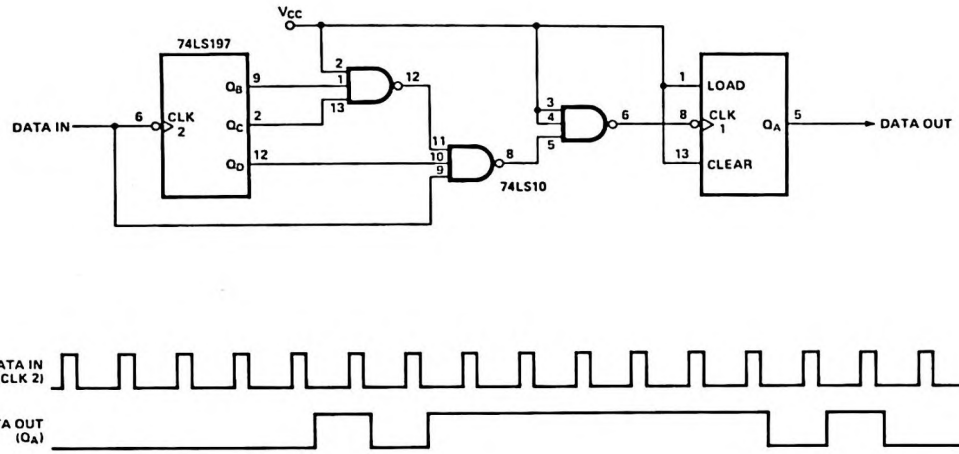


Figure 24. 16-Bit TTL Data Exerciser Circuit and Corresponding Waveforms

Using equations (6) through (10), the worst case output power dissipated in the HCPL-4100 transmitter can be calculated for the following operating conditions.

L = 200 metres (656 ft.)

C_L = 36,000 pF (180 pF/m)

V_{COMP} = 23.5 V DC (V_{CC} = 24 V DC)

I_{LOOP} = 22 mA (20 mA + 10%)

I_{SC} = 85 mA

T_A = 70°C

CMOS LOGIC (15 V ± 5%)

HCPL-4100 Power Dissipation Limits at 70°C
P_{IN} = 208 mW, P_{TOTAL} = 283.5 mW

V_{MO} = 2.75 V at 22 mA

I_{SO} = 2 mA

t_{BIT} = 104.1 μs

(9600 Baud, NRZ* alternating MARK and SPACE states. Reference Figure 25.)

*Non Return to Zero data format.

D = 25% Distortion

Calculation of maximum input power to the HCPL-4100 is based upon linear interpolation of maximum I_{CC} and I_{IH}.

$$P_{IN} = V_{CC}I_{CC} + V_{IH}I_{IH} \quad (11)$$
$$= (15.8\ V)(12.6\ mA) + (15.8\ V)(0.206\ mA)$$
$$= 202.3\ mW. < 208\ mW\ max$$

Consequently, maximum derated output power is

$$P_O = P_{TOTAL} - P_{IN} \quad (12)$$
$$= 81.2\ mW$$

Applying given values to equations (7), (8), (9), and (10) results in

P_{SM} = 1115.6 mW

P_M = 60.5 mW

P_S = 47 mW

t_{SM} = 8.8 μs

Equation (6) yields average output power per bit interval of

P_O = 98.4 mW > 81.2 mW max

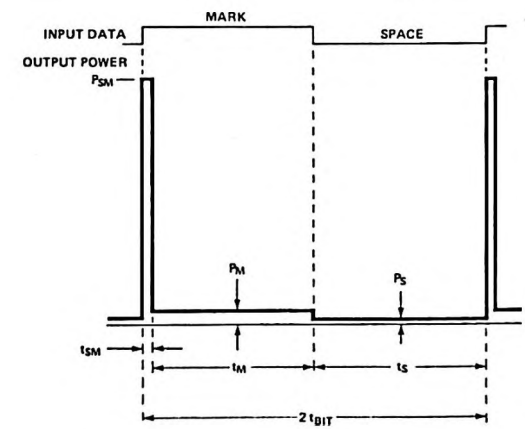


Figure 25. Output Power Dissipation over Two Bit Intervals in HCPL-4100 Transmitter

To circumvent this excess output power dissipation condition, V_{CC} of current source can be reduced from 24 V DC to 15 V DC. Recalculation with V_{CC} = 15 V DC yields

P_{SM} = 733.1 mW

P_M = 60.5 mW

P_S = 29 mW

t_{SM} = 5.0 μs

P_O = 60.9 mW < 81.2 mW max

The major compromises which would be given up are: a. maximum loop length is reduced by one half, and b. less capability for multidrop applications. However, data rate can be doubled to 20 kBd at V_{CC} = 15 V DC over 200 metres.

APPENDIX C.

Cable Data

The cable which was used throughout this application note contained five pairs of unshielded, twisted, 22 AWG wire (Dearborn No. 862205). Typical measured properties of this cable are listed below. Other manufacturers provide cable with similar characteristics (Belden No. 9745). Consult cable manufacturer catalogs for detailed information.

Z_O = 75 Ω, Characteristic Impedance – line to line

R_{LINE} = 52.91 Ω/1000 m, DC Resistance – single conductor

C = 174 pF/m, Capacitance – line to line

t_{DELAY} = 5.9 nsec/m

APPENDIX D.

List of Parameters

C_L = Total load capacitance

f_D = Data rate at which D% output pulse distortion occurs

I_{LOOP} = Operating loop current

I_{SC} = MARK state short circuit output current

I_{SO} = SPACE state output current

L = Length of wire in one direction

P_S = Power dissipated during SPACE state

P_O = Average output power dissipated over a time interval

P_{SM} = Power dissipated during SPACE to MARK transition

P_M = Power dissipated during MARK state

R_{LINE} = DC resistance of wire per length

R_S = Current setting resistor from non-isolated power supply

t_{BIT} = Time of bit interval

t_S = Duration time of SPACE state

t_M = Duration time of MARK state

t_{SM} = Duration time of SPACE to MARK transition

V_{CC} = Power supply voltage

V_{COMP} = Compliance voltage of current source

V_{MO} = MARK state output voltage

$V_{RCVR\ MARK}$ = Voltage across current loop receiver terminals when MARK state current flows

V_{SAT} = Saturation voltage of current source

$V_{XMTR\ MARK}$ = Voltage across current loop transmitter terminals when MARK state current flows

APPENDIX E.

References

1. *Optoelectronics/Fiber Optics Application Manual*, Hewlett-Packard Company, Second Edition, McGraw-Hill, New York, 1981, pp. 3.1–3.77, 10.1–10.8.
2. True, Kenneth M., *The Interface Handbook – Line Drivers and Receivers*, Fairchild Semiconductor Components Group, Mountain View, CA., 1975, pp. 1-1 – 5-12.
3. McNamara, John E., *Technical Aspects of Data Communications*, Second Edition, Digital Equipment Corporation, Bedford, MA., 1982, pp. 13-21, 233-242.
4. Larsen, David G., Ronz, Peter R., Titus, Jonathan A., "INWAS: Interfacing with Asynchronous Serial Mode," *IEEE Transactions on Industrial Electronics and Control Instrumentation*, Vol. IECI-24, No. 1, February 1977, pp. 2–10.
5. *HP 13266A Current Loop Converter User's Manual*, Hewlett-Packard Company, Palo Alto, CA 1979

HEWLETT PACKARD

APPLICATION NOTE 1019

Using the HLMP-4700/-1700/-7000 Series Low Current Lamps

INTRODUCTION

The quest for the reduction of power consumption has long been a struggle for design engineers. In many systems, reductions in power requirements mean reductions in driver circuitry and heat dissipation requirements. Individual component power reduction in the telecommunications field adds up to a significant savings in power for large circuits and networks. Reducing power becomes particularly important in the design of portable instruments; the greater the power requirement is, the larger the power supply needs to be and the less portable the instrument becomes.

Hewlett-Packard has now made progress toward LED lamp power reduction by introducing the HLMP-4700/-1700/-7000 series low current lamps. These lamps, available in yellow and high efficiency red, are designed and tested for operation at 2 mA DC. The tinted, diffused packages, available in T-1 3/4, T-1, and subminiature styles, provide the designer a convenient way to reduce power in many applications.

This application note begins by outlining some major characteristics of the low current lamp and compares these characteristics with those of Hewlett-Packard's standard lamp. Luminous intensity and forward voltage as functions of current as well as pulsed mode operating efficiency are examined and discussed. Savings in interface techniques employing CMOS, LSTTL and LTTL logic are covered, and an example analysis of savings in production costs is presented. Also discussed are the ways in which other circuits that operate on power supplies that are greater than 5 volts, effect significant power reductions by the reduction in drive requirements. Telecommunications information on current and voltage requirements pertaining specifically to the telephone and typical telephone networks is covered. Finally, battery information on common household cells also is provided; sizes and capacities are tabled and compared.

DEVICE CHARACTERISTICS

The HLMP-4700/-1700/-7000 series lamps were designed specifically with low current DC operation in mind. Hewlett-Packard's advancements in LED technology and optimization of the chip geometry have increased the light output of the lamp at lower currents. Figure 1 shows typical luminous intensity as a function of forward current for the HLMP-3300/-3301 conventional lamps and the HLMP-4700 low current lamp. From these graphs, it is evident that for currents up to 7 mA DC the low current lamp yields a higher luminous intensity than the conventional lamp shown. For instance, given lamps in identical packages with the same optical characteristics at a forward current of 2 mA, it can be observed that whereas the conventional lamp yields 0.5 mcd, the low current lamp typically yields a luminous intensity of 2.0 mcd.

The operating forward voltage is directly influenced by the low drive conditions as well. The graph of Figure 2 compares typical forward electrical characteristics of conventional lamps and the low current lamp. From the graph, it is evident that at any one value of current the forward voltage is higher for the low current lamp than for the conventional lamp. However, since the higher light output at lower current allows the lamp to be driven at lower cur-

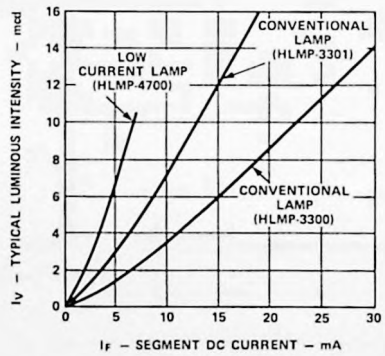


Figure 1. Typical Luminous Intensity vs. Forward Current

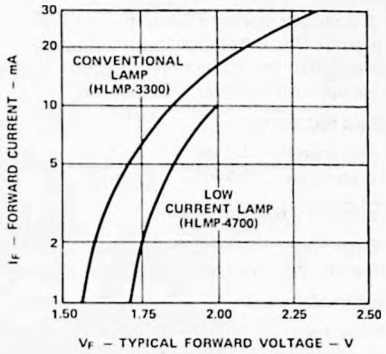


Figure 2. Forward Current vs. Forward Voltage

rents, we may compare the forward voltage of the conventional lamp at 10 mA to that of the low current lamp at 2 mA. The values, typically 2.2 volts and 1.8 volts respectively, indicate that the forward voltage is lower for the low current lamp at the respective appropriate drive conditions.

As mentioned earlier, the low current lamp was optimized specifically for DC operation up to 7 mA. This device is not recommended for operation at high pulsed currents due to increased intensity degradation. The HLMP-3301/-3401 are the respective high efficiency red and yellow lamps in the T-1 3/4 package recommended for high peak pulsed applications. Similar parts exist in T-1 and subminiature packages.

INTERFACE TECHNIQUES

One of the prime uses for the low current lamp is in conjunction with CMOS circuitry. Because the lamp requires lower drive current levels, the power and drive circuitry involved in conjunction with CMOS are very often significantly less than the circuitry and power required to drive a conventional lamp. The use of the low current lamp then may result in significant savings in time, materials and money.

One major area of savings lies in the number of components used in the drive circuit; less circuitry allows fewer components to be used. The resulting layout of the schematic will take a smaller area of the PC board to implement and the built-up circuit will use less space (lower volume), leaving room for other components or subassemblies, or for enhancing the overall compactness of the instrument. Thus, direct materials savings are achieved in actual component count and PC board fabrication.

By using less power, the designer also worries less about heatsinking and cooling systems. Because the actual power is lessened, less power needs to dissipate through metalized PC boards and heatsinks. Moreover, less power through less circuitry in a given volume decreases the operating ambient temperature inside the case, which is a consideration in deciding whether a given device will

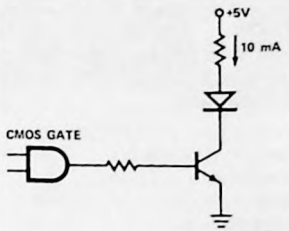


Figure 3. Circuit to Drive a Conventional Lamp

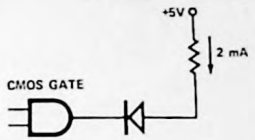


Figure 4. Circuit to Drive a Low Current Lamp

require any form of heatsinking (see Application Note 1005, "Operational Considerations for LED Lamps and Display Devices").

Figures 3 and 4 illustrate some of these cost savings. Figure 3 shows a drive configuration for a conventional lamp at a typical current of 10 mA. With this drive current, the circuit driven by a CMOS gate requires buffering by some external driver, namely the transistor and current limiting resistor shown. On the other hand, the circuit of Figure 4 shows the drive circuitry from the same CMOS gate supplying 2 mA to the low current lamp in the circuit. Since many CMOS devices are able to sink approximately 2 mA directly, external drivers are no longer necessary to turn the lamp on and the circuit is simplified to that of Figure 4. The power dissipation for the conventional lamp circuit is calculated to be:

$$Pd = I\,E = (10\text{ mA})(5V) = 50\text{ mW}$$

For the low current lamp circuit:

$$Pd = I\,E = (2\text{ mA})(5V) = 10\text{ mW}$$

The power savings is then 40 mW

If typical costs are considered, some reasonable cost savings can be calculated. Suppose that the typical driver transistor costs $.05 each and resistors $.01 each, both in large quantities. Each low current lamp substituted for a conventional lamp could save $.06 in actual components. In the PC board layout, this savings in component usage may allow 1/2 square inch of PC board area to be saved. Assuming the cost of fabricated PC board to be $.18 per square inch, we can calculate the savings in these materials.

In addition, the power savings stemming from the substitution of lamps results in savings in the power supply cost. If the cost of a basic power supply runs approximately $1.00 per watt, then our savings of 40 mW yields a savings of ($1.00/W) (0.040W) = $.04 per LED. PC board loading costs, assumed to be $.05 per component, may be added to total the savings by using the low current lamp rather than a conventional lamp.

Resistor	$.01
Transistor	.05
PC Board	.09
Power Supply	.04
PC Board Loading	.10
	$.29 per LED used

Figure 5 lists some CMOS components which will sink approximately 2 mA or more to drive the low current lamp with a 5 volt source. There are other CMOS drivers which will do so at 10 volts. In the case of LTTL or LSTTL logic families, most components at 5 volts will typically sink 4 to 8 mA or more, which is quite sufficient for the lamp to operate.

HIGHER VOLTAGE CONSIDERATIONS

In circuits where higher voltages are involved, power reductions become even more significant. Figure 6 shows a 12 volt DC supply driving a lamp in series with a current-limiting resistor. The difference in total power in the circuit is significant when the comparison is made between conventional lamps and the low current lamp.

For standard red lamps:

If I_f = 20 mA, then P_d = I E (20 mA) (12V) = 240 mW
for 10 units, P_d = (240 mW) (10 lamps) = 2.4 W

For high efficiency red lamps:

If I_f = 10 mA, then P_d = I E (10 mA) (12V) = 120 mW
for 10 units, P_d = (120 mW) (10 lamps) = 1.2 W

For low current lamps:

If I_f = 2 mA, then P_d = I E (2 mA) (12V) = 24 mW
for 10 units, P_d = (24 mW) (10 lamps) = 240 mW

As shown in the example above, the power consumption is reduced by a factor of 5 to 10 simply by the substitution of the low current lamps for the conventional lamps.

		I_{OL} (mA)				
		-40° C	25° C		85° C	
Vendor	Part Number	Min.	Min.	Typ.	Min.	Description
Motorola	MC14049UB	3.6	3.2	6.0	2.6	Hex Inverter/Buffer
	MC14050B	3.6	3.2	6.0	2.6	Non-Inverting Hex Buffer
	MC14053B	2.3	2.1	2.3	1.3	Non-Inverting 3-State Hex Buffer
RCA	CD4009A/ CD4009UB	3.6	3	4	2.4	Hex Inverting Buffer
	CD4010A/ CD4010B	3.6	3	4	2.4	Non-Inverting Hex Buffer
	CD4041A/ CD4041UB	1.8	1.6	3.2	1.44	Quad/True/Comp. Buffer
	CD4049A/ CD4049UB	3.6	3.0	6.0	2.5	Hex Inverting Buffer
	CD4050A/ CD4050B	3.6	3.0	6.0	2.5	Non-Inverting Hex Buffer
National	CD4049C	4.6	4.0	5	3.2	Hex Inverting Buffer
	CD4049M	5.6	4.6	5	3.2	Hex Inverting Buffer
	CD4050BC	4.6	4.0	5	3.2	Non-Inverting Hex Buffer
	CD4050BM	5.6	4.6	5	3.2	Non-Inverting Hex Buffer
	MM70C95/ MM80C95 MM70C97/ MM80C97	4.35	4.35	-	4.35	3-State Hex Buffer
	MM70C96/ MM80C96 MM70C98/ MM80C98	4.35	4.35	—	4.35	3-State Hex Inverter

Figure 5. CMOS Buffers/Drivers

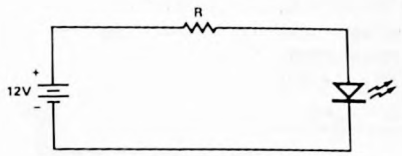


Figure 6. Lamp Circuit Using 12 Volt DC Supply

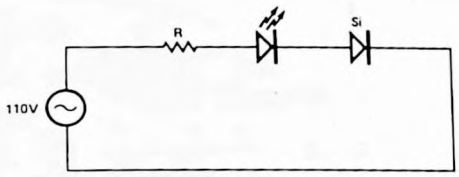


Figure 7. Lamp Circuit Using 110 Volt AC Supply

In the circuit of Figure 7, the lamp is driven by 110 volts AC; a current-limiting resistor and a silicon diode for protection are included.

Power dissipated by the resistor, the major power-using component, can be calculated assuming the voltage drops across the lamp and the silicon diode are insignificant relative to the 110 volt supply:

$$R = \frac{V_{PEAK} - V_f - V_{Si}}{I_{PEAK}} \approx \frac{V_{PEAK}}{I_{PEAK}}$$

Then

$$P_R = I_{RMS}{}^2R = \frac{I_{PEAK}{}^2}{4} R$$

The calculations for all three lamps are tabulated in Figure 8. It can be seen that by reducing power, the low current lamp allows the use of smaller, lower wattage resistors to save space and money.

Lamp	I_{PEAK} (mA)	I_{RMS} (mA)	R (kΩ)	P_R (W)
Standard Red (HLMP-3000)	20	14.1	7.8	0.75
High Efficiency Red (HLMP-3300)	10	7.1	15.0	0.04
Low Current (HLMP-4700)	2	1.4	7.8	0.08

Figure 8. Power Calculations for AC Circuit

TELECOMMUNICATIONS

In telecommunications applications there are only limited amounts of current available to drive the accessories within a telephone. The reduced power consumption of the low current lamp makes it ideal for telecommunications applications. A simplified diagram, shown in Figure 9, depicts signaling with a conventional telephone. When the telephone is on-hook, the circuit is open and there is no current flow. In this condition, an incoming call triggers the ringing generator to energize the ringer. When the receiver is picked up, the telephone goes into the off-hook condition. At this time current is allowed to flow, allowing the user to connect with the calling party via transmitter and receiver.

According to AT&T Technical Publication 48002, the DC supply voltage usually comes from the central office battery, which is nominally 48 volts. In the on-hook condition, the telephone essentially draws no current; otherwise, the central office senses a trouble condition. When the telephone is off-hook and being used, the telephone must draw a minimum of 20 mA and a maximum of 135 mA. As with the on-hook condition, the central office senses a trouble condition for currents outside this acceptable range. The low current lamp can make efficient use of this limited supply of current in applications such as dial edge lighting, keypad illumination, or other indicator requirements without the need for an external power source.

In the case of Private Branch Exchange (PBX) systems it is customary for the manufacturer of the system t provide an additional power supply for functions no already covered by the central office power supply, such as indicators. This supply varies with each manufacturer, but for message indication in the on-hook condition there are typically limited amounts of current available. An ideal application for the low current lamp is line status indication on a system PBX panel. Other applications include message waiting lamps for hotel telephone units, or busy lamp fields at a PBX attendant console. Each lamp in the field is associated with a push button switch by which the attendant may place a call to a particular station. The lamp indicates whether the station is busy or idle.

NOTE: Since a particular central office or interface may vary and therefore change the power supplied, the individual specifications for that system should be consulted. In most countries, the connection of equip-

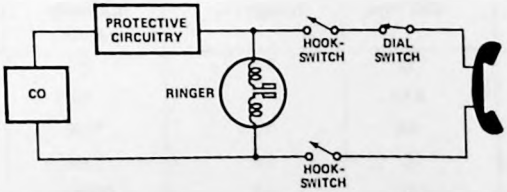


Figure 9. Simplified Telephone Diagram

ment to the telephone network is regulated by a government agency. In the U.S., Part 68 of the FCC Rules and Regulations governs the connection of terminal equipment to the telephone network. There are also available Bell System Technical Publications which document various aspects of the telephone network. For more specific information, contact:

Division Manager — Information Systems
American Telephone and Telegraph Company
30 Knightsbridge Road
Piscataway, NJ 08854
(201) 966-7111

BATTERIES

Minimizing size and weight for a power supply has always been an objective for those who design instruments, especially portable equipment. The reduction of drive current required for adequate brightness and visibility means that smaller, lighter power supplies may be used without sacrificing performance, or that a given power supply will not be as heavily loaded, extending the operating life of the supply. Such is the case with the battery, a common portable, lightweight power source. A smaller drain imposed on a given size cell extends the service life of the cells; for example, Figure 10 shows some typical discharge characteristics at several drain values for an alkaline "C" cell. In order to drive 25 conventional lamps, a supply of (25) (10 mA) = 250 mA forward current is required. According to Figure 10, a 250 mA drain would typically exhaust the battery in less than 15 hours. However, 25 low current lamps would need only (25) (2 mA) = 50 mA drive current. The discharge characteristics indicate that the battery would last for 125 hours at 50 mA.

Another possibility is that the decrease in drive requirements may make appropriate the use of "AA" cells instead of the same number of "C" cells without sacrificing performance. A typical drain characteristic for an "AA" cell is graphed in Figure 11. From the previous example, 15 hours of service life can be obtained from the "C" cell to drive the 25 regular lamps; if 25 low current lamps are used, the current decreases to 50 mA. From Figure 11, it can be seen that a drain of 50 mA would yield approximately 15 hours as well; the same amount of service is obtained with a set of batteries which are not only physically smaller by about 80%, but are also typically less expensive.

Figure 12 lists the typical household alkaline cells according to ANSI specification C18.1979. The table, restricted to the common household cells only, charts approximate voltages and dimensions. In addition to these ANSI specifications, the table also lists comparative capacities and weights.

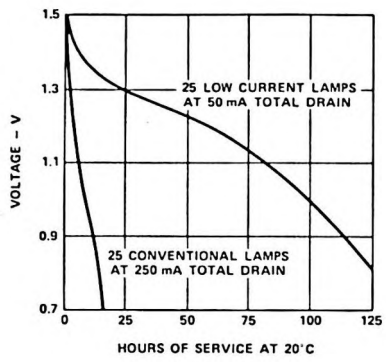


Figure 10. Typical "C" Cell Discharge Characteristics

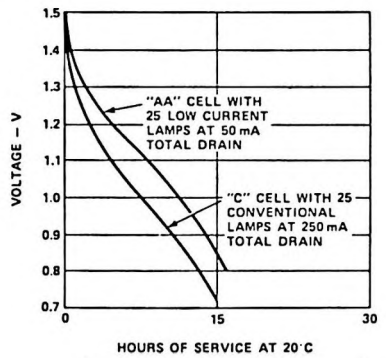


Figure 11. Typical "AA" and "C" Cell Discharge Characteristics

Cell Type	Voltage (V)	Typical Capacity (mA/hr)	Approximate Volume		Approximate Weight	
			(cu. in.)	(cc)	(oz.)	(gm)
N	1.5	700	0.19	3.1	0.34	9.6
AAA	1.5	800	0.22	3.6	0.42	11.9
AA	1.5	1700	0.48	7.8	0.82	23.3
C	1.5	5000	1.59	26.1	2.28	64.9
D	1.5	10000	3.31	54.3	4.47	127.0
1604	9.0	500	1.26	20.6	1.72	48.9

Figure 12. Alkaline Battery Types, Capacities, and Weights

For further information on selecting the appropriate battery for a given application, the following resources may be contacted:

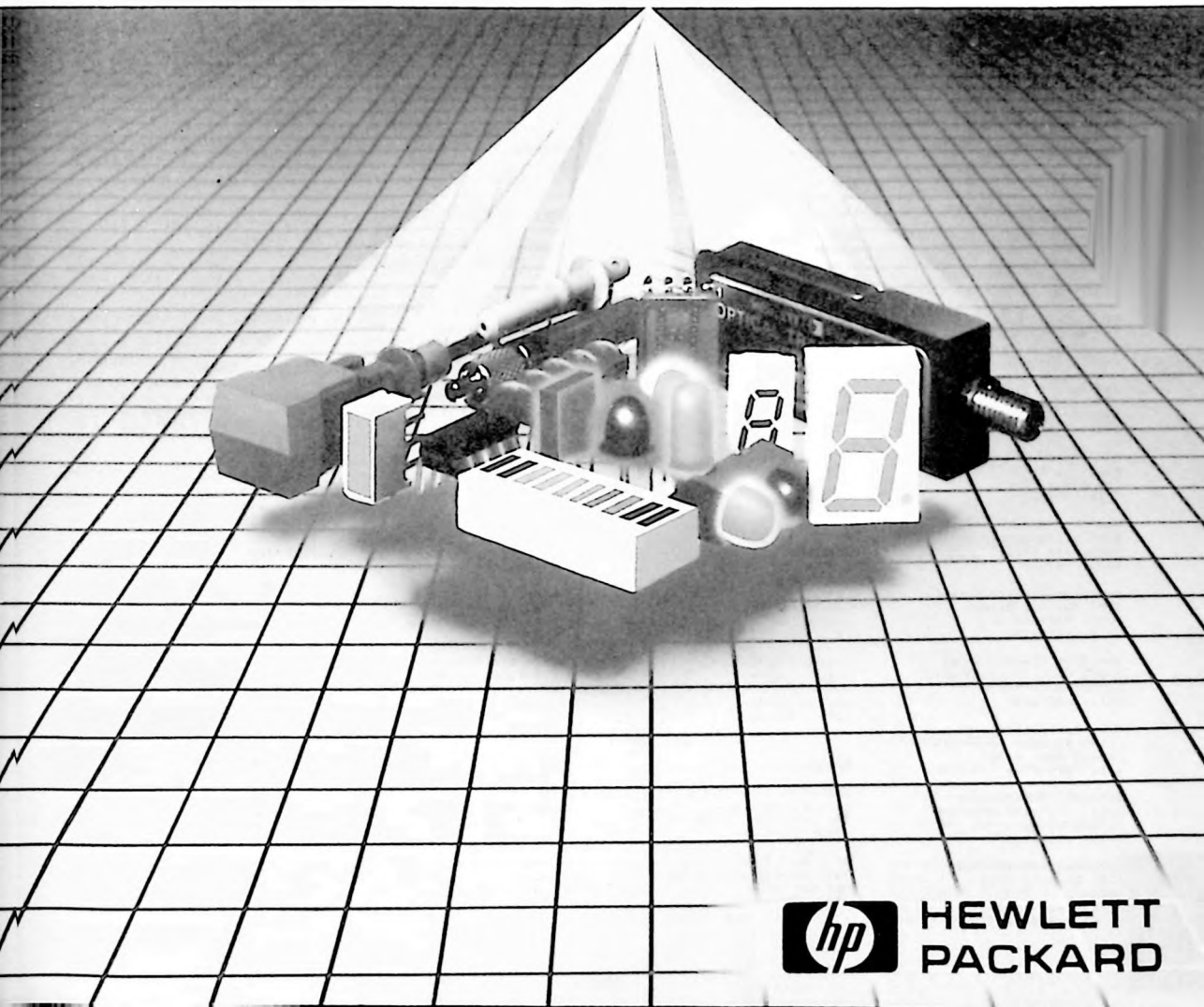
Duracell International Inc.
Battery Technology Company
So. Broadway
Tarrytown, New York 10591
(914) 591-7000

Ray-O-Vac Corporation
101 E. Washington Avenue
Madison, Wisconsin 53703
(608) 252-7400

Union Carbide
Battery Products Division
Old Ridgebury Road
Danbury, Connecticut 06817
(203) 794-2000

10. Appendix

- Hewlett-Packard Components Authorized Distributors and Representatives
- Hewlett-Packard Sales and Service Offices



HEWLETT PACKARD

HP Components Authorized Distributor and Representative Directory

United States

Alabama

Hall-Mark Electronics
4900 Bradford Drive
Huntsville 35805
(205) 837-8700

Hamilton/Avnet
4812 Commercial Drive
Huntsville 35805
(205) 837-7210

Schweber Electronics
2227 Drake Avenue, S.W.
Suite 14
Huntsville 35805
(205) 882-2200

Arizona

Hamilton/Avnet
505 South Madison
Tempe 85281
(602) 231-5100

Wyle Laboratories
Electronics Marketing Group
8155 North 24th Avenue
Phoenix 85021
(602) 249-2232
in Tucson (602) 884-7082

California

Hall-Mark Electronics
500 Mercury Drive
Sunnyvale 94086
(408) 773-9990

Hamilton/Avnet
4103 Northgate Blvd.
Sacramento 95834
(916) 925-2216

Hamilton/Avnet
4545 Viewridge Avenue
San Diego 92123
(619) 571-7510

Hamilton/Avnet
1175 Bordeaux Drive
Sunnyvale 94086
(408) 743-3355

Hamilton Electro Sales
3170 Pullman Street
Costa Mesa 92626
(714) 641-4100

Hamilton Electro Sales
10950 W. Washington Blvd.
Culver City 90230
(213) 558-2121

Schweber Electronics
21139 Victory Boulevard
Canoga Park 91303
(213) 999-4702

Schweber Electronics
17811 Gillette Avenue
Irvine 92714
(714) 863-0200

Schweber Electronics
1771 Tribute Road
Suite B
Sacramento 95815
(916) 929-9732

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3110 Patrick Henry Drive
Santa Clara 95050
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Wyle Laboratories
Electronics Marketing Group
124 Maryland Street
El Segundo 90245
(213) 322-8100

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Electronics Marketing Group
17872 Cowan Avenue
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(714) 863-1611

Wyle Laboratories
Electronics Marketing Group
11151 Sun Center Drive
Rancho Cordova 95670
(916) 638-5282

Wyle Laboratories
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9525 Chesapeake Drive
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(619) 565-9171

Wyle Laboratories
Electronics Marketing Group
3000 Bowers Avenue
Santa Clara 95052
(408) 727-2500

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8765 East Orchard
Suite 708
Englewood 80111
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Electronics Marketing Group
451 E. 124th Avenue
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Connecticut

Hamilton/Avnet
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Commerce Industrial Park
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Finance Drive
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Hall-Mark Electronics
1671 W. McNab Road
Ft. Lauderdale 33309
(305) 971-9280

Hall-Mark Electronics
7233 Lake Ellenor Drive
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St. Petersburg 33702
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AltaMonte Springs 32701
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Hollywood 33020
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Hall-Mark Electronics
6410 Atlantic Boulevard
Suite 115
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Hamilton/Avnet
5825 D. Peachtree Corners East
Norcross 30092
(404) 447-7507

Schweber Electronics
303 Research Drive
Suite 210
Norcross 30092
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1177 Industrial Drive
Bensenville 60106
(312) 860-3800

Hamilton/Avnet
1130 Thorndale Avenue
Bensenville 60106
(312) 860-7700

Schweber Electronics
904 Cambridge Drive
Elk Grove Village 60007
(312) 364-3750

Indiana

Hamilton/Avnet
485 Gradle Drive
Carmel 46032
(317) 844-9333

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6408 Castleplace Drive
Indianapolis 46250
(317) 849-7300

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5270 North Park Place N.E.
Cedar Rapids 52402
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(913) 888-4747

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50 Tower Office Park
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Ryoyo Electric Corporation
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Arranged alphabetically by country

Product Line Sales/Support Key

Key Product Line
- A Analytical
- CM Components
- C Computer Systems Sales only
- CH Computer Systems Hardware Sales and Services
- CS Computer Systems Software Sales and Services
- E Electronic Instruments & Measurement Systems
- M Medical Products
- MP Medical Products Primary SRO
- MS Medical Products Secondary SRO
- P Personal Computation Products
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After Jan. 1, 1984
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Tel: (204) 786-6701
A,CH,CM,E,MS,P*

Nova Scotia
Hewlett-Packard (Canada) Ltd.
P.O. Box 931
900 Windmill Road
DARTMOUTH, Nova Scotia B2Y 3Z6
Tel: (902) 469-7820
CH,CM,CS,E*,MS,P*

Ontario
Hewlett-Packard (Canada) Ltd.
3325 N. Service Rd., Unit 6
BURLINGTON, Ontario P3A 2A3
Tel: (416) 335-8644
CS,M*

Hewlett-Packard (Canada) Ltd.
552 Newbold Street
LONDON, Ontario N6E 2S5
Tel: (519) 686-9181
A,CH,CM,E*,MS,P*

Hewlett-Packard (Canada) Ltd.
6877 Goreway Drive
MISSISSAUGA, Ontario L4V 1M8
Tel: (416) 678-9430
A,CH,CM,CS,E,MP,P

Hewlett-Packard (Canada) Ltd.
2670 Queensview Dr.
OTTAWA, Ontario K2B 8K1
Tel: (613) 820-6483
A,CH,CM,CS,E*,MS,P*

Hewlett-Packard (Canada) Ltd.
220 Yorkland Blvd., Unit #11
WILLOWDALE, Ontario M2J 1R5
Tel: (416) 499-9333
CH

Quebec
Hewlett-Packard (Canada) Ltd.
17500 South Service Road
Trans-Canada Highway
KIRKLAND, Quebec H9J 2M5
Tel: (514) 697-4232
A,CH,CM,CS,E,MP,P*

Hewlett-Packard (Canada) Ltd.
Les Galeries du Vallon
2323 Du Versont Nord
STE. FOY, Quebec G1N 4C2
Tel: (418) 687-4570
CH

CHILE

Jorge Calcagni y Cia. Ltda.
Av. Italia 634 Santiago
Casilla 16475
SANTIAGO 9
Tel: 222-0222
Telex: Public Booth 440001
A,CM,E,M

Olympia (Chile) Ltda.
Av. Rodrigo de Araya 1045
Casilla 256-V
SANTIAGO 21
Tel: (02) 22 55 044
Telex: 240-565 OLYMP CL
Cable: Olympiachile Santiagochile
CH,CS,P

CHINA, People's Republic of

China Hewlett-Packard Rep. Office
P.O. Box 418
1A Lane 2, Luchang St.
Beiwei Rd., Xuanwu District
BEIJING
Tel: 33-1947, 33-7426
Telex: 22601 CTSHP CN
Cable: 1920
A,CH,CM,CS,E,P

COLOMBIA

Instrumentación
H. A. Langebaek & Kier S.A.
Carrera 4A No. 52A-26
Apartado Aereo 6287
BOGOTA 1, D.E.
Tel: 212-1466
Telex: 44400 INST CO
Cable: AARIS Bogota
CM,E,M

Casa Humboldt Ltda.
Carrera 14, No. 98-60
Apartado Aereo 51283
BOGOTA 1, D.E.
Tel: 256-1686
Telex: 45403 CCAL CO.
A

COSTA RICA

Cientifica Costarricense S.A.
Avenida 2, Calle 5
San Pedro de Montes de Oca
Apartado 10159
SAN JOSE
Tel: 24-38-20, 24-08-19
Telex: 2367 GALGUR CR
CM,E,M

CYPRUS

Telerexa Ltd.
P.O. Box 4809
14C Stassinos Avenue
NICOSIA
Tel: 62698
Telex: 2894 LEVIDO CY
E,M,P

DENMARK

Hewlett-Packard A/S
Datavej 52
DK-3460 BIRKEROD
Tel: (02) 81-66-40
Telex: 37409 hpas dk
A,CH,CM,CS,E,MS,P

Hewlett-Packard A/S
Rolighedsvej 32
DK-8240 RISSKOV, Aarhus
Tel: (06) 17-60-00
Telex: 37409 hpas dk
CH,E

DOMINICAN REPUBLIC

Microprog S.A.
Juan Tomás Mejía y Cotes No. 60
Arroyo Hondo
SANTO DOMINGO
Tel: 565-6268
Telex: 4510 ARENTA DR (RCA) P

ECUADOR

CYEDE Cia. Ltda.
Avenida Eloy Alfaro 1749
Casilla 6423 CCI
QUITO
Tel: 450-975, 243-052
Telex: 2548 CYEDE ED
CM,E,P

Hospitalar S.A.
Robles 625
Casilla 3590
QUITO
Tel: 545-250, 545-122
Telex: 2485 HOSPTL ED
Cable: HOSPITALAR-Quito
M

EGYPT

International Engineering Associates
24 Hussein Hegazi Street
Kasr-el-Aini
CAIRO
Tel: 23829, 21641
Telex: IEA UN 93830
CH,CS,E,M

EGYPOR
P.O.Box 2558
42 El Zahraa Street
CAIRO, Egypt
Tel: 65 00 21
Telex: 93 337
P

EL SALVADOR

IPESA de El Salvador S.A.
29 Avenida Norte 1216
SAN SALVADOR
Tel: 26-6858, 26-6868
Telex: 20539 IPESASAL
A,CH,CM,CS,E,P

FINLAND

Hewlett-Packard Oy
Revontulentie 7
PL 24
SF-02101 ESPOO 10
Tel: (90) 4550211
Telex: 121563 hewpa sf
CH,CM,CS,P

Hewlett-Packard Oy
(Olarinluoma 7)
PL 24
02101 ESPOO 10
Tel: (90) 4521022
A,E,MS

Hewlett-Packard Oy
Aatoksenkatv 10-C
SF-40720-72 JYVASKYLA
Tel: (941) 216318
CH

Hewlett-Packard Oy
Kainvuntie 1-C
SF-90140-14 OULU
Tel: (981) 338785
CH

FRANCE

Hewlett-Packard France
Z.I. Mercure B
Rue Berthelot
F-13763 Les Milles Cedex
AIX-EN-PROVENCE
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Telex: 410770F
A,CH,E,MS,P*

Hewlett-Packard France
64, rue Marchand Saillant
F-61000 ALENCON
Tel: 16 (33) 29 04 42

Hewlett-Packard France
Boite Postale 503
F-25026 BESANCON
28 rue de la Republique
F-25000 BESANCON
Tel: 16 (81) 83-16-22
CH,M

Hewlett-Packard France
13, Place Napoleon III
F-29000 BREST
Tel: 16 (98) 03-38-35

Hewlett-Packard France
Chemin des Mouilles
Boite Postale 162
F-69130 ECULLY Cedex (Lyon)
Tel: 16 (78) 833-81-25
Telex: 310617F
A,CH,CS,E,MP

Hewlett-Packard France
Tour Lorraine
Boulevard de France
F-91035 EVRY Cedex
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E

Hewlett-Packard France
Parc d'Aclivite du Bois Briard
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F-91040 EVRY Cedex
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Telex: 692315F
E

Hewlett-Packard France
5, avenue Raymond Chanas
F-38320 EYBENS (Grenoble)
Tel: 16 (76) 25-81-41
Telex: 980124 HP GRENOB EYBE
CH

Hewlett-Packard France
Centre d'Affaire Paris-Nord
Bâtiment Ampère 5 étage
Rue de la Commune de Paris
Boite Postale 300
F-93153 LE BLANC MESNIL
Tel: 16 (1) 865-44-52
Telex: 211032F
CH,CS,E,MS

Hewlett-Packard France
Parc d'Activités Cadera
Quartier Jean Mermoz
Avenue du Président JF Kennedy
F-33700 MERIGNAC (Bordeaux)
Tel: 16 (56) 34-00-84
Telex: 550105F
CH,E,MS

Hewlett-Packard France
Immueble "Les 3 B"
Nouveau Chemin de la Garde
ZAC de Bois Briand
F-44085 NANTES Cedex
Tel: 16 (40) 50-32-22
CH**

SALES & SUPPORT OFFICES

Arranged alphabetically by country

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Hewlett-Packard France
125, rue du Faubourg Bannier
F-45000 **ORLEANS**
Tel: 16 (38) 68 01 63

Hewlett-Packard France
Zone Industrielle de Courtaboeuf
Avenue des Tropiques
F-91947 Les Ulis Cedex **ORSAY**
Tel: (6) 907-78-25
Telex: 600048F
A,CH,CM,CS,E,MP,P

Hewlett-Packard France
Paris Porte-Maillot
15, Avenue de L'Amiral Bruix
F-75782 **PARIS** CEDEX 16
Tel: 16 (1) 502-12-20
Telex: 613663F
CH,MS,P

Hewlett-Packard France
124, Boulevard Tourasse
F-64000 **PAU**
Tel: 16 (59) 80 38 02

Hewlett-Packard France
2 Allée de la Bourgonnette
F-35100 **RENNES**
Tel: 16 (99) 51-42-44
Telex: 740912F
CH,CM,E,MS,P*

Hewlett-Packard France
98 Avenue de Bretagne
F-76100 **ROUEN**
Tel: 16 (35) 63-57-66
CH**,CS

Hewlett-Packard France
4 Rue Thomas Mann
Boite Postale 56
F-67033 **STRASBOURG** Cedex
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Telex: 890141F
CH,E,MS,P*

Hewlett-Packard France
Le Péripole
20, Chemin du Pigeonnier de la Cépière
F-31083 **TOULOUSE** Cedex
Tel: 16 (61) 40-11-12
Telex: 531639F
A,CH,CS,E,P*

Hewlett-Packard France
9, rue Baudin
F-26000 **VALENCE**
Tel: 16 (75) 42 76 16

Hewlett-Packard France
Carolor
ZAC de Bois Briand
F-57640 **VIGY** (Metz)
Tel: 16 (8) 771 20 22
CH

Hewlett-Packard France
Immeuble Péricentre
F-59658 **VILLENEUVE D'ASCQ** Cedex
Tel: 16 (20) 91-41-25
Telex: 160124F
CH,E,MS,P*

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Geschäftsstelle
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D-1000 **BERLIN** 30
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Telex: 018 3405 hpbln d
A,CH,E,M,P

Hewlett-Packard GmbH
Geschäftsstelle
Herrenberger Strasse 130
D-7030 **BOBLINGEN**
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Hewlett-Packard GmbH
Geschäftsstelle
Emanuel-Leutze-Strasse 1
D-4000 **DUSSELDORF**
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Telex: 085/86 533 hpdd d
A,CH,CS,E,MS,P

Hewlett-Packard GmbH
Geschäftsstelle
Schleefstr. 28a
D-4600 **DORTMUND**-Aplerbeck
Tel: (0231) 45001

Hewlett-Packard GmbH
Vertriebszentrale Frankfurt
Berner Strasse 117
Postfach 560 140
D-6000 **FRANKFURT** 56
Tel: (0611) 50-04-1
Telex: 04 13249 hpffm d
A,CH,CM,CS,E,MP,P

Hewlett-Packard GmbH
Geschäftsstelle
Aussenstelle Bad Homburg
Louisenstrasse 115
D-6380 **BAD HOMBURG**
Tel: (06172) 109-0

Hewlett-Packard GmbH
Geschäftsstelle
Kapstadtring 5
D-2000 **HAMBURG** 60
Tel: (040) 63804-1
Telex: 021 63 032 hphh d
A,CH,CS,E,MS,P

Hewlett-Packard GmbH
Geschäftsstelle
Heidering 37-39
D-3000 **HANNOVER** 61
Tel: (0511) 5706-0
Telex: 092 3259
A,CH,CM,E,MS,P

Hewlett-Packard GmbH
Geschäftsstelle
Rosslauer Weg 2-4
D-6800 **MANNHEIM**
Tel: (0621) 70050
Telex: 0462105
A,C,E

Hewlett-Packard GmbH
Geschäftsstelle
Messerschmittstrasse 7
D-7910 **NEU ULM**
Tel: 0731-70241
Telex: 0712816 HP ULM-D
A,C,E*

Hewlett-Packard GmbH
Geschäftsstelle
Ehhericherstr. 13
D-8500 **NÜRNBERG** 10
Tel: (0911) 5205-0
Telex: 0623 860
CH,CM,E,MS,P

Hewlett-Packard GmbH
Geschäftsstelle
Eschenstrasse 5
D-8028 **TAUFKIRCHEN**
Tel: (089) 6117-1
Telex: 0524985
A,CH,CM,E,MS,P

GREAT BRITAIN

See United Kingdom

GREECE

Kostas Karaynnis S.A.
8 Omirou Street
***ATHENS** 133*
Tel: 32 30 303, 32 37 371
Telex: 215962 RKAR GR
A,CH,CM,CS,E,M,P

PLAISIO S.A.
G. Gerardos
24 Stournara Street
ATHENS
Tel: 36-11-160
Telex: 221871
P

GUATEMALA

IPESA
Avenida Reforma 3-48, Zona 9
GUATEMALA CITY
Tel: 316627, 314786
Telex: 4192 TELTRO GU
A,CH,CM,CS,E,M,P

HONG KONG

Hewlett-Packard Hong Kong, Ltd.
G.P.O. Box 795
5th Floor, Sun Hung Kai Centre
30 Harbour Road
HONG KONG
Tel: 5-8323211
Telex: 66678 HEWPA HX
Cable: HEWPACK HONG KONG
E,CH,CS,P

CET Ltd.
1402 Tung Wah Mansion
199-203 Hennessy Rd.
*Wanchia, **HONG KONG***
Tel: 5-729376
Telex: 85148 CET HX
CM

Schmidt & Co. (Hong Kong) Ltd.
Wing On Centre, 28th Floor
Connaught Road, C.
HONG KONG
Tel: 5-455644
Telex: 74766 SCHMX HX
A,M

ICELAND

Elding Trading Company Inc.
Hafnarnvoli-Tryggvagotu
P.O. Box 895
IS-REYKJAVIK
Tel: 1-58-20, 1-63-03
M

INDIA

Computer products are sold through Blue Star Ltd. All computer repairs and maintenance service is done through Computer Maintenance Corp.

Blue Star Ltd.
Sabri Complex II Floor
24 Residency Rd.
***BANGALORE** 560 025*
Tel: 55660
Telex: 0845-430
Cable: BLUESTAR
A,CH,CM,CS*,E*

Blue Star Ltd.
Band Box House
Prabhadevi
***BOMBAY** 400 025*
Tel: 422-3101
Telex: 011-3751
Cable: BLUESTAR
A,M

Blue Star Ltd.
Sahas
414/2 Vir Savarkar Marg
Prabhadevi
***BOMBAY** 400 025*
Tel: 422-6155
Telex: 011-4093
Cable: FROSTBLUE
A,CH,CM,CS*,E,M*

Blue Star Ltd.
Kalyan, 19 Vishwas Colony
*Alkapuri, **BORODA**, 390 005*
Tel: 65235
Cable: BLUE STAR
A

Blue Star Ltd.
7 Hare Street
***CALCUTTA** 700 001*
Tel: 12-01-31
Telex: 021-7655
Cable: BLUESTAR
A,M

Blue Star Ltd.
133 Kodambakkam High Road
***MADRAS** 600 034*
Tel: 82057
Telex: 041-379
Cable: BLUESTAR
A,M

Blue Star Ltd.
Bhandari House, 7th/8th Floors
91 Nehru Place
***NEW DELHI** 110 024*
Tel: 682547
Telex: 031-2463
Cable: BLUESTAR
A,CH,CM,CS*,E,M*

Blue Star Ltd.
15/16:C Wellesley Rd.
***PUNE** 411 011*
Tel: 22775
Cable: BLUE STAR
A

Blue Star Ltd.
2-2-47/1108 Bolarum Rd.
***SECUNDERABAD** 500 003*
Tel: 72057
Telex: 0155-459
Cable: BLUEFROST
A,E

Blue Star Ltd.
T.C. 7/603 Poornima
Maruthankuzhi
***TRIVANDRUM** 695 013*
Tel: 65799
Telex: 0884-259
Cable: BLUESTAR
E

Computer Maintenance Corporation Ltd.
115, Sarojini Devi Road
***SECUNDERABAD** 500 003*
Tel: 310-184, 345-774
Telex: 031-2960
*CH***

APPENDIX

SALES & SUPPORT OFFICES

Arranged alphabetically by country

INDONESIA

BERCA Indonesia P.T.
P.O.Box 496/Jkt.
Jl. Abdul Muis 62
JAKARTA
Tel: 21-373009
Telex: 46748 BERSAL IA
Cable: BERSAL JAKARTA
P

BERCA Indonesia P.T.
P.O.Box 2497/Jkt
Antara Bldg., 17th Floor
Jl. Medan Merdeka Selatan 17
JAKARTA-PUSAT
Tel: 21-344-181
Telex: BERSAL IA
A,CS,E,M

BERCA Indonesia P.T.
P.O. Box 174/SBY.
Jl. Kutei No. 11
SURABAYA
Tel: 68172
Telex: 31146 BERSAL SB
Cable: BERSAL-SURABAYA
A,E,M,P*

IRAQ

Hewlett-Packard Trading S.A.
Service Operation
Al Mansoor City 9B/3/7
BAGHDAD
Tel: 551-49-73
Telex: 212-455 HEPAIRAQ IK
CH,CS

IRELAND

Hewlett-Packard Ireland Ltd.
82/83 Lower Leeson Street
DUBLIN 2
Tel: 0001 608800
Telex: 30439
A,CH,CM,CS,E,M,P

Cardiac Services Ltd.
Kilmore Road
Artane
DUBLIN 5
Tel: (01) 351820
Telex: 30439
M

ISRAEL

Eldan Electronic Instrument Ltd.
P.O.Box 1270
JERUSALEM 91000
16, Ohaliav St.
JERUSALEM 94467
Tel: 533 221, 553 242
Telex: 25231 AB/PAKRD IL
A

Electronics Engineering Division
Motorola Israel Ltd.
16 Kremenetski Street
P.O. Box 25016
TEL-AVIV 67899
Tel: 3 88 388
Telex: 33569 Motil IL
Cable: BASTEL Tel-Aviv
CH,CM,CS,E,M,P

ITALY

Hewlett-Packard Italiana S.p.A
Traversa 99C
Via Giulio Petroni, 19
I-70124 BARI
Tel: (080) 41-07-44
M

Hewlett-Packard Italiana S.p.A.
Via Martin Luther King, 38/III
I-40132 BOLOGNA
Tel: (051) 402394
Telex: 511630
CH,E,MS

Hewlett-Packard Italiana S.p.A.
Via Principe Nicola 43G/C
I-95126 CATANIA
Tel: (095) 37-10-87
Telex: 970291
C,P

Hewlett-Packard Italiana S.p.A.
Via G. Di Vittorio 9
I-20063 CERNUSCO SUL NAVIGLIO
(Milano)
Tel: (02) 923691
Telex: 334632
A,CH,CM,CS,E,MP,P

Hewlett-Packard Italiana S.p.A.
Via C. Colombo 49
I-20090 TREZZANO SUL NAVIGLIO
(Milano)
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Telex: 322116
C,M

Hewlett-Packard Italiana S.p.A.
Via Nuova San Rocco a
Capodimonte, 62/A
I-80131 NAPOLI
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Telex: 710698
A,CH,E

Hewlett-Packard Italiana S.p.A.
Viale G. Modugno 33
I-16156 GENOVA PEGLI
Tel: (010) 68-37-07
Telex: 215238
E,C

Hewlett-Packard Italiana S.p.A.
Via Pelizzo 15
I-35128 PADOVA
Tel: (049) 664888
Telex: 430315
A,CH,E,MS

Hewlett-Packard Italiana S.p.A.
Viale C. Pavese 340
I-00144 ROMA EUR
Tel: (06) 54831
Telex: 610514
A,CH,CM,CS,E,MS,P*

Hewlett-Packard Italiana S.p.A.
Via di Casellina 57/C
I-50018 SCANDICCI-FIRENZE
Tel: (055) 753863

Hewlett-Packard Italiana S.p.A.
Corso Svizzera, 185
I-10144 TORINO
Tel: (011) 74 4044
Telex: 221079
CH,E

JAPAN

Yokogawa-Hewlett-Packard Ltd.
152-1, Onna
ATSUGI, Kanagawa, 243
Tel: (0462) 28-0451
CM,C*,E

Yokogawa-Helwett-Packard Ltd.
Meiji-Seimei Bldg. 6F
3-1 Hon Chiba-Cho
CHIBA, 280
Tel: 472 25 7701
E,CH,CS

Yokogawa-Hewlett-Packard Ltd.
Yasuda-Seimei Hiroshima Bldg.
6-11, Hon-dori, Naka-ku
HIROSHIMA, 730
Tel: 82-241-0611

Yokogawa-Hewlett-Packard Ltd.
Towa Building
2-3, Kaigan-dori, 2 Chome Chuo-ku
KOBE, 650
Tel: (078) 392-4791
C,E

Yokogawa-Hewlett-Packard Ltd.
Kumagaya Asahi 82 Bldg
3-4 Tsukuba
KUMAGAYA, Saitama 360
Tel: (0485) 24-6563
CH,CM,E

Yokogawa-Hewlett-Packard Ltd.
Asahi Shinbun Daiichi Seimei Bldg.
4-7, Hanabata-cho
KUMAMOTO,860
Tel: (0963) 54-7311
CH,E

Yokogawa-Hewlett-Packard Ltd.
Shin-Kyoto Center Bldg.
614, Higashi-Shiokoji-cho
Karasuma-Nishiiru
Shiokoji-dori, Shimogyo-ku
KYOTO, 600
Tel: 075-343-0921
CH,E

Yokogawa-Hewlett-Packard Ltd.
Mito Mitsui Bldg
4-73, Sanno-maru, 1 Chome
MITO, Ibaraki 310
Tel: (0292) 25-7470
CH,CM,E

Yokogawa-Hewlett-Packard Ltd.
Sumitomo Seimei 14-9 Bldg.
Meieki-Minami, 2 Chome
Nakamura-ku
NAGOYA, 450
Tel: (052) 571-5171
CH,CM,CS,E,MS

Yokogawa-Hewlett-Packard Ltd.
Chuo Bldg.,
4-20 Nishinakajima, 5 Chome
Yodogawa-ku
OSAKA, 532
Tel: (06) 304-6021
Telex: YHPOSA 523-3624
A,CH,CM,CS,E,MP,P*

Yokogawa-Hewlett-Packard Ltd.
27-15, Yabe, 1 Chome
SAGAMIHARA Kanagawa, 229
Tel: 0427 59-1311

Yokogawa-Hewlett-Packard Ltd.
Daiichi Seimei Bldg.
7-1, Nishi Shinjuku, 2 Chome
Shinjuku-ku,TOKYO 160
Tel: 03-348-4611
CH,E

Yokogawa-Hewlett-Packard Ltd.
29-21 Takaido-Higashi, 3 Chome
Suginami-ku TOKYO 168
Tel: (03) 331-611
Telex: 232-2024 YHPTOK
A,CH,CM,CS,E,MP,P*

Yokogawa-Hewlett-Packard Ltd.
Daiichi Asano Building
2-8, Odori, 5 Chome
UTSUNOMIYA, Tochigi 320
Tel: (0286) 25-7155
CH,CS,E

Yokogawa-Hewlett-Packard Ltd.
Yasuda Seimei Nishiguchi Bldg.
30-4 Tsuruya-cho, 3 Chome
YOKOHAMA 221
Tel: (045) 312-1252
CH,CM,E

JORDAN

Mouasher Cousins Company
P.O. Box 1387
AMMAN
Tel: 24907, 39907
Telex: 21456 SABCO JO
CH,E,M,P

KENYA

ADCOM Ltd., Inc., Kenya
P.O.Box 30070
NAIROBI
Tel: 331955
Telex: 22639
E,M

KOREA

Samsung Electronics HP Division
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San 75-31, Yeoksam-Dong
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Yeongdong P.O. Box 72
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Telex: K27364 SAMSAN
A,CH,CM,CS,E,M,P

KUWAIT

Al-Khaldiya Trading & Contracting
P.O. Box 830 Safat
KUWAIT
Tel: 42-4910, 41-1726
Telex: 22481 Areeg kt
CH,E,M

Photo & Cine Equipment
P.O Box 270 Safat
KUWAIT
Tel: 42-2846, 42-3801
Telex: 22247 Matin kt
P

LEBANON

G.M. Dolmadjian
Achrafieh
P.O. Box 165.167
BEIRUT
Tel: 290293
*MP**
Computer Information Systems
P.O. Box 11-6274
BEIRUT
Tel: 89 40 73
Telex: 22259
C

LUXEMBOURG

Hewlett-Packard Belgium S.A./N.V.
Blvd de la Woluwe, 100
Woluwedal
B-1200 BRUSSELS
Tel: (02) 762-32-00
Telex: 23-494 paloben bru
A,CH,CM,CS,E,MP,P

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Jalan Semantan, Damansara Heights
KUALA LUMPUR 23-03
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SALES & SUPPORT OFFICES

Arranged alphabetically by country

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Protel Engineering
P.O.Box 1917
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23/4 Pending Road
Kuching, SARAWAK
Tel: 36299
Telex: MA 70904 PROMAL
Cable: PROTELENG
A,E,M

MALTA

Philip Toledo Ltd.
Notabile Rd.
MRIEHEL
Tel: 447 47, 455 66
Telex: Media MW 649
E,P

MEXICO

Hewlett-Packard Mexicana, S.A. de C.V.
Av. Periferico Sur No. 6501
Tepepan, Xochimilco
16020 **MEXICO D.F.**
Tel: 6-76-46-00
Telex: 17-74-507 HEWPACK MEX
A,CH,CS,E,MS,P

Hewlett-Packard Mexicana, S.A. de C.V.
Ave. Colonia del Valle 409
Col. del Valle
Municipio de Garza Garcia
MONTERREY, Nuevo Leon
Tel: 78 42 41
Telex: 038 410
CH

ECISA
José Vasconcelos No. 218
Col. Condesa Deleg. Cuauhtémoc
MEXICO D.F. 06140
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Telex: 17-72755 ECE ME
M

MOROCCO

Dolbeau
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CASABLANCA
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Telex: 23051, 22822
E

Gerep
2 rue d'Agadir
Boite Postale 156
CASABLANCA
Tel: 272093, 272095
Telex: 23 739
P

NETHERLANDS

Hewlett-Packard Nederland B.V.
Van Heuven Goedhartlaan 121
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P.O. Box 667
NL1180 AR **AMSTELVEEN**
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Bongerd 2
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Telex: 21261 HEPAC NL
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Pastoor Petersstraat 134-136
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P.O. Box 2342
NL 5600 CH **EINDHOVEN**
Tel: (040) 326911
Telex: 51484 hepae nl
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Northrop Instruments & Systems Ltd.
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Telex: 60605
A,M

Northrop Instruments & Systems Ltd.
110 Mandeville St.
P.O. Box 8388
CHRISTCHURCH
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Telex: 4203
A,M

Northrop Instruments & Systems Ltd.
Sturdee House
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NORTHERN IRELAND

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NORWAY

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OMAN

Khimjil Ramdas
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P

Suhail & Saud Bahwan
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Telex: 3274 BAHWAN MB

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Cable: FEMUS Rawalpindi
A,E,M

Mushko & Company Ltd.
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Tel: 524131, 524132
Telex: 2894 MUSKO PK
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A,E,M,P

PANAMA

Electrónico Balboa, S.A.
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PANAMA 5
Tel: 63-6613, 63-6748
Telex: 3483 ELECTRON PG
A,CM,E,M,P

PERU

Cia Electro Médica S.A.
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Casilla 1030
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Tel: 41-4325, 41-3703
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CM,E,M,P

PHILIPPINES

The Online Advanced Systems Corporation
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Legaspi Village, Makati
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Telex: 3274 ONLINE
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P.O. Box 2649 Manila
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P

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M

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1298 LISBOA Codex
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Hewlett-Packard Española S.A.
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Telex:27333 HPAG CH
CH,CM,CS

Hewlett-Packard (Schweiz) AG
Allmend 2
CH-8967 **WIDEN**
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A,CH,CM,CS,E,MS,P

SYRIA

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Nuri Basha Ahnaf Ebn Kays Street
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DAMASCUS
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Telex: 411 215
Cable: ELECTROBOR DAMASCUS
E

Middle East Electronics
P.O.Box 2308
Abu Rumnaneh
DAMASCUS
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Telex: 411 304
M

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3rd Floor, 7 Jen-Ai Road, Sec. 2
TAIPEI 100
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Cable: INGLIH TAIPEI
A

THAILAND

Unimesa
30 Patpong Ave., Suriwong
BANGKOK 5
Tel: 235-5727
Telex: 84439 Simonco TH
Cable: UNIMESA Bangkok
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Bangkok Business Equipment Ltd.
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Telex: 87669-BEQUIPT TH
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P

TRINIDAD & TOBAGO

Caribbean Telecoms Ltd.
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P.O. Box 732
PORT-OF-SPAIN
Tel: 62-44213, 62-44214
Telex: 235,272 HUGCO WG
CM,E,M,P

TUNISIA

Tunisie Electronique
31 Avenue de la Liberte
TUNIS
Tel: 280-144
E,P

Corema
1 ter. Av. de Carthage
TUNIS
Tel: 253-821
Telex: 12319 CABAM TN
M

TURKEY

Teknim Company Ltd.
Iran Caddesi No. 7
*Kavaklidere, **ANKARA***
Tel: 275800
Telex: 42155 TKNM TR
E

E.M.A.
Medina Eldem Sokak No.41/6
Yuksel Caddesi
ANKARA
Tel: 175 622
Telex: 42 591
M

UNITED ARAB EMIRATES

Emilac Ltd.
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ABU DHABI
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Cable: EMITAC ABUDHABI

Emilac Ltd.
P.O Box 1641
SHARJAH
Tel: 591 181
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CH,CS,E,M,P

UNITED KINGDOM

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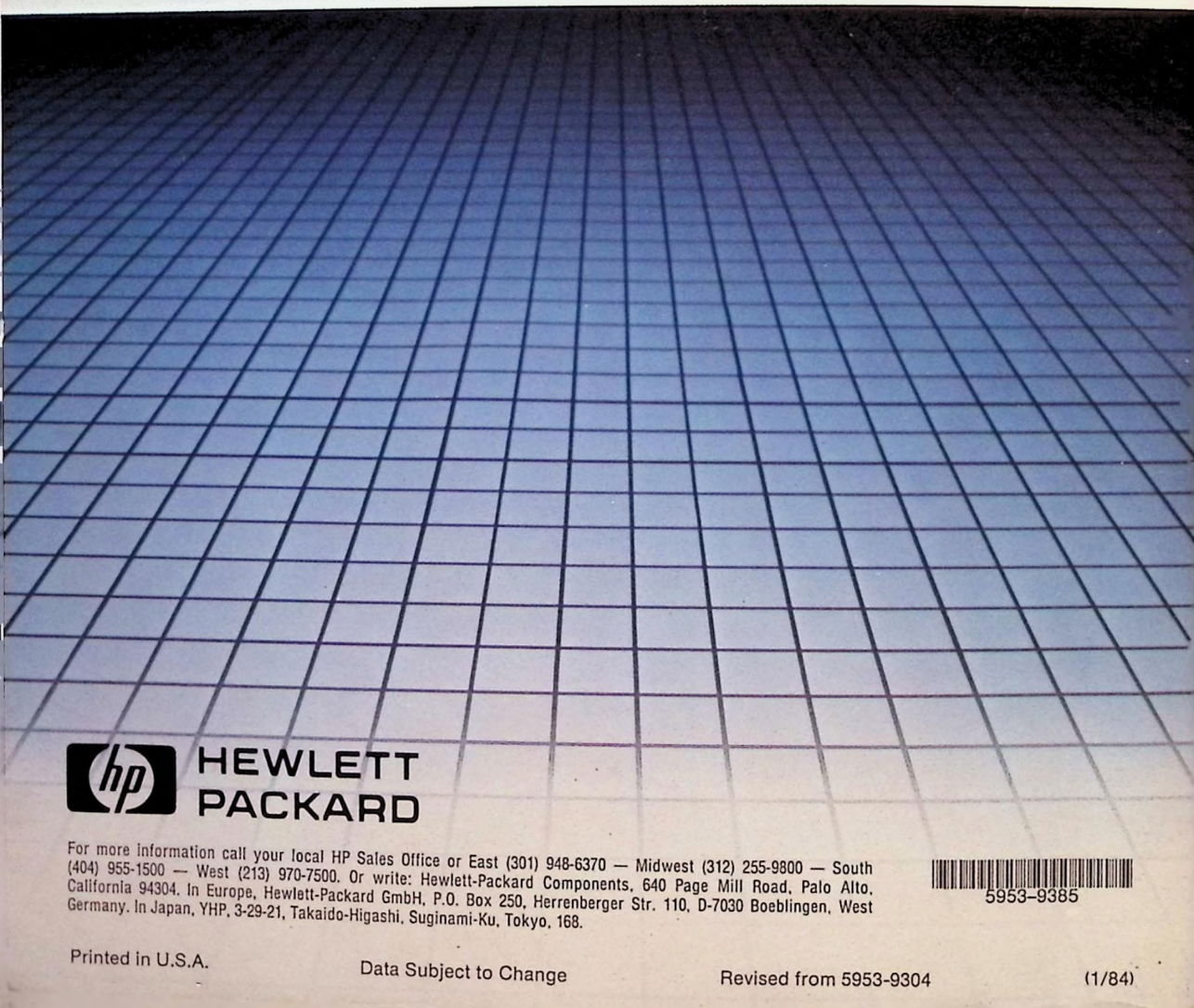

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